**VCodec Datasheet**

Project: Sirius

Author:

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**Revision History**

|  |  |  |
| --- | --- | --- |
| Date | Revision | Description |
| 15/12/2016 | 0.1 | Initial Creation |
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# Introduction

## Release

### H264

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Version | Release Time | Release Note |  |  |
| Cnm-coda988-pkg-v3.3.20 |  | The first release |  |  |
| Cnm-coda988-pkg-v3.5.23 |  | Move ME Line Buffer to the top. |  |  |
| Cnm-coda988-pkg-v3.7.26 |  | Wire Based sub frame sync enable |  |  |
|  |  |  |  |  |
|  |  |  |  |  |
|  |  |  |  |  |

# System Block

## Integration

### H264

VPU\_IDLE: clock gating

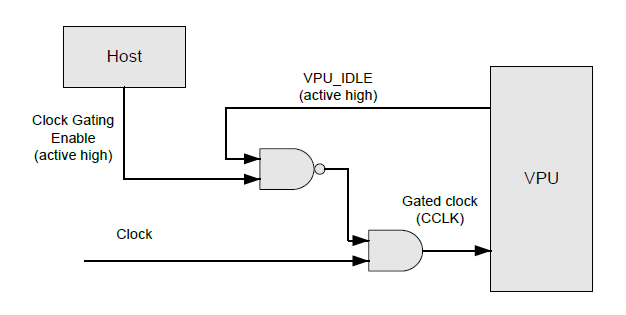
Interrupt 后 4个cclock后VPU\_IDLE拉起。

NOTE:

VPU\_IDLE: 采用的电路类似于下面这种状况，但是，如果IDLE gating 掉cclk后，apb将不能访问内部的register，会把apb的访问拉死。如果想用这个功能，host必须先de-assert clock gating,保证cclk进入，在访问register。

由于采用来外部的clock gating，因此建议IDLE就不再处理拉。

另外，建议IP 的core clk/ apb clock /axi clock gating 都用一个register控制。



### HEVC

VPU\_IDLE: clock gating

## Interrupts

* HEVC interrupts

|  |  |  |
| --- | --- | --- |
| Interrupts | Frequency |  |
| VPU\_INIT | Initial |  |
| CREATE\_INSTANCE | Initial |  |
| GET\_FW\_VERSION | Initial |  |
| FINI\_SEQ | End | TODO: How it works? |
| FLUSH\_DECODER | End | TODO: How it works? |
| SLEEP\_VPU | >>Sequence Level | TODO: How it works? |
| WAKE\_VPU | >>Sequence Level | TODO: How it works? |
| SET\_PARAM/DEC\_PIC\_HDR | <=Sequence Level  >=Frame Level |  |
| SET\_FRAMEBUF | >=Frame Level | TODO: Maybe Initial |
| StreamBuf Empty/Full | >Frame Level(Most) | Depend on buffer size. |
| ENC\_PIC/DEC\_PIC | =Frame Level | Cause CPU busy |

* H264 interrupts

|  |  |  |
| --- | --- | --- |
| Interrupt | Frequency |  |
| BIT\_CODE\_RUN | Initial |  |
| SET\_FRAME\_BUF | Initial | TODO: Maybe Intial |
| SEQ\_INIT | Sequence |  |
| ENC\_SEQ\_END | Sequence |  |
| ENC\_PARA\_SET/DEC\_PARA\_SET | Sequence |  |
| ENC\_HEADER\_SET | Sequence |  |
| DEC\_BUF\_FLUSH | End | TODO: How it works? |
| BUF empty/full | >Frame (Most) | Depend on buf size |
| DEC\_PIC/ENC\_PIC | Frame |  |
| User\_data buffer full |  |  |
| Decode one field for field picture | Field | TODO: How it works? |
| NumMbRows decoding is done | MB Rows | Low delay usage |

JPEG interrupts

|  |  |  |
| --- | --- | --- |
| Interrupt | Frequency |  |
| STOP | End |  |
|  |  |  |
|  |  |  |



## Datapath Control Flow

### Path0: ISP(Bypass ISP, Dec, DSP) -> Encoder (H264, HEVC encoder)

* + Frame Level
    - Single
    - Two
    - Multi
      * HEVC: 4K@30 + 1080P@30
      * H264: 2x720p@60fps
  + Line Level
    - Single
    - Two (TODO: Mostly with problem)
    - Multi

### Path1: ISP(Bypass ISP, Dec, DSP) -> JPEG Encoder

* + Frame Level
    - Single
    - Two
    - Multi

### Path2: ISP(Bypass ISP, Dec, DSP)-> Display

* + Frame Level
    - Single
    - Two (Overlay, TODO: how many layer?)
    - Multi

### Path3: Enc( HEVC/H264) -> (DMA(AES))-> BB

* + Single
  + Two
  + Multi ( TODO：check with Shenglong )

### Path4: USB ->(AES)-> BB

* + Single
  + Multi ( TODO: how many channels? By time-divided)

### Path5: Dec -> Display

* + Frame Level
  + Line Level
    - (TODO) Need check

### Path7: BB->(AES)->Decoder

### Encoder User Case

#### Case 0: Single In/Single Out Per Encoder

Basic function

Case1: Multi In/Multi Out Per Encoder

### Decoder

Interrupt:

Frequent Interrupts: One frame Done Interrupts

### Display

One-channel display

HEVC -> Display

H264 -> Display

JPEG -> Display

ISP -> Display

UI( Include Hardware Cursor) -> Display?

Multi-Channel Display ( Only By Overlay )

Picture In Picture

UI + Picture

The flow of display??

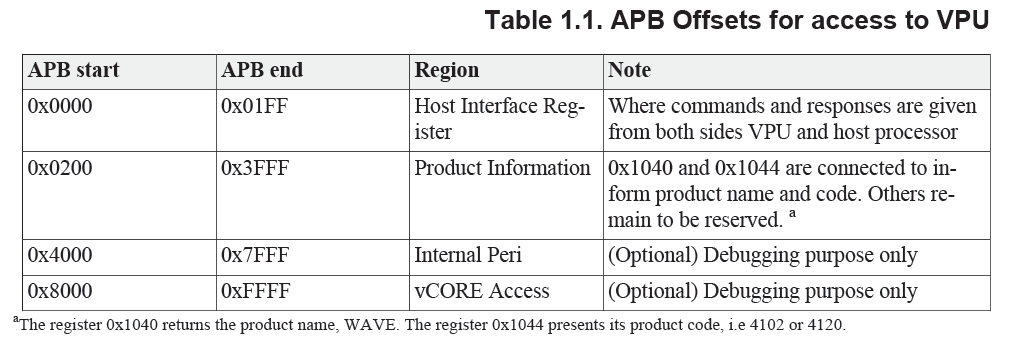
Confirm one thing:

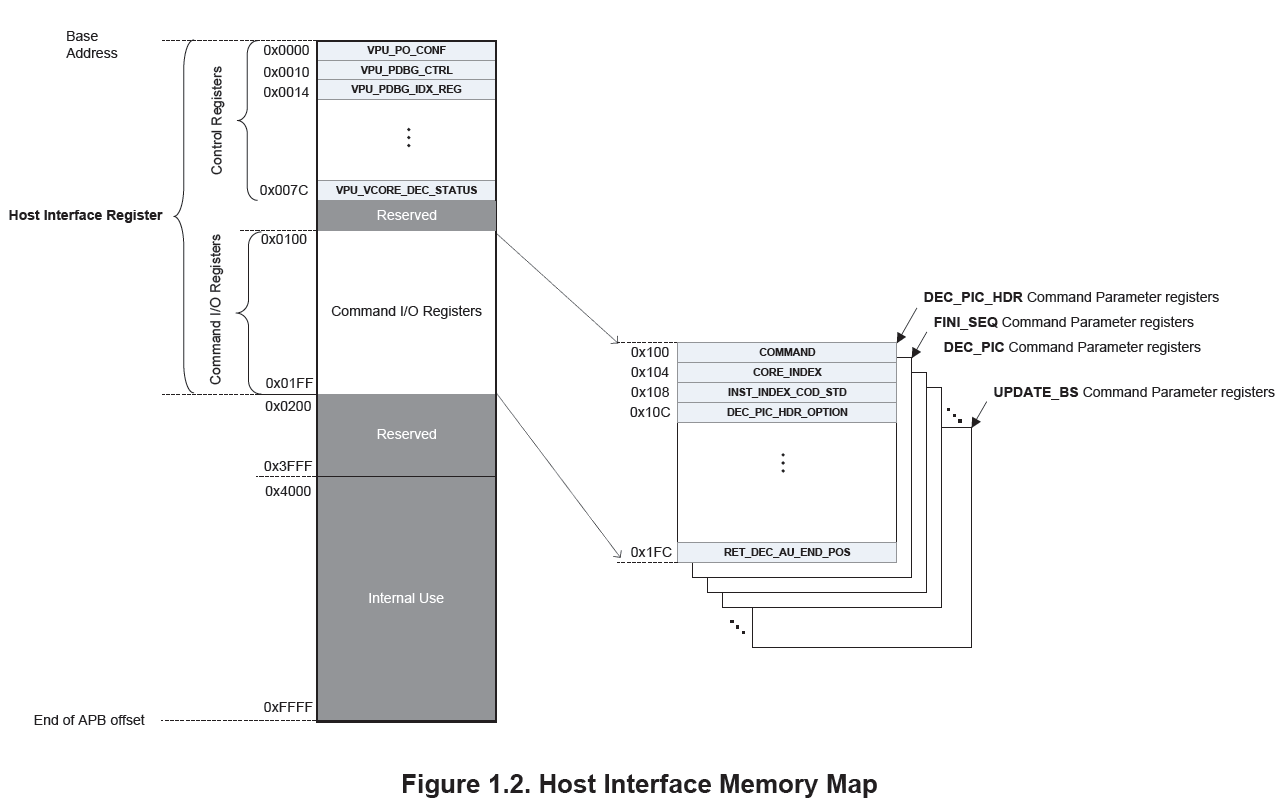
Display re-ordering in H.264 is enable.

## Host Interface Memory Map

### HEVC

Here are the general HEVC host interface registers’ address map.

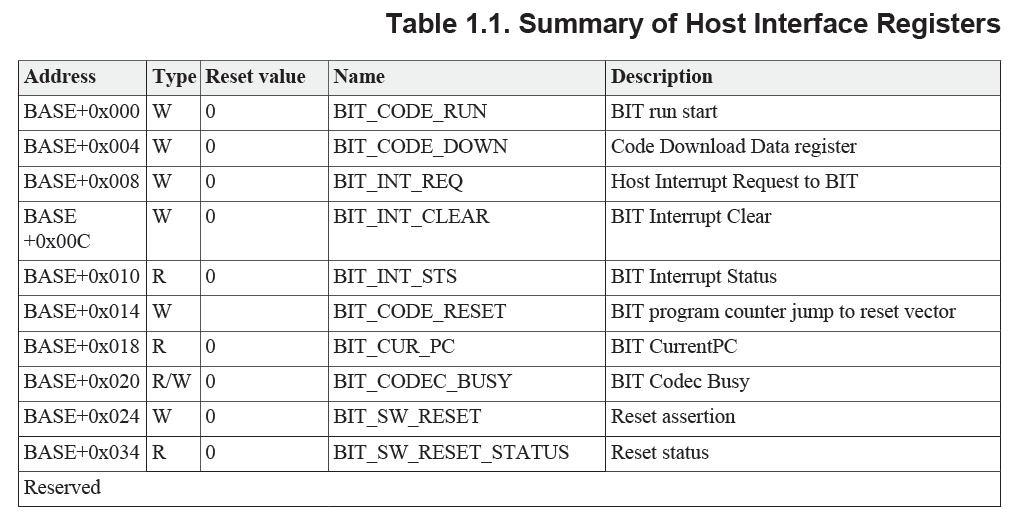


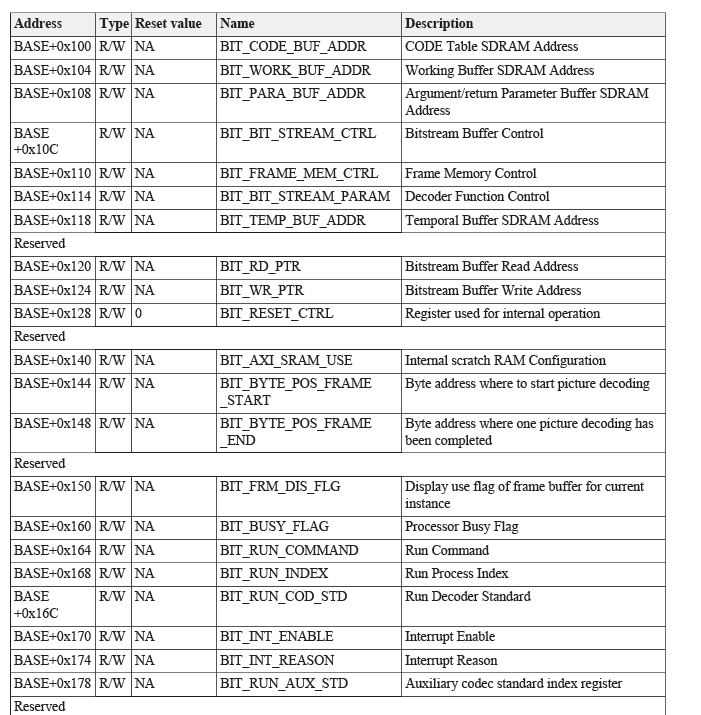


### H264

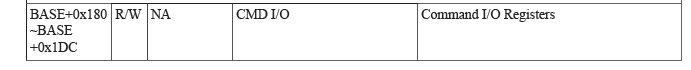
Here are the general H264 host registers’ address map.

* BIT processor Global Registers/Control Registers





* BIT Processor Command I/O Registers



# Features

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  | HEVC | H264 | JPEG | Display |
| FBC | O | X | X | X |
| 8bit | O | O | O | O |
| 10bit | O | X | O(12bit) | O |
| Cropping | O | O | X | O |
| Low-Delay Encoding | O | O | X | X |
| Low-Delay Decoding | X | O | X | X |
| Interlace | X | O | X | ? |
| Low delay with CF50 | X | X | X | X |
| Mono-chroma |  |  |  |  |

NOTE:

WAVE420+CF50 will support low delay with CF50 bypass mode **only**.

TODO:   
1. 需要确认Display是否支持Mono-chroma；

Cursor：支持

Video layer是不支持的。（已经跟Vivante确认过。）

2. 需要确认 Mono-chroma中YUV分量和RGB分量分别是多少？

# Buffer & AXI request & Clocks

## Source Image Buffer Requirement

## Buffers

### HEVC Enc

Summary:

Work buffer:

Max Outstanding:

Max BL:

Size: 128 bit / size = 4

Example:

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| Buffers | Addr | Size | ID | BL | Size | Note |
| Code | 80c0\_0000 |  | 0 | 4 | 4 | 读取的时间点:  一帧开始时，大量读取，中间过程还没发现存在  读取的方式:  RD请求之间似乎存在数据依赖，下一笔需要上一笔回来后，才能出去。 |
| STACK (4K aligned) |  |  |  |  |  |  |
| Temp |  |  |  |  |  |  |
| Report |  |  |  |  |  |  |
| BS |  |  |  |  |  |  |
| Work | 0x8190\_0000 | 0x0002\_0000 | 300 | 16/14 | 4 | 读取的时间点:  一帧开始时，读取。  读取的方式: |
| ROI\_MAP |  |  |  |  |  |  |
| ROI\_MODE |  |  |  |  |  |  |
| ROI\_QP |  |  |  |  |  |  |
| SRCY | 8760\_0000 |  | 305 | 4 | 4 | 读取的时间点：  每个CTU时，都会发生读。  读取方式:  64x32block进行读  It’s better to make the stride to be 64Byte, in order to avoid 4K access. |
| SRCCb |  |  | 305 | 2 | 4 |  |
| SRCCr |  |  | 305 | 2 | 4 |  |
| Rec0Y |  |  |  |  |  |  |
| Rec0Cb |  |  |  |  |  |  |
| Rec0Cr |  |  |  |  |  |  |
| Rec1Y |  |  |  |  |  |  |
| Rec1Cb |  |  |  |  |  |  |
| Rec1Cr |  |  |  |  |  |  |
| CompY |  |  |  |  |  |  |
| CompC |  |  |  |  |  |  |
| YOFF |  |  |  |  |  |  |
| COFF |  |  |  |  |  |  |
| MV0 |  |  |  |  |  |  |
| CompY |  |  |  |  |  |  |
| CompC |  |  |  |  |  |  |
| YOFF |  |  |  |  |  |  |
| COFF |  |  |  |  |  |  |
| MV1 |  |  |  |  |  |  |

TODO: Buffer Size Callculation 的方式

### H264 Enc

#### Working Buffer:

Stores the information required during decoding process. (不清楚都是些什么信息)

Encoder: 128Kbyte

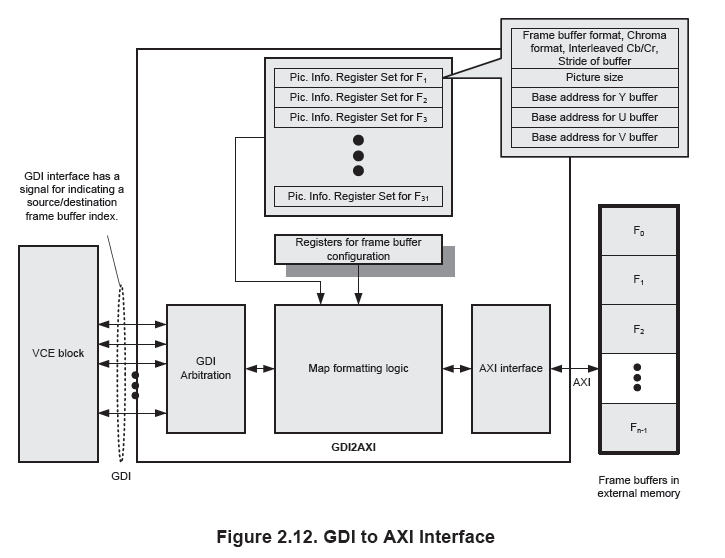
Decoder: 3Mbyte

#### Parameter Buffer:

Is used as input command arguments or output return data at certain commands.

Such as,

*Frame Buffer Address:* Input command arguments for SET\_FRAME\_BUF command.



#### TEMP Buffer:

Reconstructed pixel row buffer for H264 Intra Prediction

Context saving buffer for running multiple processes.

Deblock temporal data

#### External Memories

**Secondary AXI**:

**Configure**:

BIT\_AXI\_SRAM\_USE (0x140) cmd

**Bandwidth**:

Encoder:

Decoder:

**Performance**:

Summary

Pri-AXI:

Sec-AXI:

TODO:

1. 怎样用Sec-AXI interface?

BIT\_AXI\_SRAM\_USE (0x140) cmd

1. 带来的performance?

Example

1920x1080 case

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Buffers | Addr | Size | ID | BL |  |
| BitStreamBuf | 80e00000 | 1c00 | 1 | 2 |  |
| Param Buf | 80cb\_9800 |  | 1 | 16 (RD) | SW write it. And HW read |
| Temp:Intra Prediction | 80c4\_8000  80c4\_8780 |  | 1 | 2  2 (rd/wr) |  |
| Temp: DBK | 80c4\_b000 : luma  80c4\_f000 : chroma |  | 1 | 8  8  (rd/wr) |  |
| Work Buf | 8150\_0000 |  | 1 | 16 (rd/wr) |  |
| Reconstruct | 8160\_0000 (luma)  817f\_e000  (Linear) |  | 1  1 | 1 (wr for first mb col luma, chroma, 12x8 tile)  2 (wr for others, 12 x 16 tile)  8 (rd at the beginning of each frame, read 100 line, and it is 16x64 tiled.  ) |  |
| Source Image | 8230\_0000 |  | 1 | 2( rd, 16x16 Tile) |  |

### Display

## Clocks

Details, please refer to Sirius\_doc\Soc\Sirius\_clocks\_vx.x.xlsx.

### Display

AXI: 500M， fixed

### JPEG

AXI: frequency is same as core clock. Signoff clock is 450MHz.

### H264

AXI\_Pri: frequency is same as core clock. Signoff clock is 400MHz.

AXI\_Sec: frequency is same as core clock. Signoff clock is 400MHz.

### HEVC

AXI: frequency is same as core clock. Signoff clock is 360MHz.

### JPEG

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| Buffers | Addr | Size | ID | BL | Size |  |  |
| Source-Y(8bit) |  |  | 1 | 4 | 3 |  |  |
| Source-UV(8bit) |  |  | 1 | 2 | 3 |  |  |
| BS |  |  | 1 | 8 | 3 |  |  |
|  |  |  |  |  |  |  |  |
| Source-Y(12t) |  |  | 1 | 8 | 3 |  |  |
| Source-UV(12t) |  |  | 1 | 4 | 3 |  |  |
| BS |  |  | 1 | 8 | 3 |  |  |

### Display

连续发送请求的数目：

NV12 linear 是16笔， burst length = 3。

YV12好像是32笔，这个应该不会跟ISP进行打架，（潘淞曾经问过这个问题，但是后来我告诉他16的时候，跟我说不会出现打架的问题）。

# Error Concealment

Error Resilience and Concealment is an important feature for codecs. It need HW and SW cooperation to make it better.

A lot of error tests are need.

## H264 Decoder

* HW Error Detection and Concealment
  + Header Level Error detection and Concealment:
  + Slice data level Error Detection and Concealment:
* SW Error Detection and Concealment
  + What kind of information that CPU can get? (This can help sw do something.)

Acquiring Decoder Results, whenever a picture decoding is completed, host application can get the decoded output such as **display frame index**, **decoded frame index**, **decoded frame picture type**, **number of error concealed MBs**.

## HEVC Decoder

* HW Error Detection and Concealment
  + Header Level Error detection and Concealment:
  + Slice data level Error Detection and Concealment:
* SW Error Detection and Concealment
  + What kind of information that CPU can get?

VPU reports error information on the RET\_DEC\_ERR\_INFO register and warning information on RET\_DEC\_WARN\_INFO register, after DEC\_PIC\_HDR and DEC\_PIC command.

Two severity levels:

ERROR: VPU cannot proceed DEC\_PIC command with the error and stops decoding.

WARNING: VPU can decode it, but may be with problem.

* + What can SW do?

Check the information from RET\_DEC\_ERR\_INFO and RET\_DEC\_WARN\_INFO registers, then decide to do:

(TODO: need to test and try.)

1. Drop this frame, repeat previous frames.

# Bandwidth

## HEVC Dec

10 bit, 4096x2160, ~1.4GB/s

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  | RD(MB) | WR(MB) | Total(MB) |  |
| I | 2.5 | 36.3 | 38.8 |  |
| P | 11.1 | 36.3 | 47.4 |  |
| P | 11.1 | 36.2 | 47.3 |  |
| P | 11.0 | 36.2 | 47.2 |  |
| P | 10.9 | 36.2 | 47.1 |  |

## HEVC Enc

# Performance

## Target

### HEVC Dec

* Max Resolution:

8192 x 4096

* Design Target:
  + 4096x2160@30fps + 1080p@30fps
  + 100Mbps
* Final Result:

### HEVC Enc

* Max Resolution:
  + 8192x4096
* Design Target:
  + 4096x2160@30fps + 1080p@30fps
  + 100Mbps
* Final Result:
  + Simulation:
    - Single IP:

Duck 1080P

### H264 Dec

* Max Resolution:
  + 2048x2048
* Target:
  + 1080p @ 60fps
  + 100Mbps
* Final Result:

### H264 Enc

* Max Resolution:
  + 2048x2048(TODO: Need confirm)
* Target:
  + 1080p @ 60fps @600MHz
  + 100Mbps
* Final Result:
  + Simulation:
    - Single IP:

Duck 1080P, SearchRange: +/-64, +/-48, QP:30

Original Env Vs. WAXI 100 RAXI 100 delay Vs. LongBurst Read

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
|  | Original | Need  (MHz) | Ori+LB | Need  (MHz) | Ori+LB+Map | Ori+LB+MAP+Delay100 |
| I | 6639589 | 398.4 | 4339229 | 260.4 |  |  |
| P | 8526873 | 511.8 | 6093776 | 366.0 |  |  |
| P | 8545138 | 513.0 | 6111433 |  |  |  |

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | **Original** | **Need (MHz)** | **Ori+LB** | **Need (MHz)** | **Ori+LB+Map** | **Need (MHz)** | **Ori+LB+MAP+Delay100** |  |
| I | 6639589 | 398.4 | 4339229 | 260.35374 | 5298146 | 317.88876 |  |  |
| P | 8526873 | 511.8 | 6093776 | 365.62656 | 5874699 | 352.48194 |  |  |
| P | 8545138 | 513 | 6111433 | 366.68598 | 5888644 | 353.31864 |  |  |

WAXi100 RAXI 100 delay Vs. Emulation

|  |  |  |  |
| --- | --- | --- | --- |
|  |  |  |  |
|  |  |  |  |
|  |  |  |  |
|  |  |  |  |

* + - * Improve performance
        + LongBurst Read:

CMD\_ENC\_PIC\_ROT\_MODE (0x190) [4] bit

* + - * Issue:
        + Write rec image is single burst.
        + Read Rec ??(TODO

### JPEG Enc

* Max Resolution:
  + 32Kx32K
* Target:
  + ??
* Final Test:

### JPEG Dec

* Max Resolution:
  + 32Kx32K
* Target:
  + ??
* Final Result:

### Display

* Max Resolution:
  + 4096x2304( TODO: Need Confirm)
* Target:
  + 4096x2160@30fps
* Final Result:

## Real Test

# Low-Delay

## Target

ISP -> Encoder -> BB( SKY ) -> BB( Ground ) -> USB 输出码流：target delay 是50ms, 总延时（PAD解码）可以达到100ms。

IPS->Encoder->BB( SKY ) -> BB( Groud ) -> Decoder -> Display: target delay 是70ms

**NOTE**：

BB一次性发送的数据量是192\*96\*8\*6/5/8 = 112K Bytes（大块，10ms）, 1152 Bytes( 小块，10ms )

The work flow

# SignOff

## CheckList

|  |  |  |  |
| --- | --- | --- | --- |
| **IDs** | **CheckItems** | **Checked** |  |
| 1 | Replaced Cells |  |  |
| 2 | LS |  | HEVC |
| 3 | SRAM power gating |  | H264 SRAM power gating |
| 4 | RESET synchronization |  |  |
| 5 | SRAM ASIC Model仿真 |  |  |

## Results

HEVC

4K@30fps + 1080p@30fps

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  | Target  Freq(MHz) | Synthesis  Freq(MHz) | Clock Uncertainty | area |
| CCLK | 550 | 360 | 30% | 3.44  Logic: 2.18  Mem: 1.26 |
| BCLK | 400 | 300 | 30% |
| PCLK | 150 | 150 | 20% |
| ACLK | 500 | 360 | 20% |

H264

1080p@60fps

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  | Target  Freq(MHz) | Synthesis  Freq(MHz) | Clock Uncertainty | area |
| CCLK | 600 | 400MHz | 30% |  |
| PCLK | 150 | 150MHz | 30% |
| ACLK | 500 | 400MHz | 30% |

JPEG

320Mpixels/s ( YUV420 ), 200Mpixels/s (YUV444)

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | Target  Freq(MHz) | Synthesis  Freq(MHz) | Clock Uncertainty | area |  |  |  |  |  |  |
| CCLK | 500 | 450MHz | 30% |  |  |  |  |  |  |  |
| PCLK | 150 | 150MHz | 30% |  |  |  |  |  |  |
| ACLK | 500 | 450MHz | 30% |  |  |  |  |  |  |

Display

4K@30fps

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | Target  Freq(MHz) | Synthesis  Freq(MHz) | Clock Uncertainty | area |  |  |  |  |  |  |
| CCLK | 500 | 450MHz ( 476MHz， 2.1ns, confirmed with zqchen, at 2017/5/4， with jiajie and weiweishen | 30% |  |  |  |  |  |  |  |
| PCLK | 150 | 150MHz | 30% |  |  |  |  |  |  |
| ACLK | 500 | 500MHz (2ns, confirmed with zqchen, at 2017/5/4， with jiajie.) | 30% |  |  |  |  |  |  |

# Verification

## Simulation Env

### Files/Directories

**Filelist directory**: *filelist2/*

**Simulation directory**: *sim2/sim\_vcodec*

### Compile

1. Prepare the environment variables

*$cd sim2*

*$source common/simsetup*

1. Run compile

*$cd sim\_vcodec*

*$scompile <case\_test> -vcs –docompile –norun –nofwgen*

**After compiling, there are two directories being generated under sim2/sim\_vcodec/tmpdir/.**

**\_db\_VCS:** The directory is used to run simulation.

**h4esim\_test\_VCS:** The directory which is store the vectors, such as code.hex, ddr initial files.

**NOTE:**

*case\_test*: the cases that are created in C\_testcases. So far, we have these cases.

* + - * 1. h4esim\_test: h264 encoding simulation test case.
        2. h4eemu\_test:h264 encoding emulation test case.
        3. h4dsim\_test: h264 decoding simulation test case.
        4. H4demu\_test: h264 decoding emulation test case.

What is the difference between h4esim and h4eemu?

Simulation is slow. It is only config registers. No too much software running.

Emulation is faster. It calls a lot of software functions.

*-vcs:* vcs simulation

*-vel:* veloce emulation

*-docompile:* do compile

*-nocompile:* no compile

*-dorun:* running

*-norun:* no running

*-dofwgen:* generate the code.hex

*-nofwgen:* no code.hex generation

### Prepare simulation vectors

*$cd firmware/vcodec/cnm-wave420\_coda988\_codec\_v5.2.21*

*$make*

This will generate executable file, h264enc.

*$run\_h264enc.sh*

This will generate the memory initial files, which are used as the simulation vectors.

These files are stored at

*firmware/vcodec/cnm-wave420\_coda988\_codec\_v5.2.21/out*

### Run Simulation

*$cd <Sirius\_root>/sim2/sim\_vcodec/tmpdir/\_db\_VCS*

*$ln –s <Sirius\_root>/firmware/vcodec/cnm-wave420\_coda988\_codec\_v5.2.21/out*

*$cd <Sirius\_root>/sim2/sim\_vcodec/*

*$scompile h2esim\_test –vcs –dorun –dofwgen –nocompile*

## Global Features

SW reset sync;

## H264

Sequence 切换

## HEVC

### HEVC Dec Special features

* Thumbnail mode

VPU can decode only I-RAP pictures with a minimum number of DPB.

* Trick Mode
* Frame Skip Mode
* Multiple SPS/PPS

### H264 Dec Special features

* Low Delay Decoding
* Multiple SPS/PPS

Display:

System:

DDR3/DDR4/LPDDR3

32bit mode/64bit mode/ 64bit mode with inline ECC

DDR Control ：

4K@30fps DDR 的下限是多少？也就是要用多大的DDR才能解决问题。

Compression /uncompression

Decoder / Encoder performance

4K @30fps时候性能是多少？1080P@60fps的时候DDR跑的频率是多少？

压缩，非压缩下需要分别需要什么样的频率？

分为两种verification: 一种内部feature的验证，一种是跟系统的测试结果。

出报告，给沈老师。

# Annex A: Rate Control

## HEVC Enc

# Performance Data

## H264 Enc

Duck 1080P, SearchRange: +/-64, +/-48, QP:30

Original

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
|  | I( 6639589) | | P(8526873) | | P(8545138) | |
| IME\_LOAD | 0 | 0 | 433 | 43075 | 431 | 43086 |
| IME\_SEARCH | 0 | 0 | 397 | 423 | 396 | 423 |
| FME\_SEARCH | 0 | 0 | 467 | 492 | 468 | 492 |
| MC\_LOAD | 0 | 0 | 538 | 2165 | 563 | 1970 |
| MC\_INTP\_Y | 0 | 0 | 214 | 393 | 215 | 392 |
| MC\_INTP\_C | 0 | 0 | 73 | 87 | 73 | 87 |
| ACDC | X | 0 | X | 0 | X | 0 |
| IP | X | 593 | X | 593 | X | 500 |
| INVTQ | 503 | 759 | 485 | 759 | 486 | 517 |
| RECON | 444 | 591 | 336 | 591 | 339 | 498 |
| DEBLK | 377 | 1449 | 344 | 1354 | 354 | 1428 |
| BPU | 208 | 1285 | 177 | 841 | 179 | 1287 |
| ALL | 798 | 1453 | 1029 | 43079 | 1031 | 43090 |

## JPEG

Hi，all

对JPEG的性能统计如下：

以下实测试使用图像pakyjoy\_1280x720\_8bit中第300帧、图像复杂度较大、4:2:2与4:4:4图像由4:2:0变化得出

1、Encoder

  实测：  色度格式       编码时间(cycle)

               4:4:4             1830402

               4:2:2             1217582

               4:2:0             940415

    等效：

               4:4:4 时 8Kx4K 每帧约 67Mcycle （~ [8Kx4K@5.8fps](mailto:8Kx4K@5.8fps) / 400MHz）

               4:2:2 时 8Kx4K 每帧约 45Mcycle （~ [8Kx4K@8.7fps](mailto:8Kx4K@8.7fps) / 400MHz）

               4:2:0 时 8Kx4K 每帧约 35Mcycle （~ [8Kx4K@11.3fps](mailto:8Kx4K@11.3fps) / 400MHz）

2、Decoder

  实测：  色度格式       编码时间(cycle)

               4:4:4             1751633

               4:2:2             1134367

               4:2:0             931058

    等效：

               4:4:4 时 8Kx4K 每帧约 64Mcycle （~ [8Kx4K@6.2fps](mailto:8Kx4K@6.2fps) / 400MHz）

               4:2:2 时 8Kx4K 每帧约 41Mcycle （~ [8Kx4K@9.6fps](mailto:8Kx4K@9.6fps) / 400MHz）

               4:2:0 时 8Kx4K 每帧约 34Mcycle （~ [8Kx4K@11.6fps](mailto:8Kx4K@11.6fps) / 400MHz）

**\*\*  以上实测数据并未包含APB配置时间**

**\*\*  数据在AXI通道为理想状态下取得**

# Final Check

1. SRAM 要按照新的命名规则重新生成；
   1. 加上前缀
   2. 都用大写
2. SRAM有些需要生成新的。

CF50 768x175

HEVC spreg512x160

HEVC spreg128x160

1. 最终的时候要把SRAM再仔细查看一边。

# Memory

## H264

Details: Please refer to

## HEVC

## Display

# Program

## HEVC

Note: HW Constraints

Required Size = actual bitstream size + 32Kbytes

Minimum size of bitstream: 96Kbytes

Margin: 32Kbytes

Return after one frame:

# Post Simulation

## LiHu: SUB2 ( JPEG/Display )

|  |  |
| --- | --- |
| a) soc rtl + sub2 netlist (1021) + SDF (cbest) | |
| Dir | /home/lhu/eda12/soc\_proj/Sirius/trunk/sim2/sim\_system/tmpdir/jpegenc\_test\_VCS |
| Netlist | /projects/sirius/backend\_pool/final\_database/netlist/sirius\_sub\_2.v.gz |
| Sdf | /home/lhu/eda12/soc\_proj/Sirius/trunk/sim2/testbench/tb\_common/testbench.v line 275 ~ line284 |
| Logs | /home/lhu/eda12/soc\_proj/Sirius/trunk/sim2/sim\_system/tmpdir/jpegenc\_test\_VCS /simv.log |
| Wave | /home/lhu/eda12/soc\_proj/Sirius/trunk/sim2/sim\_system/tmpdir/jpegenc\_test\_VCS/novas.fsdb |
| Result | Check rtl\_jpeg.bs |
| Cmd | Compile: scompile jpegenc\_test -docompile -dofwgen –norun |
| Run: scompile jpegenc\_test –nocompile –mywave.do |
| Note | Key files: mydefine.v myenvvar C\_testcases/jpegenc\_test/main\_a7.c mywave.do /home/lyu/post\_dat/jpeg/enc/yuv\_sim\_ddr\*.dat |
| filelist2/rtl\_vcs.f  sim2/testbench/tb\_common/vcodec/check\_save.v  sim2/testbench/tb\_common/h264\_top\_tb.v  sim2/testbench/tb\_common/testbench.v |

|  |  |
| --- | --- |
| b) soc rtl + sub2 netlist (1021) + SDF (cbest) | |
| Dir | /home/lhu/eda12/soc\_proj/Sirius/trunk/sim2/sim\_system/tmpdir/jpegdec\_test\_VCS |
| Netlist | /projects/sirius/backend\_pool/final\_database/netlist/sirius\_sub\_2.v.gz |
| Sdf | /home/lhu/eda12/soc\_proj/Sirius/trunk/sim2/testbench/tb\_common/testbench.v line 275 ~ line284 |
| Logs | /home/lhu/eda12/soc\_proj/Sirius/trunk/sim2/sim\_system/tmpdir/jpegdec\_test\_VCS /simv.log |
| Wave | /home/lhu/eda12/soc\_proj/Sirius/trunk/sim2/sim\_system/tmpdir/jpegdec\_test\_VCS/novas.fsdb |
| Result | Check rtl\_jpeg.yuv |
| Cmd | Compile: scompile jpegdec\_test -docompile -dofwgen –norun |
| Run: scompile jpegdec\_test –nocompile –mywave.do |
| Note | Key files: mydefine.v myenvvar C\_testcases/jpegdec\_test/main\_a7.c mywave.do /home/lyu/post\_dat/jpeg/dec/bs\_sim\_ddr\*.dat |
| filelist2/rtl\_vcs.f  sim2/testbench/tb\_common/vcodec/check\_save.v  sim2/testbench/tb\_common/h264\_top\_tb.v  sim2/testbench/tb\_common/testbench.v |

|  |  |
| --- | --- |
| c) soc rtl + sub2 netlist (1021) + SDF (cbest) | |
| Dir | /home/lhu/eda12/soc\_proj/Sirius/trunk/sim2/sim\_system/tmpdir/display\_test\_VCS\_150 |
| Netlist | /projects/sirius/backend\_pool/final\_database/netlist/sirius\_sub\_2.v.gz |
| Sdf | /home/lhu/eda12/soc\_proj/Sirius/trunk/sim2/testbench/tb\_common/testbench.v line 275 ~ line284 |
| Logs | /home/lhu/eda12/soc\_proj/Sirius/trunk/sim2/sim\_system/tmpdir/display\_test\_VCS\_150/simv.log |
| Wave | /home/lhu/eda12/soc\_proj/Sirius/trunk/sim2/sim\_system/tmpdir/display\_test\_VCS\_150/novas.fsdb |
| Result | Check RTL\_DISPLAY\_OUT.txt  copy RTL\_DISPLAY\_OUT.txt $ROOT/script/video\_tools  ./rgb888\_2\_oneframe.py |
| Cmd | Compile: scompile display\_test –depat 150 -docompile -dofwgen –norun |
| Run: scompile jpegdec\_test –depat 150 –nocompile –mywave.do |
| Note | Key files: mydefine.v myenvvar C\_testcases/display\_test/main\_a7.c mywave.do $ROOT/sim2/testbench/tb\_common/tb\_display/memory\_file\_\*.txt |
| filelist2/rtl\_vcs.f  sim2/testbench/tb\_common/vcodec/check\_save.v  sim2/testbench/tb\_common/h264\_top\_tb.v  sim2/testbench/tb\_common/testbench.v |

|  |  |
| --- | --- |
| d) sub2+top+sub\_top+sub4+ca7+ddr netlist (1021) + SDF (cworst) | |
| Dir | /home/lhu/eda12/proj/sirius/trunk/sim2/sim\_system\_mini/tmpdir/jpegenc\_test\_VCS |
| Netlist | /projects/sirius/backend\_pool/final\_database/netlist/sirius\_sub\_2.v.gz  /archive/lhu/Sirius/backend\_pool/top/final\_database/top\_postcts.v  /projects/sirius/backend\_pool/final\_database/netlist/sirius\_sub\_4.v.gz  /projects/sirius/backend\_pool/final\_database/netlist/a7\_harden\_subsystem\_postcts.v.gz  /projects/sirius/backend\_pool/final\_database/netlist/cortexa7core\_postcts.v.gz  /projects/sirius/backend\_pool/final\_database/netlist/sirius\_sub\_ca7.v.gz  /projects/sirius/backend\_pool/final\_database/netlist/DDR\_TOP\_postcts.v.gz |
| Sdf | /home/lhu/eda12/proj/sirius/trunk/sim2/testbench/tb\_common/testbench.v line 252 ~ line280 |
| Logs | /home/lhu/eda12/proj/sirius/trunk/sim2/sim\_system\_mini/tmpdir/jpegenc\_test\_VCS /simv.log |
| Wave | /home/lhu/eda12/proj/sirius/trunk/sim2/sim\_system\_mini/tmpdir/jpegenc\_test\_VCS /novas.fsdb |
| Result | Check rtl\_jpeg.bs |
| Cmd | Compile: scompile jpegenc\_test -docompile -dofwgen –norun |
| Run: scompile jpegenc\_test –nocompile –mywave.do |
| Note | Key files: mydefine.v myenvvar C\_testcases/jpegenc\_test/main\_a7.c mywave.do /home/lyu/post\_dat/jpeg/enc/yuv\_sim\_ddr\*.dat |
| filelist2/rtl\_vcs.f  filelist2/sirius\_top.f  filelist2/a7\_harden\_subsystem.f  filelist2/a7\_subsystem.f  filelist2/ddr\_vcs\_nls.f  sim2/testbench/tb\_common/vcodec/check\_save.v  sim2/testbench/tb\_common/h264\_top\_tb.v  sim2/testbench/tb\_common/post\_timing\_disable\_warning.v  sim2/testbench/tb\_common/testbench.v |

|  |  |
| --- | --- |
| e) sub2+top+sub\_top+sub4+ca7+ddr netlist (1021) + SDF (cworst) | |
| Dir | /home/lhu/eda12/proj/sirius/trunk/sim2/sim\_system\_mini/tmpdir/jpegdec\_test\_VCS |
| Netlist | /projects/sirius/backend\_pool/final\_database/netlist/sirius\_sub\_2.v.gz  /archive/lhu/Sirius/backend\_pool/top/final\_database/top\_postcts.v  /projects/sirius/backend\_pool/final\_database/netlist/sirius\_sub\_4.v.gz  /projects/sirius/backend\_pool/final\_database/netlist/a7\_harden\_subsystem\_postcts.v.gz  /projects/sirius/backend\_pool/final\_database/netlist/cortexa7core\_postcts.v.gz  /projects/sirius/backend\_pool/final\_database/netlist/sirius\_sub\_ca7.v.gz  /projects/sirius/backend\_pool/final\_database/netlist/DDR\_TOP\_postcts.v.gz |
| Sdf | /home/lhu/eda12/proj/sirius/trunk/sim2/testbench/tb\_common/testbench.v line 252 ~ line280 |
| Logs | /home/lhu/eda12/proj/sirius/trunk/sim2/sim\_system\_mini/tmpdir/jpegdec\_test\_VCS /simv.log |
| Wave | /home/lhu/eda12/proj/sirius/trunk/sim2/sim\_system\_mini/tmpdir/jpegdec\_test\_VCS /novas.fsdb |
| Result | Check rtl\_jpeg.yuv |
| Cmd | Compile: scompile jpegdec\_test -docompile -dofwgen –norun |
| Run: scompile jpegdec\_test –nocompile –mywave.do |
| Note | Key files: mydefine.v myenvvar C\_testcases/jpegdec\_test/main\_a7.c mywave.do /home/lyu/post\_dat/jpeg/dec/bs\_sim\_ddr\*.dat |
| filelist2/rtl\_vcs.f  filelist2/sirius\_top.f  filelist2/a7\_harden\_subsystem.f  filelist2/a7\_subsystem.f  filelist2/ddr\_vcs\_nls.f  sim2/testbench/tb\_common/vcodec/check\_save.v  sim2/testbench/tb\_common/h264\_top\_tb.v  sim2/testbench/tb\_common/post\_timing\_disable\_warning.v  sim2/testbench/tb\_common/testbench.v |

|  |  |
| --- | --- |
| f) sub2+top+sub\_top+sub4+ca7+ddr netlist (1021) + SDF (cworst) | |
| Dir | /home/lhu/eda12/proj/sirius/trunk/sim2/sim\_system\_mini/tmpdir/h264\_clksw\_test\_VCS |
| Netlist | /projects/sirius/backend\_pool/final\_database/netlist/sirius\_sub\_2.v.gz  /archive/lhu/Sirius/backend\_pool/top/final\_database/top\_postcts.v  /projects/sirius/backend\_pool/final\_database/netlist/sirius\_sub\_4.v.gz  /projects/sirius/backend\_pool/final\_database/netlist/a7\_harden\_subsystem\_postcts.v.gz  /projects/sirius/backend\_pool/final\_database/netlist/cortexa7core\_postcts.v.gz  /projects/sirius/backend\_pool/final\_database/netlist/sirius\_sub\_ca7.v.gz  /projects/sirius/backend\_pool/final\_database/netlist/DDR\_TOP\_postcts.v.gz |
| Sdf | /home/lhu/eda12/proj/sirius/trunk/sim2/testbench/tb\_common/testbench.v line 252 ~ line280 |
| Logs | /home/lhu/eda12/proj/sirius/trunk/sim2/sim\_system\_mini/tmpdir/h264\_clksw\_test\_VCS /simv.log |
| Wave | /home/lhu/eda12/proj/sirius/trunk/sim2/sim\_system\_mini/tmpdir/h264\_clksw\_test\_VCS /novas.fsdb |
| Result | Check waveform |
| Cmd | Compile: scompile h264\_clksw\_test -docompile -dofwgen –norun |
| Run: scompile h264\_clksw\_test –nocompile –mywave.do |
| Note | Key files: mydefine.v myenvvar C\_testcases/h264\_clksw\_test/main\_a7.c mywave.do |
| filelist2/rtl\_vcs.f  filelist2/sirius\_top.f  filelist2/a7\_harden\_subsystem.f  filelist2/a7\_subsystem.f  filelist2/ddr\_vcs\_nls.f  sim2/testbench/tb\_common/vcodec/check\_save.v  sim2/testbench/tb\_common/h264\_top\_tb.v  sim2/testbench/tb\_common/post\_timing\_disable\_warning.v  sim2/testbench/tb\_common/testbench.v |

|  |  |
| --- | --- |
| g) sub2+top+sub\_top+sub4+ca7+ddr netlist (1021) + SDF (cworst) | |
| Dir | /home/lhu/eda12/proj/sirius/trunk/sim2/sim\_system\_mini/tmpdir/jpeg\_clksw\_test\_VCS |
| Netlist | /projects/sirius/backend\_pool/final\_database/netlist/sirius\_sub\_2.v.gz  /archive/lhu/Sirius/backend\_pool/top/final\_database/top\_postcts.v  /projects/sirius/backend\_pool/final\_database/netlist/sirius\_sub\_4.v.gz  /projects/sirius/backend\_pool/final\_database/netlist/a7\_harden\_subsystem\_postcts.v.gz  /projects/sirius/backend\_pool/final\_database/netlist/cortexa7core\_postcts.v.gz  /projects/sirius/backend\_pool/final\_database/netlist/sirius\_sub\_ca7.v.gz  /projects/sirius/backend\_pool/final\_database/netlist/DDR\_TOP\_postcts.v.gz |
| Sdf | /home/lhu/eda12/proj/sirius/trunk/sim2/testbench/tb\_common/testbench.v line 252 ~ line280 |
| Logs | /home/lhu/eda12/proj/sirius/trunk/sim2/sim\_system\_mini/tmpdir/jpeg\_clksw\_test\_VCS /simv.log |
| Wave | /home/lhu/eda12/proj/sirius/trunk/sim2/sim\_system\_mini/tmpdir/jpeg\_clksw\_test\_VCS /novas.fsdb |
| Result | Check waveform |
| Cmd | Compile: scompile jpeg\_clksw\_test -docompile -dofwgen –norun |
| Run: scompile jpeg\_clksw\_test –nocompile –mywave.do |
| Note | Key files: mydefine.v myenvvar C\_testcases/jpeg\_clksw\_test/main\_a7.c mywave.do |
| filelist2/rtl\_vcs.f  filelist2/sirius\_top.f  filelist2/a7\_harden\_subsystem.f  filelist2/a7\_subsystem.f  filelist2/ddr\_vcs\_nls.f  sim2/testbench/tb\_common/vcodec/check\_save.v  sim2/testbench/tb\_common/h264\_top\_tb.v  sim2/testbench/tb\_common/post\_timing\_disable\_warning.v  sim2/testbench/tb\_common/testbench.v |

|  |  |
| --- | --- |
| h) sub2+top+sub\_top+sub4+ca7+ddr netlist (1021) + SDF (cworst) | |
| Dir | /home/lhu/eda12/proj/sirius/trunk/sim2/sim\_system\_mini/tmpdir/disp\_clksw\_test\_VCS |
| Netlist | /projects/sirius/backend\_pool/final\_database/netlist/sirius\_sub\_2.v.gz  /archive/lhu/Sirius/backend\_pool/top/final\_database/top\_postcts.v  /projects/sirius/backend\_pool/final\_database/netlist/sirius\_sub\_4.v.gz  /projects/sirius/backend\_pool/final\_database/netlist/a7\_harden\_subsystem\_postcts.v.gz  /projects/sirius/backend\_pool/final\_database/netlist/cortexa7core\_postcts.v.gz  /projects/sirius/backend\_pool/final\_database/netlist/sirius\_sub\_ca7.v.gz  /projects/sirius/backend\_pool/final\_database/netlist/DDR\_TOP\_postcts.v.gz |
| Sdf | /home/lhu/eda12/proj/sirius/trunk/sim2/testbench/tb\_common/testbench.v line 252 ~ line280 |
| Logs | /home/lhu/eda12/proj/sirius/trunk/sim2/sim\_system\_mini/tmpdir/disp\_clksw\_test\_VCS /simv.log |
| Wave | /home/lhu/eda12/proj/sirius/trunk/sim2/sim\_system\_mini/tmpdir/disp\_clksw\_test\_VCS /novas.fsdb |
| Result | Check waveform |
| Cmd | Compile: scompile disp\_clksw\_test -docompile -dofwgen –norun |
| Run: scompile disp\_clksw\_test –nocompile –mywave.do |
| Note | Key files: mydefine.v myenvvar C\_testcases/disp\_clksw\_test/main\_a7.c mywave.do |
| filelist2/rtl\_vcs.f  filelist2/sirius\_top.f  filelist2/a7\_harden\_subsystem.f  filelist2/a7\_subsystem.f  filelist2/ddr\_vcs\_nls.f  sim2/testbench/tb\_common/vcodec/check\_save.v  sim2/testbench/tb\_common/h264\_top\_tb.v  sim2/testbench/tb\_common/post\_timing\_disable\_warning.v  sim2/testbench/tb\_common/testbench.v |

|  |  |
| --- | --- |
| i) sub2+top+sub\_top+sub4+ca7+ddr netlist (1021) + SDF (cworst) | |
| Dir | /home/lhu/eda12/proj/sirius/trunk/sim2/sim\_system\_mini/tmpdir/h264shram\_test\_VCS |
| Netlist | /projects/sirius/backend\_pool/final\_database/netlist/sirius\_sub\_2.v.gz  /archive/lhu/Sirius/backend\_pool/top/final\_database/top\_postcts.v  /projects/sirius/backend\_pool/final\_database/netlist/sirius\_sub\_4.v.gz  /projects/sirius/backend\_pool/final\_database/netlist/a7\_harden\_subsystem\_postcts.v.gz  /projects/sirius/backend\_pool/final\_database/netlist/cortexa7core\_postcts.v.gz  /projects/sirius/backend\_pool/final\_database/netlist/sirius\_sub\_ca7.v.gz  /projects/sirius/backend\_pool/final\_database/netlist/DDR\_TOP\_postcts.v.gz |
| Sdf | /home/lhu/eda12/proj/sirius/trunk/sim2/testbench/tb\_common/testbench.v line 252 ~ line280 |
| Logs | /home/lhu/eda12/proj/sirius/trunk/sim2/sim\_system\_mini/tmpdir/h264shram\_test\_VCS /simv.log |
| Wave | /home/lhu/eda12/proj/sirius/trunk/sim2/sim\_system\_mini/tmpdir/h264shram\_test\_VCS /novas.fsdb |
| Result | Check waveform |
| Cmd | Compile: scompile h264shram\_test -docompile -dofwgen –norun |
| Run: scompile h264shram\_test –nocompile –mywave.do |
| Note | Key files: mydefine.v myenvvar C\_testcases/h264shram\_test/main\_a7.c mywave.do |
| filelist2/rtl\_vcs.f  filelist2/sirius\_top.f  filelist2/a7\_harden\_subsystem.f  filelist2/a7\_subsystem.f  filelist2/ddr\_vcs\_nls.f  sim2/testbench/tb\_common/vcodec/check\_save.v  sim2/testbench/tb\_common/h264\_top\_tb.v  sim2/testbench/tb\_common/post\_timing\_disable\_warning.v  sim2/testbench/tb\_common/testbench.v |

## LeiYu: HEVC

|  |  |
| --- | --- |
| a) soc rtl + hevc netlist (0929) NoSDF | |
| Dir | /video\_space/video/lyu/tmp\_sirius/trunk/sim2/sim\_system\_post/ |
| Netlist | /video\_space/video/lyu/hevc\_post/0929/hevc\_top.v.pr.0929 |
| Sdf |  |
| Logs | /video\_space/video/lyu/hevc\_post/log/0929\_netlist.log |
| Wave |  |
| Result | Check wave form; save rtl's bitstream and use hevcvisa display right |
| Cmd | Compile: scompile h5esim\_test -docompile -nofwgen –norun |
| Run: ./run\_sim -f -r |
| Note | Key files: mydefine.v myenvvar C\_testcases/h5esim\_test/main\_a7.c tb.sim.f mywave.do /tmpdir/h5esim\_test\_VCS/h265\_testcase postfiles/mem\_init\_0\_1024x32.dat mem\_init\_1\_1024x32.dat |
| DO USE mem\_init\_0\_1024x32.dat/mem\_init\_1\_1024x32.dat initial …/hevc\_top\_inst/uhevc\_core.\_u\_vcodec\_hevc.u\_wave420\_mg\_vcore\_top.vcpu\_dc\_data1.uHEVC\_RG\_1P\_1024X32B1 Before enable hevc |

|  |  |
| --- | --- |
| b) soc rtl + hevc netlist (1021) NoSDF | |
| Dir | /video\_space/video/lyu/tmp\_sirius/trunk/sim2/sim\_system\_post/ |
| Netlist | /soc\_space/20171021/netlist/hevc\_top.v.gz |
| Sdf |  |
| Logs | /video\_space/video/lyu/tmp\_sirius/trunk/sim2/sim\_system\_post/tmpdir/h5esim\_test\_VCS/simv.log |
| Wave |  |
| Result | Check wave form; save rtl's bitstream and use hevcvisa display right |
| Cmd | Compile: scompile h5esim\_test -docompile -nofwgen –norun |
| Run: ./run\_sim -f -r |
| Note | Key files: mydefine.v myenvvar C\_testcases/h5esim\_test/main\_a7.c tb.sim.f mywave.do /tmpdir/h5esim\_test\_VCS/h265\_testcase postfiles/ |
| DO USE mem\_init\_0\_1024x32.dat/mem\_init\_1\_1024x32.dat initial …/hevc\_top\_inst/uhevc\_core.\_u\_vcodec\_hevc.u\_wave420\_mg\_vcore\_top.vcpu\_dc\_data1.uHEVC\_RG\_1P\_1024X32B1 Before enable hevc |

|  |  |
| --- | --- |
| c) soc rtl + hevc netlist (0929) + SDF(worst) | |
| Dir | /video\_space/video/lyu/tmp\_sirius/trunk/sim2/sim\_system\_post\_sdf |
| Netlist | /video\_space/video/lyu/hevc\_post/0929/hevc\_top.v.pr.0929 |
| Sdf | /video\_space/video/lyu/hevc\_post/0929/sirius\_top.37077358332.flat\_func\_merge.wcl\_cworst\_CoreND\_IOND.cworst\_m40\_flat.setup1.hold0.clkearly0.961\_clklate1.039\_dataearly0.961\_datalate1.077.SI1.postcts1.20170929.hevc\_top.sdf.0929 |
| Logs | /video\_space/video/lyu/hevc\_post/log/0929\_setup.log |
| Wave |  |
| Result | Check simv.log without "violation" after RESET; Check wave form; save rtl's bitstream and use hevcvisa display right |
| Cmd | Compile: scompile\_sdf h5esim\_test -docompile -nofwgen –norun |
| Run: ./run\_sim -f -r |
| Note | Key files: mydefine.v myenvvar C\_testcases/h5esim\_test/main\_a7.c tb.sim.f mywave.do hevc\_distiming.do /tmpdir/h5esim\_test\_VCS/h265\_testcase postfiles/delay.v |
| Initial HEVC\_RG\_1P\_1024X32B1 Before enable hevc; Use delay.v moduel to delay axi output signals 0.5-cycle & stretch 0.5-cycle |

|  |  |
| --- | --- |
| d) soc rtl + hevc netlist (1021) + SDF(worst) | |
| Dir | /video\_space/video/lyu/tmp\_sirius/trunk/sim2/sim\_system\_post\_sdf |
| Netlist | /soc\_space/20171021/netlist/hevc\_top.v.gz |
| Sdf | /soc\_space/20171021/func\_sdf/sirius\_top.28595326880.flat\_func\_merge.wcl\_cworst\_CoreND\_IOND.cworst\_m40\_flat.setup1.hold0.clkearly0.961\_clklate1.039\_dataearly0.961\_datalate1.077.SI1.postcts1.20171019.hevc\_top.sdf.gz |
| Logs | /video\_space/video/lyu/tmp\_sirius/trunk/sim2/sim\_system\_post\_sdf/tmpdir/h5esim\_test\_VCS/simv.log |
| Wave |  |
| Result | Check simv.log without "violation" after RESET; Check wave form; save rtl's bitstream and use hevcvisa display right |
| Cmd | Compile: scompile\_sdf h5esim\_test -docompile -nofwgen –norun |
| Run: ./run\_sim -f -r |
| Note | Key files: mydefine.v myenvvar C\_testcases/h5esim\_test/main\_a7.c tb.sim.f mywave.do hevc\_distiming.do /tmpdir/h5esim\_test\_VCS/h265\_testcase postfiles/delay.v |
| Initial HEVC\_RG\_1P\_1024X32B1 Before enable hevc; Use delay.v moduel to delay axi output signals 0.5-cycle & stretch 0.5-cycle |

|  |  |
| --- | --- |
| e) testebnch(rtl) + hevc pg netlist (1021) | |
| Dir | /video\_space/video/lyu/tmp\_sirius/trunk/sim2/sim\_hevc/cnm-wave420-verilog\_n\_testbench-v1.8.0/sim/vectors/codec |
| Netlist | /soc\_space/20171021/pg\_netlist/hevc\_top.pg.v.gz |
| Sdf |  |
| Logs | /video\_space/video/lyu/tmp\_sirius/trunk/sim2/sim\_hevc/cnm-wave420-verilog\_n\_testbench-v1.8.0/sim/vectors/codec/simv.log |
| Wave | /video\_space/video/lyu/tmp\_sirius/trunk/sim2/sim\_hevc/cnm-wave420-verilog\_n\_testbench-v1.8.0/sim/vectors/codec/pg\_000.fsdb |
| Result | Check wave form; before power off write/read apb's register right, after power re-enable write/read apb's register right |
| Cmd | Compile: ./runif.pl |
| Run: ./runif.pl |
| Note | Key files: /video\_space/video/lyu/tmp\_sirius/trunk/sim2/sim\_hevc/cnm-wave420-verilog\_n\_testbench-v1.8.0/sim/testbench\_v/testbench\_pg.v post\_files/post\_cell.v |
| define DITS\_PINS to enable stand cell with power pins; use with power pins sram model; Add some DCAP's cell model; |

|  |  |
| --- | --- |
| f) Wholechip netlist + sdf ( 1021 bc ) | |
| Dir | */video\_space/video/jlliu/backup/sirius/trunk/sim2/sim\_system\_hevc\_prnls\_wholechip\_min/tmpdir/hevcpostsim\_test\_VCS* |
| Netlist | *See tb.sim.f* |
| Sdf | See simv.log |
| Logs | simv.log |
| Wave |  |
| Result | Check wave form, get a couple of bitstream writes are matched with YULei’s result (sim\_system\_post/tmpdir/).  第一笔的a0e00000的写是matched。 |
| Cmd | Compile: scompile hevcpostsim\_test -docompile -dofwgen –norun  Run: make sim –f Makefile\_sim |
| Note | Key files: mydefine.v myenvvar vcsfiles/initreg\_file vcsfiles/synchronizer.lst mywave.do tb.sim.f hevc\_distiming.do  Before configure PMU info, please firstly configure PUM protected register to be 0xacce55.  Note: Close ddr training in DDR.c code. |

## Jlliu: SUB2( H264 )

1. Sub2 netlist + RTL + nosdf (0929)

|  |  |
| --- | --- |
|  |  |
| Dir | */video\_space/video/jlliu/backup/sirius/trunk/sim2/sim\_system\_sub2\_prnls\_nosdf/tmpdir/sub2postsim\_test\_VCS* |
| Netlist | */projects/sirius/backend\_pool/sub\_2/0929/sirius\_sub\_2.v.pr.0929.gz* |
| Sdf |  |
| Logs | simv.log |
| Wave |  |
| Result | rtl\_h264.bs, RTL\_H264\_APB\_WRITE.txt, RTL\_SUB2\_AXI\_xxx.txt |
| Cmd | compile & run : scompile\_nosdf sub2postsim\_test -docompile -dofwgen -dorun |
| Note | * + - * 1. ddr.c: Mapping is that #if 0 .         2. cortexa7: Makefile is refined to speed up simulation, to reduce the .data section size. |

1. Sub2 netlist + RTL + sdf (0929 wc)

|  |  |
| --- | --- |
|  |  |
| Dir | */video\_space/video/jlliu/backup/sirius/trunk/sim2/sim\_system\_sub2\_prnls/tmpdir/sub2postsim\_test\_VCS* |
| Netlist | */projects/sirius/backend\_pool/sub\_2/0929/sirius\_sub\_2.v.pr.0929.gz* |
| Sdf | See simv.log |
| Logs | Simv.log |
| Wave | Wave\_000.fsdb – wave\_023.fsdb |
| Result | rtl\_h264.bs, RTL\_H264\_APB\_WRITE.txt, RTL\_SUB2\_AXI\_xxx.txt  only I frame is encoded, then the simulation is termitted. I frame are matched with that no\_sdf |
| Cmd | compile: scompile sub2postsim\_test -docompile -dofwgen –norun  run: make sim -f Makesim\_sim |
| Note | disable timing: mywave.do  violation: there are two violations.  Timing violation in testbench.u\_sirius\_top.sirius\_sub\_2\_inst.h264\_top\_inst.u\_coda980\_msvc.u\_vce\_top.u\_vce\_core\_loop.u\_qcm\_if.u\_qcm\_if\_nzflag.u\_flag15.clk\_gate\_nzflag\_2\_reg.latch  They are because of internal reset( IP into IDLE ), this reset cause signals transition, and this is async, which casue this vio. This can be ignore. |

1. Wholechip netlist + sdf (0929 wc)

|  |  |
| --- | --- |
|  |  |
| Dir | */video\_space/video/jlliu/backup/sirius/trunk/sim2/sim\_system\_sub2\_prnls\_wholechip/tmpdir/sub2postsim\_test\_VCS* |
| Netlist | *See tb.sim.f* |
| Sdf | See simv.log |
| Logs | Simv.log simv\_start\_breakpoint.log |
| Result | This simulation is FAILED. Since ddr model is not updated by Maji, the read data is not written data. |
| Cmd |  |
| Note | This simulation is Failed. The passed one is the following ( d ).  Open ddr training in ddr.c code. |

1. Wholechip netlist + sdf (0929 wc)

Don’t know why, this simulation directory is lost without any rm operation.

To prove post simulation pass, please refer to ( e ) item, which is the finial netlist.

|  |  |
| --- | --- |
|  |  |
| Dir | */video\_space/video/jlliu/backup/sirius/trunk/sim2/sim\_system\_sub2\_prnls\_wholechip\_new/tmpdir/sub2postsim\_test\_VCS* |
| Netlist | *See tb.sim.f* |
| Sdf | See simv.log |
| Logs | Simv.log |
| Result | RTL\_SUB2\_AXI\_XXX.txt  ( which compare with those txt in (b) item to check if pass or not. Note, some data maybe sampled multiple times, this is because of my testbench, the clock phase can't be matched with data.) |
| Cmd | set POST\_SIM 1 in myenvvar  scompile sub2postsim\_test -docompile -dofwgen –norun  make sim -f Makefile\_sim |
| Note | key files: mydefine.v myenvvar vcsfiles/initreg\_file vcsfiles/synchronizer.lst mywave.do tb.sim.f  don't know why i can't find this directory. I never did remove operation.  please check the tb.sim.f file to check all netlist.  please to check simv.log to check all sdf files.  in order to make filelists are available for rtl simulation, I've moved the ddr netlist filelist to tb.sim.f.  Open ddr training in ddr.c code. |

1. Wholechip netlist + sdf (1021 wc)

|  |  |
| --- | --- |
|  |  |
| Dir | */video\_space/video/jlliu/backup/sirius/trunk/sim2/sim\_system\_sub2\_prnls\_wholechip\_1021nls/tmpdir/sub2postsim\_test\_VCS* |
| Netlist | *See tb.sim.f* |
| Sdf | See simv.log |
| Logs | Simv.log |
| Result | RTL\_SUB2\_AXI\_xxx.txt  11/3: 我已经check了RTL\_H264\_AXI\_WRITE.txt，能够完全比对上。  ( which compare with those txt in (b) item to check if pass or not. Note, some data maybe sampled multiple times, this is because of my testbench, the clock phase can't be matched with data.) |
| Cmd | set POST\_SIM 1 in myenvvar file  scompile sub2postsim\_test -docompile -dofwgen –norun  make sim -f Makefile\_sim |
| Note | key files: mydefine.v myenvvar vcsfiles/initreg\_file vcsfiles/synchronizer.lst mywave.do tb.sim.f  if with ddr netlist, please be care that filelist2/rtl\_vcs.f must remove the ddr rtl file list, otherwise scompile will be error.  Open ddr training in ddr.c code. |

1. Wholechip netlist + sdf (1021 bc)

|  |  |
| --- | --- |
|  |  |
| Dir | */video\_space/video/jlliu/backup/sirius/trunk/sim2/sim\_system\_hevc\_prnls\_wholechip\_min/tmpdir/sub2postsim\_test\_VCS* |
| Netlist | *See tb.sim.f* |
| Sdf | See simv.log |
| Logs | Simv.log |
| Result | RTL\_SUB2\_AXI\_xxx.txt  11/3: 我已经check了RTL\_H264\_AXI\_WRITE.txt，能够完全比对上。  ( which compare with those txt in (b) item to check if pass or not. Note, some data maybe sampled multiple times, this is because of my testbench, the clock phase can't be matched with data.) |
| Cmd | set POST\_SIM 1 in myenvvar file  scompile sub2postsim\_test -docompile -dofwgen –norun  make sim -f Makefile\_sim |
| Note | Key files: mydefine.v myenvvar vcsfiles/initreg\_file vcsfiles/synchronizer.lst mywave.do tb.sim.f hevc\_distiming.do  Before configure PMU info, please firstly configure PUM protected register to be 0xacce55.  Note: Close ddr training in DDR.c code. |