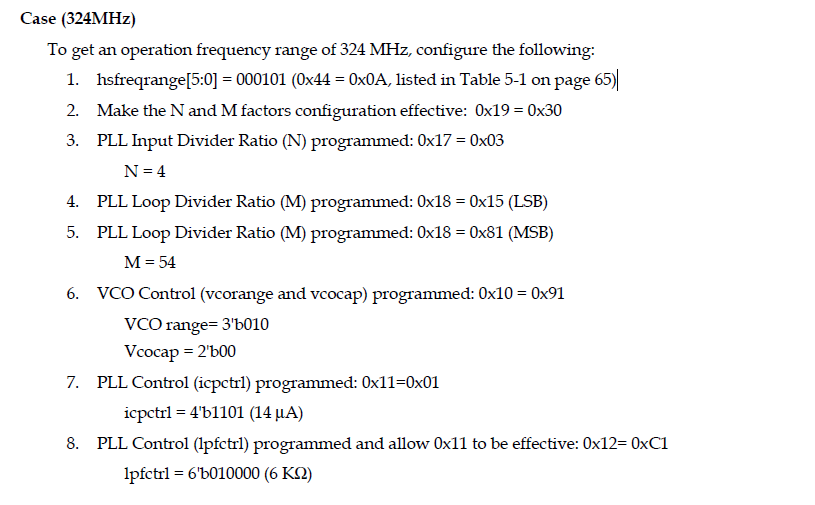
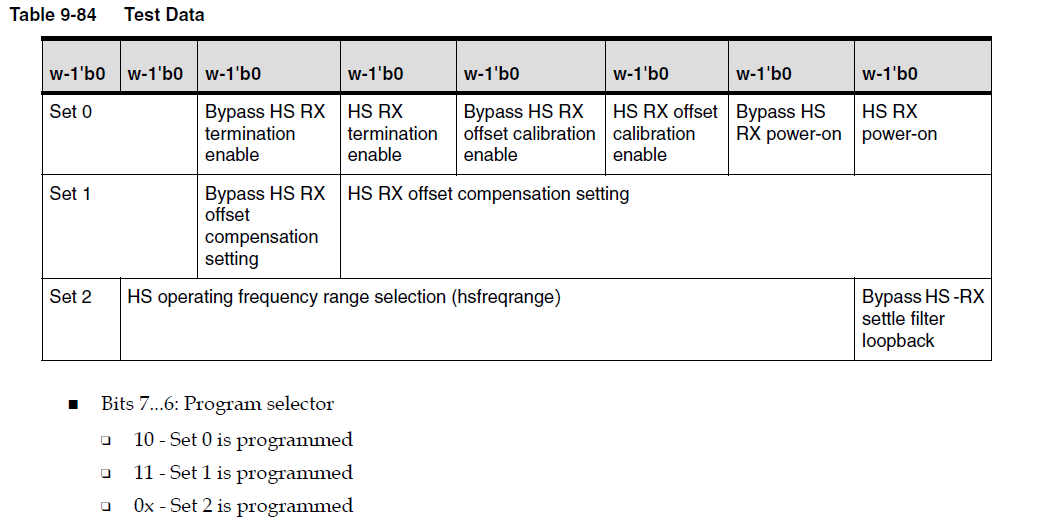
1. PLL\_CFG

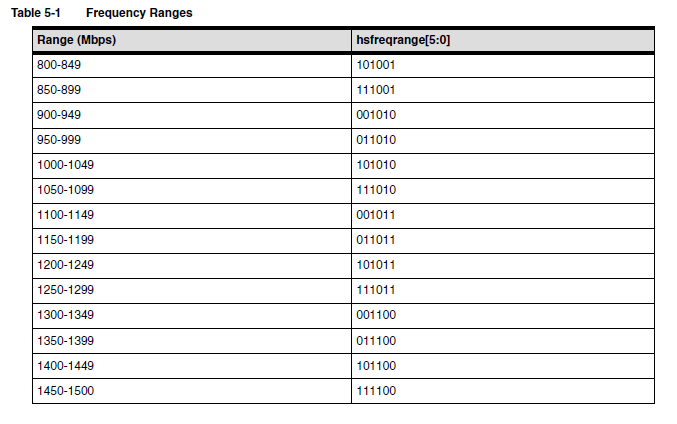
Example:



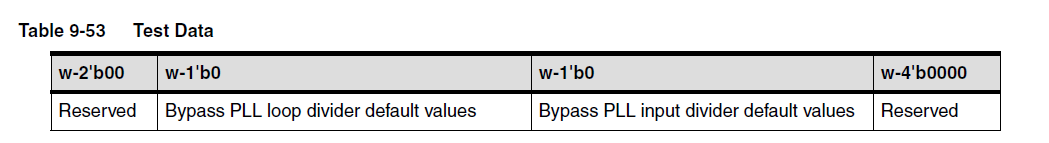
Note: <phy\_reset=0&&phy\_shutdown=0>, testclr< high pluse>

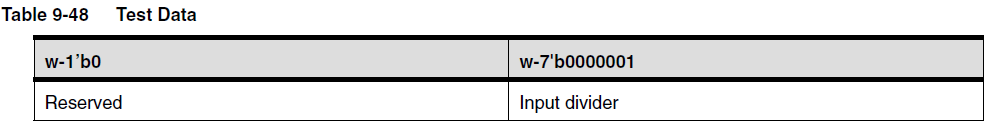
1,hsfreqrange;

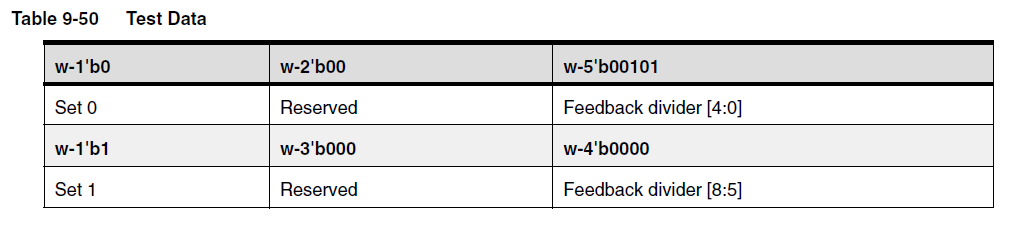




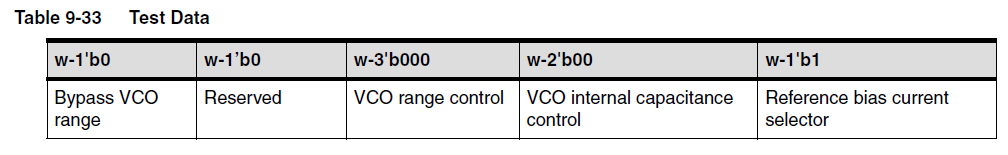
2,N/M;

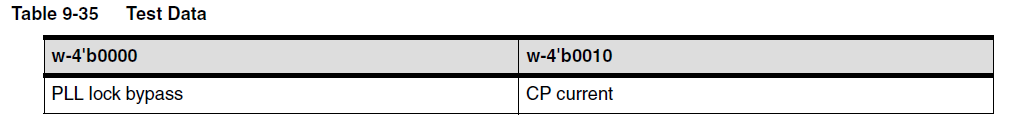


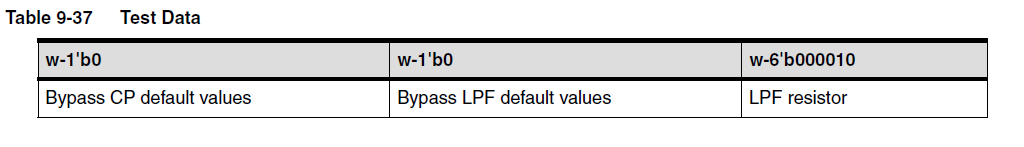


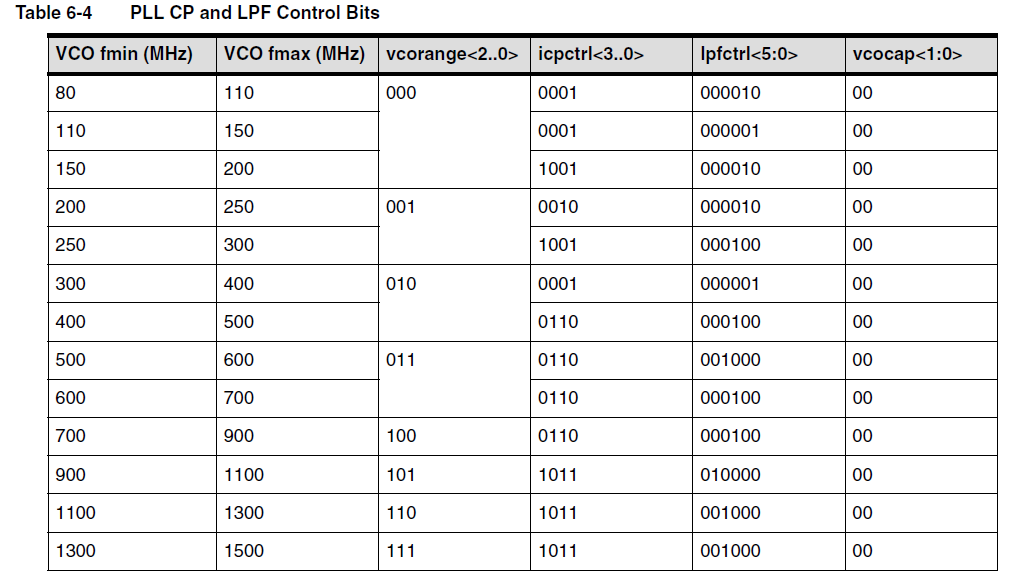


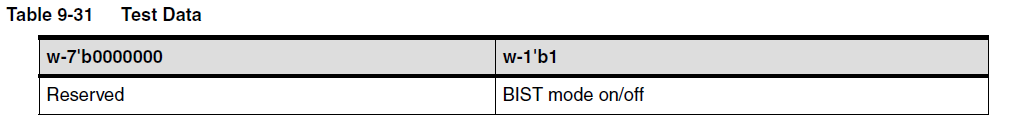
3. vcorange/vcocap/icpctrl/lpfctrl

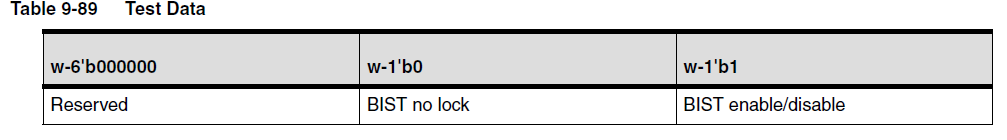


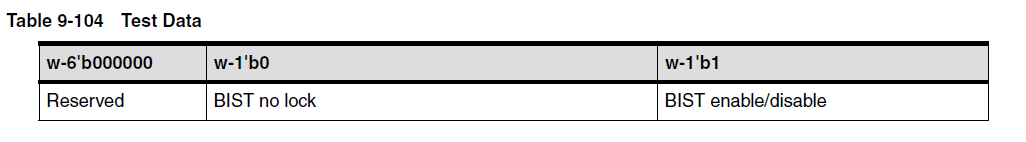












**HOST\_CFG/**

**Number of lanes/interrupt/data\_type/sync\_feathers/timing\_mode/has/hbp/hfp/**