**MIPI\_ATE\_TEST**

Revision history

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| --- | --- | --- | --- |
| Revision | Date | Description | Author |
| 0.1 | 2017-09-13 | Initial | ZhengXie |
| 0.2 |  |  |  |
|  |  |  |  |

# 1. IP overview

## ATE test Design

The DPHY relative signal with ATE test is connected to Sirius I/O pad with mux isolation to provide top-level controllability and observability, the corresponding signal and pad is as follows:

ATE\_TEST\_IN:

|  |  |  |
| --- | --- | --- |
| Pad name | ATE\_Test\_In | Signal name |
| QE0\_0 | ATE\_IN[0] | SHUTDOWNZ |
| QE0\_1 | ATE\_IN[1] | RSTZ |
| QE0\_2 | ATE\_IN[2] | -- |
| QE0\_3 | ATE\_IN[3] | -- |
| QE0\_4 | ATE\_IN[4] | MASTERSLAVEZ |
| QE0\_5 | ATE\_IN[5] | BASEDIR0 |
| QE0\_6 | ATE\_IN[6] | BASEDIR1 |
| QE0\_7 | ATE\_IN[7] | ENABLECLK |
| I2S\_WS2 | ATE\_IN[8] | ENABLE0 |
| I2S\_SDI2 | ATE\_IN[9] | ENABLE1 |
| I2S\_SDO2 | ATE\_IN[10] | BISTON |
| I2S\_CLK2 | ATE\_IN[11] | TESTCLK |
| I2S\_WS3 | ATE\_IN[12] | TESTCLR |
| I2S\_SDI3 | ATE\_IN[13] | TESTEN |
| I2S\_SDO3 | ATE\_IN[14] | TESTDIN[0] |
| I2S\_CLK3 | ATE\_IN[15] | TESTDIN[1] |
| GP0 | ATE\_IN[16] | TESTDIN[2] |
| GP1 | ATE\_IN[17] | TESTDIN[3] |
| GP2 | ATE\_IN[18] | TESTDIN[4] |
| GP3 | ATE\_IN[19] | TESTDIN[5] |
| GP4 | ATE\_IN[20] | TESTDIN[6] |
| GP5 | ATE\_IN[21] | TESTDIN[7] |
| GP6 | ATE\_IN[22] | [2:0]  DPHY Select |
| GP7 | ATE\_IN[23] |
| UART\_RX2 | ATE\_IN[24] |

ATE\_TEST\_OUT

|  |  |  |
| --- | --- | --- |
| Pad name | ATE\_Test\_out | Signal name |
| PCLK1 | ATE\_TEST\_OUT[0] | BISTOK |
| DE1 | ATE\_TEST\_OUT[1] | PLL\_LOCK |
| VSYNC1 | ATE\_TEST\_OUT[2] | STOPSTATECLK |
| HSYNC1 | ATE\_TEST\_OUT[3] | STOPSTATEDATA\_0 |
| QE1\_0 | ATE\_TEST\_OUT[4] | STOPSTATEDATA\_1 |
| QE1\_1 | ATE\_TEST\_OUT[5] | TESTDOUT[0] |
| QE1\_2 | ATE\_TEST\_OUT[6] | TESTDOUT[1] |
| QE1\_3 | ATE\_TEST\_OUT[7] | TESTDOUT[2] |
| QE1\_4 | ATE\_TEST\_OUT[8] | TESTDOUT[3] |
| QE1\_5 | ATE\_TEST\_OUT[9] | TESTDOUT[4] |
| QE1\_6 | ATE\_TEST\_OUT[10] | TESTDOUT[5] |
| QE1\_7 | ATE\_TEST\_OUT[11] | TESTDOUT[6] |
| PCLK0 | ATE\_TEST\_OUT[12] | TESTDOUT[7] |

## ATE Test Architecture

As eight DPHY is to be tested, ATE\_TEST\_IN[24:22] is used to control the test order.

There are two PLL which is connected with DPHY\_0 and DPHY\_1 respectively. The power on sequence is as follows:  
PLL\_0/PLL\_1/DPHY0/DPHY1🡪DPHY1🡪DPHY2🡪DPHY3🡪DPHY4🡪DPHY5🡪DPHY6🡪DPHY7

The ATE\_TEST architecture is below:



# 2. ATE test

This section presents an example for a possible set of tests that can be used for test production under ATE environment. The focus is on both parametric and functional tests.

## **Shutdown**

This test verifies that, when placed in Shutdown mode, the PHY is characterized by the lowest power consumption of all powered modes, mostly deriving from internal leakage currents. No activity on the PHY is expected.

**Setup sequence:**

1. Set SHUTDOWNZ and RSTZ signals to logic low, and TESTCLR to logic high. This step places the PHY in Shutdown mode; in Master mode, this step also sets ONPLL to logic low, putting the PLL in Shutdown mode.

2. Ensure that no clock is driving the PHY (CFG\_BCLK, TXCLKESC, TXBYTECLKHS, TESTCLK, REFCLK, and SCANCLK).

**Measure:**

3. Check that all digital outputs referred to as externally observable are at default values, usually logic-low state;

4. No clock should be output by the PHY when placed in this mode.

5. Measure the power consumption from both digital and analog supplies to check that they are at the minimum values as defined in “Power Consumption” on page 230.

## PLL Locking (D-PHY Master Only)

This test checks if the PLL has properly locked, a crucial condition for the proper initialization of the PHY in Master mode.

**Setup sequence:**

1. Set SHUTDOWNZ and RSTZ signals to logic low, and TESTCLR to logic high.

2. Apply an appropriate frequency to the REFCLK signal; REFCLK=24MHZ, directly from CGU.

3. Apply an appropriate frequency to the CFG\_CLK signal; REFCLK=24MHZ, directly from CGU.

4. Set MASTERSLAVEZ = 1 for Master mode selection.

5. Wait for 15 ns.

6. Set TESTCLR to low.

7. Wait for 15 ns.

8. Configure Test Code 0x44 hsfreqrange based on the frequency range.

9. Configure PLL parameters:

* VCO Control (vcorange and vcocap): Test Code 0x10
* PLL Control (icpctrl): Test Code 0x11
* PLL Control (lpfctrl): Test Code 0x12
* PLL Input Divider Ratio (N): Test Code 0x17
* PLL Loop Divider Ratio (M): Test Code 0x18

10. Set ENABLE\_*N* to logic high.

11. Wait 5 ns.

12. Set SHUTDOWNZ signal to logic high.

13. Wait 5 ns.

14. Set RSTZ signal to logic high.

**Measure**

15. Wait for 1 ms after the SHUTDOWNZ and RSTZ signals are released.

16. Check that the LOCK signal is asserted.

## **AFE Initialization**

This test verifies the completeness of the AFE initialization process, whether the PHY is configured as Master or Slave.

**Setup sequence:**

1. Depending on whether the PHY is to be tested in Master or Slave mode, follow the appropriate steps.

**Master:**

* Perform step1 to step 9 of the section “PLL Locking (D-PHY Master Only)” .
* Configure the following analog references of Test Code 0x22:
* bandgap reference voltage
* BIASEXTR internal resistor control
* LPTX bias current control
* Set BASEDIR\_N to low.
* Perform step 10 to step 14 of the section “PLL Locking (D-PHY Master Only)”
* Continue with AFE Initialization steps.

**Slave:**

* Perform step1 and steps 3 to 8 of the section “PLL Locking (D-PHY Master Only)” ; ensure that MASTERSLAVEZ = 0.
* Configure the following analog references of Test Code 0x22:
* BIASEXTR internal resistor control
* LPTX bias current control
* Set BASEDIR\_N to high.
* Perform step 10 to step 14 of the section “PLL Locking (D-PHY Master Only)”
* Continue with AFE Initialization steps.
* Drive LP-11 through the clock lane and all enabled data lanes.

**Measure:**

1. Wait for 500 μs.

The initialization sequence determines that biasing blocks are enabled first. After the related voltage and current references get settled, a second step is triggered where the internal calibrations are performed. This can include internal resistors, receivers offset compensation, and so on. The 500 μs time is sufficient to accommodate the complete initialization process with different CFG\_CLK frequencies.

4. Check that the STOPSTATEDATA\_N and STOPSTATECLK PPI signals for the data lanes and clock lane are asserted.

5. In Master mode, evaluate the DC level in all enabled data lanes and clock lane, and ensure they conform to the specification values for VOH of LP-TX provided in Table 12-4 on page 231.

## High-Speed BIST

A High-Speed BIST test enables a functional verification of the overall mixed-signal logic present in the data lanes through the use of an internal loopback connection, in each lane and a PRBS generator.

A High-Speed BIST test is an intra-lane test, while a High-Speed loopback is an inter-lane test.

**Setup sequence:**

1-9. Perform step1 to step 9 of the section “PLL Locking (D-PHY Master Only)”

10. Apply an appropriate frequency to the TXBYTECLKHS signal; The TXBYTECLKHS signal is generated from the PLL out clock.

11. Set ENABLE\_*N* to logic high.

12. Wait 5 ns.

13. Set the SHUTDOWNZ signal to logic high.

14. Wait 5 ns.

15. Set the RSTZ signal to logic high.

16. Wait for 1.5 ms for the initialization period.

**17. [Measure 1]**

18. Set BISTON to 1'b1.

**19. [Measure 2]**

20. Set BISTON to 1'b0.

**Measures:**

* [Measure 1]

Check that the STOPSTATEDATA\_0 and STOPSTATEDATA\_1 signals are asserted LP-TX to LP-RX.

* [Measure 2]

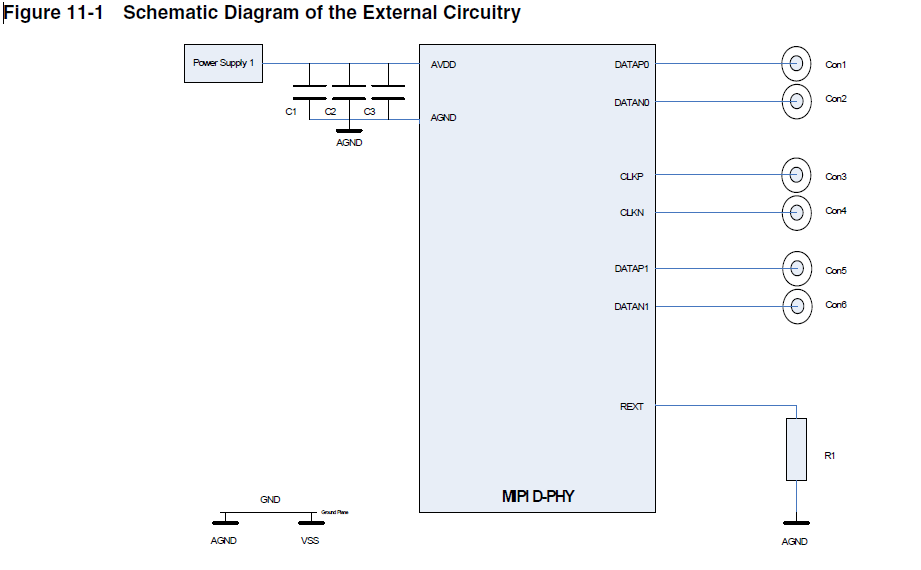
Check that the BISTOK signal is asserted.

* 60 us, when maximum serial data rate is set to 80 Mbps
* 7.2 us, when maximum serial data rate is set to 1 Gbps
* 5.7 us, when maximum serial data rate is set to 1.5 Gbps

In our ATE high-speed bist test, 1.5 Gbps is selected.

# 3. Schematic Diagram

The figure below shows a high level schematic diagram of the external circuitry required by the PHY. The table provides the power supply requirements.



**Figure schematic diagram of the external circuitry**

