**IP engineering spec**

Revision history

|  |  |  |  |
| --- | --- | --- | --- |
| Revision | Date | Description | Author |
| 0.1 | 2016-11-14 | Initial | xxx |
| 0.2 |  |  |  |
|  |  |  |  |

# IP overview

## Introduce the IP’s features, functions

xxxxxxxxx

## Block diagram

Top diagram

# Hardware interface description

## Input/output signals

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Port name | Input/output | width | Clock (domain) | Description |
| **System signal** | | | | |
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## More description on the input/output signals

### Interface protocol

### Requirements on the signals (clock, reset, …)

RESETN: it is asynchronous reset signal for this module.

CLK: it can be gated by ACTIVE signal to save power.

# Software interface description

## Register definition

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Register name | width | offset | R/W | description |
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# Memory requirement

(With below description for each UMAC agent or PMAN node)

## Memory space requirement

## Memory bandwidth requirement in each use case scenario

### Memory access pattern (burst characteristics)

### Memory latency requirement (consequence if the latency is not guaranteed)

### Peak bandwidth and average bandwidth requirement

# Power saving modes

## Clock gating/throttling, automatic or register controllable.

## Clock frequency per use case

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## Power down control for ROM/RAM/analog macros.

No.

## Power Island (if applicable)

No.

# Synthesis tips

## Suggestions for Placement in terms of performance, routing, timing, etc.

## Suggestions for Routing

## Suggestions for clock tree

## Information on LVT/SVT ratio to achieve timing closure

## Information on gate count, timing constraints

# DFT/test

## Test scheme for each of ROM/RAM/OTP/analog macros

### Input/output signal requirement

### Register setting

## Test scheme for special logic (asynchronous logic, clock generation logic, reset logic, etc)

# Performance tuning, IP profiling and debugging

# ROM/RAM/analog macro spec (requirement)

## Macro list with detail requirement

## Interface description (waveform)

# I/O pad requirement

## Clock I/O

## Fast speed I/O

## I/O with different power (other than 3.3V digital and DDR I/O)