



Arquitectura de Computadoras

LAB 5 part 1

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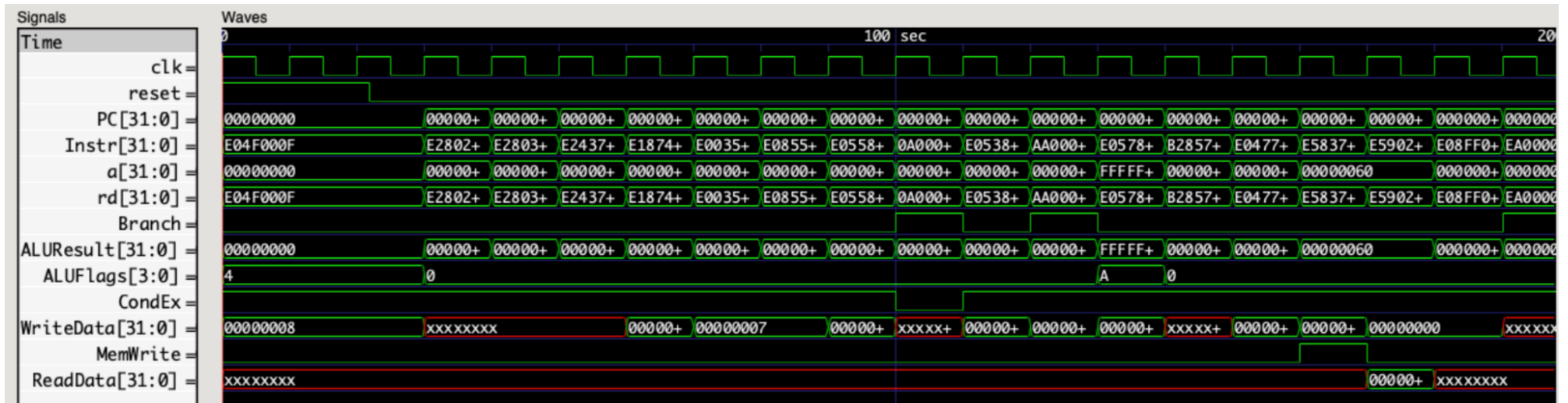
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Cycle	reset	PC	Instr	SrcA	SrcB	Branch	AluResult	Flags _{3:0} [NZCV]	CondEx	WriteData	MemWrite	ReadData
1	1	00	SUB R0, R15, R15 E04F000F	8	8	0	0	?	1	8	0	x
2	0	04	ADD R2, R0, #5 E2802005	0	5	0	0	?	1	x	0	x
3	0	08	ADD R3, R0, #12 E280300C	0	C	0	5	?	1	x	0	x
4	0	0C	SUB R7, R3, #9	C	9	0	C	4	1	x	0	x
5	0	10	ORR R4, R7, R2	3	5	0	3	0	1	x	0	x
6	0	14	AND R5, R3, R4	C	7	0	7	0	1	5	0	x
7	0	18	ADD R5, R5, R4	4	7	0	4	0	1	7	0	x
8	0	1C	SUBS R8, R5, R7	B	3	0	B	0	1	7	0	x
9	0	20	BEQ END	28	30	0	8	0	1	3	0	x
10	0	24	SUBS R8, R3, R4	C	7	1	58	0	0	x	0	x
11	0	28	BGE AROUND	30	0	0	5	0	1	7	0	x
12	0	30	ADD R5, R0, #0	3	5	1	30	0	1	0	0	x
13	0	34	AROUND SUBS R8, R7, R2	B	1	0	FFFFFF FE	A	1	5	0	x
14	0	38	ADDLT R7, R5, #1	C	5	0	C	0	1	x	0	x
15	0	3C	SUB R7, R7, R2	C	54	0	07	0	1	5	0	x
16	0	40	STR R7, [R3, #84]	0	60	0	60	0	1	7	1	x
17	0	44	LDR R2, [R0, #96]	4C	0	0	60	0	1	0	0	7
18	0	4C	ADD R15, R15, R0	54	4	0	4C	0	1	0	0	x

19	0	58	ADD R2, R0, #14	0	64	1	58	0	1	x	0	x
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wave form:



ZOOM:

