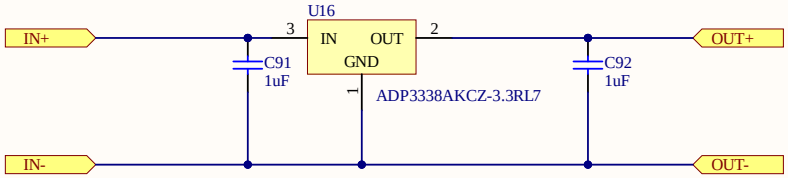
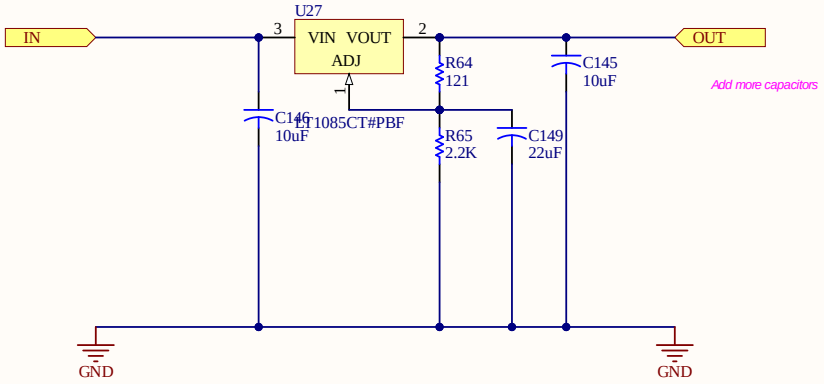


note, make sure to buy 1.8 V version

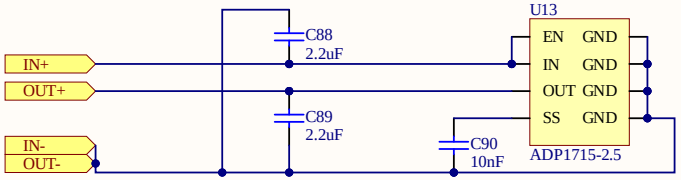
Title	*1.8V Regulator*	
RE:	Arturo di Girolamo	Size: A3
Date:	2/25/2022	

A



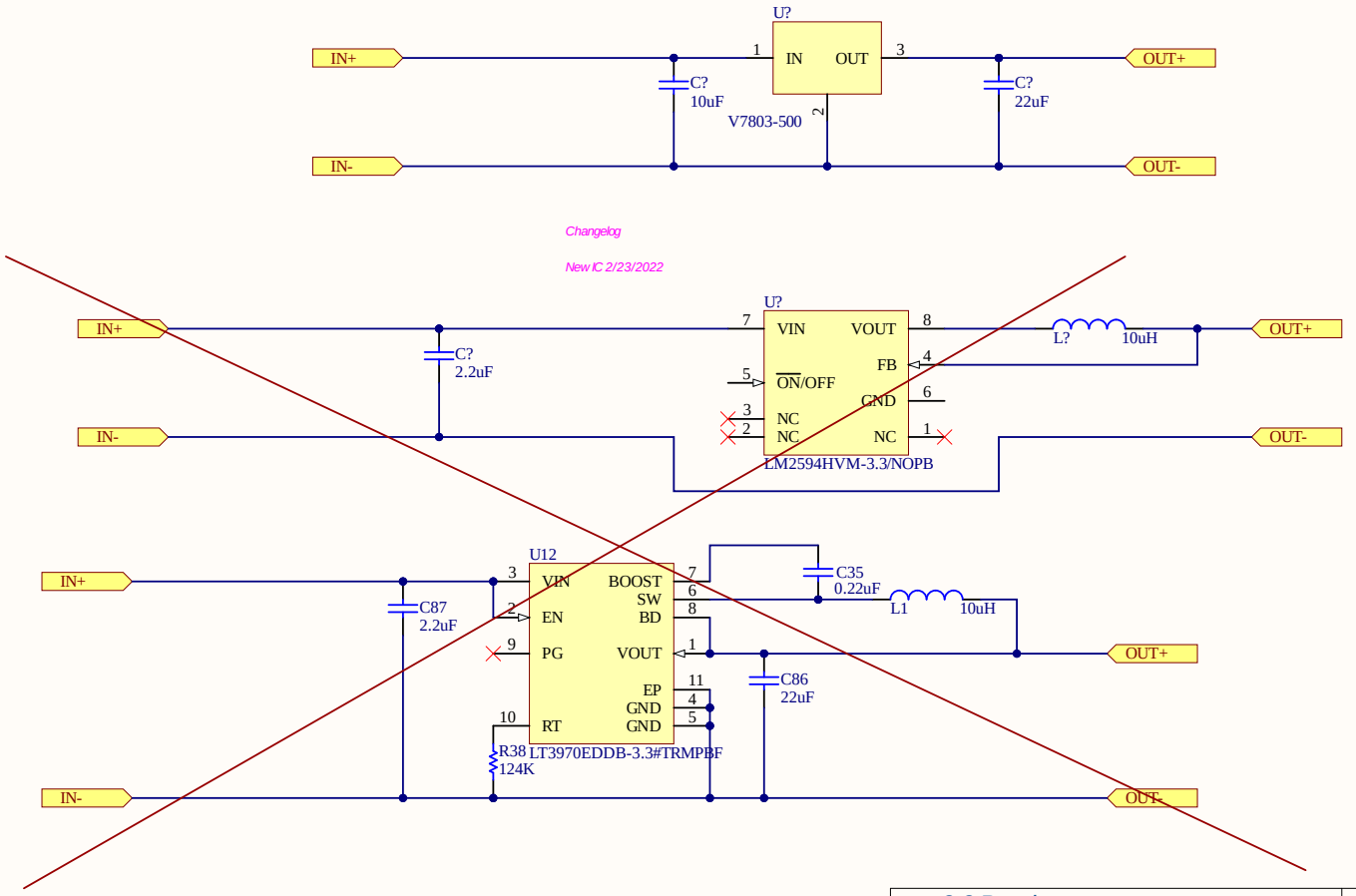
Title	+24V Regulator
RE: Arturo di Girolamo	Size: A3
Date: 2/25/2022	

A



Title	2.5V ADC Regulator
RE: Arturo di Girolamo	Size: A3
Date: 2/25/2022	

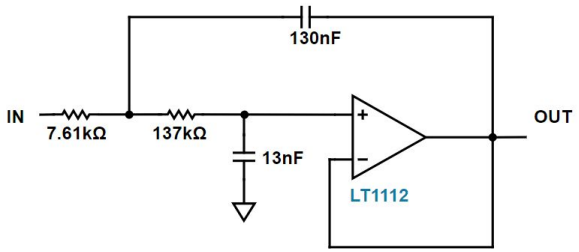
A



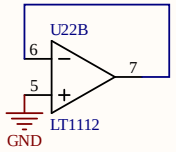
Title	3.3 Regulator	
RE:	Arturo di Girolamo	Size: A3
Date:	2/25/2022	

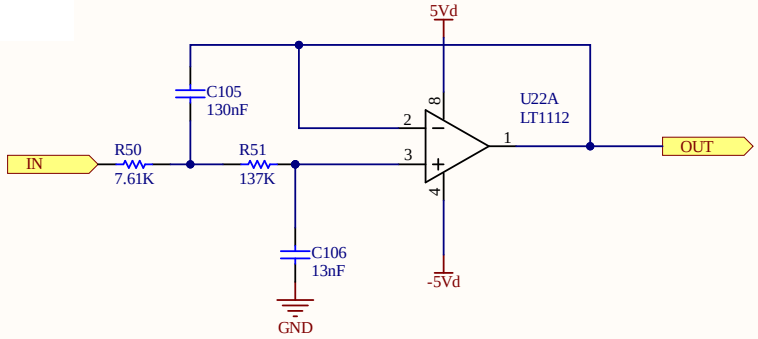
A

Stage A
2nd order
Low-Pass
Sallen Key

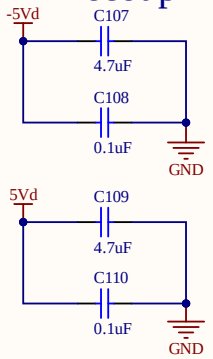


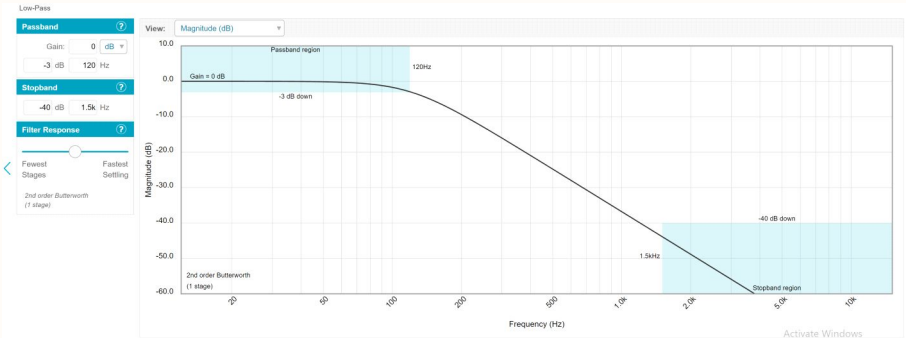
Unused OPAMP Configured as buffer to rest mid-supply





Decoupling Capacitors

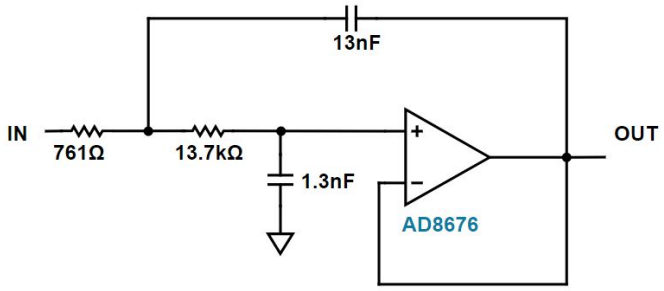


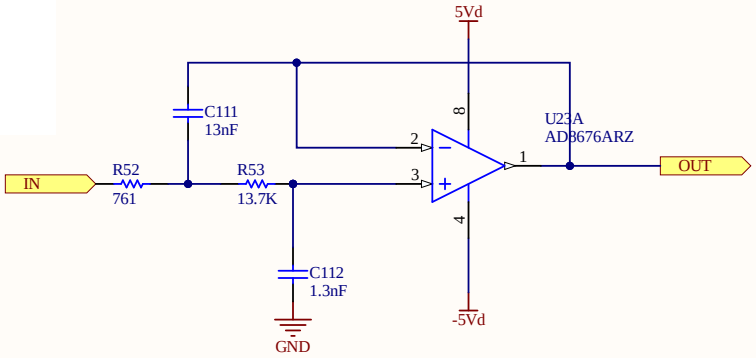


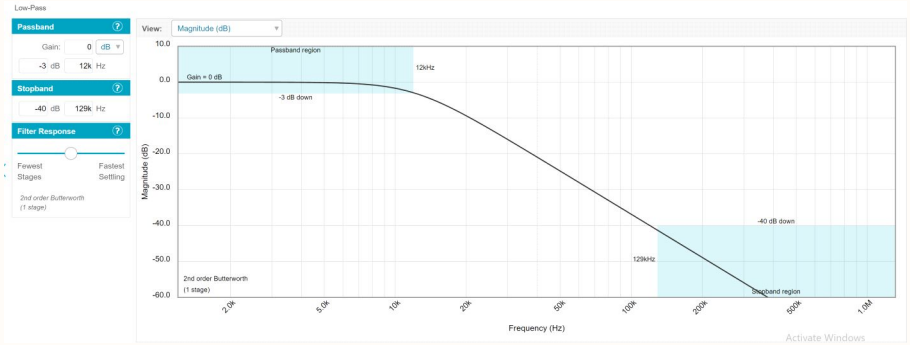
Title	*50 Hz Sine Gen LPF*		
RE:	Arturo di Girolamo	Size:	A3
Date:	2/25/2022		

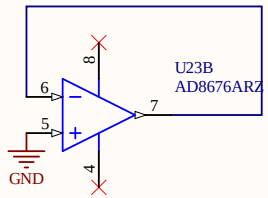
A

Stage A
2nd order
Low-Pass
Sallen Key

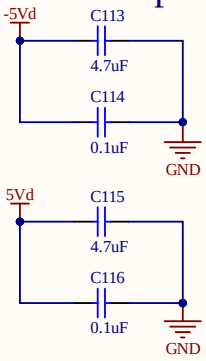






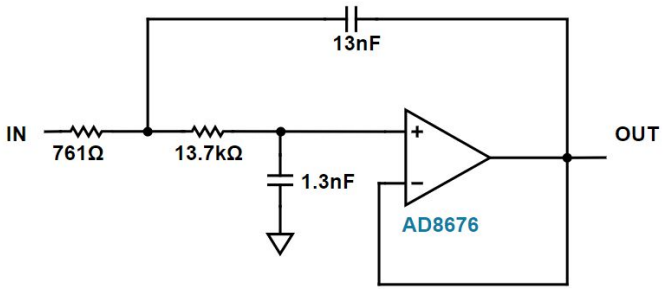


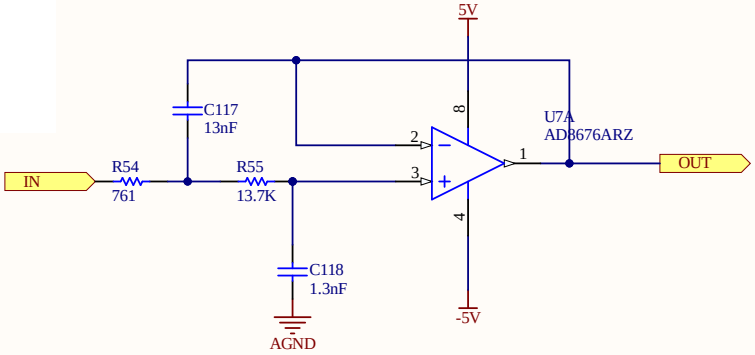
Decoupling Capacitors

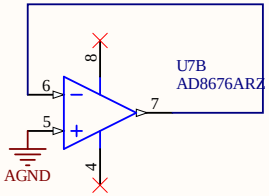


Title: 5kHz Sine Gen LPF		
RE: Arturo di Girolamo	Size: A3	A
Date: 2/25/2022		

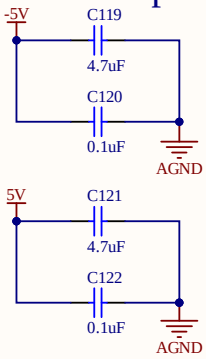
Stage A
2nd order
Low-Pass
Sallen Key

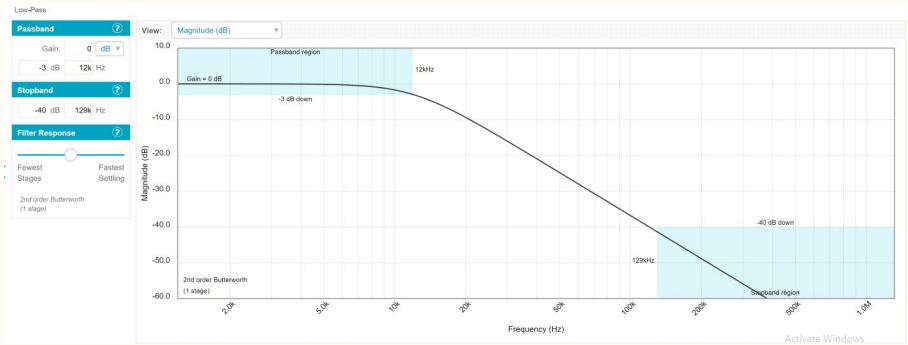






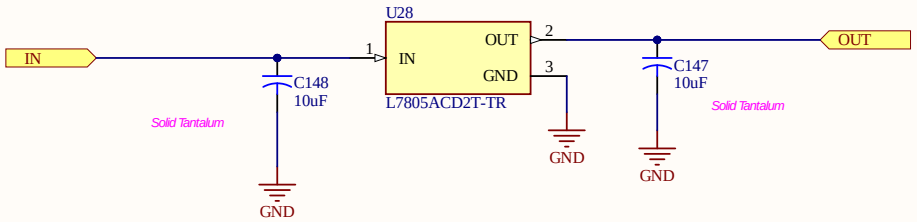
Decoupling Capacitors





Title	5kHz AD630 LPF		
RE:	Arturo di Girolamo	Size:	A3
Date:	2/25/2022		

A

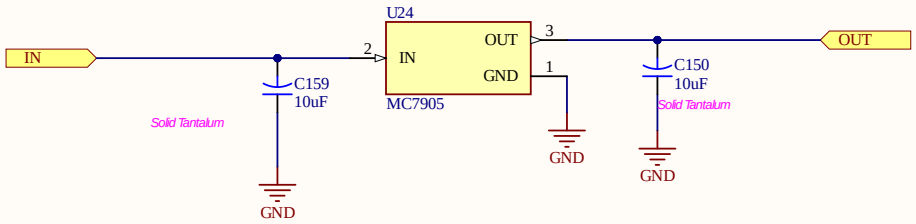


Title	5V Digital regulator
RE:	Arturo di Girolamo
Size:	A3
Date:	2/25/2022

A

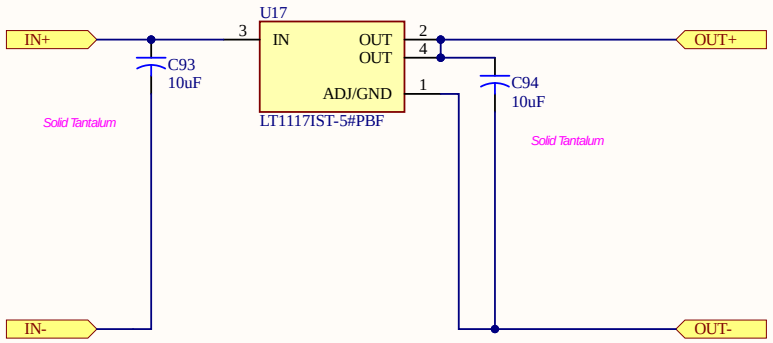
Changelog:

Footprint Changes for MC7905, See Screenshot



Title	-5V Digital Regulator
RE: Arturo di Girolamo	Size: A3
Date: 2/25/2022	

A

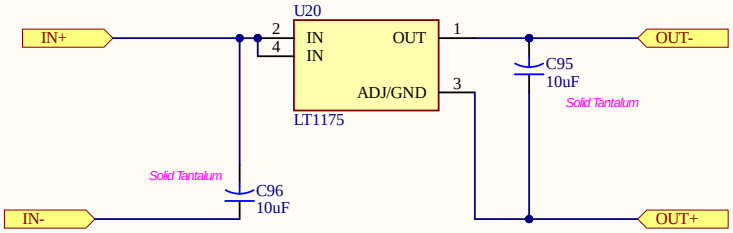


Title	5V Battery Regulator
RE:	Arturo di Girolamo
Size:	A3
Date:	2/25/2022

A

Changelog:

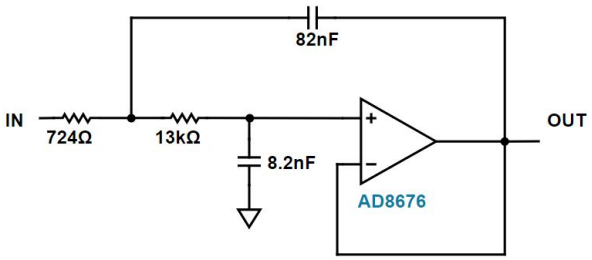
Swapped OUT- and OUT+

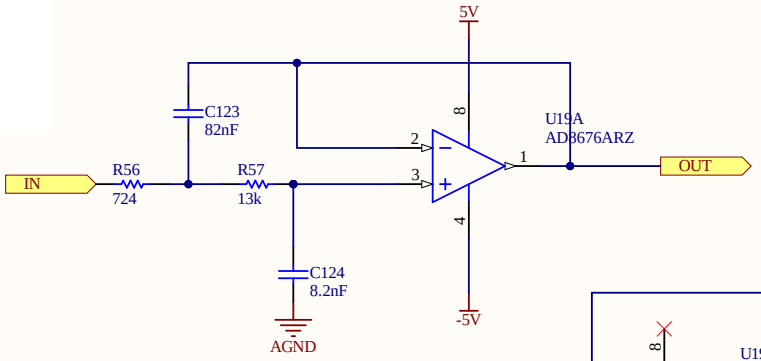


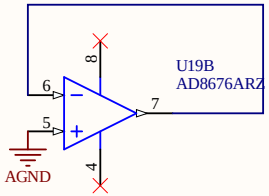
Title	-5V Battery Regulator
RE: Arturo di Girolamo	Size: A3
Date: 2/25/2022	

A

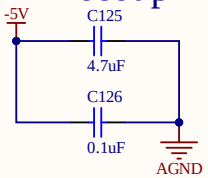
Stage A
2nd order
Low-Pass
Sallen Key

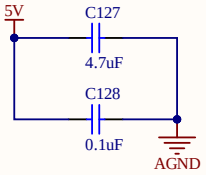


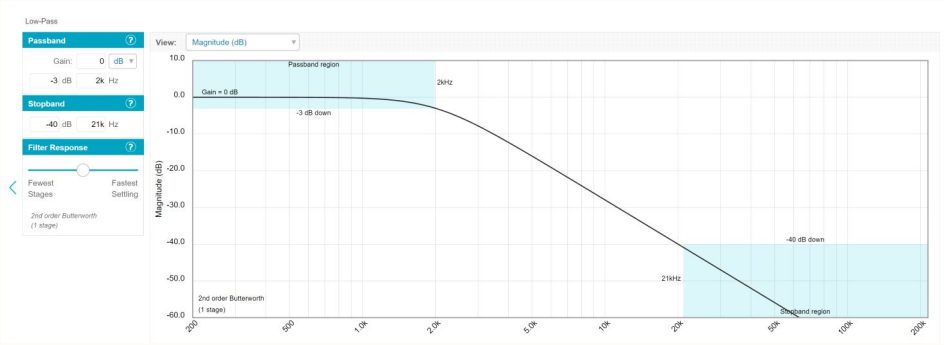




Decoupling Capacitors





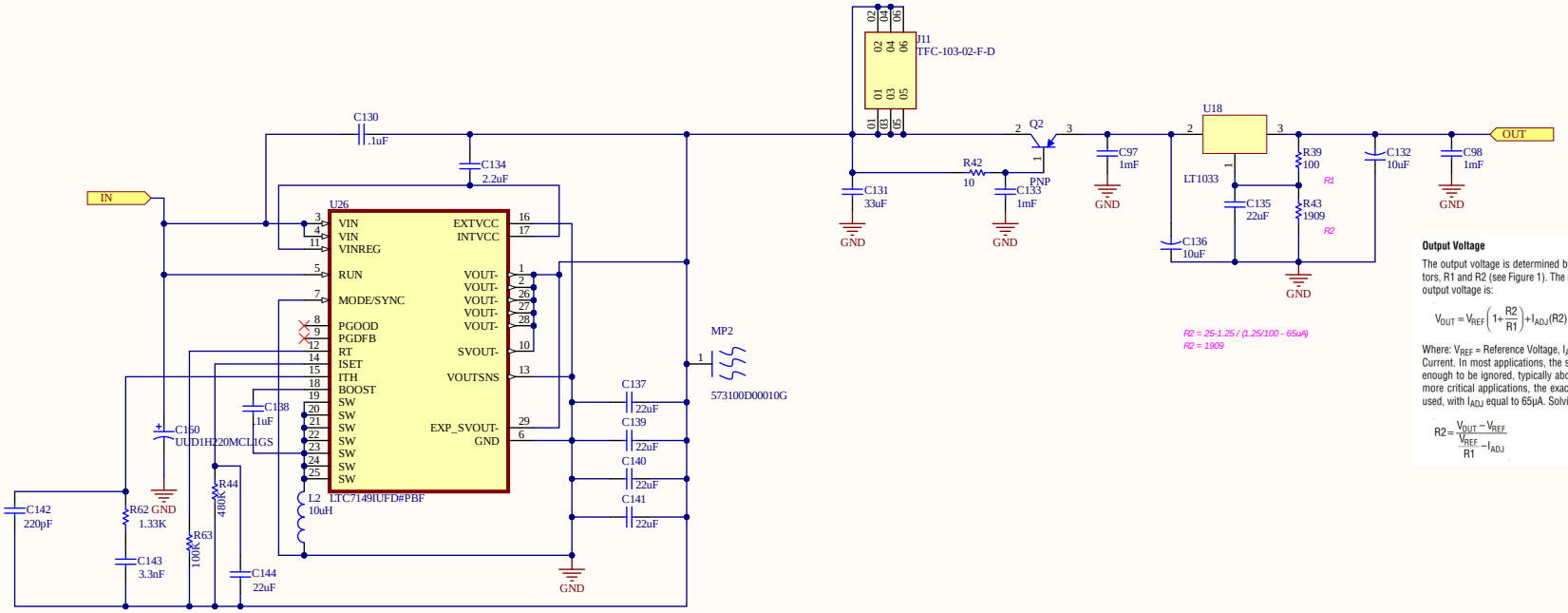


Title	LF AD630 LPF		
RE:	Arturo di Girolamo	Size:	A3
Date:	2/25/2022		

A

MAY ADD LC FILTER HERE AFTER TESTS WITH THE ONES ORDERED

Resistance Values will change with output rails



R2 = 25-1.25 / (1.25/100 - 65uA)
R2 = 1909

Output Voltage

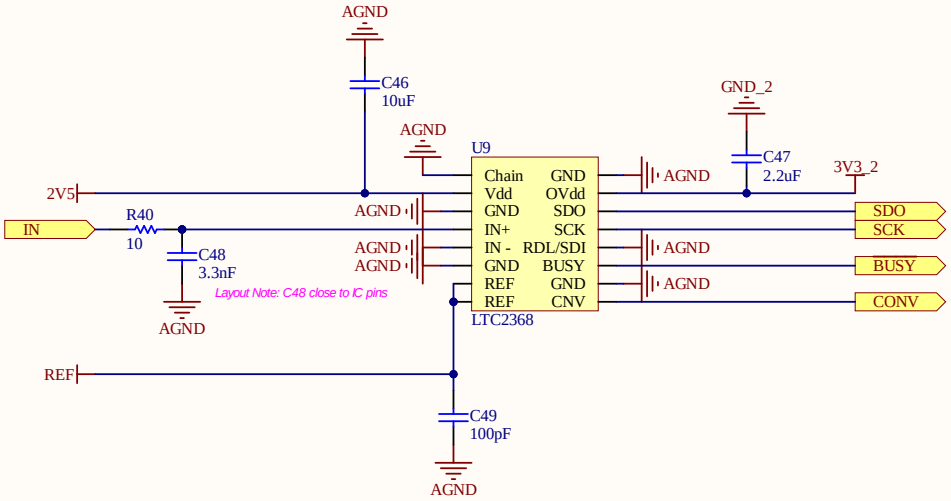
The output voltage is determined by two external resistors, R1 and R2 (see Figure 1). The exact formula for the output voltage is:

$$V_{OUT} = V_{REF}\left(1+\frac{R2}{R1}\right)+I_{ADJ}(R2)$$

Where: V_{REF} = Reference Voltage, I_{ADJ} = Adjustment Pin Current. In most applications, the second term is small enough to be ignored, typically about 0.5% of V_{OUT}. In more critical applications, the exact formula should be used, with I_{ADJ} equal to 65µA. Solving for R2 yields:

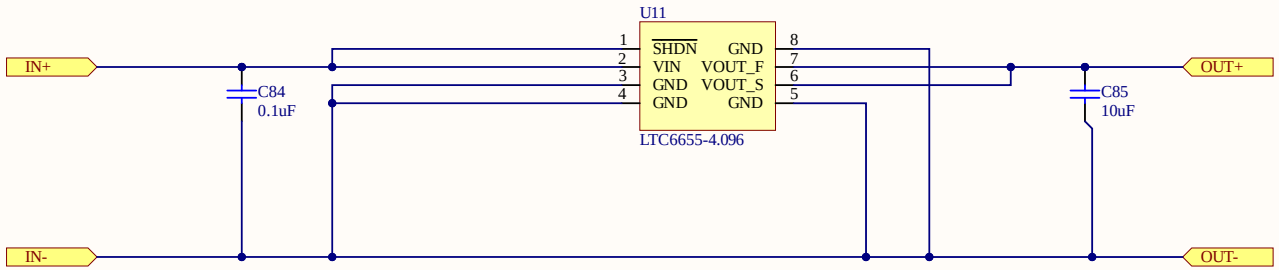
$$R2 = \frac{V_{OUT} - V_{REF}}{\frac{V_{REF}}{R1} - I_{ADJ}}$$

Title	7419 Ckt
RE:	Arturo di Girolamo
Size:	A3
Date:	2/25/2022



Title	ADC	
RE:	Arturo di Girolamo	Size: A3
Date:	2/25/2022	

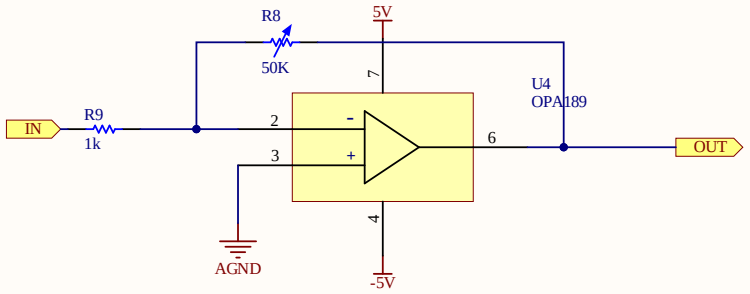
A



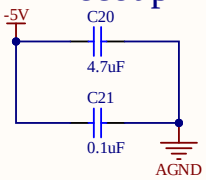
Title	*ADC Reference*	
RE:	Arturo di Girolamo	Size: A3
Date:	2/25/2022	

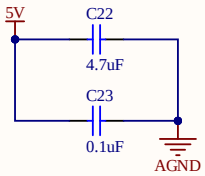
A

GAIN SET



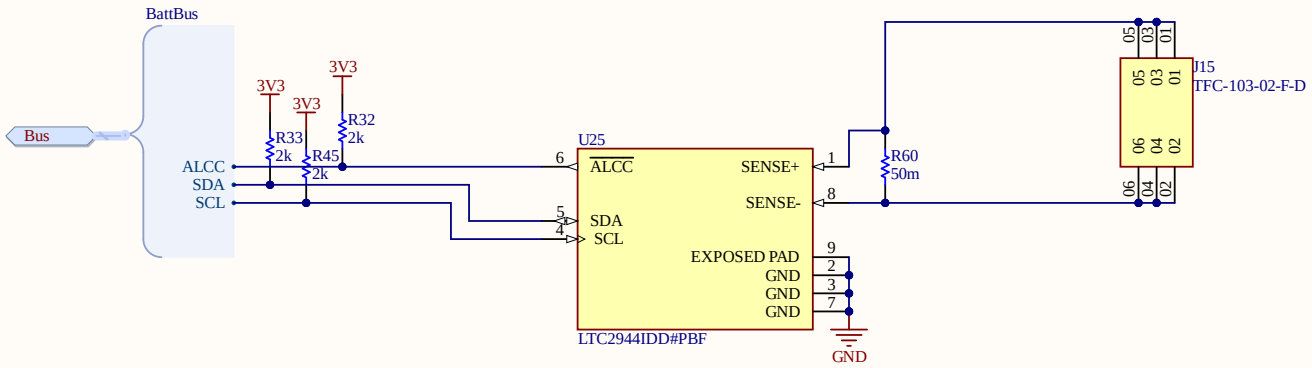
Decoupling Capacitors



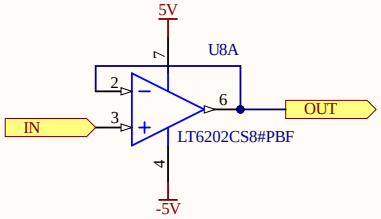


Title	*Signal Path AMP*	
RE:	Arturo di Girolamo	Size: A3
Date:	2/25/2022	

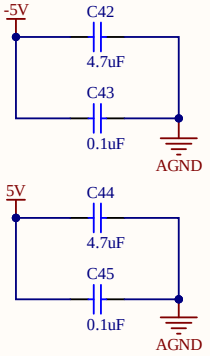
A



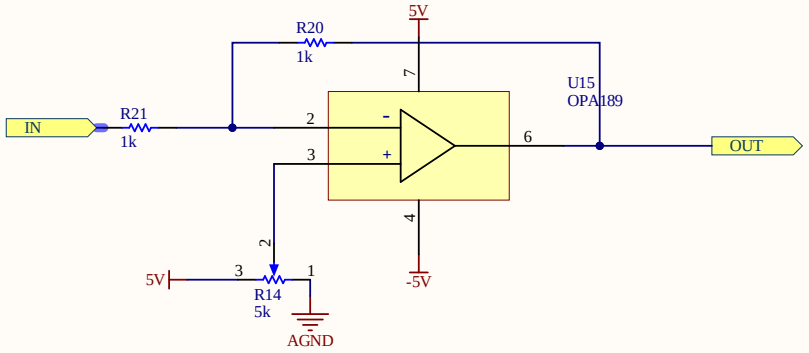
Title	Battery Charging
RE:	Arturo di Girolamo
Size:	A3
Date:	2/25/2022



Decoupling Capacitors

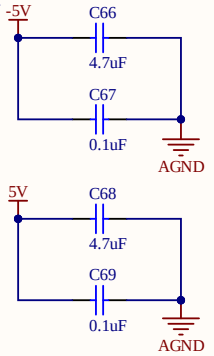


Title: ADC BUFFER		
RE: Arturo di Girolamo	Size: A3	A
Date: 2/25/2022		



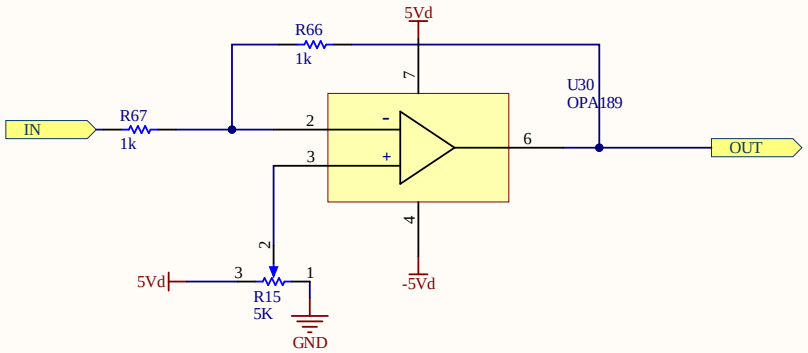
DC SHIFT

Decoupling Capacitors



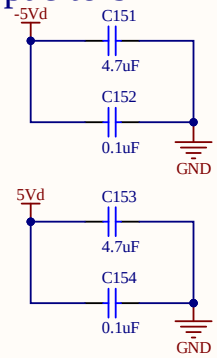
Title	*Signal Path DC Shift*	
RE:	Arturo di Girolamo	Size: A3
Date:	2/25/2022	

A



DC SHIFT

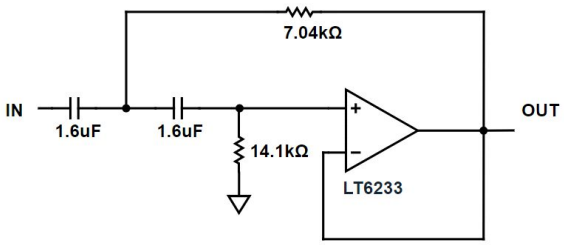
Decoupling Capacitors



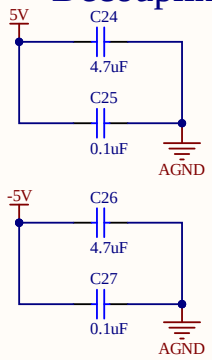
Title	*Digital DC Shift*	
RE:	Arturo di Girolamo	Size: A3
Date:	2/25/2022	

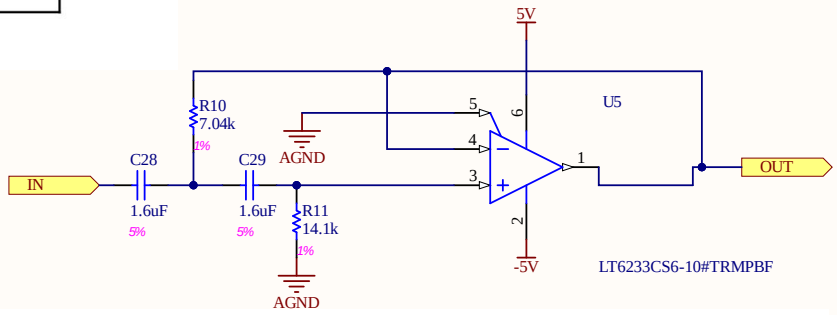
A

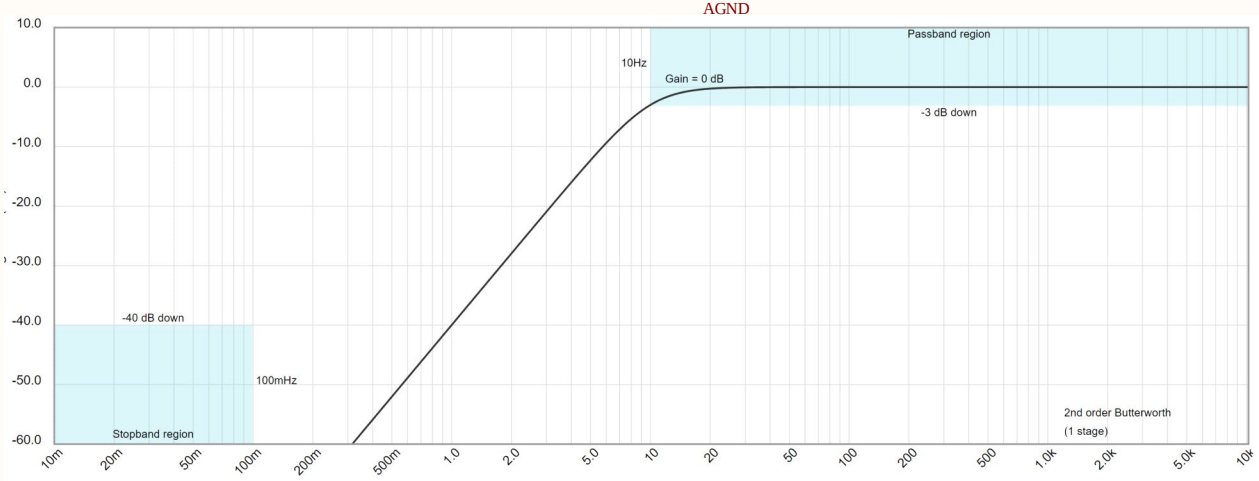
Stage A
2nd order
High-Pass
Sallen Key



Decoupling Capacitors



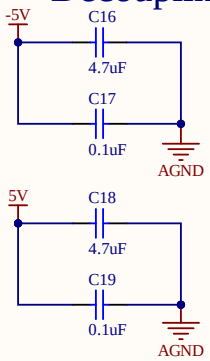




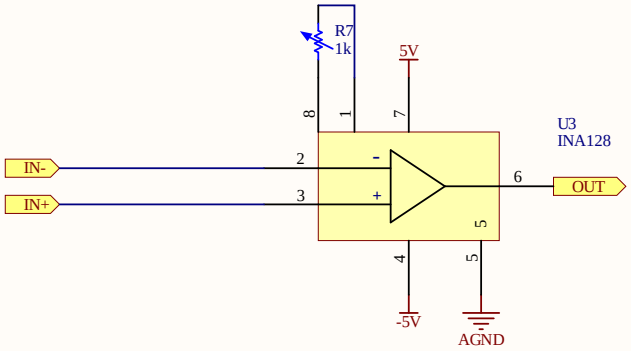
Title	*HIGH PASS*	
RE:	Arturo di Girolamo	Size: A3
Date:	2/25/2022	

A

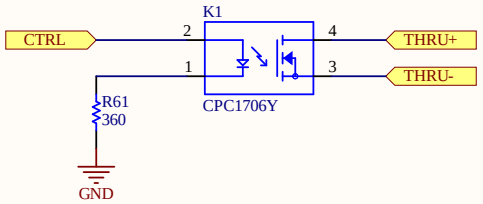
Decoupling Capacitors



Gain Set Resistor

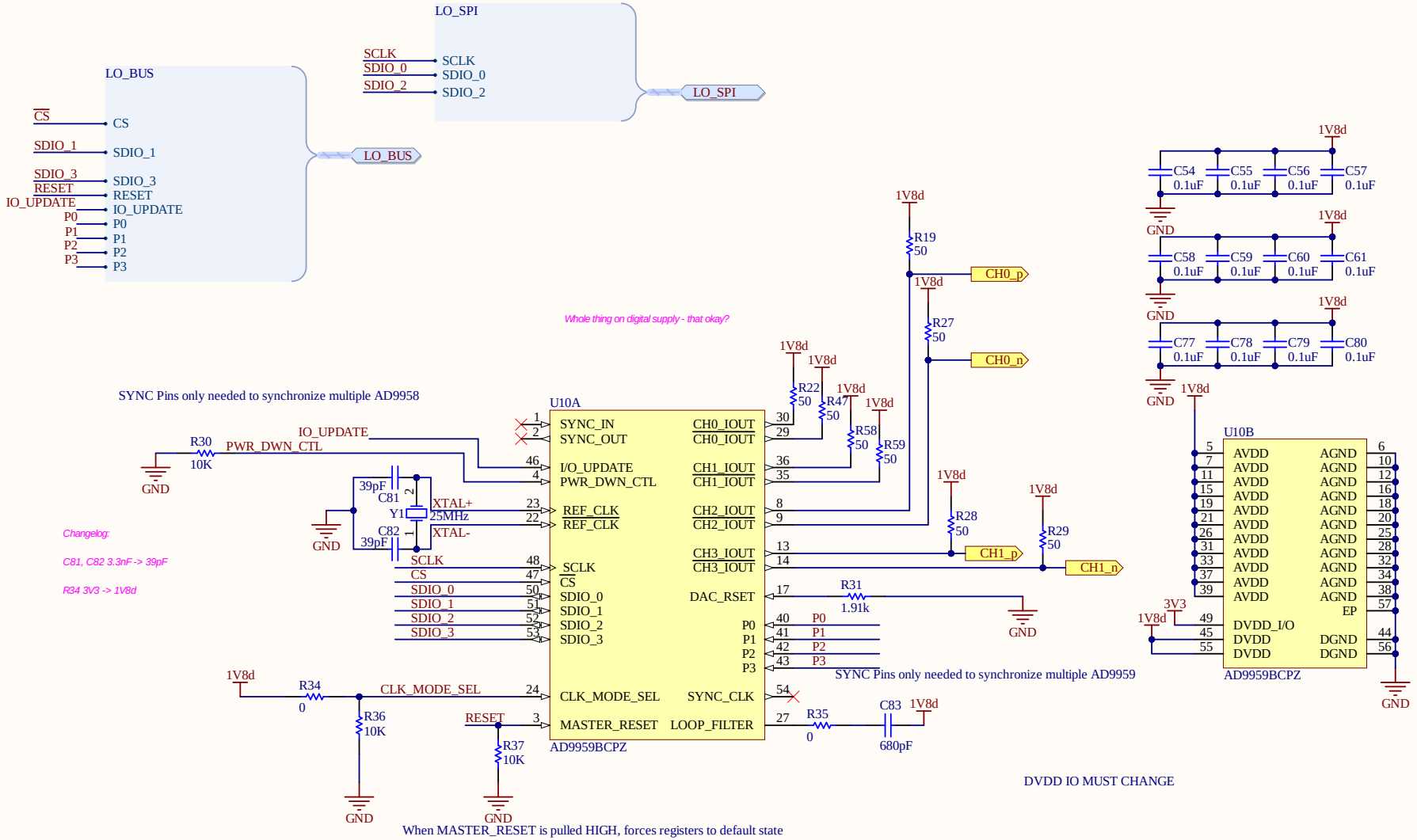


Title: INA STAGE		
RE: Arturo di Girolamo	Size: A3	A
Date: 2/25/2022		



Title	*High Current Relay*
RE:	Arturo di Girolamo
Size:	A3
Date:	2/25/2022

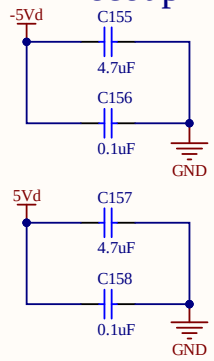
A



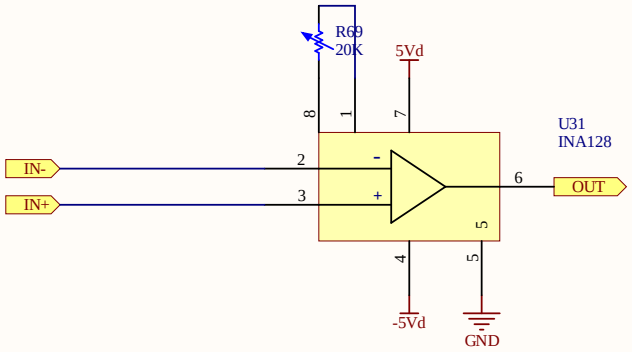
Title	DDS		
RE:	Arturo di Girolamo	Size:	A3
Date:	2/25/2022		

A

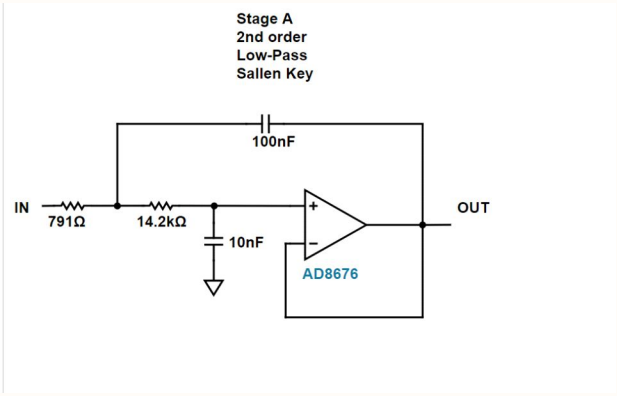
Decoupling Capacitors



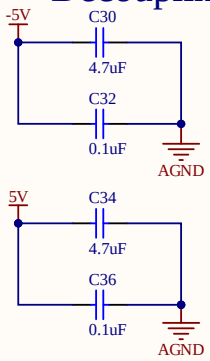
Gain Set Resistor



Title: DDS INA		
RE: Arturo di Girolamo	Size: A3	A
Date: 2/25/2022		

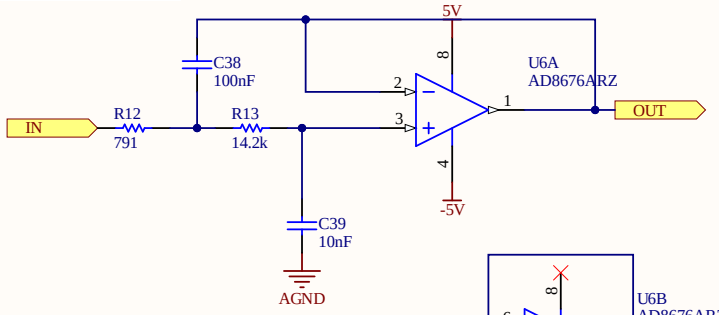


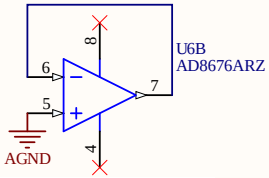
Decoupling Capacitors

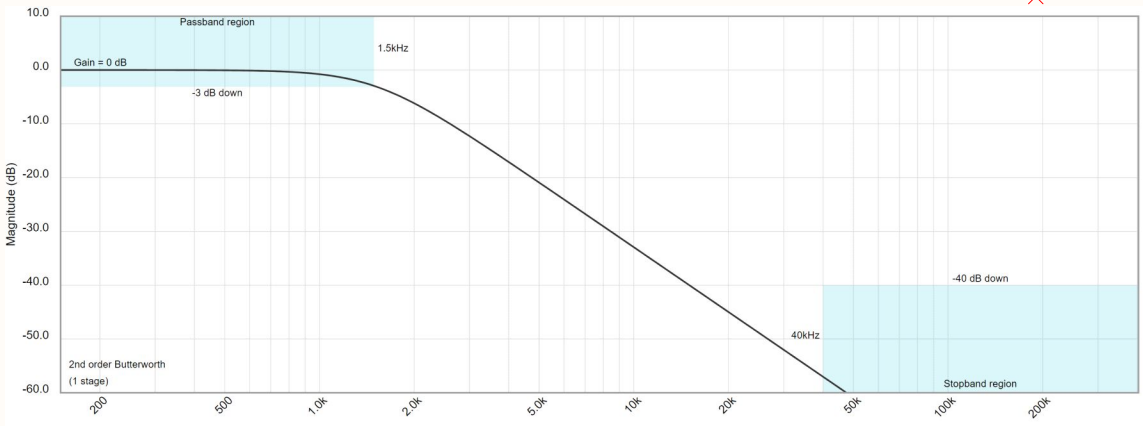


Changelog:

R12 791k -> 791

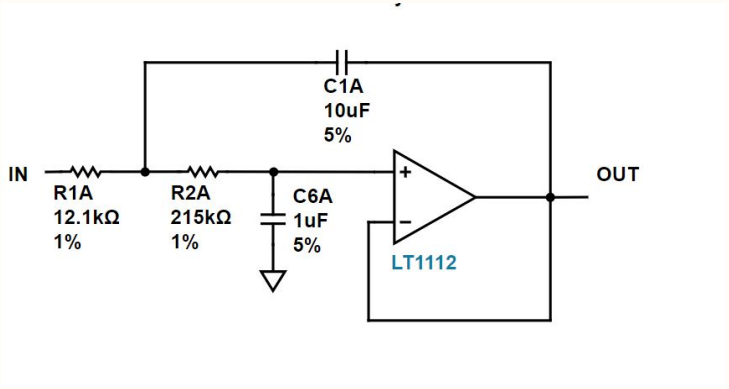




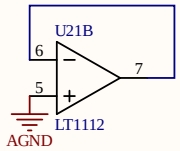


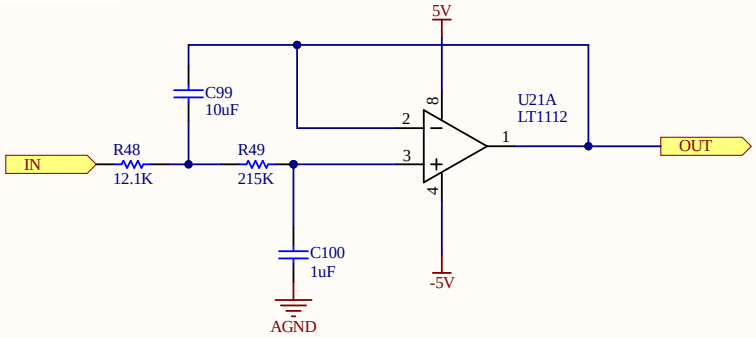
Title: *4TH ORDER LOWPASS*		
RE: Arturo di Girolamo	Size: A3	
Date: 2/25/2022		

A

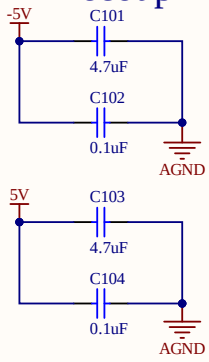


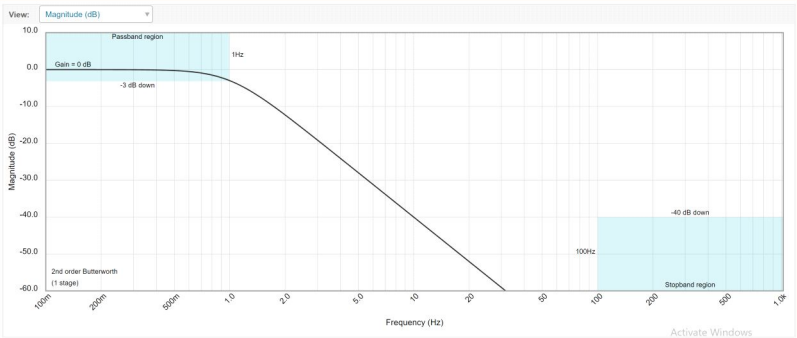
Unused OPAMP Configured as buffer to rest mid-supply





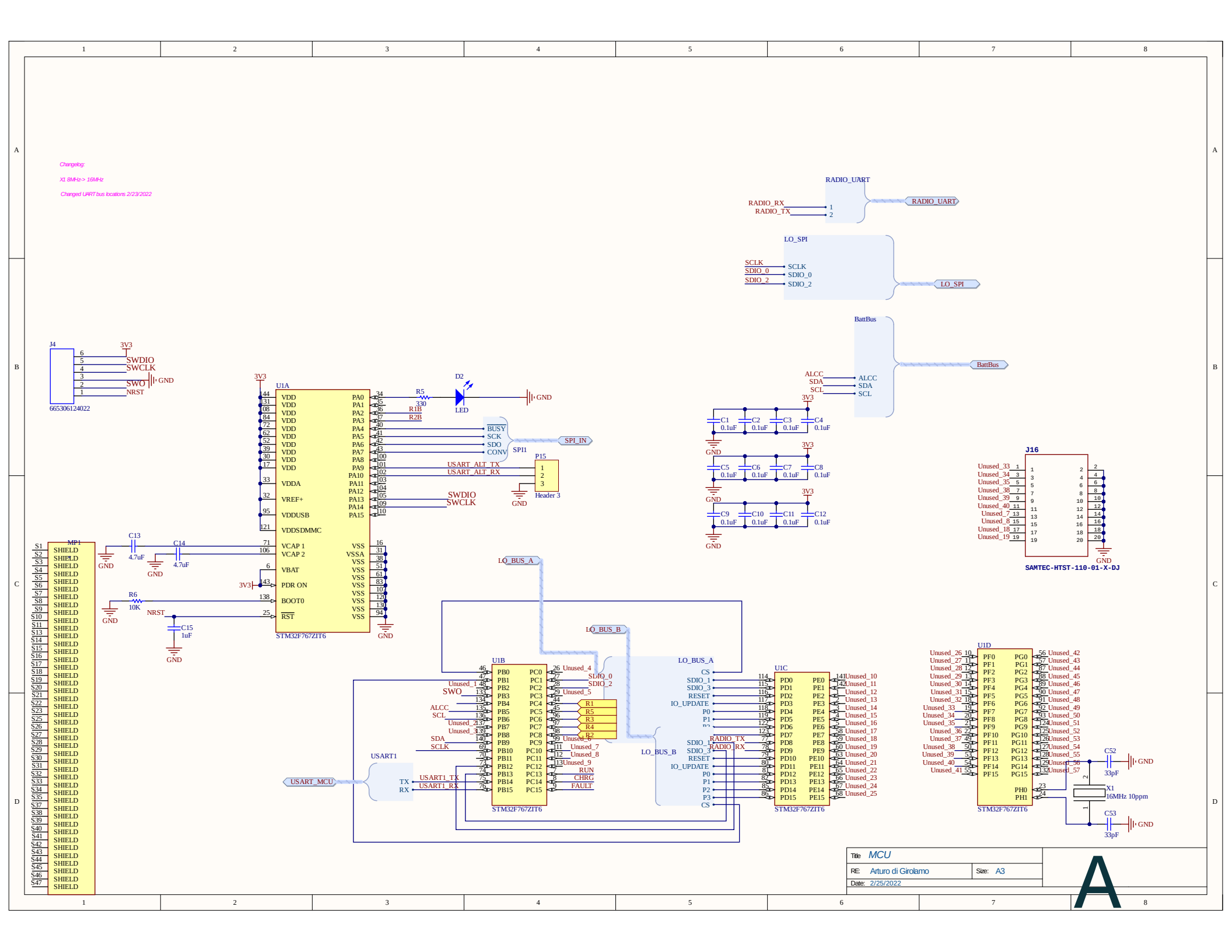
Decoupling Capacitors

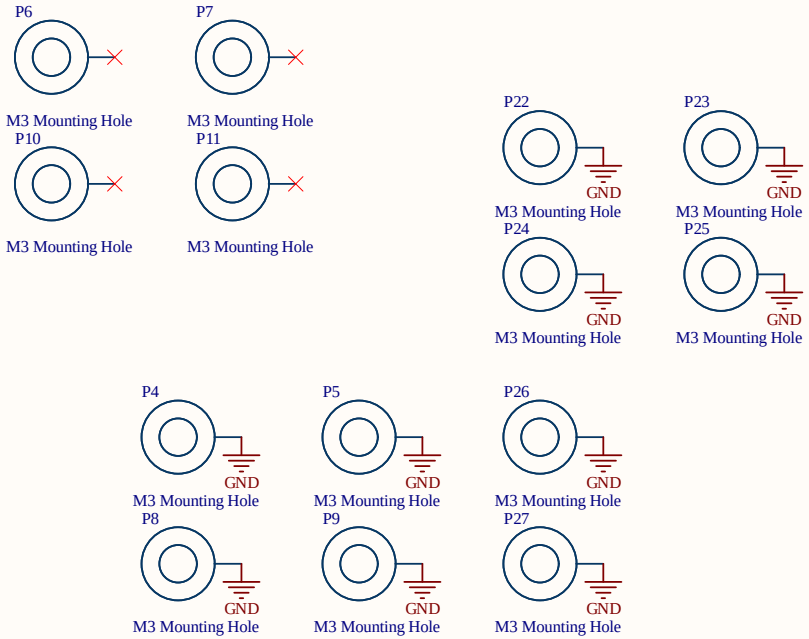




Title	ADC LPF		
RE:	Arturo di Girolamo	Size:	A3
Date:	2/25/2022		

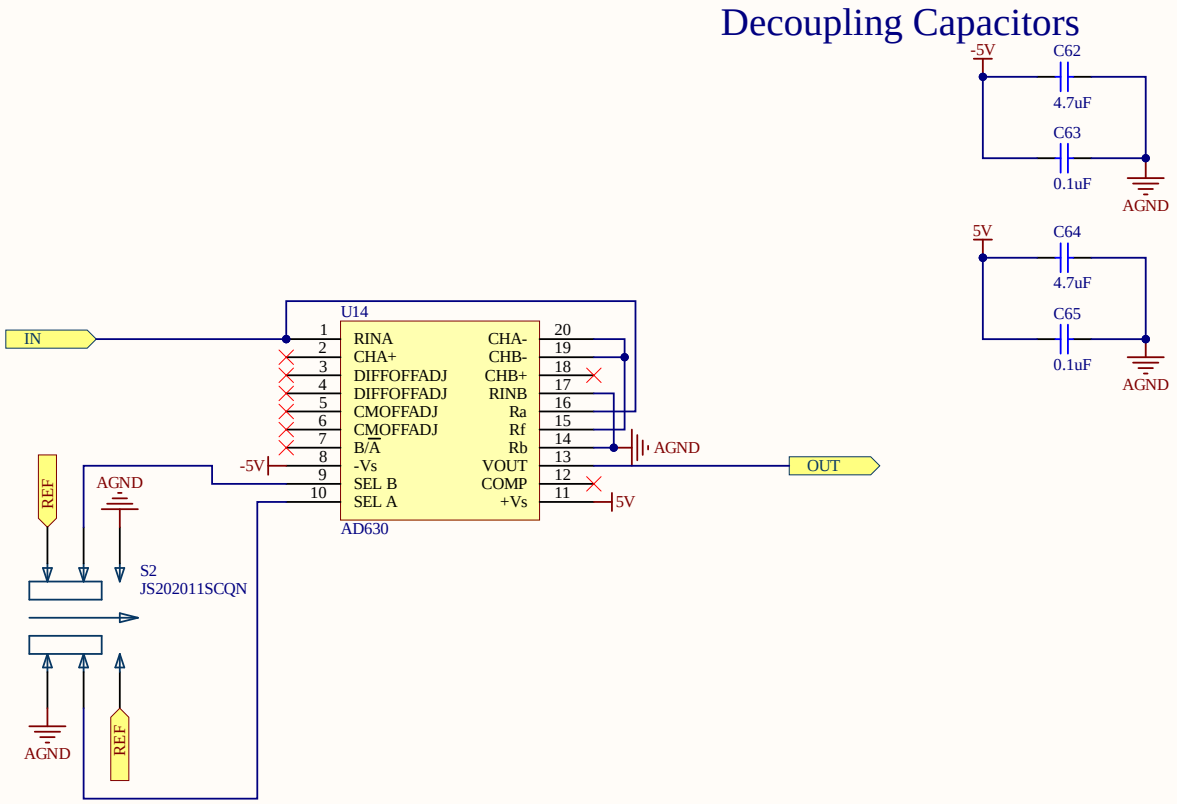
A


Changelog:
X1 8MHz-> 16MHz
Changed UART bus locations 2/23/2022
RADIO_UART
RADIO_RX
RADIO_TX
LO_SPI
SCLK
SDIO_0
SDIO_2
BattBus
ALCC
SDA
SCL
J4
3V3
SWDIO
SWCLK
SWO
NRST
GND
665306124022
U1A
STM32F767ZIT6
D2
LED
R5
330
R1B
R2B
SPI1
BUSY
SCK
SDO
CONV
SPI_IN
P15
Header 3
USART_ALT_TX
USART_ALT_RX
C1
C2
C3
C4
C5
C6
C7
C8
C9
C10
C11
C12
0.1uF
J16
SAMTEC-HTST-110-01-X-DJ
MP1
SHIELD
C13
C14
4.7uF
R6
10K
C15
1uF
LO_BUS_A
LO_BUS_B
U1B
U1C
U1D
USART1
USART_MCU
TX
RX
USART1_TX
USART1_RX
C52
C53
33pF
X1
16MHz 10ppm
Title MCU
RE: Arturo di Girolamo
Size: A3
Date: 2/25/2022
A

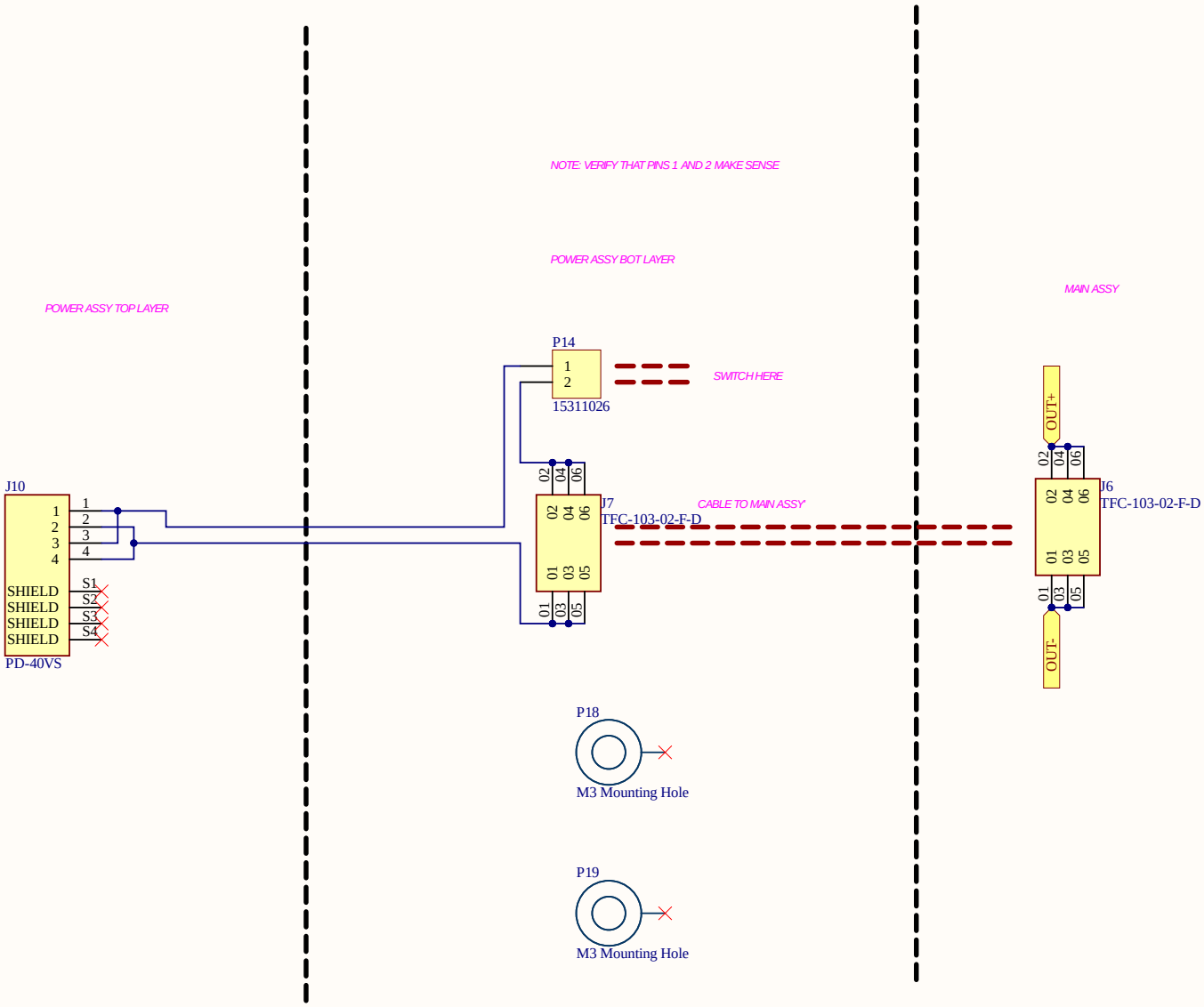


Title	*Mechanical*	
RE:	Arturo di Girolamo	Size: A3
Date:	2/25/2022	

A



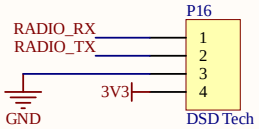
Title	*AD630 Mixer*	
RE:	Arturo di Girolamo	Size: A3
Date:	2/25/2022	



Title	Power Input PCB
RE:	Arturo di Girolamo
Size:	A3
Date:	2/25/2022

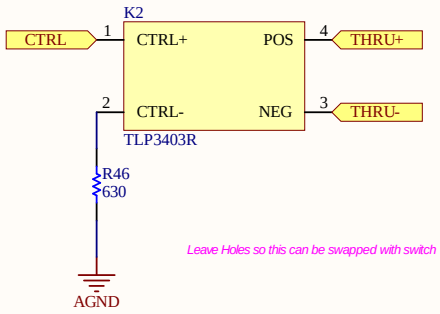
A

Changelog:
Removed uBlox 2/23/2022
Added Header



Title	uBlox Radio
RE: Arturo di Girolamo	Size: A3
Date: 2/25/2022	

A



Title	Low Current Relay
RE:	Arturo di Girolamo
Size:	A3
Date:	2/25/2022

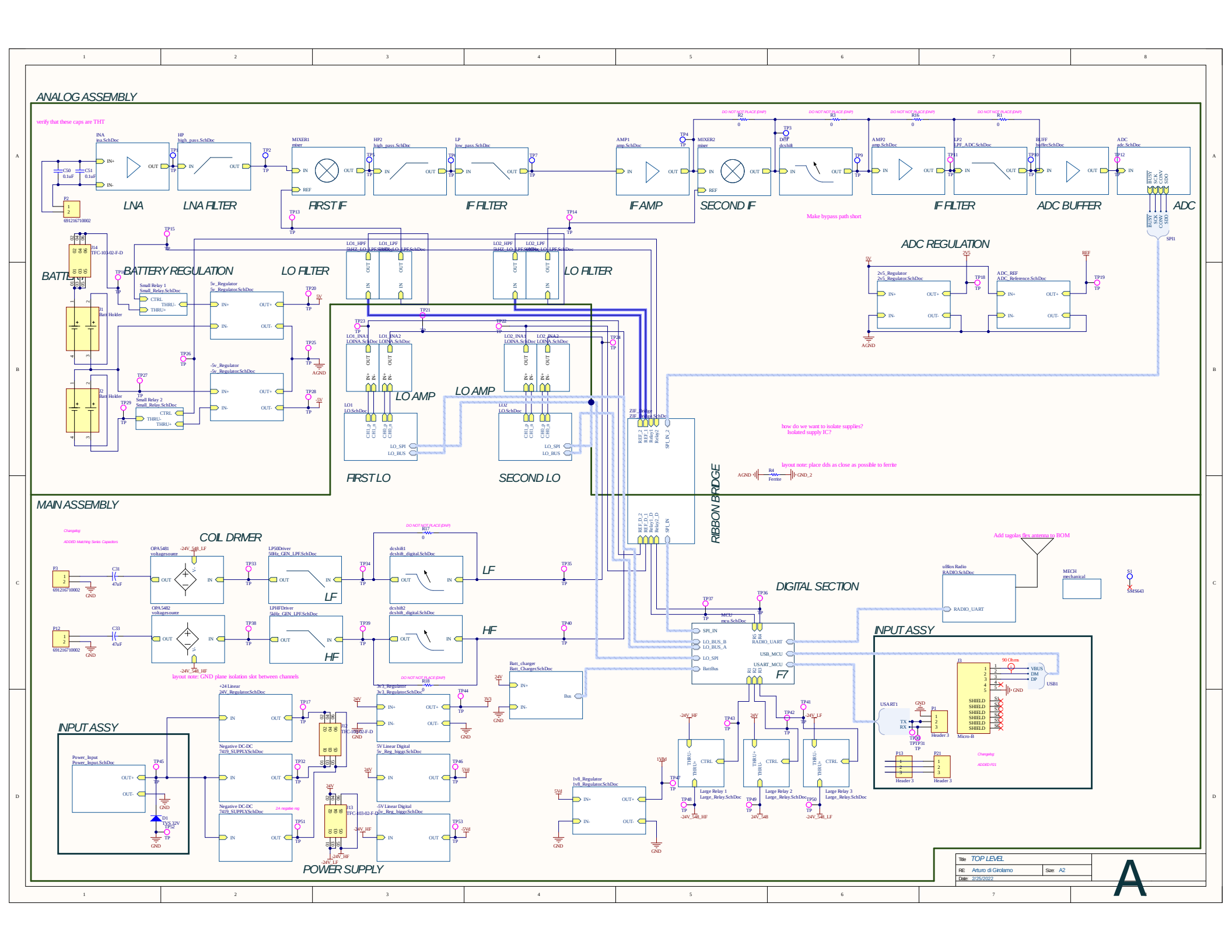
A

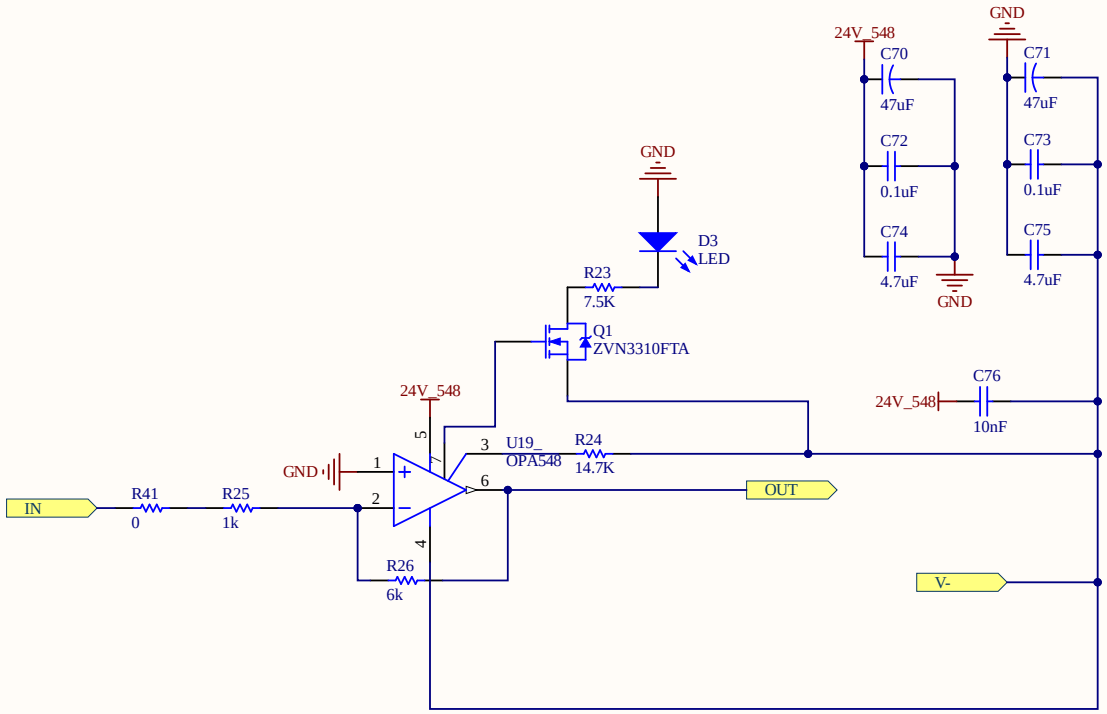
MPS SYSTEM COMPLETE ASSY

DRAWN A. DI GIROLAMO

MINNEAPOLIS, MN

Title:	*TITLE SHEET*		A
RE:	Arturo di Girolamo	Size: A3	
Date:	2/25/2022		


ANALOG ASSEMBLY
verify that these caps are THT
LNA
LNA FILTER
FIRST IF
IF FILTER
IF AMP
SECOND IF
IF FILTER
ADC BUFFER
ADC
Make bypass path short
BATTERY
BATTERY REGULATION
LO FILTER
LO FILTER
ADC REGULATION
LO AMP
LO AMP
FIRST LO
SECOND LO
how do we want to isolate supplies?
Isolated supply IC?
layout note: place dds as close as possible to ferrite
RIBBON BRIDGE
MAIN ASSEMBLY
COIL DRIVER
LF
HF
layout note: GND plane isolation slot between channels
DIGITAL SECTION
F7
Add tagolas flex antenna to BOM
INPUT ASSY
INPUT ASSY
POWER SUPPLY
Title TOP LEVEL
RE Arturo di Girolamo
Size A2
Date 2/25/2022
A

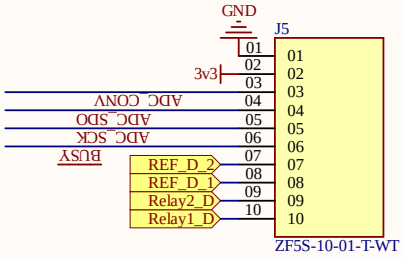


Title	548 Voltage source
RE: Arturo di Girolamo	Size: A3
Date: 2/25/2022	

A

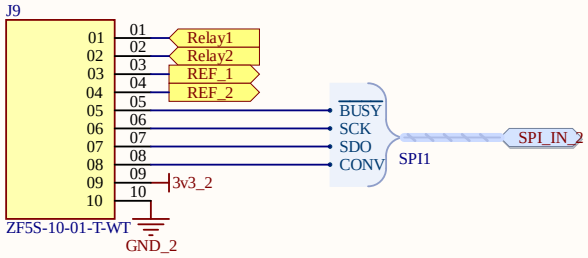
MAIN PCB

swap this for right angle



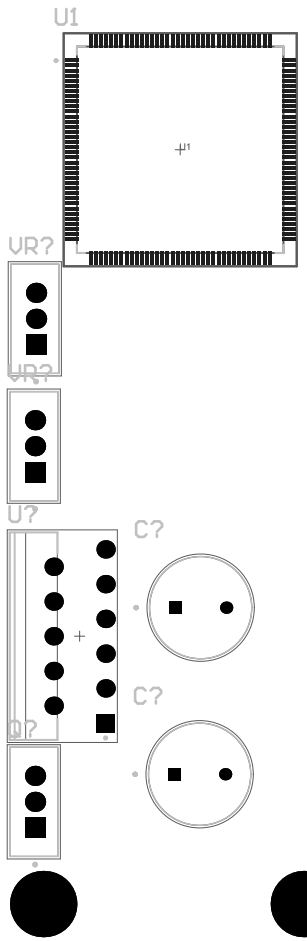
ANALOG PCB

double check pin alignment with flex cable after layout
or just rotate right angle pi rads



Title	Ribbon Bridge	
RE:	Arturo di Girolamo	Size: A3
Date:	2/25/2022	

A


U1
VR?
VR?
U?
C?
C?
D?