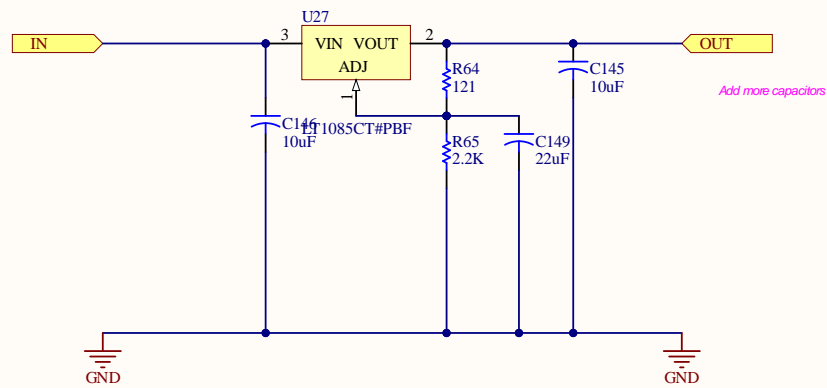


note, make sure to buy 1.8 V version

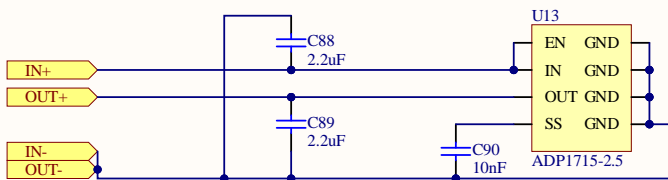
Title <i>1.8V Regulator</i>	
RE: <i>Arturo di Girolamo</i>	Size: <i>A3</i>
Date: <i>3/30/2022</i>	

A



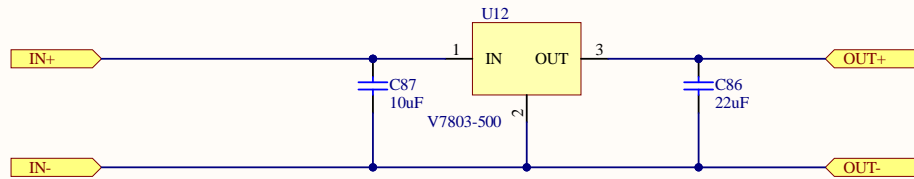
Title: <i>+24V Regulator</i>	
RE: <i>Arturo di Girolamo</i>	Size: <i>A3</i>
Date: <i>3/30/2022</i>	

A



Title <i>2.5VADC Regulator</i>		
RE: <i>Arturo di Girolamo</i>		Size: <i>A3</i>
Date: <i>3/30/2022</i>		

A



Title <i>3.3 Regulator</i>	
RE: <i>Arturo di Girolamo</i>	Size: <i>A3</i>
Date: <i>3/30/2022</i>	

A

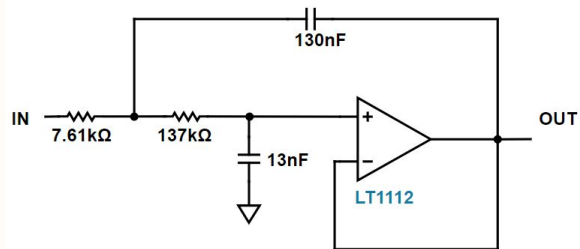
1

2

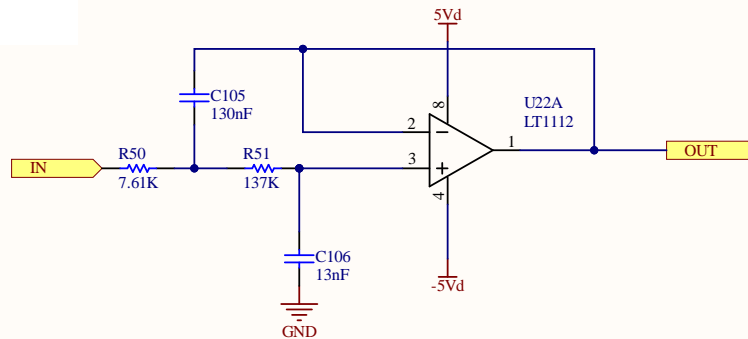
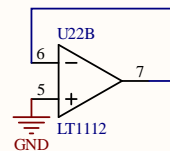
3

4

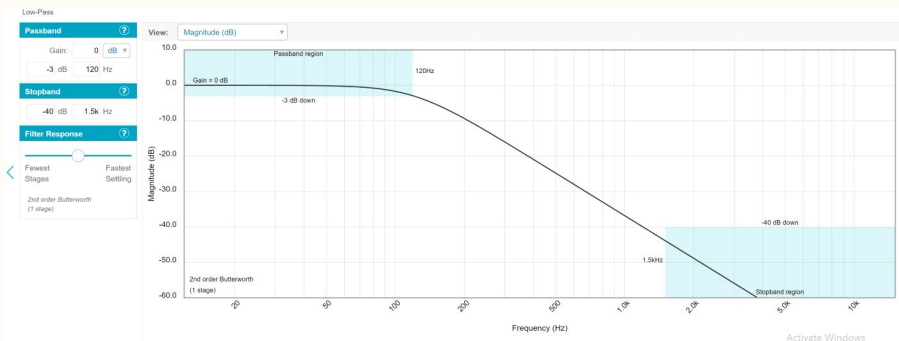
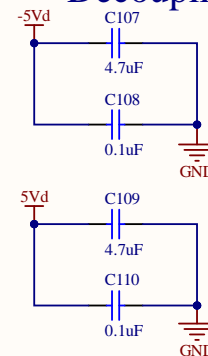
Stage A 2nd order Low-Pass Sallen Key



Unused OPAMP Configured as buffer to rest mid-supply



Decoupling Capacitors



Title **50 Hz Sine Gen LPF**

RE: Arturo di Girolamo

Size: A3

Date: 3/30/2022

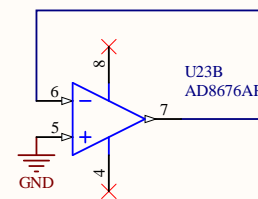
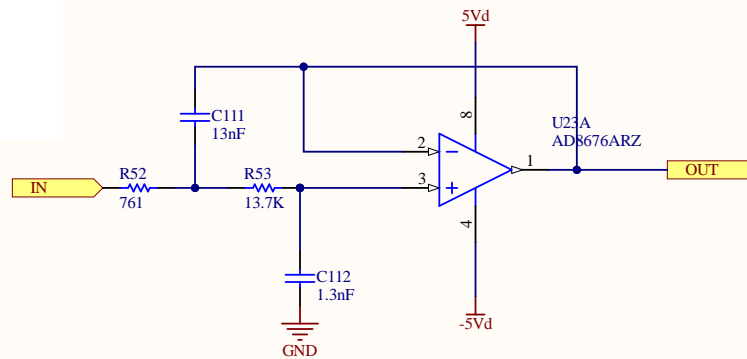
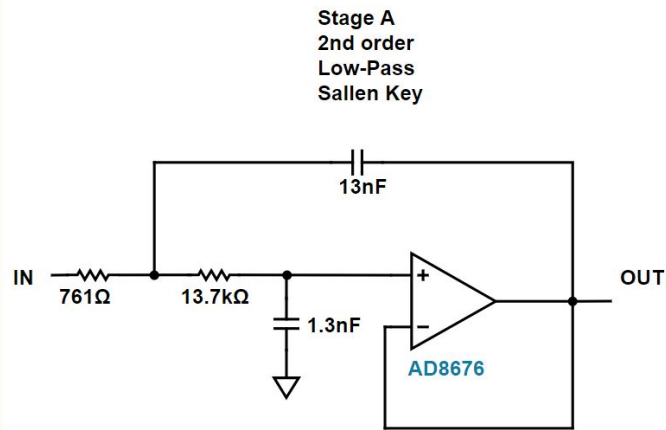
A

1

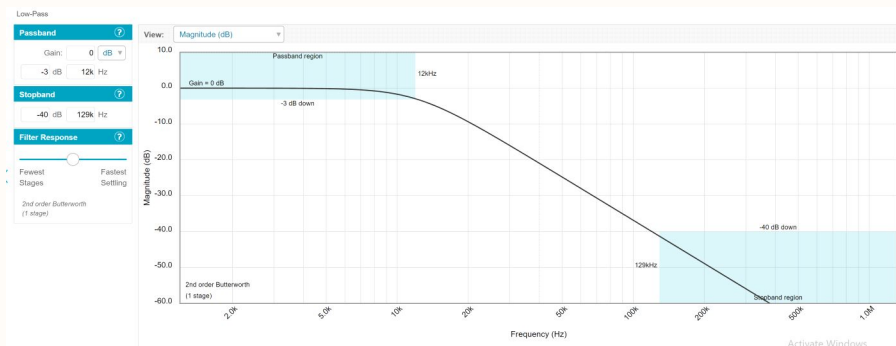
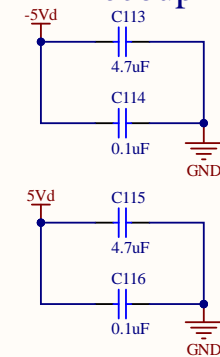
2

3

4



Decoupling Capacitors



Title	5kHz Sine Gen LPF	
RE:	Arturo di Girolamo	Size: A3
Date:	3/30/2022	

A

A

B

C

D

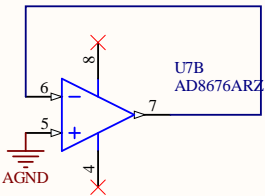
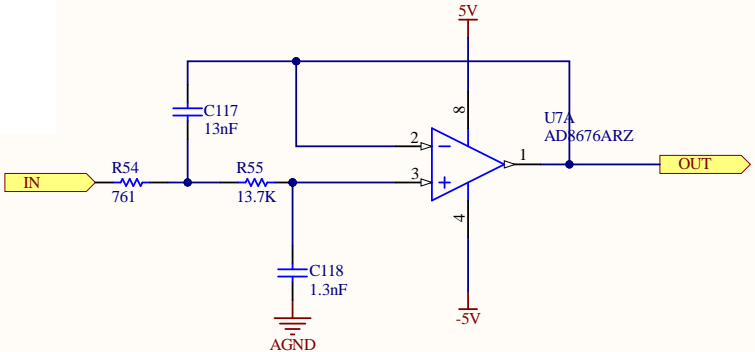
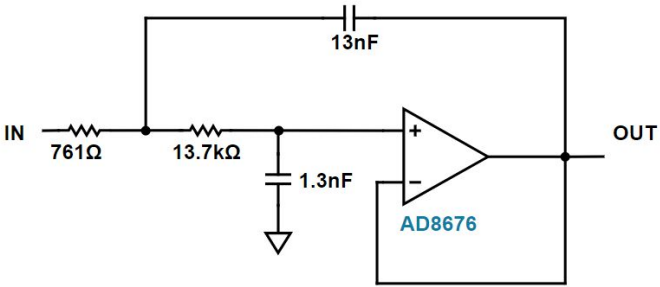
A

B

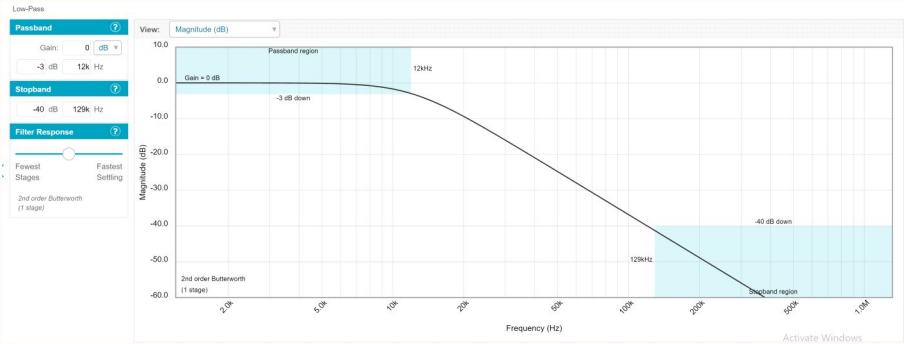
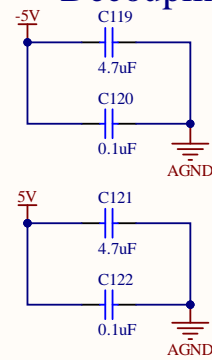
C

D

Stage A
2nd order
Low-Pass
Sallen Key

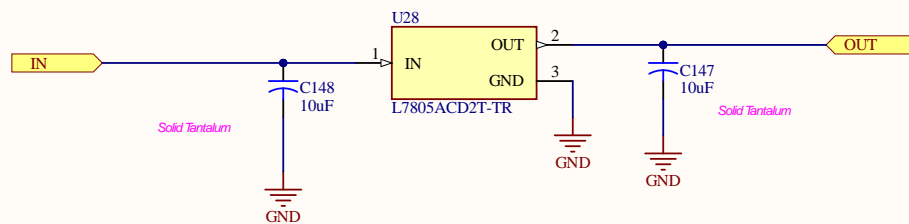


Decoupling Capacitors



Title <i>5kHz AD630 LPF</i>	
RE: <i>Arturo di Girolamo</i>	Size: <i>A3</i>
Date: <i>3/30/2022</i>	

A

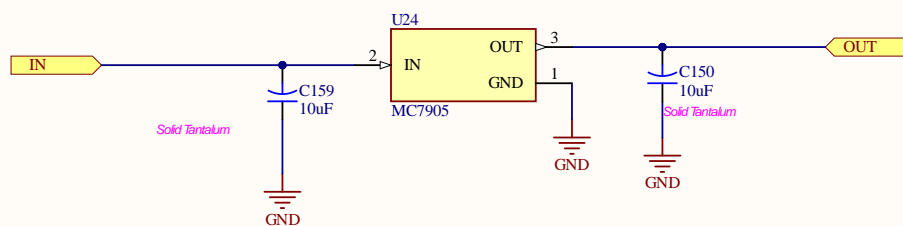


Title <i>5V Digital regulator</i>	
RE: <i>Arturo di Girolamo</i>	Size: <i>A3</i>
Date: <i>3/30/2022</i>	

A

Changelog:

Footprint Changes for MC7905, See Screenshot



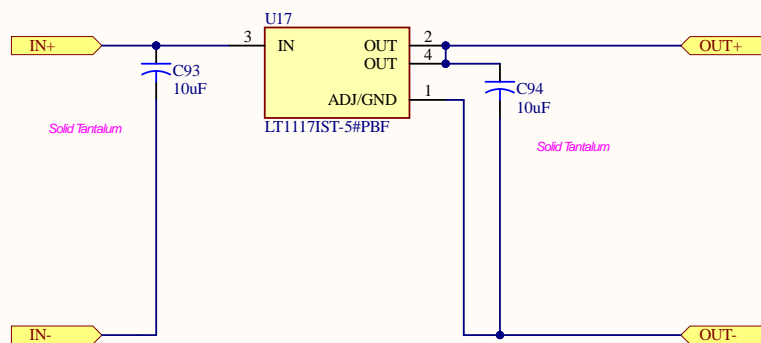
Title: *-5V Digital Regulator*

RE: *Arturo di Girolamo*

Size: *A3*

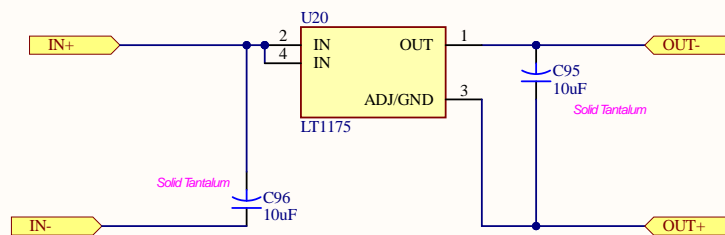
Date: *3/30/2022*

A



Title <i>5V Battery Regulator</i>		
RE: <i>Arturo di Girolamo</i>		Size: <i>A3</i>
Date: <i>3/30/2022</i>		

A

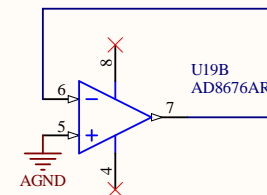
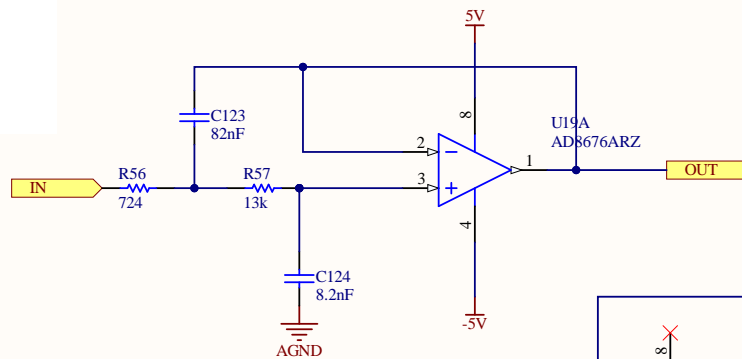
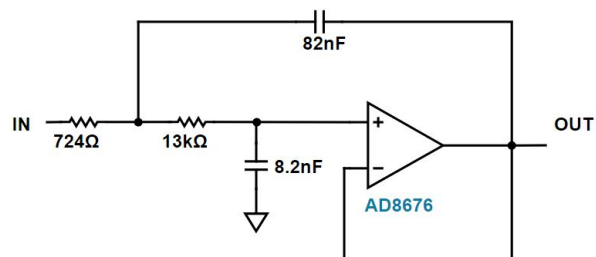


Changelog:
Swapped OUT- and OUT+

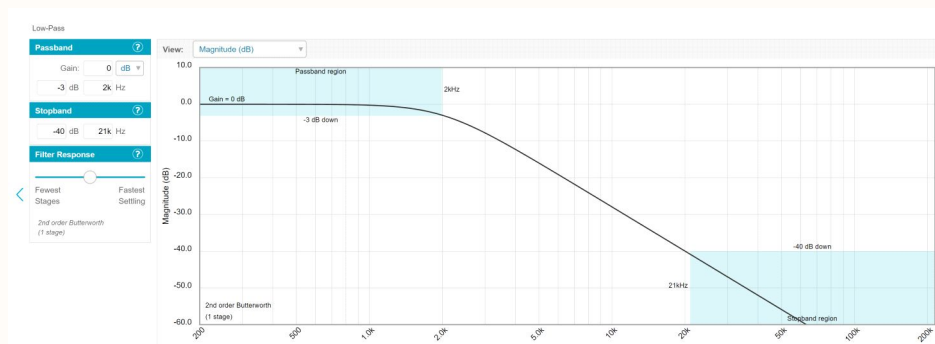
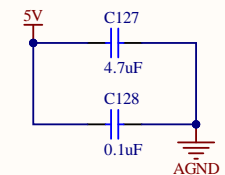
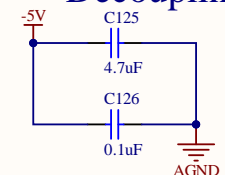
Title: <i>-5V Battery Regulator</i>	
RE: <i>Arturo di Girolamo</i>	Size: <i>A3</i>
Date: <i>3/30/2022</i>	

A

Stage A
2nd order
Low-Pass
Sallen Key



Decoupling Capacitors



Title *LFAD630 LPF*

RE: Arturo di Girolamo

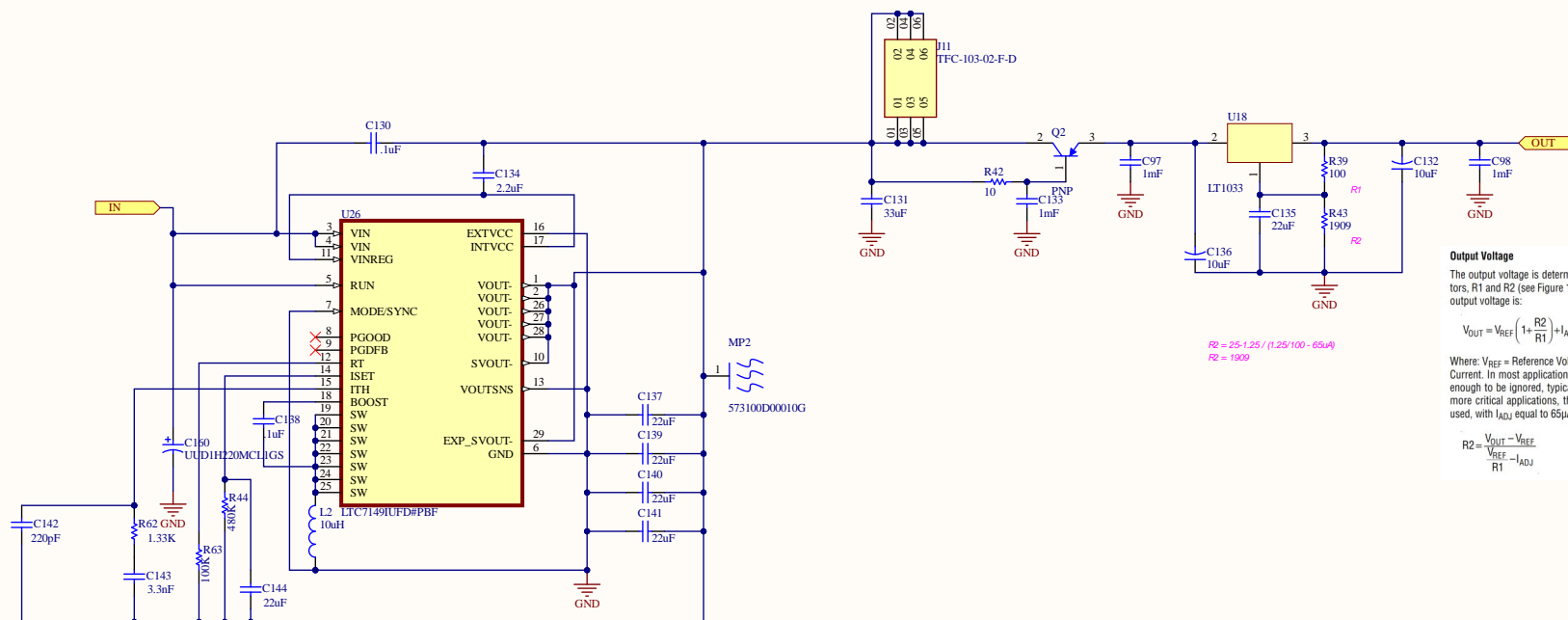
Size: A3

Date: 3/30/2022

A

MAY ADD LC FILTER HERE AFTER TESTS WITH THE ONES ORDERED

Resistance Values will change with output rails



Output Voltage

The output voltage is determined by two external resistors, R1 and R2 (see Figure 1). The exact formula for the output voltage is:

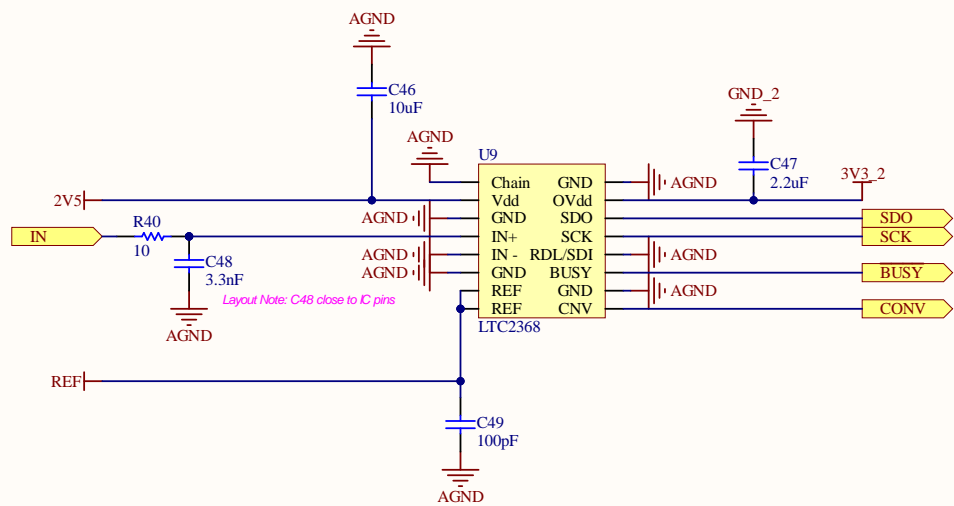
$$V_{OUT} = V_{REF} \left(1 + \frac{R2}{R1} \right) + I_{ADJ}(R2)$$

Where: V_{REF} = Reference Voltage, I_{ADJ} = Adjustment Pin Current. In most applications, the second term is small enough to be ignored, typically about 0.5% of V_{OUT} . In more critical applications, the exact formula should be used, with I_{ADJ} equal to 65uA. Solving for R2 yields:

$$R2 = \frac{V_{OUT} - V_{REF}}{\frac{V_{REF}}{R1} - I_{ADJ}}$$

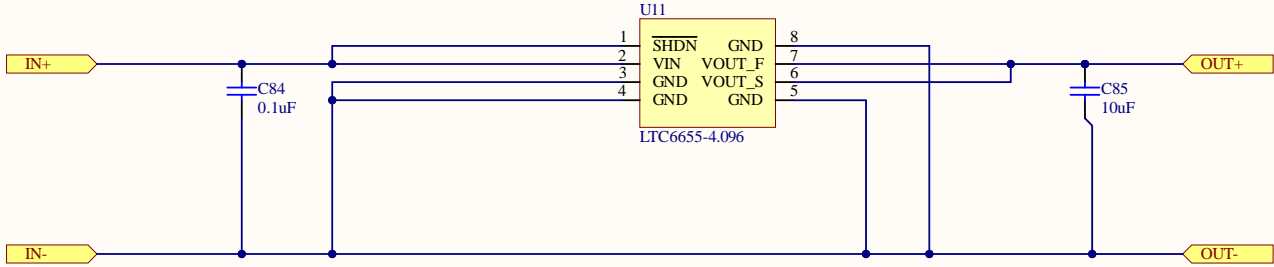
Title 7419 Ckt	
RE: Arturo di Girolamo	Size: A3
Date: 3/30/2022	





Title: ADC	
RE: Arturo di Girolamo	Size: A3
Date: 3/30/2022	

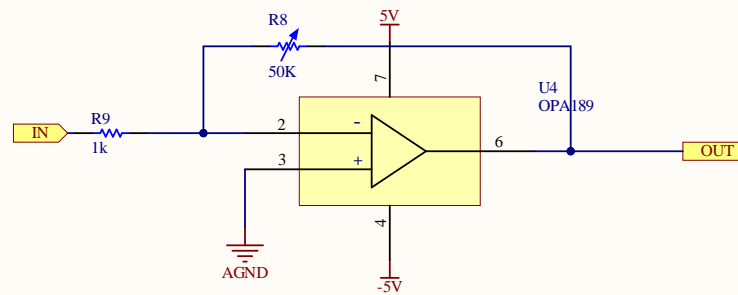
A



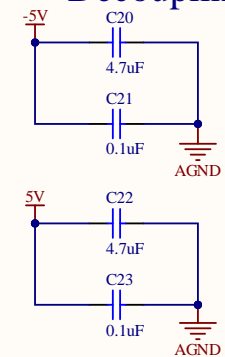
Title <i>ADC Reference</i>	
RE: <i>Arturo di Girolamo</i>	Size: <i>A3</i>
Date: <i>3/30/2022</i>	

A

GAIN SET

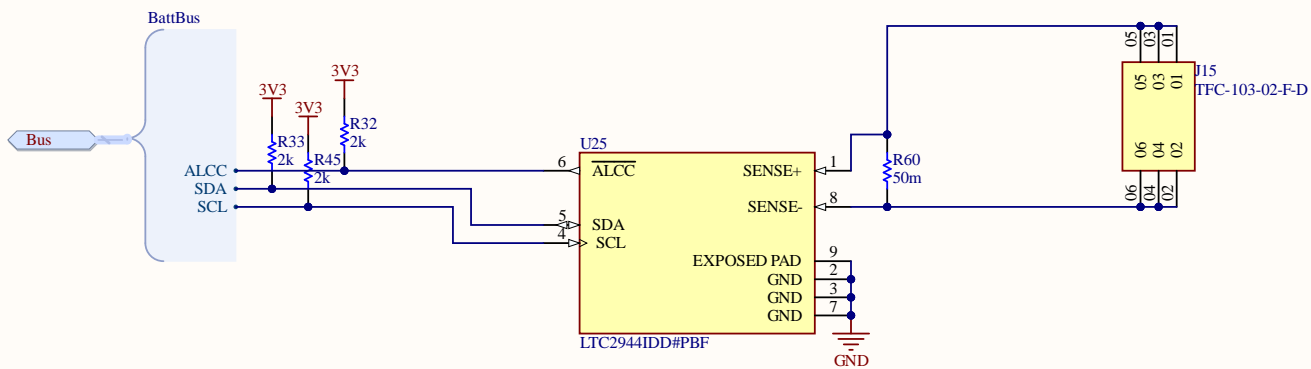


Decoupling Capacitors



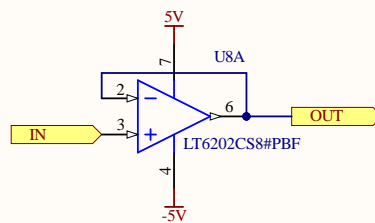
Title <i>Signal Path AMP</i>		
RE: <i>Arturo di Girolamo</i>		Size: <i>A3</i>
Date: <i>3/30/2022</i>		

A

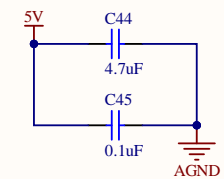
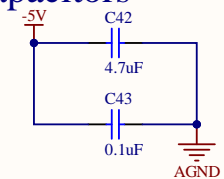


Title <i>Battery Charging</i>	
RE: Arturo di Girolamo	Size: A3
Date: 3/30/2022	

A



Decoupling Capacitors



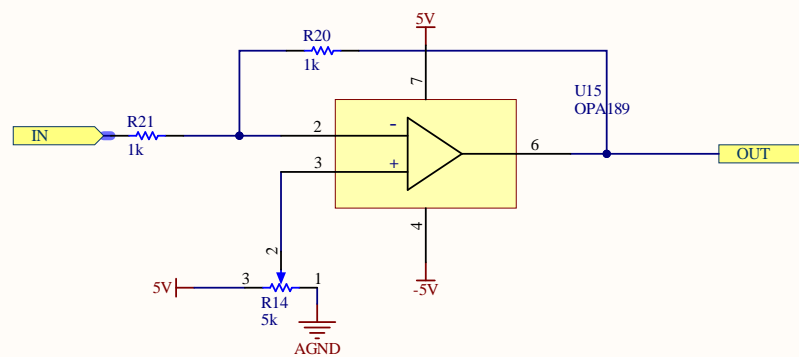
Title *ADC BUFFER*

RE: *Arturo di Girolamo*

Size: *A3*

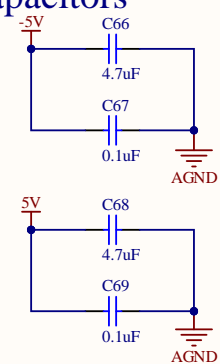
Date: *3/30/2022*

A



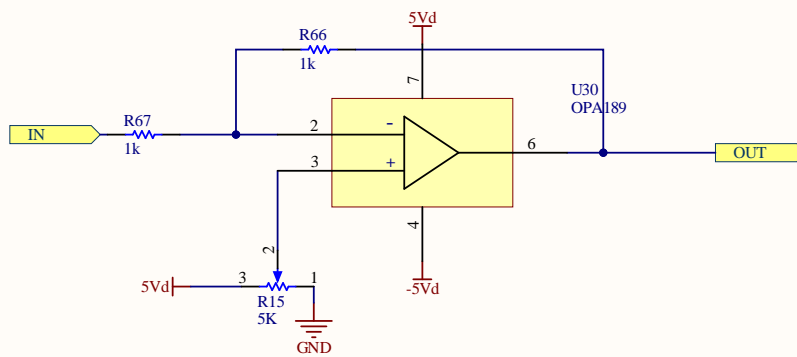
DC SHIFT

Decoupling Capacitors



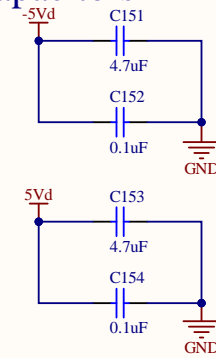
Title		Signal Path DC Shift	
RE:		Arturo di Girolamo	Size: A3
Date:		3/30/2022	

A



DC SHIFT

Decoupling Capacitors



Title <i>Digital DC Shift</i>	
RE: Arturo di Girolamo	Size: A3
Date: 3/30/2022	

A

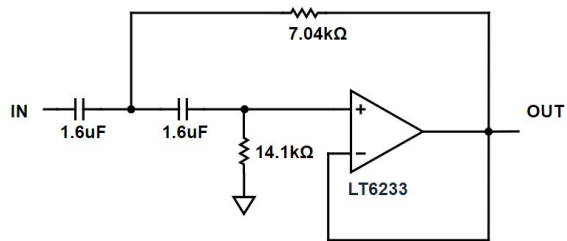
1

2

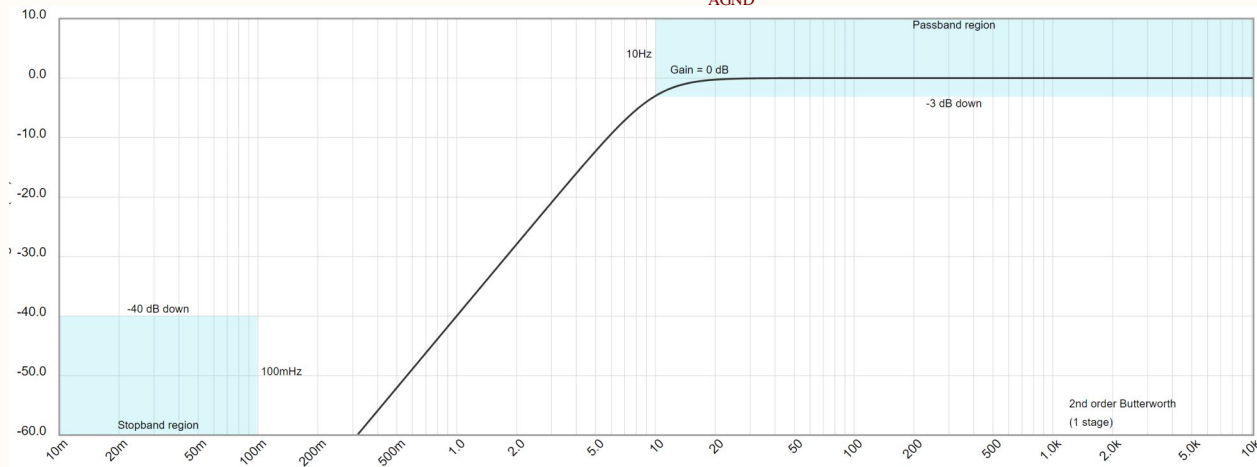
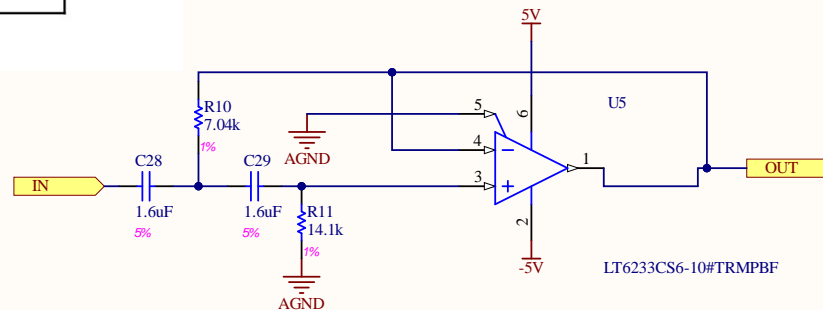
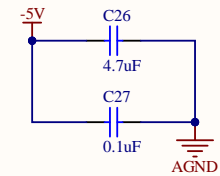
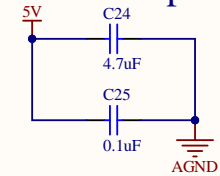
3

4

Stage A
2nd order
High-Pass
Sallen Key



Decoupling Capacitors



Title **HIGH PASS**

RE: **Arturo di Girolamo**

Size: **A3**

Date: **3/30/2022**

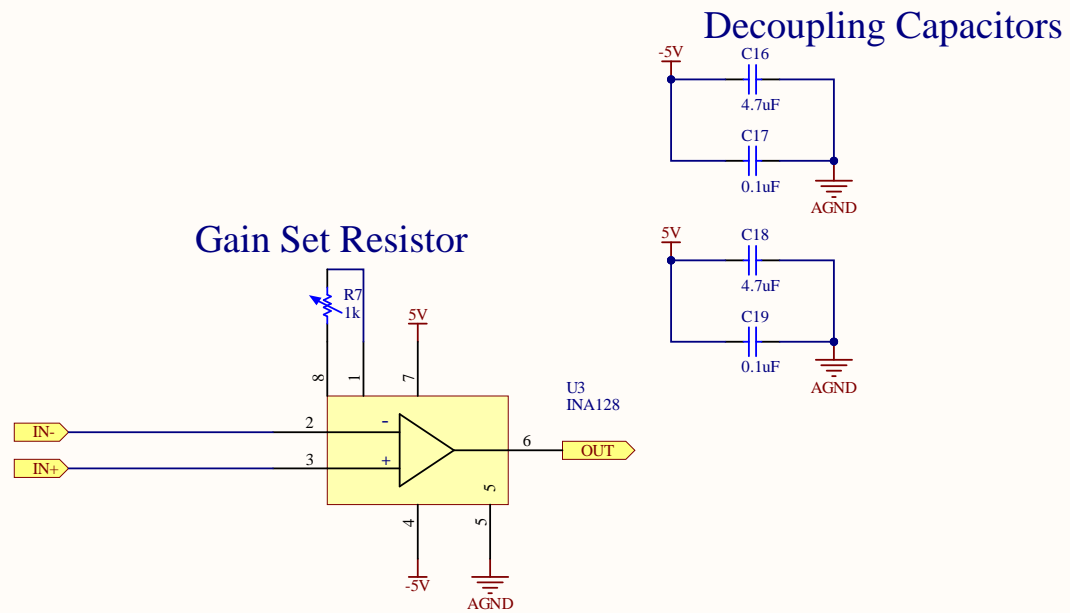
A

1

2

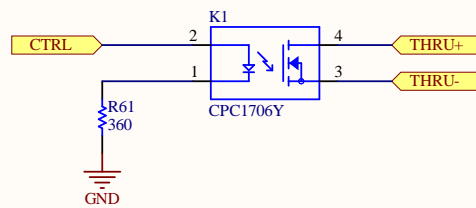
3


4



Title <i>INA STAGE</i>	
RE: Arturo di Girolamo	Size: A3
Date: 3/30/2022	

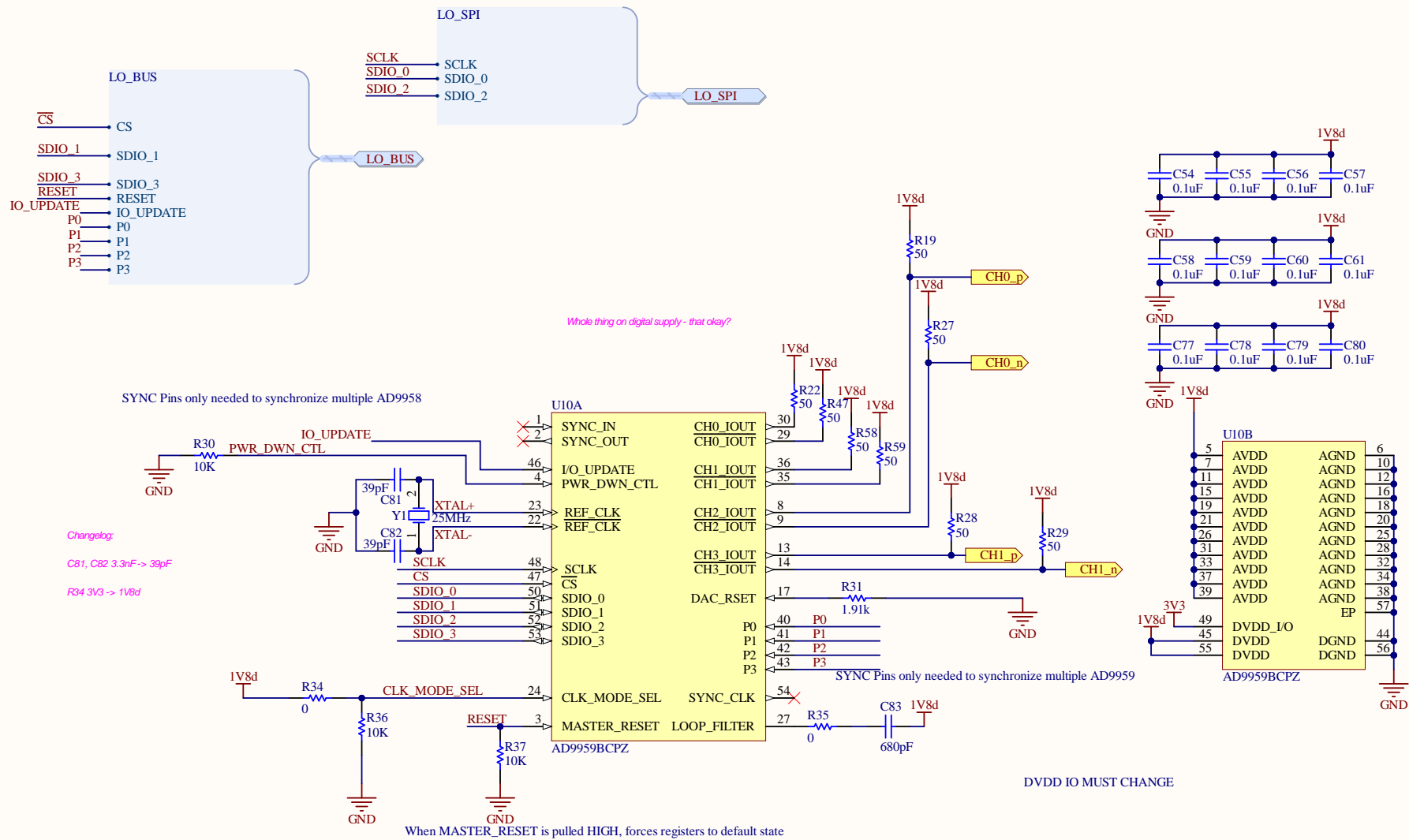
A



Title <i>High Current Relay</i>		
RE: <i>Arturo di Girolamo</i>	Size: <i>A3</i>	
Date: <i>3/30/2022</i>		

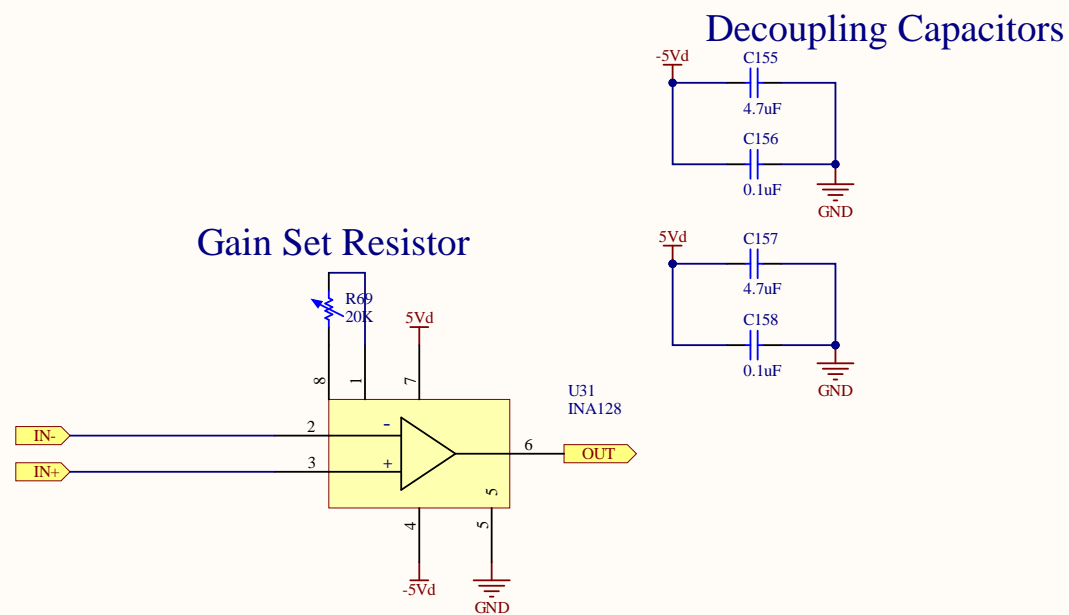
3

4



Title: DDS	
RE: Arturo di Girolamo	Size: A3
Date: 3/30/2022	





Title <i>DDS INA</i>	
RE: Arturo di Girolamo	Size: A3
Date: 3/30/2022	

A

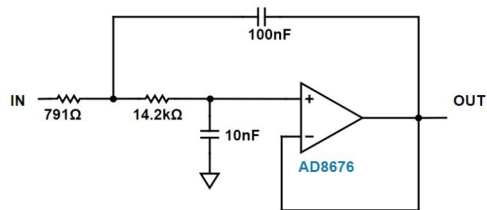
1

2

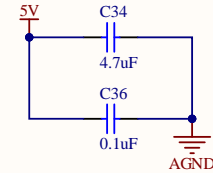
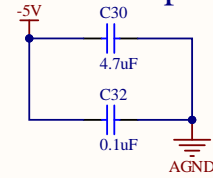
3

4

Stage A
2nd order
Low-Pass
Sallen Key

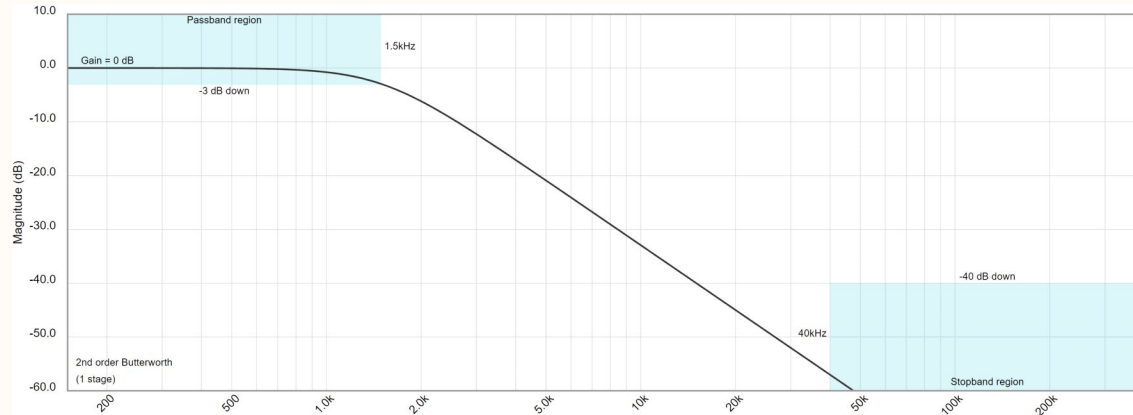
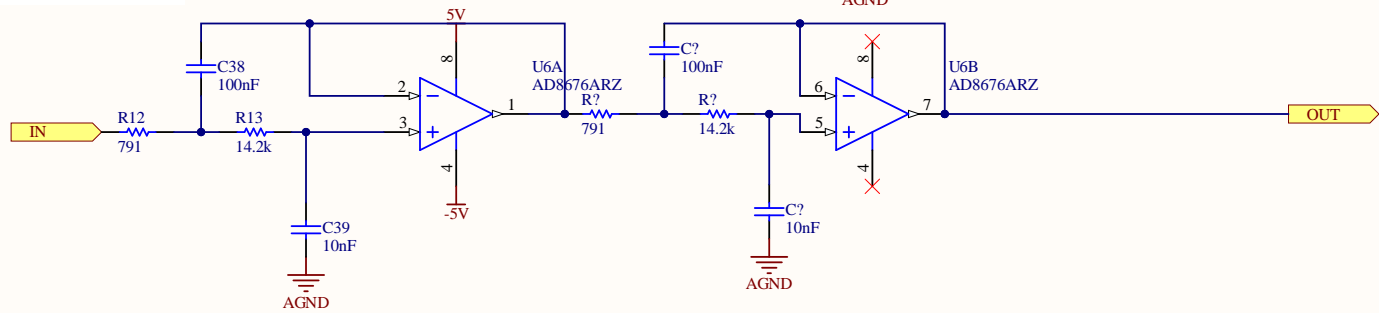


Decoupling Capacitors



Changelog:

R12 791k -> 791



Title **4TH ORDER LOWPASS**

RE: Arturo di Girolamo

Size: A3

Date: 3/30/2022

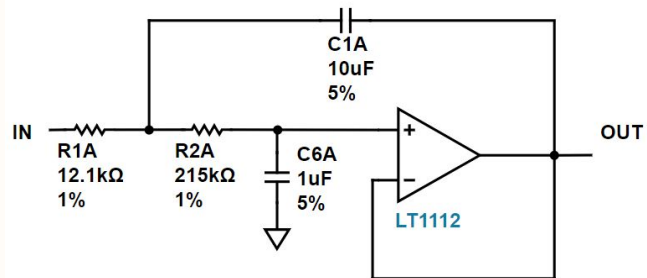
A

1

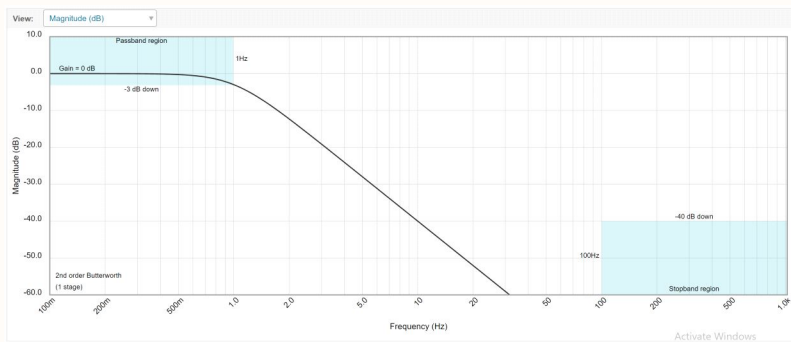
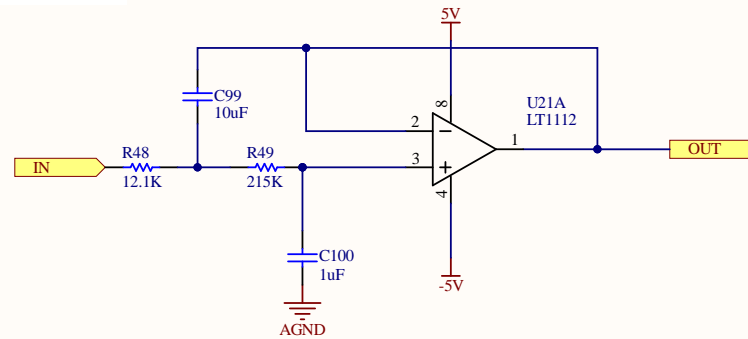
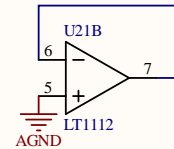
2

3

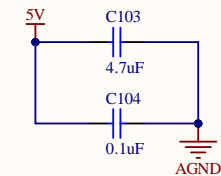
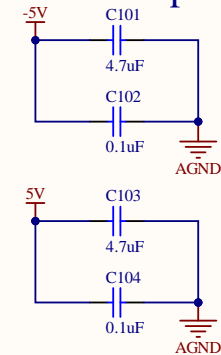
4



Unused OPAMP Configured as buffer to rest mid-supply



Decoupling Capacitors



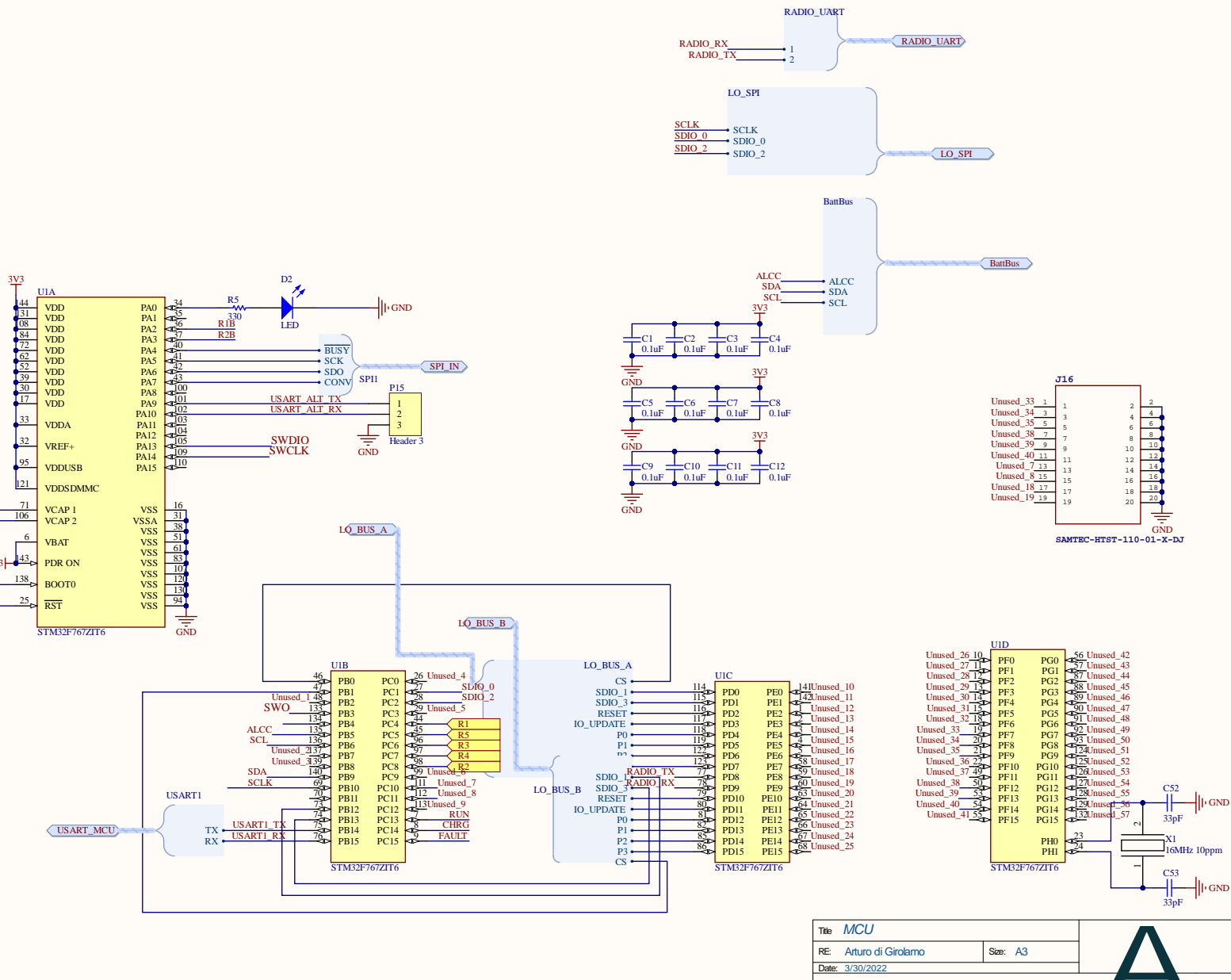
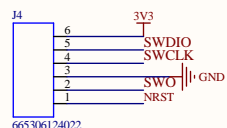
Title	ADC LPF	
RE:	Arturo di Girolamo	Size: A3
Date:	3/30/2022	

A



X1 8MHz-> 16MHz

Changed UART bus locations 2/23/2022



1

2

3

4

A

B

C

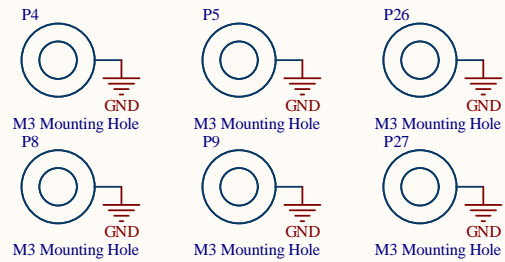
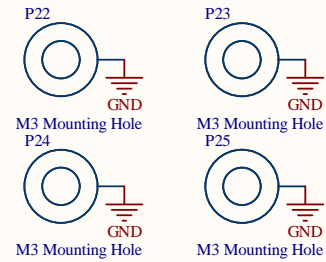
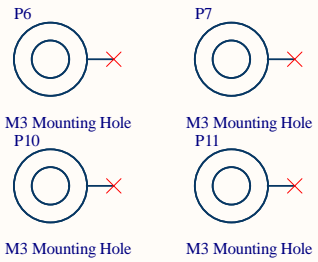
D

A

B

C

D

Title *Mechanical*

RE: Arturo di Girolamo

Size: A3

Date: 3/30/2022

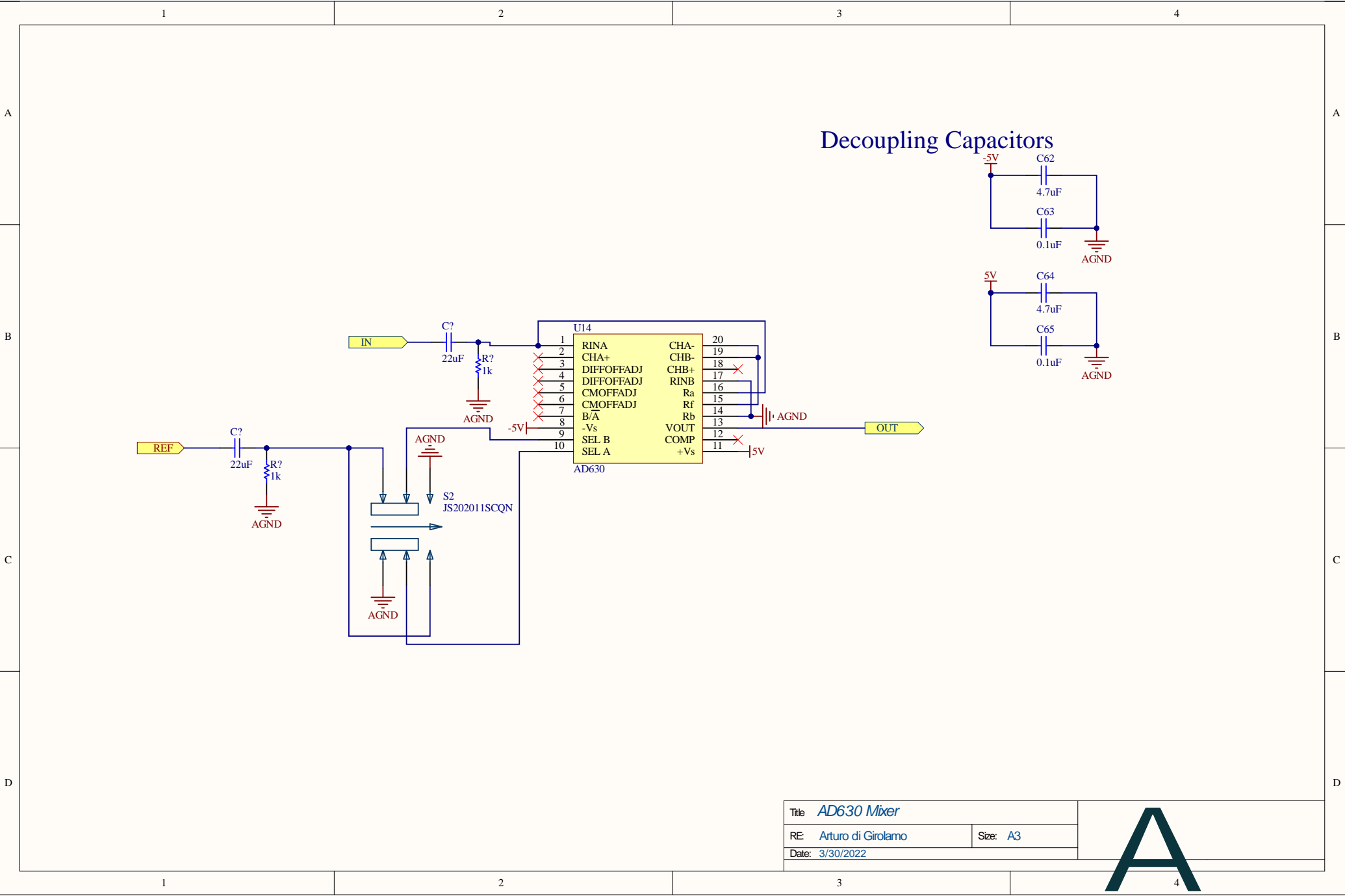
A

1

2

3

4



1

2

3

4

A

B

C

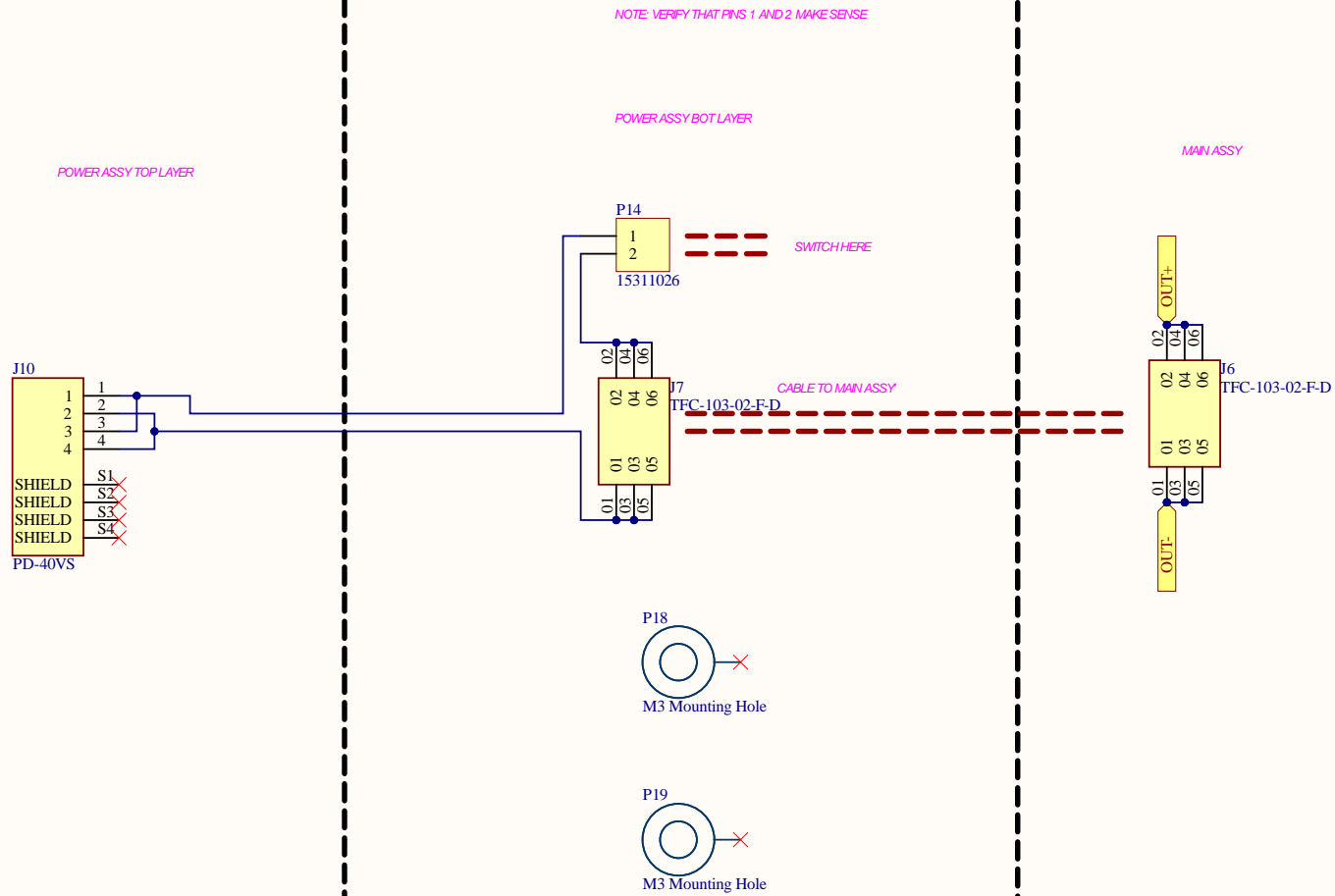
D

A

B

C

D

Title *Power Input PCB*RE: *Arturo di Girolamo*Size: *A3*Date: *3/30/2022***A**

1

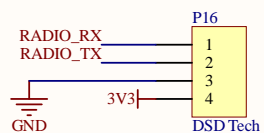
2

3

4

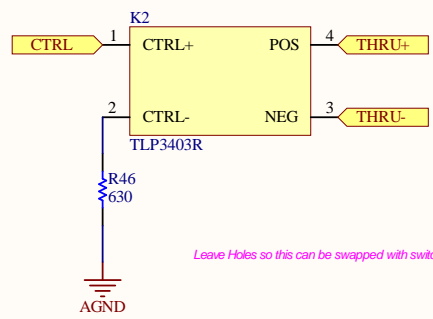
Changelog:
Removed uBlox
Added Header

2/23/2022




Title	uBlox Radio	
RE:	Arturo di Girolamo	Size: A3
Date:	3/30/2022	

A



Leave Holes so this can be swapped with switch

Title: <i>Low Current Relay</i>		
RE: <i>Arturo di Girolamo</i>	Size: <i>A3</i>	
Date: <i>3/30/2022</i>		

3	4
---	---

MPS SYSTEM COMPLETE ASSY

DRAWN A. DI GIROLAMO

MINNEAPOLIS, MN

Title <i>TITLE SHEET</i>	
RE: <i>Arturo di Girolamo</i>	Size: <i>A3</i>
Date: <i>3/30/2022</i>	

A

The diagram illustrates a software-defined radio (SDR) system architecture, divided into several functional blocks:

- Antennas:** Two antennas are connected to the system, with a note: "remember that these caps are THET".
- RF Front-End:**
 - LNA (Low Noise Amplifier):** Amplifies the received signal.
 - LNA FILTER:** Filters the amplified signal.
 - IF AMP (Intermediate Frequency Amplifier):** Amplifies the intermediate frequency signal.
- Mixing and Filtering:**
 - MIXER1:** Mixes the RF signal with the LO signal.
 - IF FILTER:** Filters the intermediate frequency signal.
 - SECOND IF:** Further processing of the intermediate frequency signal.
 - IF FILTER:** Another filter stage for the intermediate frequency.
- ADC (Analog-to-Digital Converter):**
 - ADC BUFFER:** Buffers the ADC output.
 - ADC:** Converts the analog signal to digital.
- Power Regulation:**
 - BATTERY REGULATION:** Regulates the battery input voltage.
 - LO REGULATION:** Regulates the LO (Local Oscillator) input voltage.
 - ADC REGULATION:** Regulates the ADC input voltage.
- Other Components:**
 - LO FILTER:** Filters the LO signal.
 - LO AMP (Local Oscillator Amplifier):** Amplifies the LO signal.
 - ADC REF (ADC Reference):** Provides a reference voltage for the ADC.
 - ADC BUS:** Connects the ADC to the system bus.

The diagram also includes a layout note: "layout note: place dds as close as possible to ferrite" and a note about the ADC regulation: "ADC REGULATION".

COIL DRIVER

INPUT ASSY

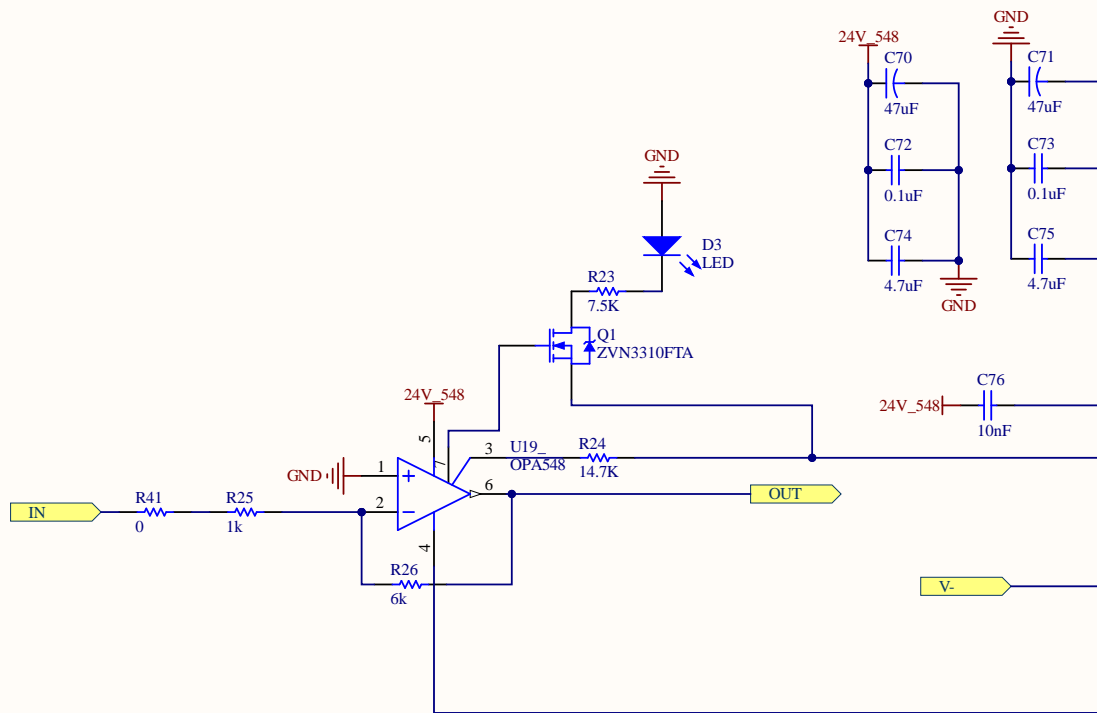
POWER SUPPLY

DIGITAL SECTION

MECH

Table:

Rev	Description	Date
1	Initial Release	01/01/2010
2	Rev. 1	01/01/2010
3	Rev. 2	01/01/2010
4	Rev. 3	01/01/2010
5	Rev. 4	01/01/2010
6	Rev. 5	01/01/2010
7	Rev. 6	01/01/2010
8	Rev. 7	01/01/2010
9	Rev. 8	01/01/2010
10	Rev. 9	01/01/2010
11	Rev. 10	01/01/2010
12	Rev. 11	01/01/2010
13	Rev. 12	01/01/2010
14	Rev. 13	01/01/2010
15	Rev. 14	01/01/2010
16	Rev. 15	01/01/2010
17	Rev. 16	01/01/2010
18	Rev. 17	01/01/2010
19	Rev. 18	01/01/2010
20	Rev. 19	01/01/2010
21	Rev. 20	01/01/2010
22	Rev. 21	01/01/2010
23	Rev. 22	01/01/2010
24	Rev. 23	01/01/2010
25	Rev. 24	01/01/2010
26	Rev. 25	01/01/2010
27	Rev. 26	01/01/2010
28	Rev. 27	01/01/2010
29	Rev. 28	01/01/2010
30	Rev. 29	01/01/2010
31	Rev. 30	01/01/2010
32	Rev. 31	01/01/2010
33	Rev. 32	01/01/2010
34	Rev. 33	01/01/2010
35	Rev. 34	01/01/2010
36	Rev. 35	01/01/2010
37	Rev. 36	01/01/2010
38	Rev. 37	01/01/2010
39	Rev. 38	01/01/2010
40	Rev. 39	01/01/2010
41	Rev. 40	01/01/2010
42	Rev. 41	01/01/2010
43	Rev. 42	01/01/2010
44	Rev. 43	01/01/2010
45	Rev. 44	01/01/2010
46	Rev. 45	01/01/2010
47	Rev. 46	01/01/2010
48	Rev. 47	01/01/2010
49	Rev. 48	01/01/2010
50	Rev. 49	01/01/2010
51	Rev. 50	01/01/2010
52	Rev. 51	01/01/2010
53	Rev. 52	01/01/2010
54	Rev. 53	01/01/2010
55	Rev. 54	01/01/2010
56	Rev. 55	01/01/2010
57	Rev. 56	01/01/2010
58	Rev. 57	01/01/2010
59	Rev. 58	01/01/2010
60	Rev. 59	01/01/2010
61	Rev. 60	01/01/2010
62	Rev. 61	01/01/2010
63	Rev. 62	01/01/2010
64	Rev. 63	01/01/2010
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68	Rev. 67	01/01/2010
69	Rev. 68	01/01/2010
70	Rev. 69	01/01/2010
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75	Rev. 74	01/01/2010
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81	Rev. 80	01/01/2010
82	Rev. 81	01/01/2010
83	Rev. 82	01/01/2010
84	Rev. 83	01/01/2010
85	Rev. 84	01/01/2010
86	Rev. 85	01/01/2010
87	Rev. 86	01/01/2010
88	Rev. 87	01/01/2010
89	Rev. 88	01/01/2010
90	Rev. 89	01/01/2010
91	Rev. 90	01/01/2010
92	Rev. 91	01/01/2010
93	Rev. 92	01/01/2010
94		



Title *548 Voltage source*

RE: Arturo di Girolamo

Size: A3

Date: 3/30/2022

A

1

2

3

4

A

A

B

B

C

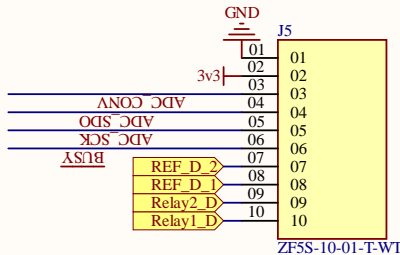
C

D

D

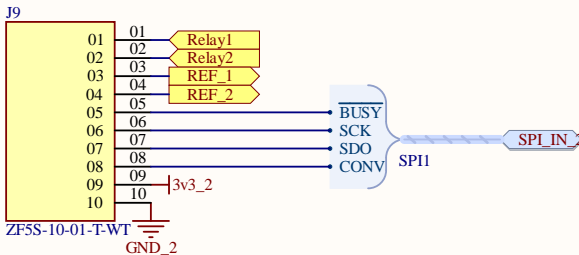
MAIN PCB

swap this for right angle



ANALOG PCB

double check pin alignment with flex cable after layout
or just rotate right angle pi rads



Title *Ribbon Bridge*

RE: Arturo di Girolamo

Size: A3

Date: 3/30/2022

A

1

2

3

4