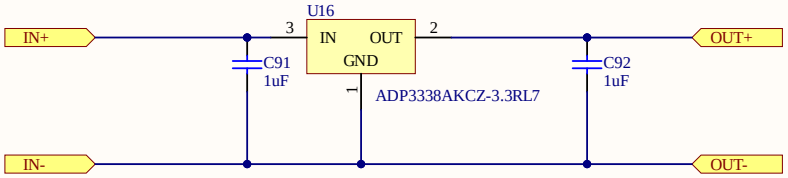
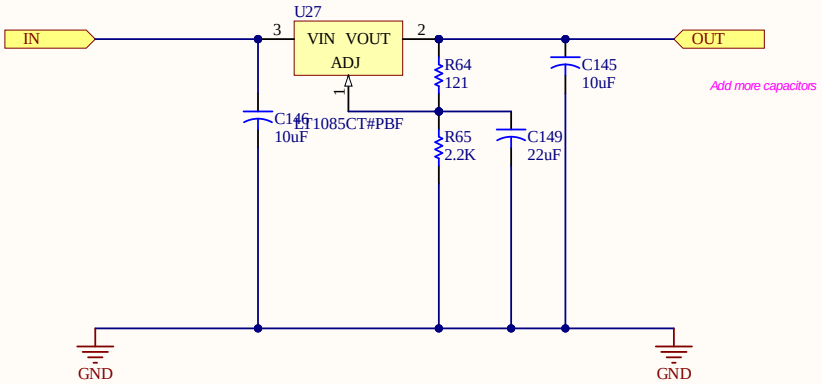


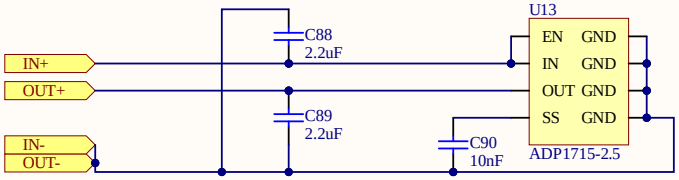
note, make sure to buy 1.8 V version

Title	*1.8V Regulator*
RE: Arturo di Girolamo	Size: A3
Date: 9/4/2021	



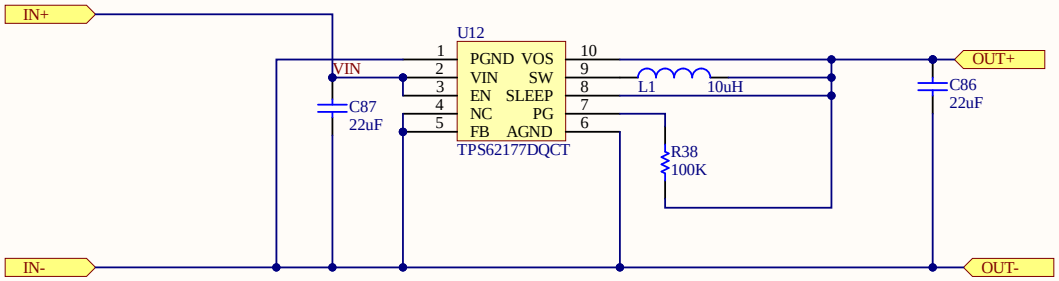
Title	+24V Regulator		
RE:	Arturo di Girolamo	Size:	A3
Date:	9/4/2021		

A



Title	*2.5V ADC Regulator*
RE: Arturo di Girolamo	Size: A3
Date: 9/4/2021	

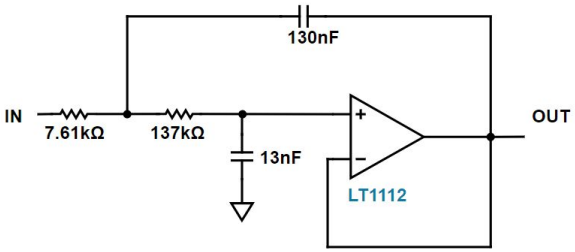
A



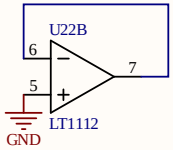
Title	*3.3 Regulator*	
RE:	Arturo di Girolamo	Size: A3
Date:	9/4/2021	

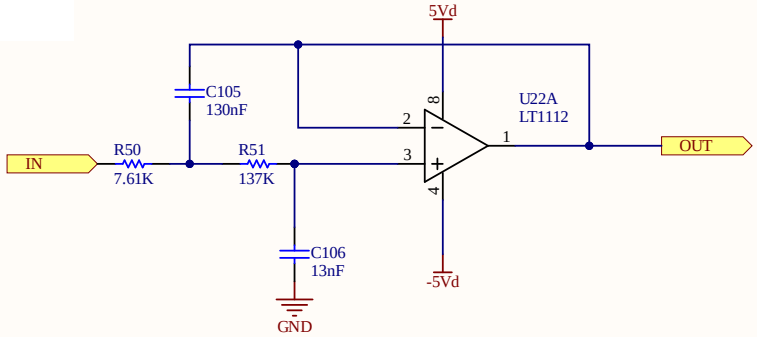
A

Stage A
2nd order
Low-Pass
Sallen Key

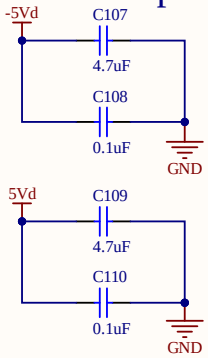


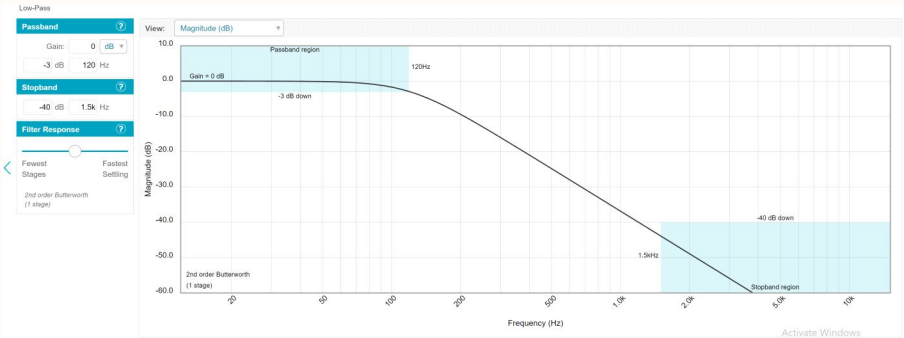
Unused OPAMP Configured as buffer to rest mid-supply





Decoupling Capacitors

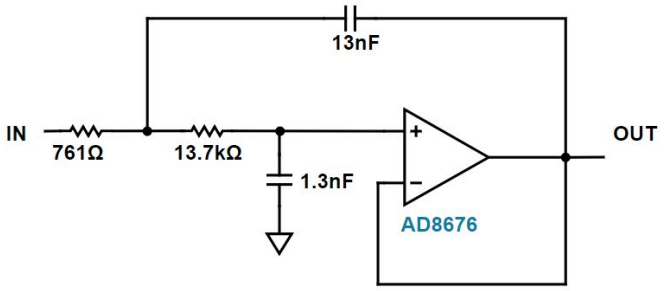


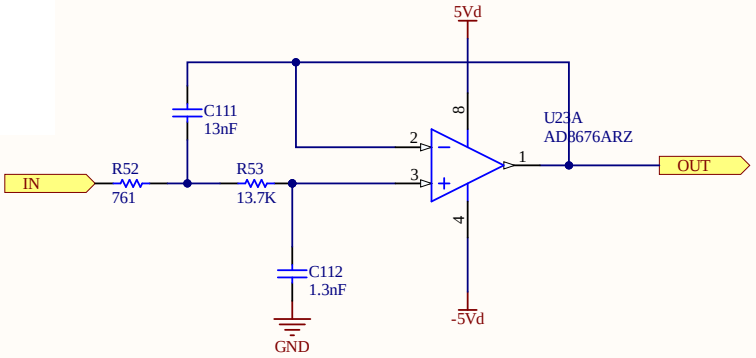


Title	*50 Hz Sine Gen LPF*		
RE:	Arturo di Girolamo	Size:	A3
Date:	9/4/2021		

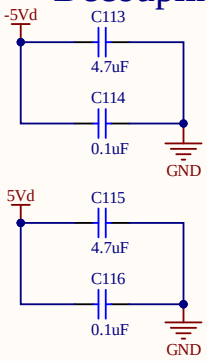
A

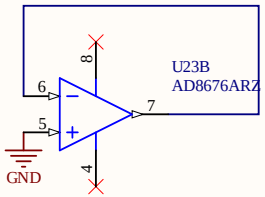
Stage A
2nd order
Low-Pass
Sallen Key

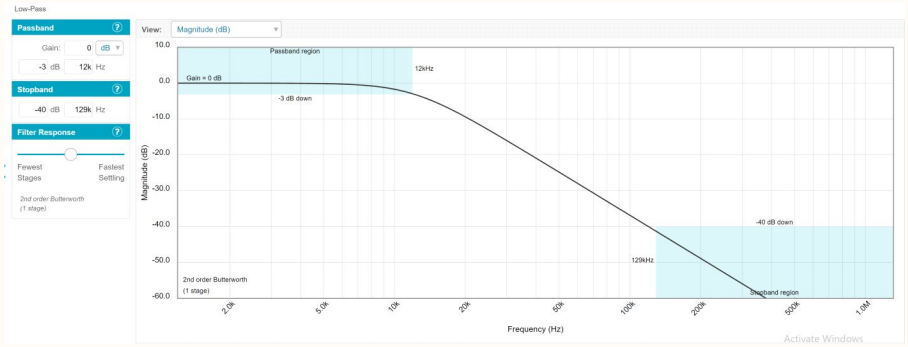




Decoupling Capacitors



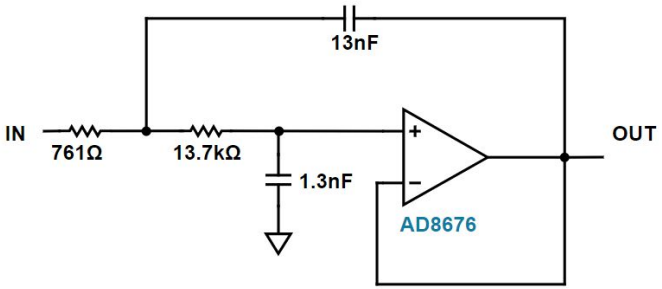


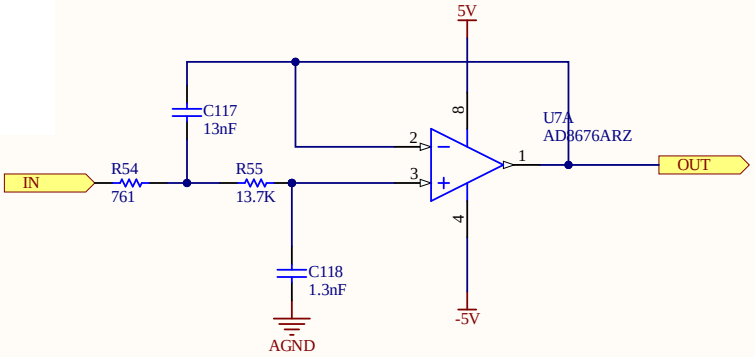


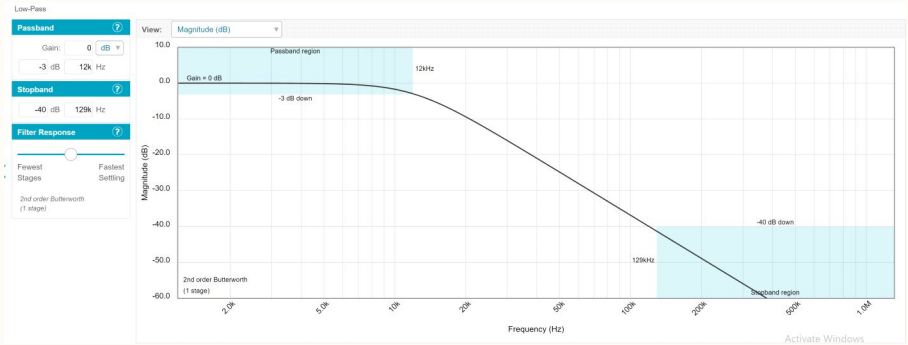
Title	*5kHz Sine Gen LPF*		
RE:	Arturo di Girolamo	Size:	A3
Date:	9/4/2021		

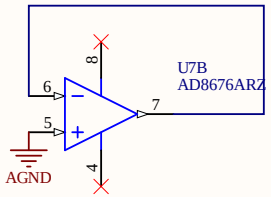
A

Stage A
2nd order
Low-Pass
Sallen Key

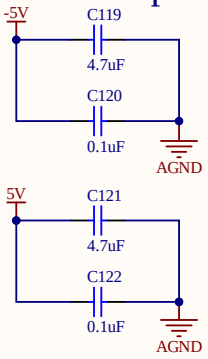






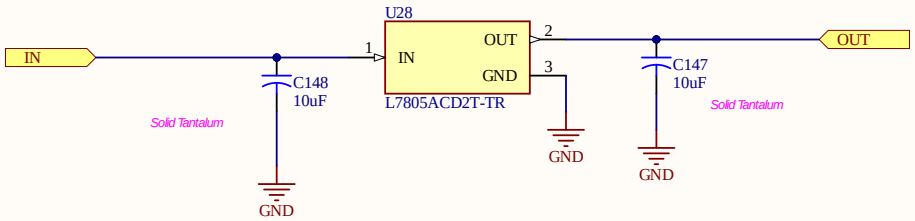


Decoupling Capacitors



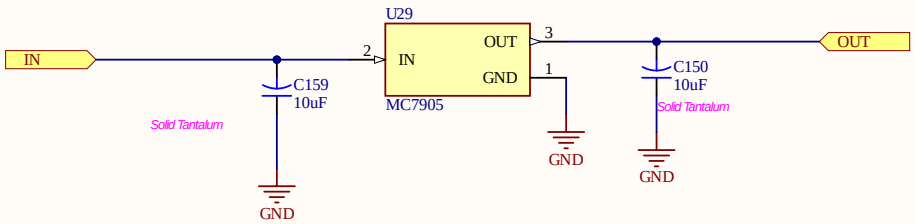
Title	5kHz AD630 LPF	
RE:	Arturo di Girolamo	Size: A3
Date:	9/4/2021	

A



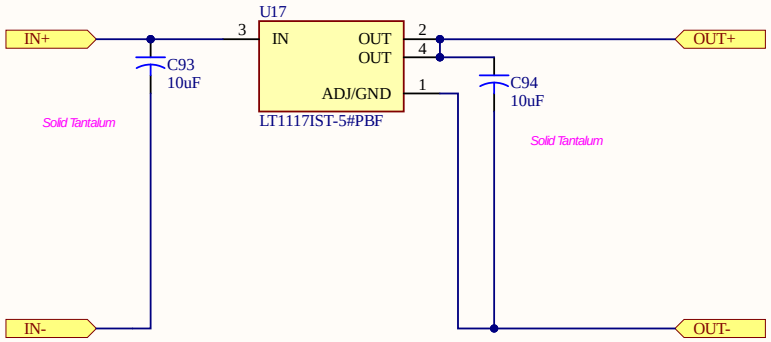
Title	5V Digital regulator
RE:	Arturo di Girolamo
Size:	A3
Date:	9/4/2021

A



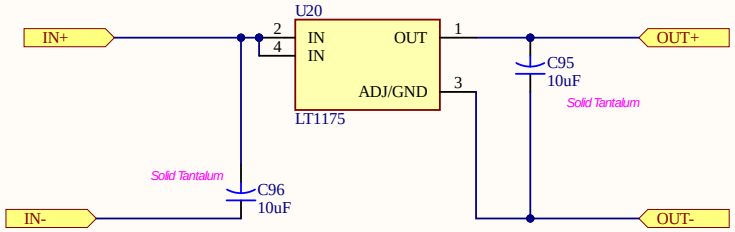
Title	-5V Digital Regulator
RE:	Arturo di Girolamo
Size:	A3
Date:	9/4/2021

A



Title	5V Battery Regulator
RE:	Arturo di Girolamo
Size:	A3
Date:	9/4/2021

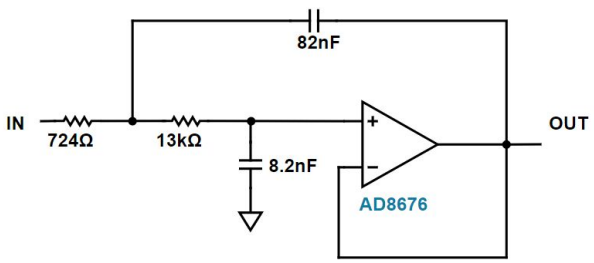
A

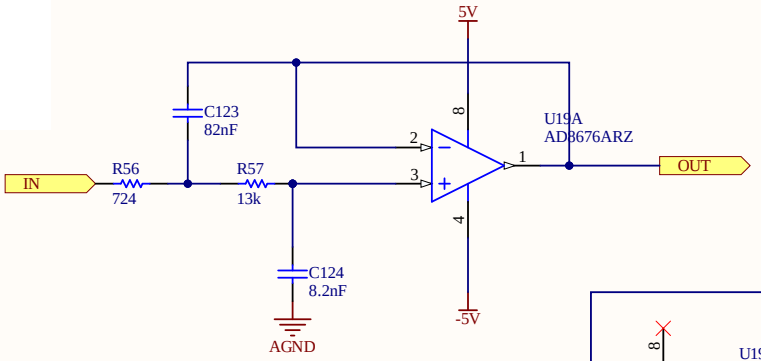


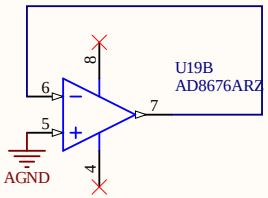
Title	-5V Battery Regulator		
RE:	Arturo di Girolamo	Size:	A3
Date:	9/4/2021		

A

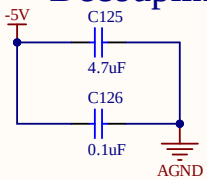
Stage A
2nd order
Low-Pass
Sallen Key

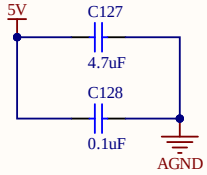


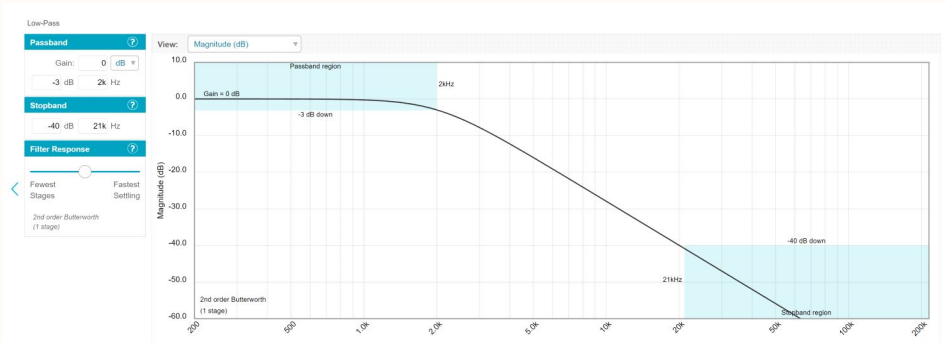




Decoupling Capacitors





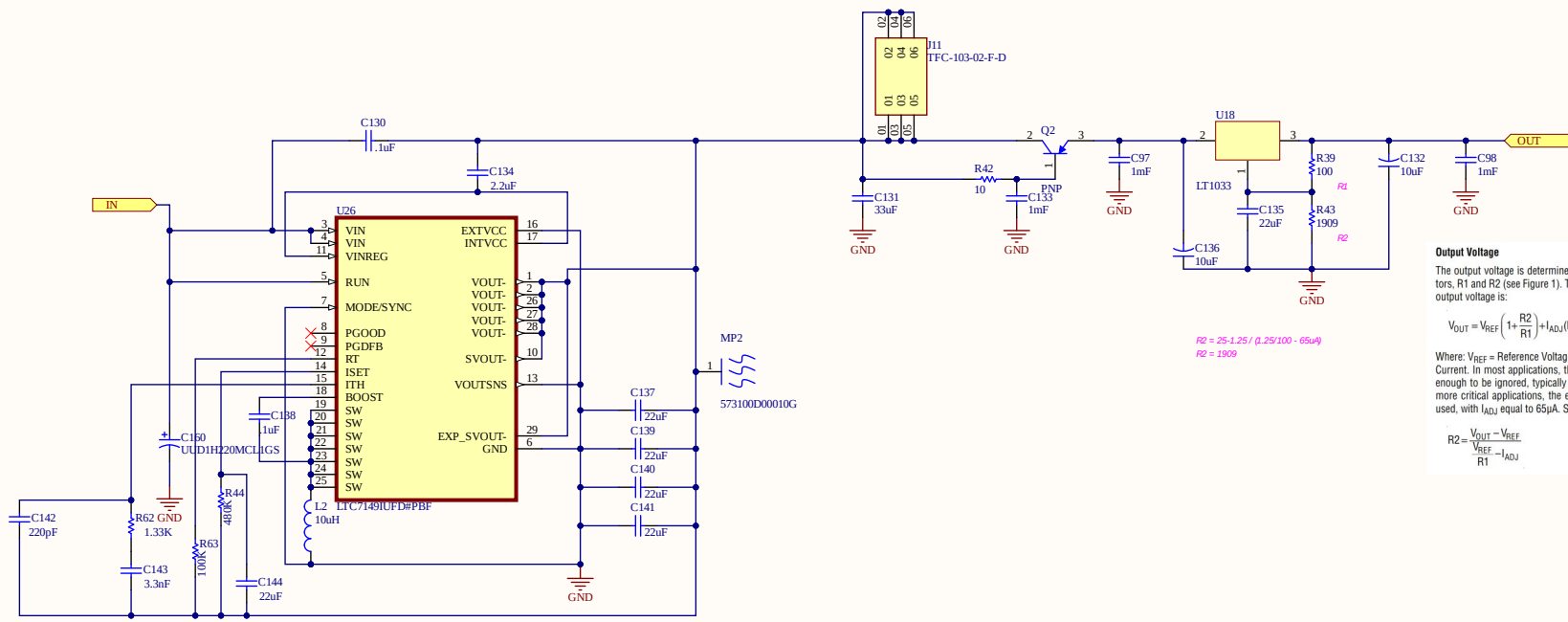


Title	LFAD630 LPF	
RE:	Arturo di Girolamo	Size: A3
Date:	9/4/2021	

A

MAY ADD LC FILTER HERE AFTER TESTS WITH THE ONES ORDERED

Resistance Values will change with output rails



R2 = 25-1.25 / (1.25/100 - 65uA)
R2 = 1909

Output Voltage

The output voltage is determined by two external resistors, R1 and R2 (see Figure 1). The exact formula for the output voltage is:

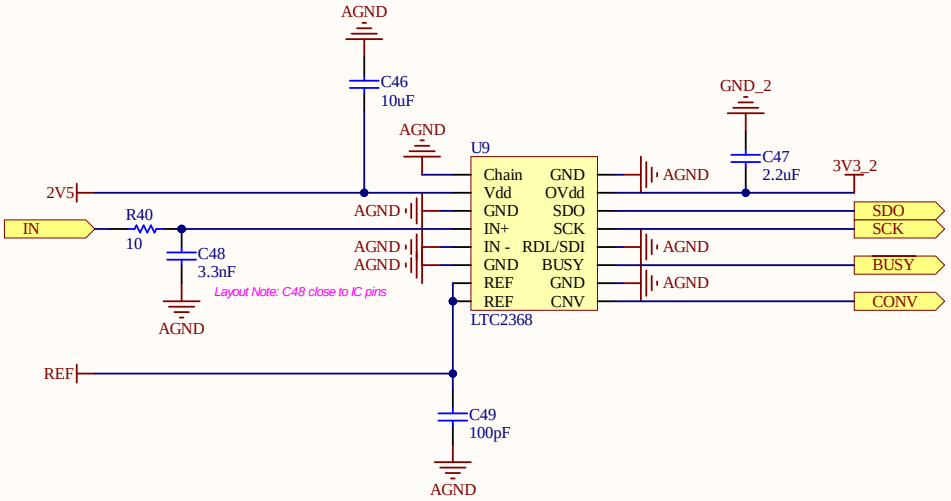
$$V_{OUT} = V_{REF}\left(1+\frac{R2}{R1}\right)+I_{ADJ}(R2)$$

Where: V_{REF} = Reference Voltage, I_{ADJ} = Adjustment Pin Current. In most applications, the second term is small enough to be ignored, typically about 0.5% of V_{OUT}. In more critical applications, the exact formula should be used, with I_{ADJ} equal to 65µA. Solving for R2 yields:

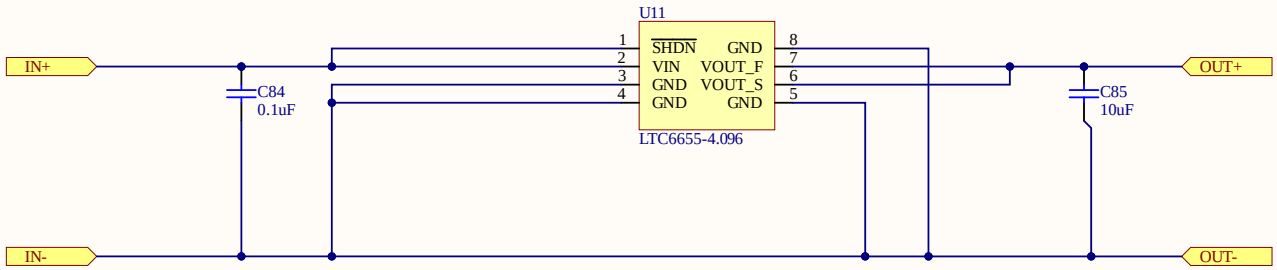
$$R2 = \frac{V_{OUT} - V_{REF}}{\frac{V_{REF}}{R1} - I_{ADJ}}$$

Title	7419 Ckt		
RE:	Arturo di Girolamo	Size:	A3
Date:	9/4/2021		

A



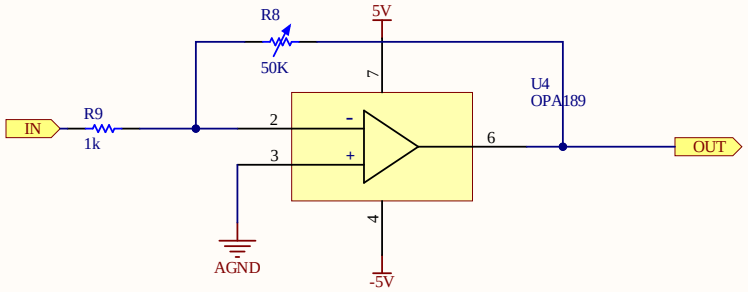
Title	ADC	
RE: Arturo di Girolamo	Size: A3	A
Date: 9/4/2021		



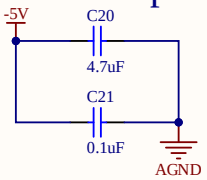
Title	*ADC Reference*	
RE:	Arturo di Girolamo	Size: A3
Date:	9/4/2021	

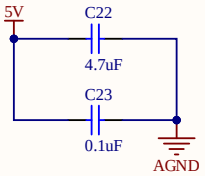
A

GAIN SET



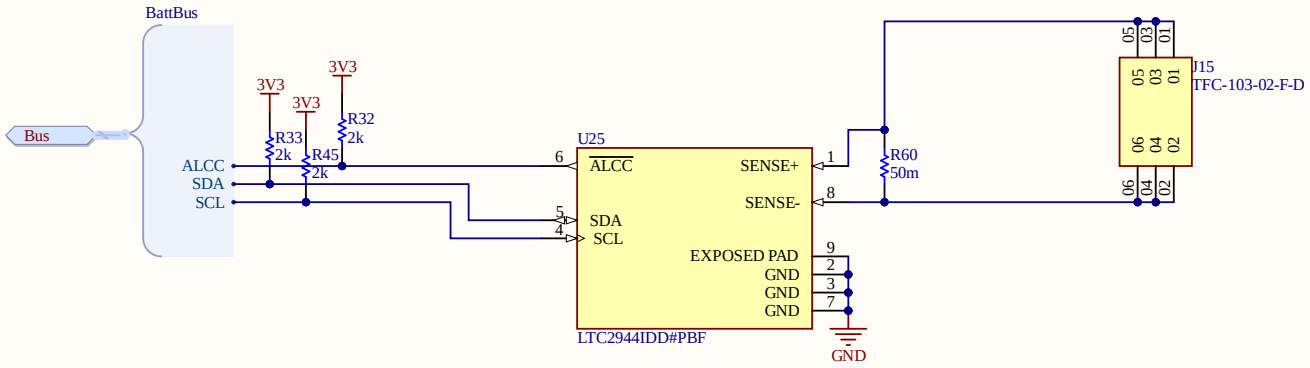
Decoupling Capacitors





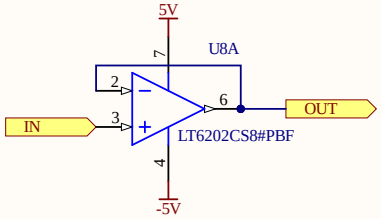
Title	*Signal Path AMP*	
RE:	Arturo di Girolamo	Size: A3
Date:	9/4/2021	

A

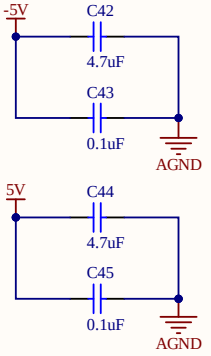


Title	Battery Charging
RE: Arturo di Girolamo	Size: A3
Date: 9/4/2021	

A

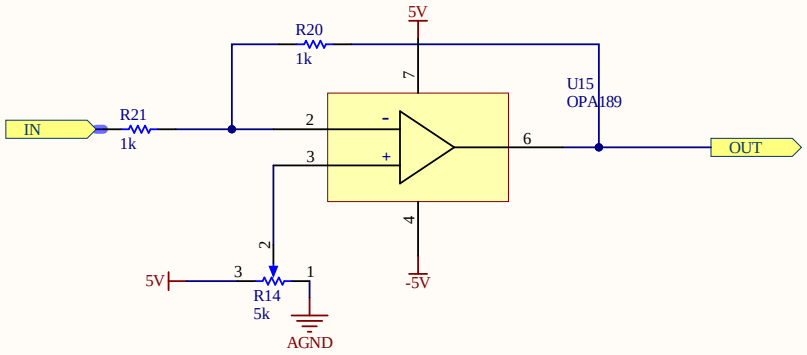


Decoupling Capacitors



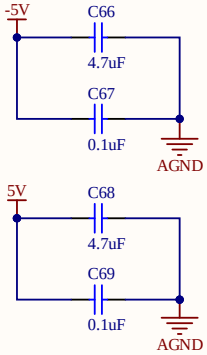
Title	ADC BUFFER
RE: Arturo di Girolamo	Size: A3
Date: 9/4/2021	

A



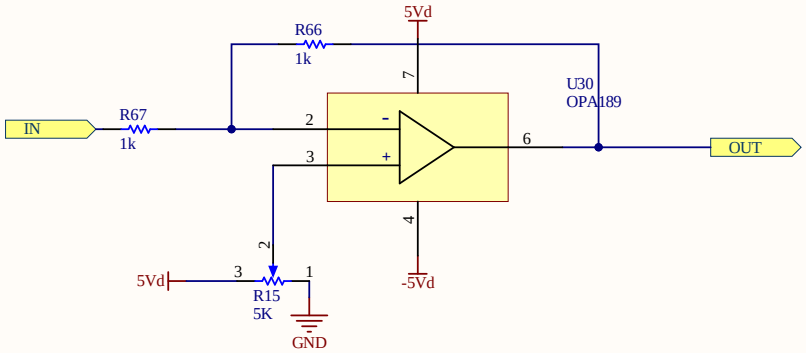
DC SHIFT

Decoupling Capacitors



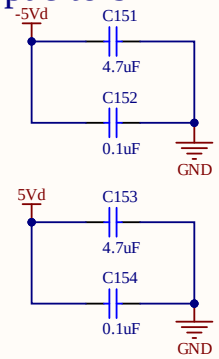
Title	*Signal Path DC Shift*	
RE:	Arturo di Girolamo	Size: A3
Date:	9/4/2021	

A



DC SHIFT

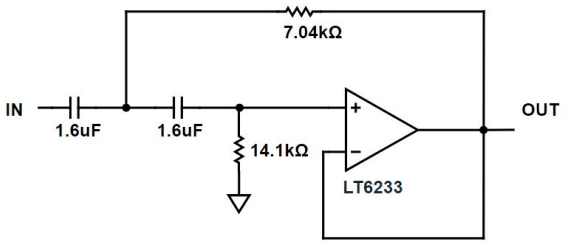
Decoupling Capacitors

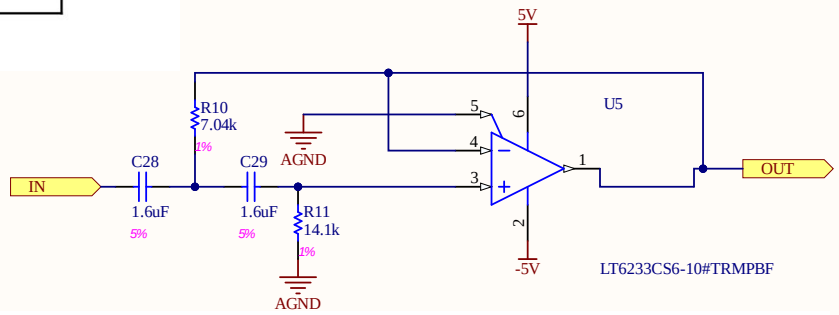


Title	*Digital DC Shift*	
RE:	Arturo di Girolamo	Size: A3
Date:	9/4/2021	

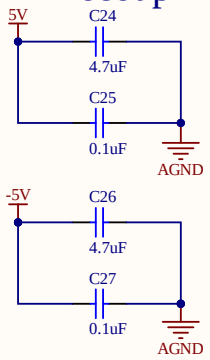
A

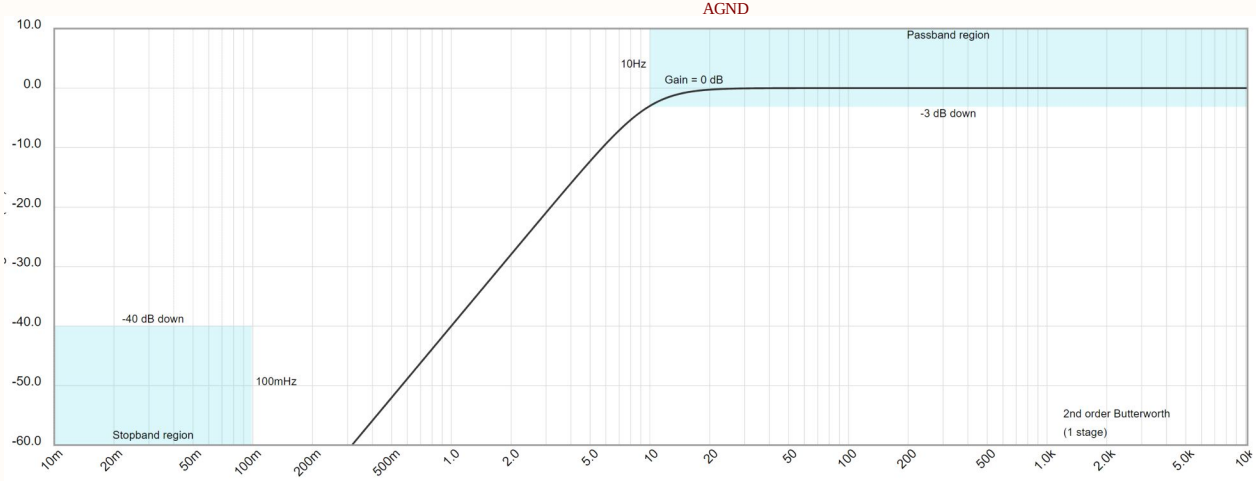
Stage A
2nd order
High-Pass
Sallen Key





Decoupling Capacitors

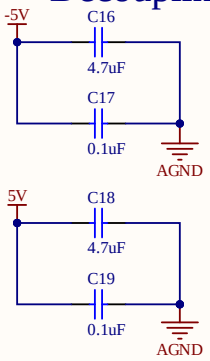




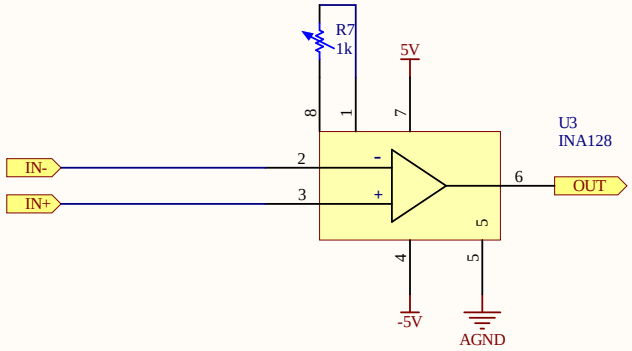
Title	HIGH PASS	
RE:	Arturo di Girolamo	Size: A3
Date:	9/4/2021	

A

Decoupling Capacitors

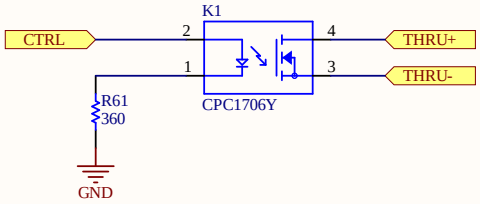


Gain Set Resistor



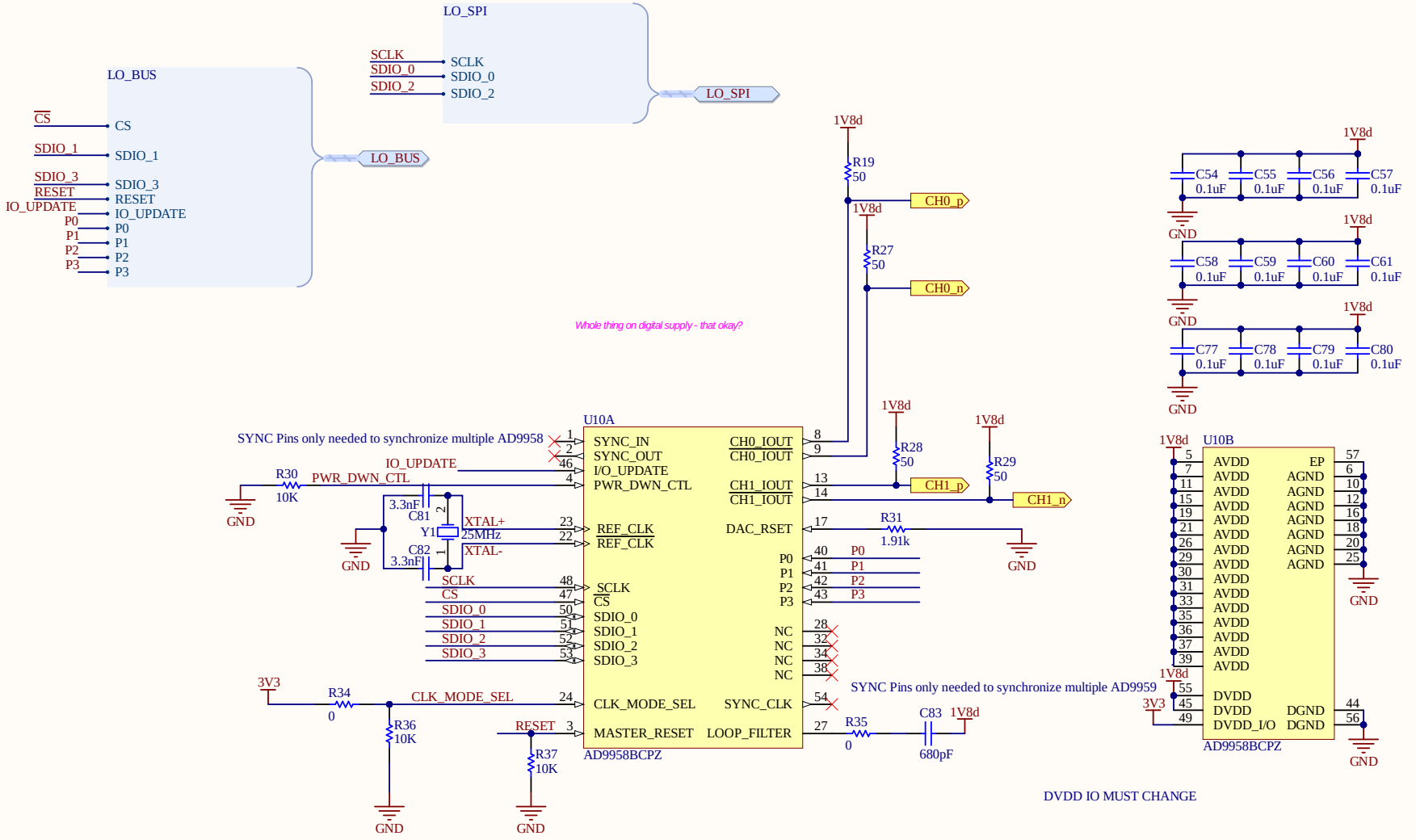
Title	*INA STAGE*	
RE:	Arturo di Girolamo	Size: A3
Date:	9/4/2021	

A

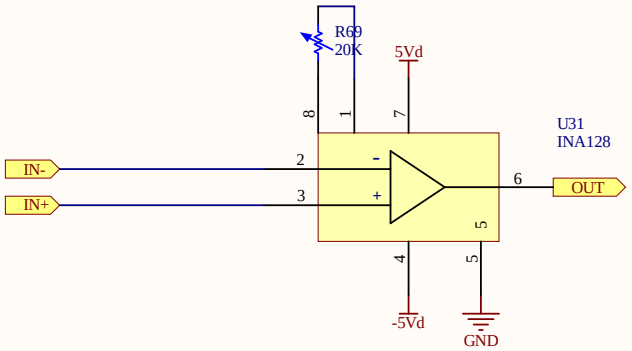


Title	*High Current Relay*
RE: Arturo di Girolamo	Size: A3
Date: 9/4/2021	

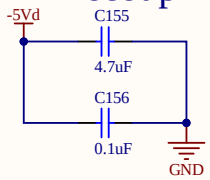
A

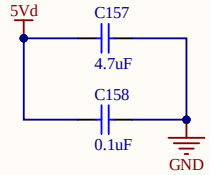

LO_SPI
SCLK
SDIO_0
SDIO_2
SCLK
SDIO_0
SDIO_2
LO_SPI
LO_BUS
CS
SDIO_1
SDIO_3
RESET
IO_UPDATE
P0
P1
P2
P3
CS
SDIO_1
SDIO_3
RESET
IO_UPDATE
P0
P1
P2
P3
LO_BUS
Whole thing on digital supply - that okay?
1V8d
R19
50
CH0_p
R27
50
CH0_n
C54 C55 C56 C57
C58 C59 C60 C61
C77 C78 C79 C80
0.1uF
GND
U10A
SYNC Pins only needed to synchronize multiple AD9958
SYNC_IN
SYNC_OUT
I/O_UPDATE
PWR_DWN_CTL
REF_CLK
REF_CLK
SCLK
CS
SDIO_0
SDIO_1
SDIO_2
SDIO_3
CLK_MODE_SEL
MASTER_RESET
CH0_IOUT
CH0_IOUT
CH1_IOUT
CH1_IOUT
DAC_RSET
P0
P1
P2
P3
NC
SYNC_CLK
LOOP_FILTER
AD9958BCPZ
IO_UPDATE
R30
10K
PWR_DWN_CTL
C81
3.3nF
Y1
25MHz
C82
3.3nF
XTAL+
XTAL-
R28
50
R29
50
CH1_p
CH1_n
R31
1.91k
3V3
R34
0
CLK_MODE_SEL
R36
10K
RESET
R37
10K
R35
0
C83
680pF
When MASTER_RESET is pulled HIGH, forces registers to default state
SYNC Pins only needed to synchronize multiple AD9959
U10B
AVDD
DVDD
DVDD_I/O
AGND
DGND
EP
AD9958BCPZ
DVDD IO MUST CHANGE
Title DDS
RE: Arturo di Girolamo
Size: A3
Date: 9/4/2021
A

Gain Set Resistor



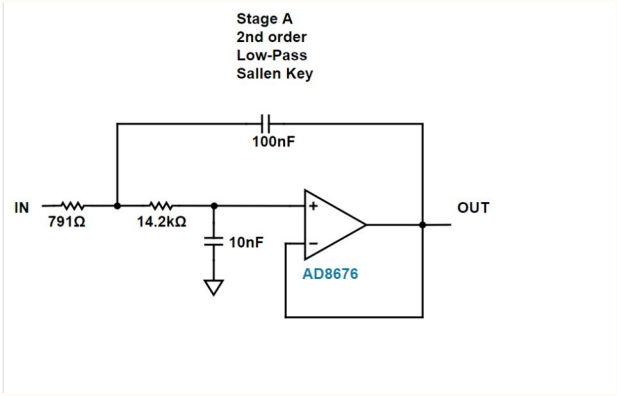
Decoupling Capacitors



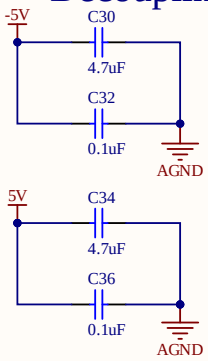


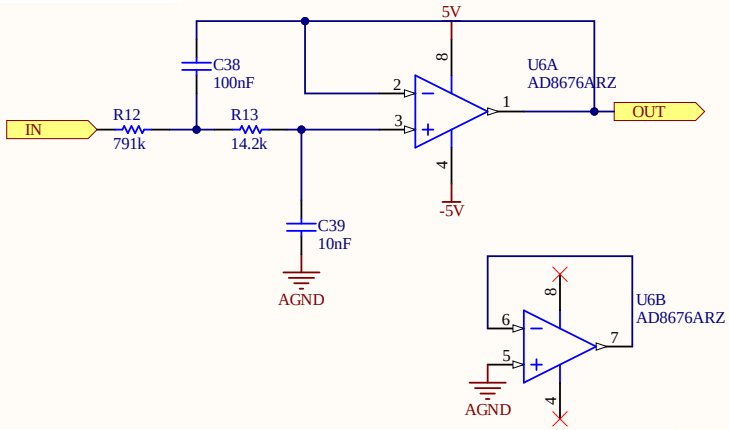
Title	*DDS INA*	
RE:	Arturo di Girolamo	Size: A3
Date:	9/4/2021	

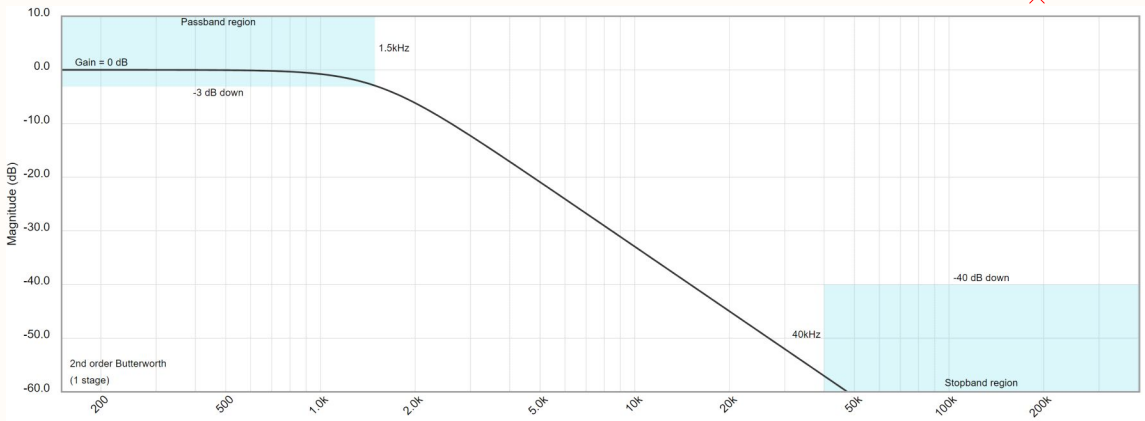
A



Decoupling Capacitors

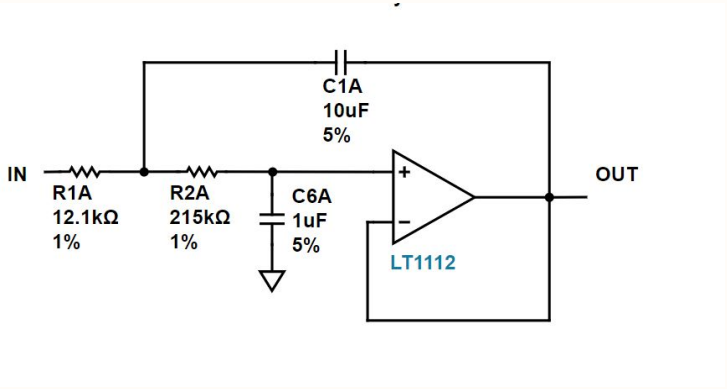




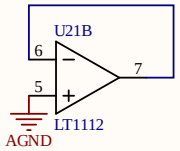


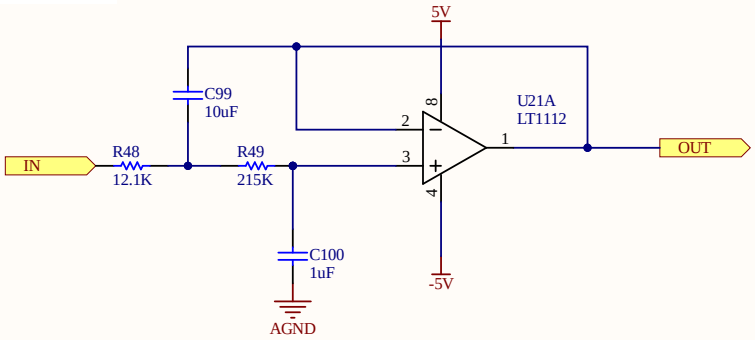
Title	*4TH ORDER LOWPASS*	
RE:	Arturo di Girolamo	Size: A3
Date:	9/4/2021	

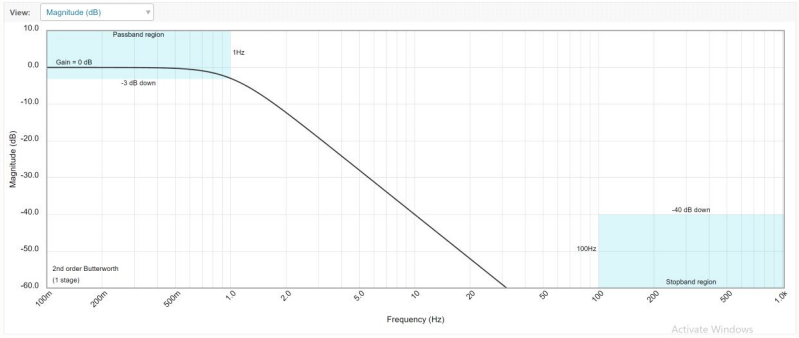
A



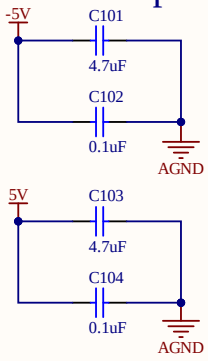
Unused OPAMP Configured as buffer to rest mid-supply





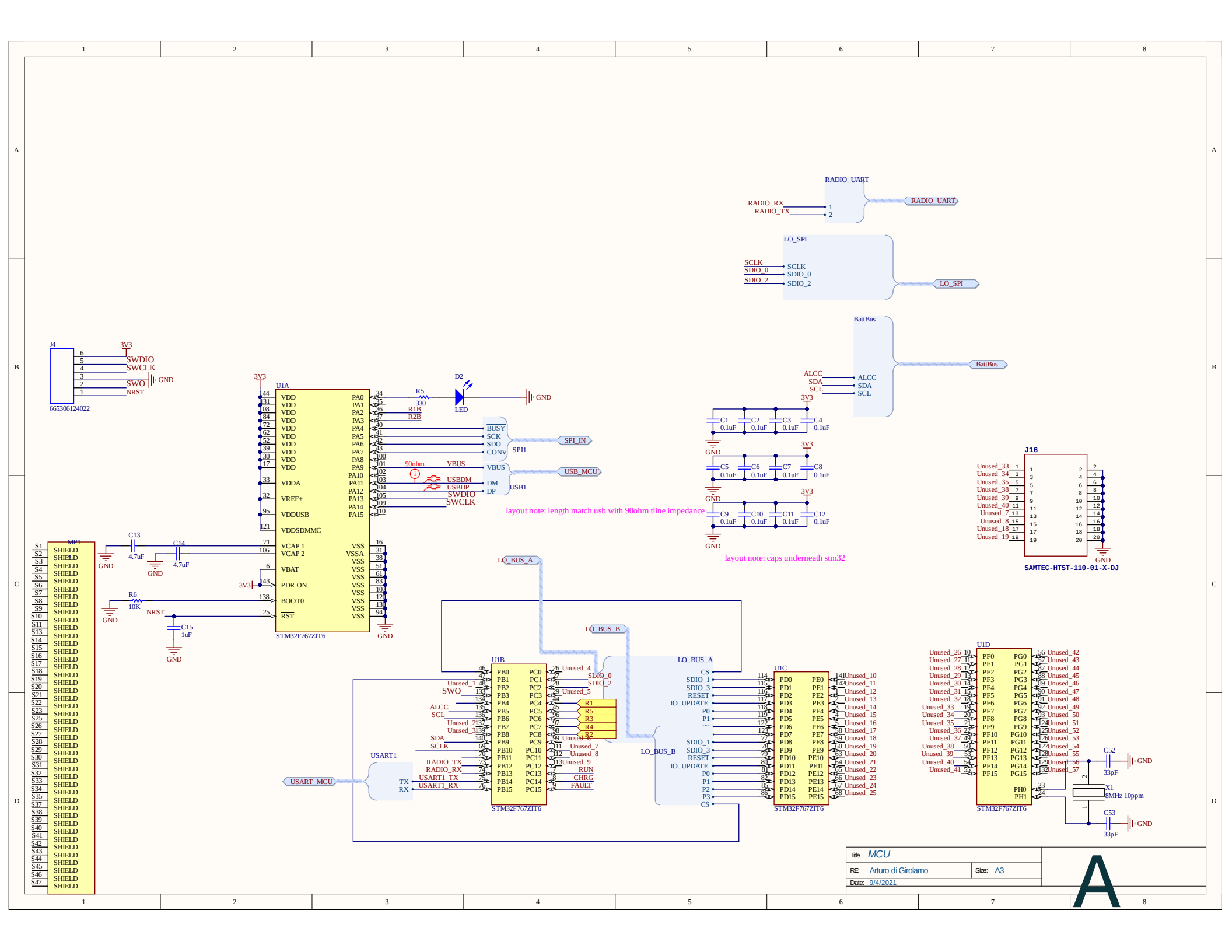


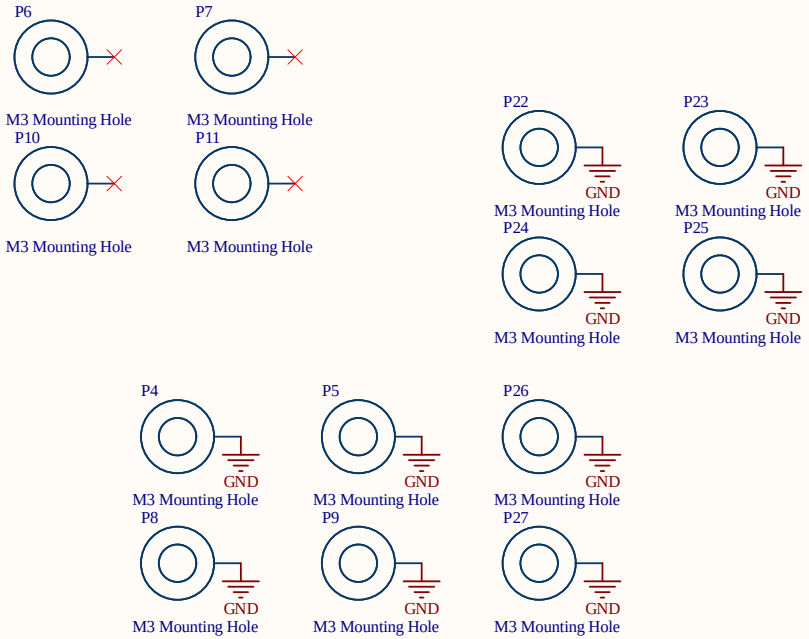
Decoupling Capacitors



Title	*ADC LPF*	
RE:	Arturo di Girolamo	Size: A3
Date:	9/4/2021	

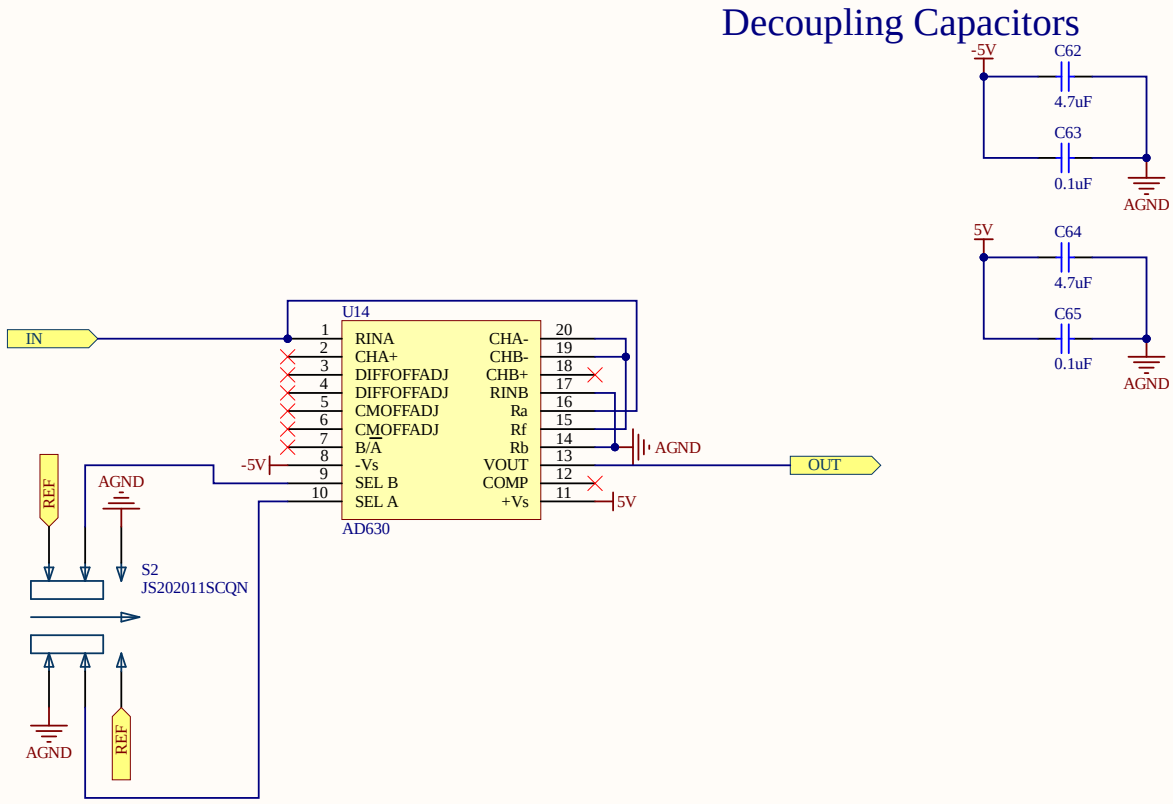
A


RADIO_UART
RADIO_RX
RADIO_TX
LO_SPI
SCLK
SDIO_0
SDIO_2
BattBus
ALCC
SDA
SCL
J4
3V3
SWDIO
SWCLK
SWO
NRST
GND
665306124022
U1A
STM32F767ZIT6
D2
LED
R5
330
R1B
R2B
BUSY
SCK
SDO
CONV
SPI1
SPI_IN
90ohm
VBUS
USB_MCU
USBDM
USBDP
DM
DP
USB1
layout note: length match usb with 90ohm tline impedance
C1
C2
C3
C4
C5
C6
C7
C8
C9
C10
C11
C12
0.1uF
layout note: caps underneath stm32
J16
SAMTEC-HTST-110-01-X-DJ
MP1
C13
C14
4.7uF
R6
10K
NRST
C15
1uF
LO_BUS_A
LO_BUS_B
U1B
U1C
U1D
USART1
USART_MCU
TX
RX
USART1_TX
USART1_RX
RADIO_TX
RADIO_RX
SDIO_0
SDIO_2
SDIO_1
SDIO_3
RESET
IO_UPDATE
P0
P1
P2
P3
CS
R1
R5
R3
R4
R2
RUN
CHRG
FAULT
C52
C53
33pF
X1
8MHz 10ppm
Title MCU
RE: Arturo di Girolamo
Size: A3
Date: 9/4/2021
A



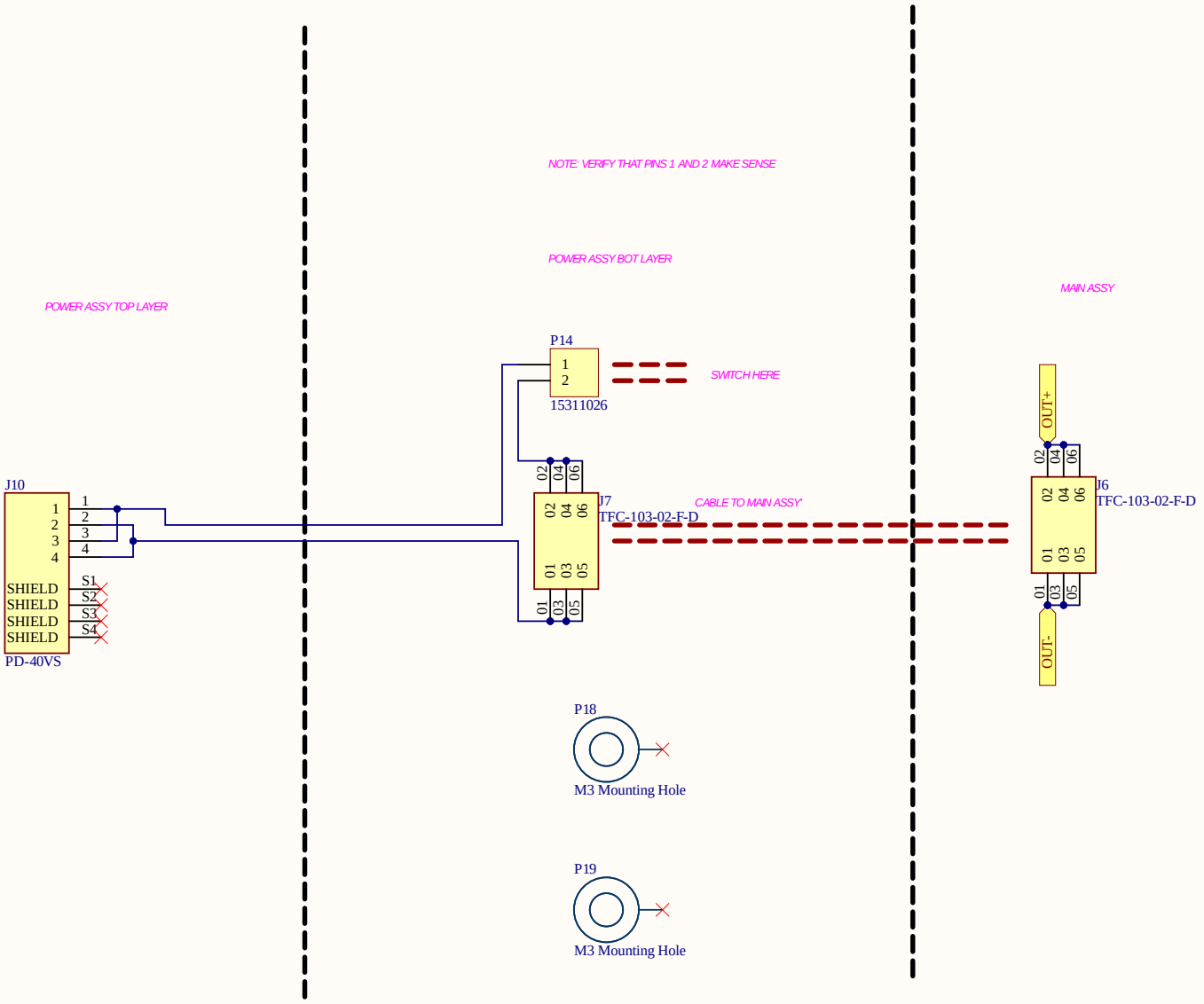
Title	*Mechanical*	
RE:	Arturo di Girolamo	Size: A3
Date:	9/4/2021	

A



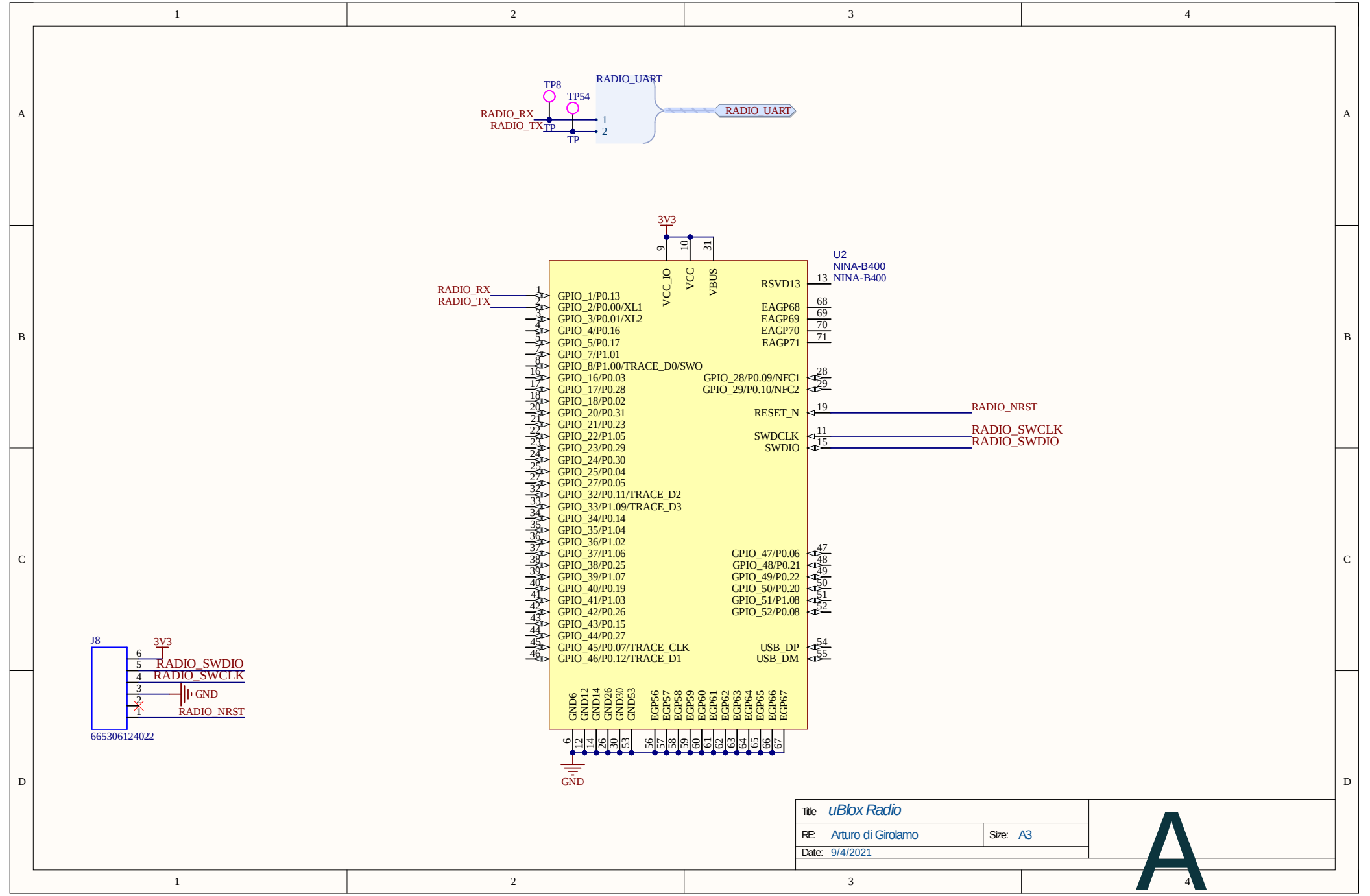
Title	*AD630 Mixer*	
RE:	Arturo di Girolamo	Size: A3
Date:	9/4/2021	

A

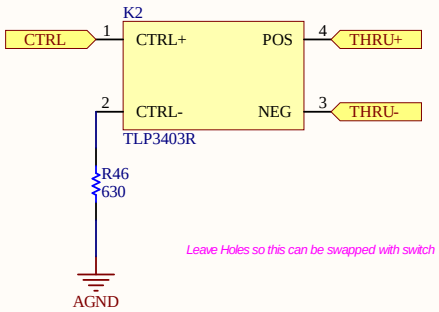


Title	*Power Input PCB*	
RE:	Arturo di Girolamo	Size: A3
Date:	9/4/2021	

A



Title	*uBlox Radio*
RE:	Arturo di Girolamo
Size:	A3
Date:	9/4/2021



Title	Low Current Relay
RE: Arturo di Girolamo	Size: A3
Date: 9/4/2021	

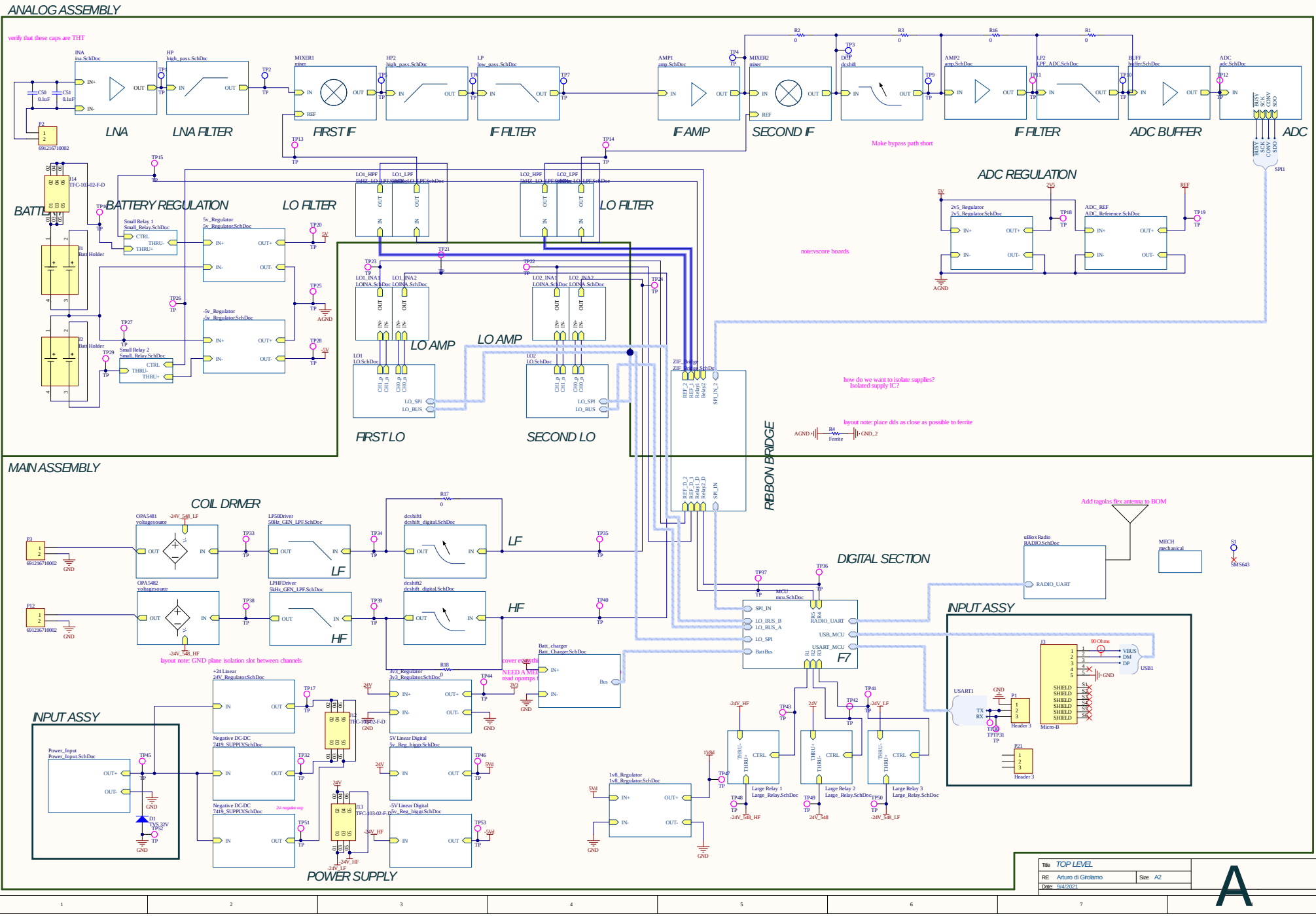
A

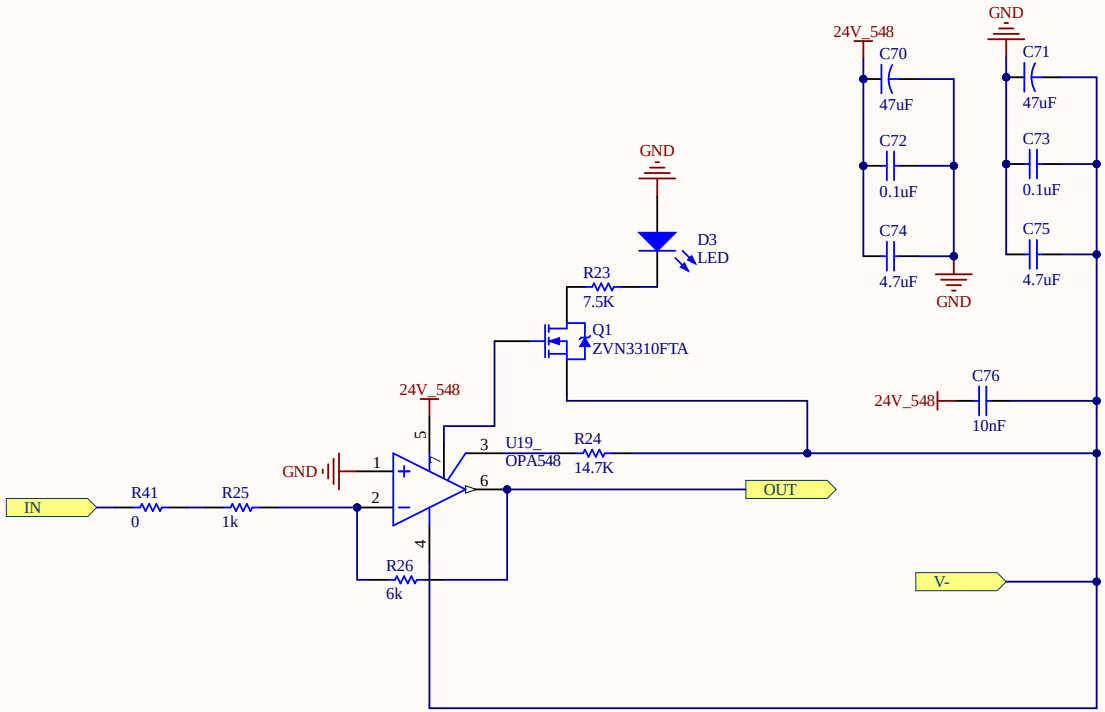
MPS SYSTEM COMPLETE ASSY

DRAWN A. DI GIROLAMO

MINNEAPOLIS, MN

Title: *TITLE SHEET*		
RE: Arturo di Girolamo	Size: A3	A
Date: 9/4/2021		


ANALOG ASSEMBLY
verify that these caps are THT
LNA
LNA FILTER
FIRST IF
IF FILTER
IF AMP
SECOND IF
IF FILTER
ADC BUFFER
ADC
Make bypass path short
BATTERY REGULATION
LO FILTER
LO FILTER
ADC REGULATION
note:vscore boards
LO AMP
LO AMP
FIRST LO
SECOND LO
how do we want to isolate supplies? Isolated supply IC?
layout note: place dds as close as possible to ferrite
RIBBON BRIDGE
MAIN ASSEMBLY
COIL DRIVER
LF
HF
layout note: GND plane isolation slot between channels
DIGITAL SECTION
Add tagalas flex antenna to BOM
INPUT ASSY
INPUT ASSY
POWER SUPPLY
Large Relay 1 Large_Relay.SchDoc
Large Relay 2 Large_Relay.SchDoc
Large Relay 3 Large_Relay.SchDoc
Title TOP LEVEL
RE Arturo di Girolamo
Size A2
Date 9/4/2021
A

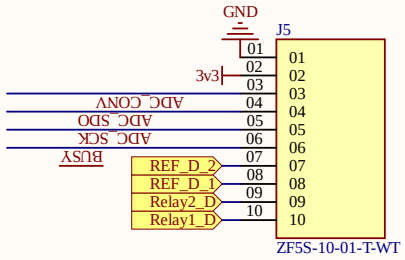


Title	*548 Voltage source*		
RE:	Arturo di Girolamo	Size:	A3
Date:	9/4/2021		

A

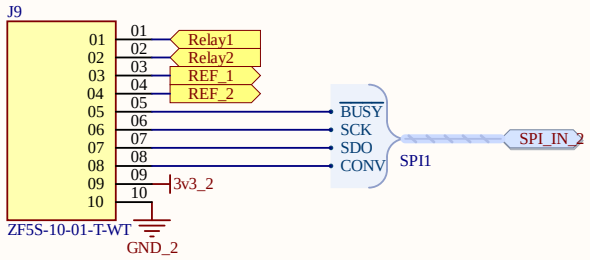
MAIN PCB

swap this for right angle



ANALOG PCB

double check pin alignment with flex cable after layout
or just rotate right angle pi rads



Title	Ribbon Bridge	
RE:	Arturo di Girolamo	Size: A3
Date:	9/4/2021	

A