Microprocessor systems

EMISY

A/D and D/A converters basics
Lecture 10

Semester 19L – Summer 2019
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Important remark

This material is intended to be used by the students during the Microprocessor Systems course for educational purposes only. The course is conducted in the Faculty of Electronics, Warsaw University of Technology.

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Warning – further reading recommended

- A/D and D/A converters is a very broad and often complicated topic. This lecture will only give a basic overview and will not cover everything in detail

- It is highly recommended to read more on this topic.

- Suggested literature:
  - P. Horowitz, W. Hill – *The Art of Electronics, 3rd edition*, chapter 13
  - Analog Dialogue 39-06, June 2005
    - Available online: https://www.analog.com/media/en/analog-dialogue/volume-39/number-2/articles/the-right-adc-architecture.pdf
  - Analog Devices Wiki pages: https://wiki.analog.com/university/courses/electronics/text/chapter-20
  - http://www.ti.com/lit/ml/sprp635/sprp635.pdf
  - TI application report SLAA510 – *High-Speed, Analog-to-Digital Converter Basics*
  - TI application report SLAA523A – *High-Speed, Digital to Analog Converter Basics*

  - https://www.maximintegrated.com/en/app-notes/index.mvp/id/1023
  - https://www.maximintegrated.com/en/app-notes/index.mvp/id/634

Digital representation of analog signal and sampling

- Conversion of analog signal to corresponding digital form is called sampling. It is based on reduction of continuous-time signal to a discrete-time representation of it.
- Sampling interval (T) is called the time between samples. Sampling rate, or sampling frequency is the average number of samples gathered in one second time interval.
- Sampling is used by A/D converters
- Samples are generated by D/A converters.
- Very broad literature devoted to sampling and signal processing is available

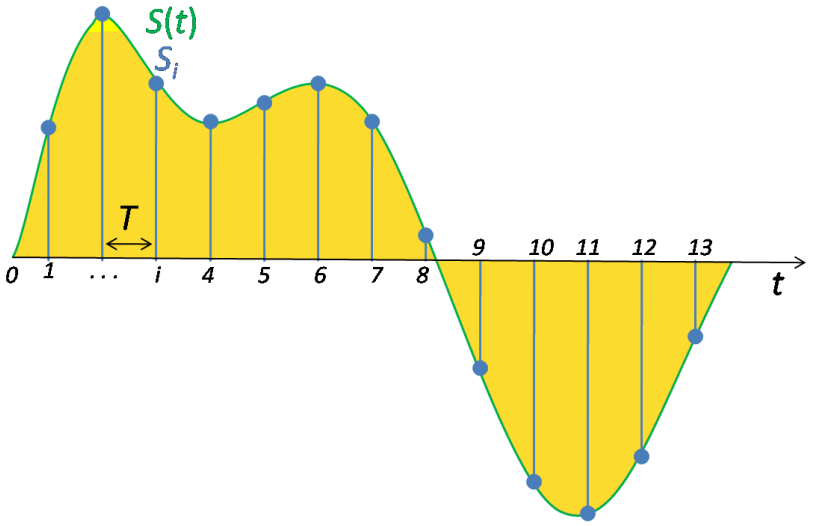


Image source: en.wikipedia.org

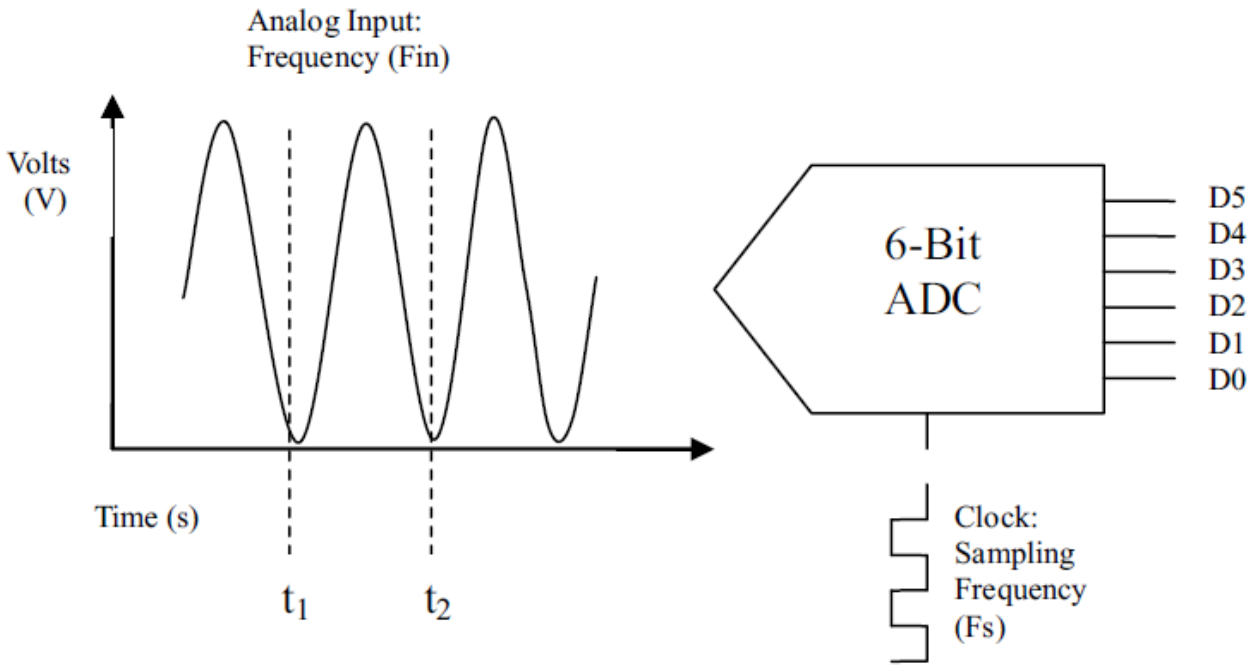
What is ADC?

An analog-to-digital converter (also known as an ADC or A/D converter) is an electronic circuit that measures a real-world signal (such as voltage, temperature, pressure, acceleration) and converts it to a digital representation of the signal.

A/D converter compares the analog input voltage to a known reference voltage and then produces a digital representation of this analog input (a digital code). Every ADC introduces a quantization error, which is simply the information that is lost. This error occurs because there are an infinite numer of voltages for a continuous analog signal, but only a finite number of ADC digital codes. Therefore, the more digital codes the ADC can resolve, the higher resolution it has and the less information ls lost due to quantization error.

Image source: commons.wikimedia.org

What is ADC?



Digital Output

Time	D5	D4	D3	D2	D1	D0
1/Fs	0	1	1	1	1	1
2/Fs	1	0	1	0	1	0
3/Fs	1	1	1	0	0	0
.	.	.	.	.	.	.
.	.	.	.	.	.	.
.	.	.	.	.	.	.
N-2/Fs	0	1	0	1	0	1
N-1/Fs	0	0	0	1	1	1
N/Fs	1	1	0	1	0	1

Fin: Analog Input Frequency = $1/(t_2 - t_1)$
Fs: Clock Frequency
N: number of digital samples captured
n: number of output bits; in this 6-bit ADC example n = 6

Image source: TI application report SLAA510

SAR ADC – Successive Approximation A/D converter

Successive approximation (SAR) ADCs have moderate speed (typically up to a few Msps), low-to-moderate resolution (8-18 bits). Their typical advantages are also low power consumption, serial interface (usually SPI or I2C) resulting in small form factor, and low price. Successive approximation ADCs are often available as multichannel converters, due to ease of mux integration within one CMOS chip.

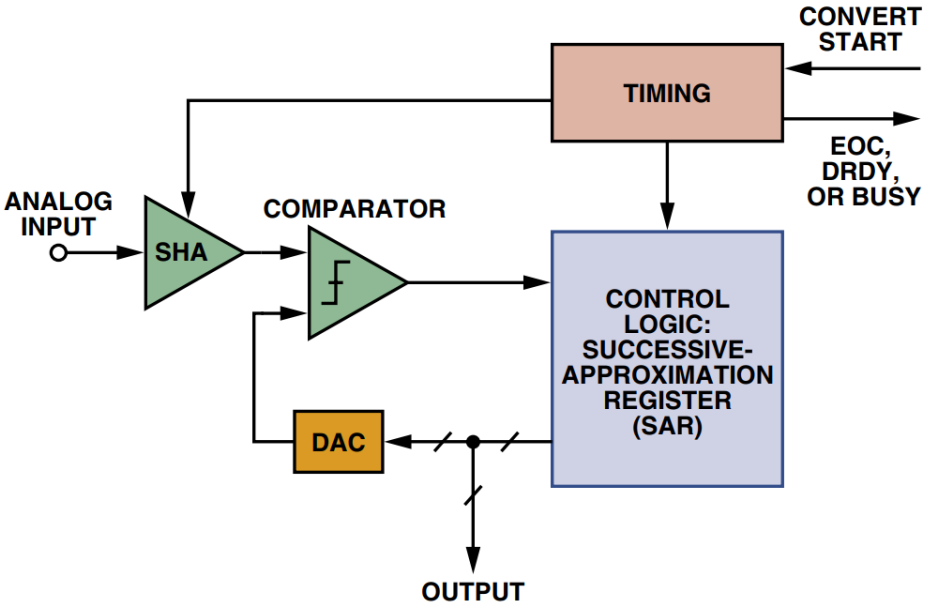


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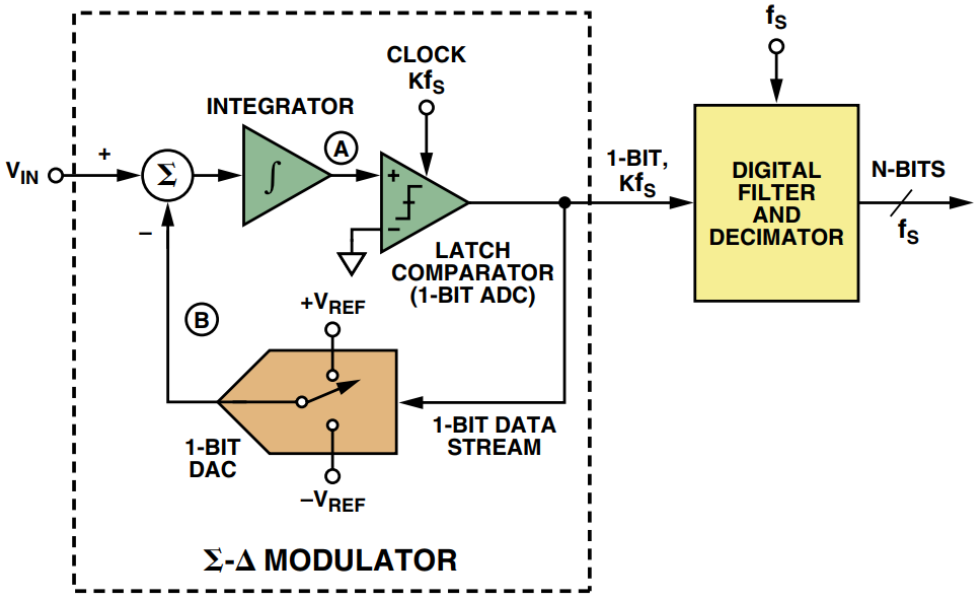
Image source: https://www.analog.com/media/en/analog-dialogue/volume-39/number-2/articles/the-right-adc-architecture.pdf

Sigma Delta ADC

The sigma-delta ADCs offer moderate speed (up to a few MSPS), high resolution (16-32 bits), line rejection, low power consumption, low price, and low noise. The density of 1s at the modulator output is proportional to the input signal. The integrator acts as a lowpass filter to the input signal and a highpass filter to the quantization noise. Thus, most of the quantization noise is pushed into higher frequencies. Oversampling has changed not the total noise power, but its distribution.



Pipeline ADC

The pipelined ADC are the most popular ADCs for sampling with rates from a few Msps up to a few hundreds Msps. Their resolution is in the range of 8-16 bits. Pipelined ADCs have moderate power consumption and moderate price. The pipelined ADC is multistage and accepts a signal before completing the conversation of the previous signal. In this method, one stage processes data received from the previous stage during a clock cycle. At the end of the clock cycle, the output of a given stage is passed to the next stage using T/H (track & hold) and new data is fed to the previous stage.

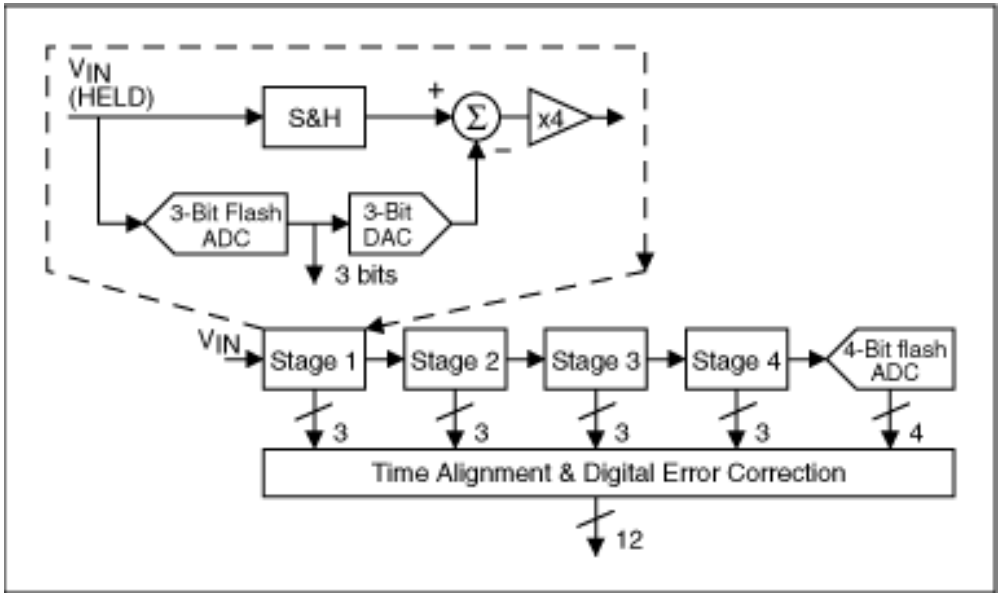


Image source: https://www.maximintegrated.com/en/app-notes/index.mvp/id/1023

Flash ADC

Flash ADCs are fastest (up to a few Gsps), but are limited to low resolutions (6-8 bits). For an N-bit converter, the circuit employs 2N-1 high-speed comparators, which results in high power consumption and high price. Flash ADCs are used only in the most demanding (in terms of speed) applications and are too fast to be served directly by a microprocessor.

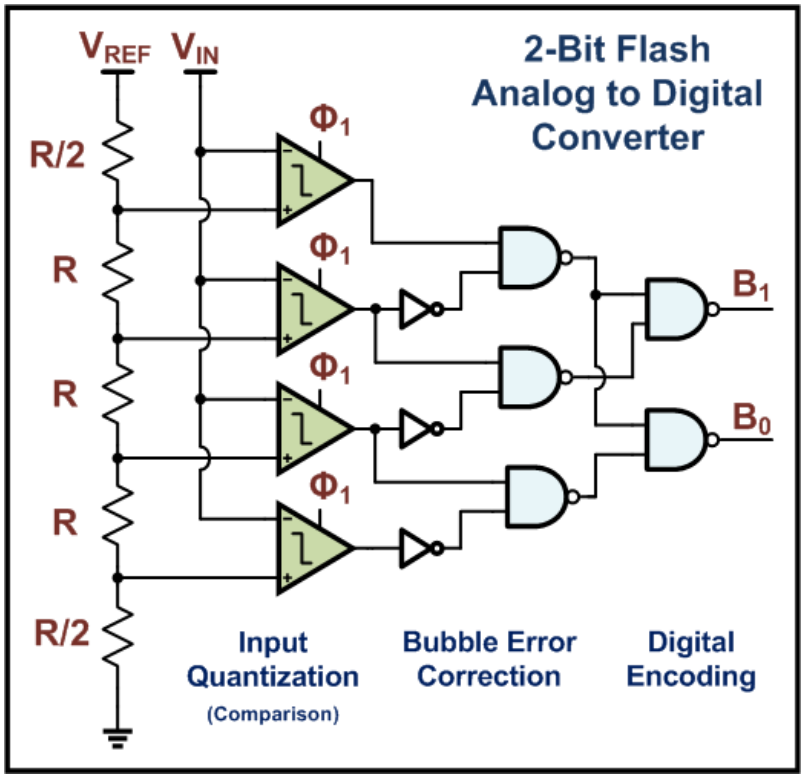


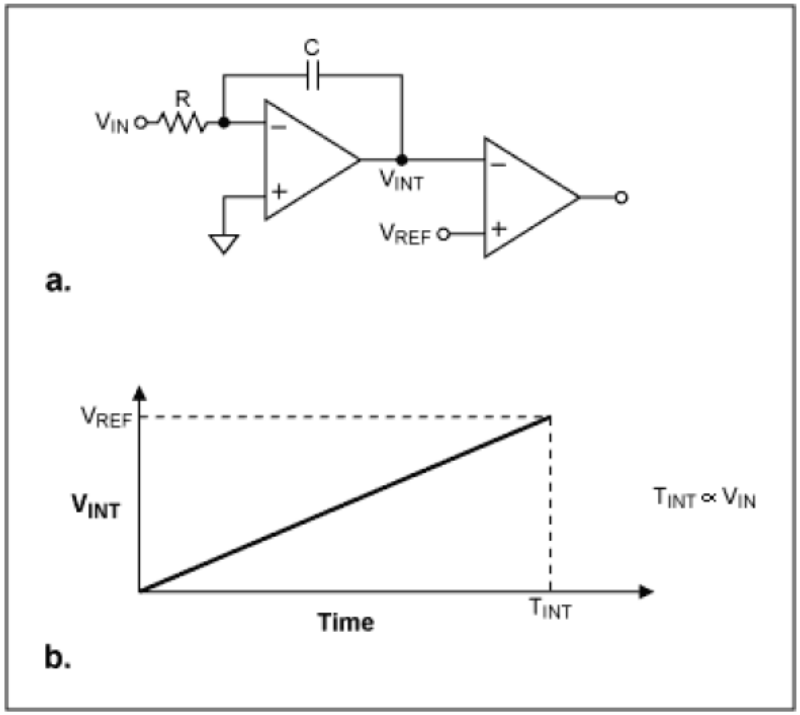
Image source: https://en.wikipedia.org/wiki/Flash_ADC

Integrating ADCs

Integrating ADCs have low speed (typically up to ksps), moderate-to-high resolution (12-28 bits), very good linearity, line rejection, low noise, low power consumption, low-to-moderate price.

Accuracy of a single-slope circuit depends on the tolerances of the R and C values. This makes measurement repeatability relatively low. To overcome this problem dual-slope architecture is used. Multi-slope solutions increase conversion speed.

single slope



dual slope

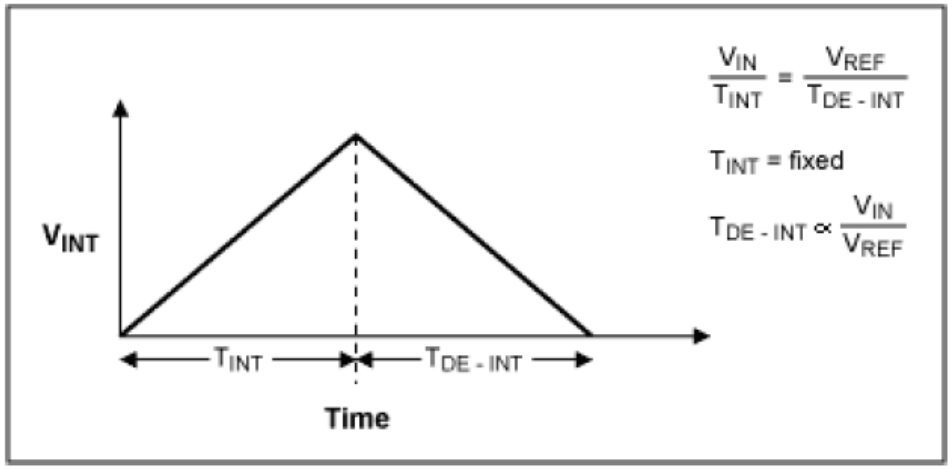


Image source: https://en.wikipedia.org/wiki/Flash_ADC

How to select a proper ADC for application?

- Successive-approximation is the architecture of choice for nearly all multiplexed data acquistition systems and many instrumentation applications.
- For a wide variety of industrial measurement applications, the sigma-delta ADC is ideal. They are suitable for sensor-conditioning, Energy-monitoring and motor-control applications.
- For high sampling rates (several MSPS) the pipeline architecture dominates. These applications typically require up to 14 bits of resolution with high SFDR and SNR

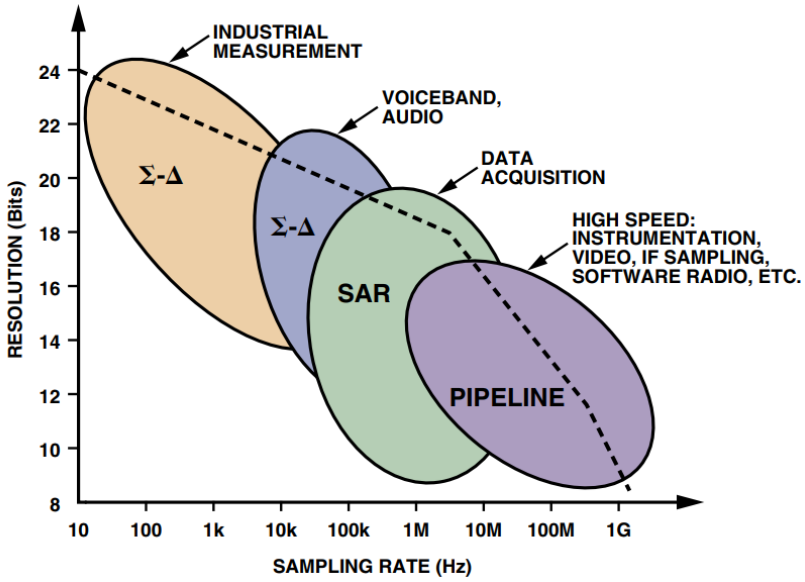


Image source: https://www.analog.com/media/en/analog-dialogue/volume-39/number-2/articles/the-right-adc-architecture.pdf

ADC parameters - aliasing and Nyquist limitations

- The Nyquist-Shannon sampling theorem states that for a true representation of waveform X, more than two samples per period are required. This means that ADC clock signal must be at least 2x higher in frequency then measured signal.
- If this theorem is violated, the aliasing effect appears. The ADC capture output translates the analog input signal at a lower frequency.
- Aliasing is not always the undesirable effect. It can be very useful and the most useful property is mixing a higher frequency signal to a lower frequency signal – there may be no need for an additional mixer in system design.

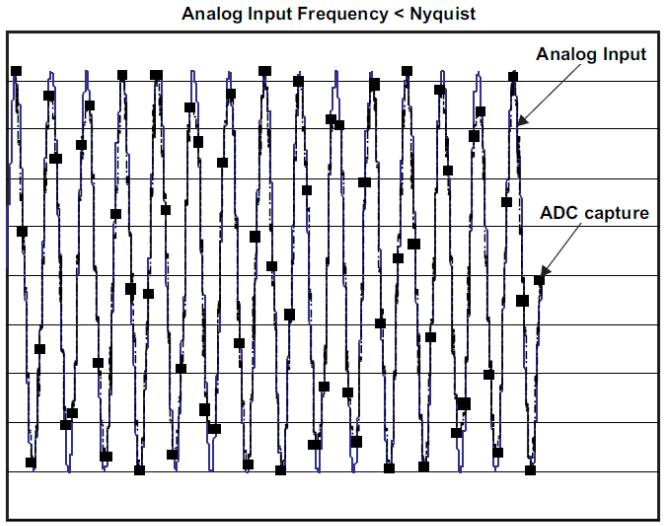


Figure 4. Oversampling Fin < Fs/2

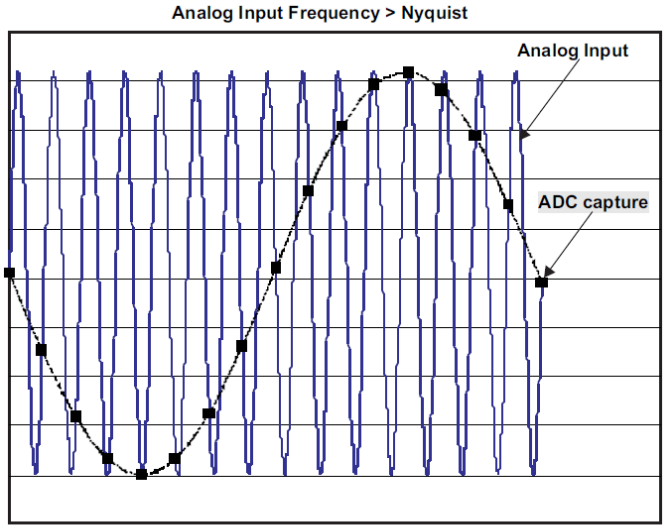
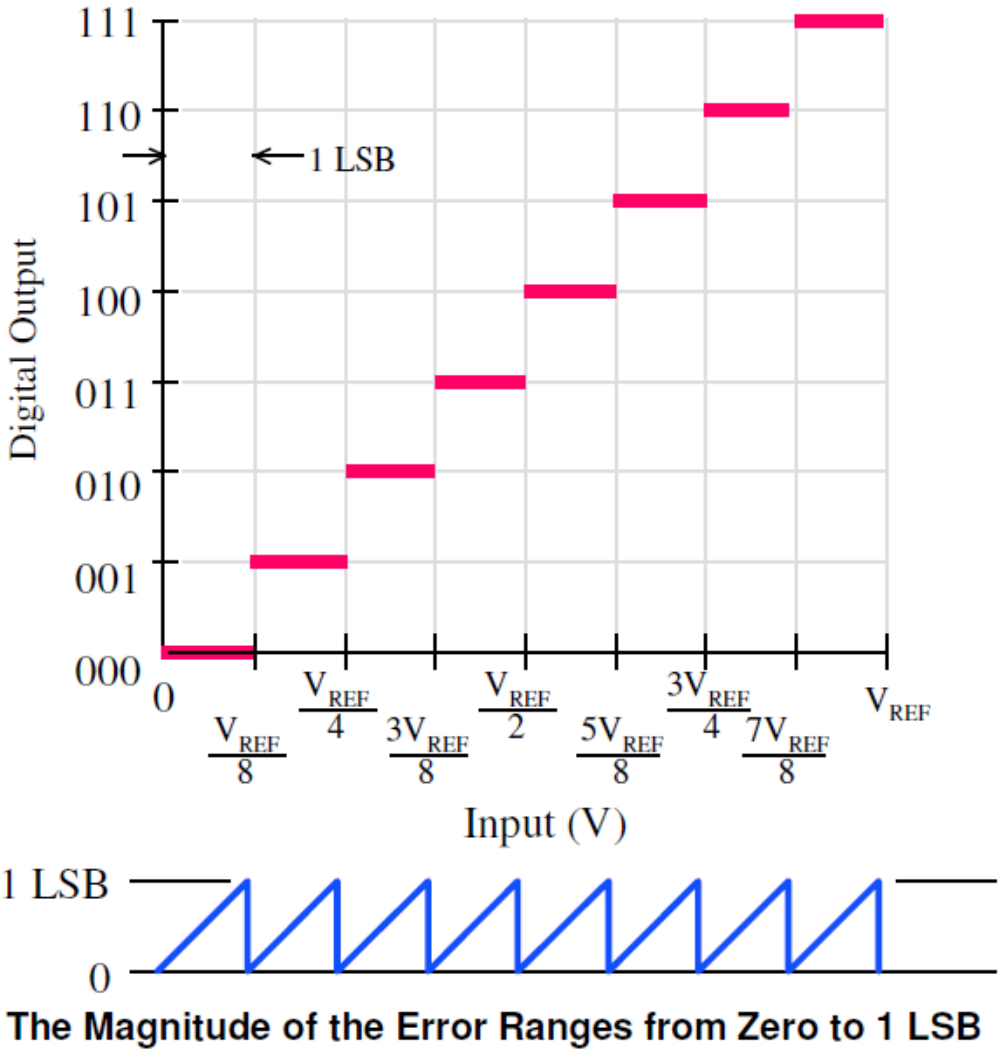


Figure 5. Undersampling Fin > Fs/2

Image source: TI application report SLAA510

Quantization error



The Magnitude of the Error Ranges from Zero to 1 LSB

Image source: National Semiconductor ABCs of ADCs – Analog-to-Digital Converter Basics

Offset error

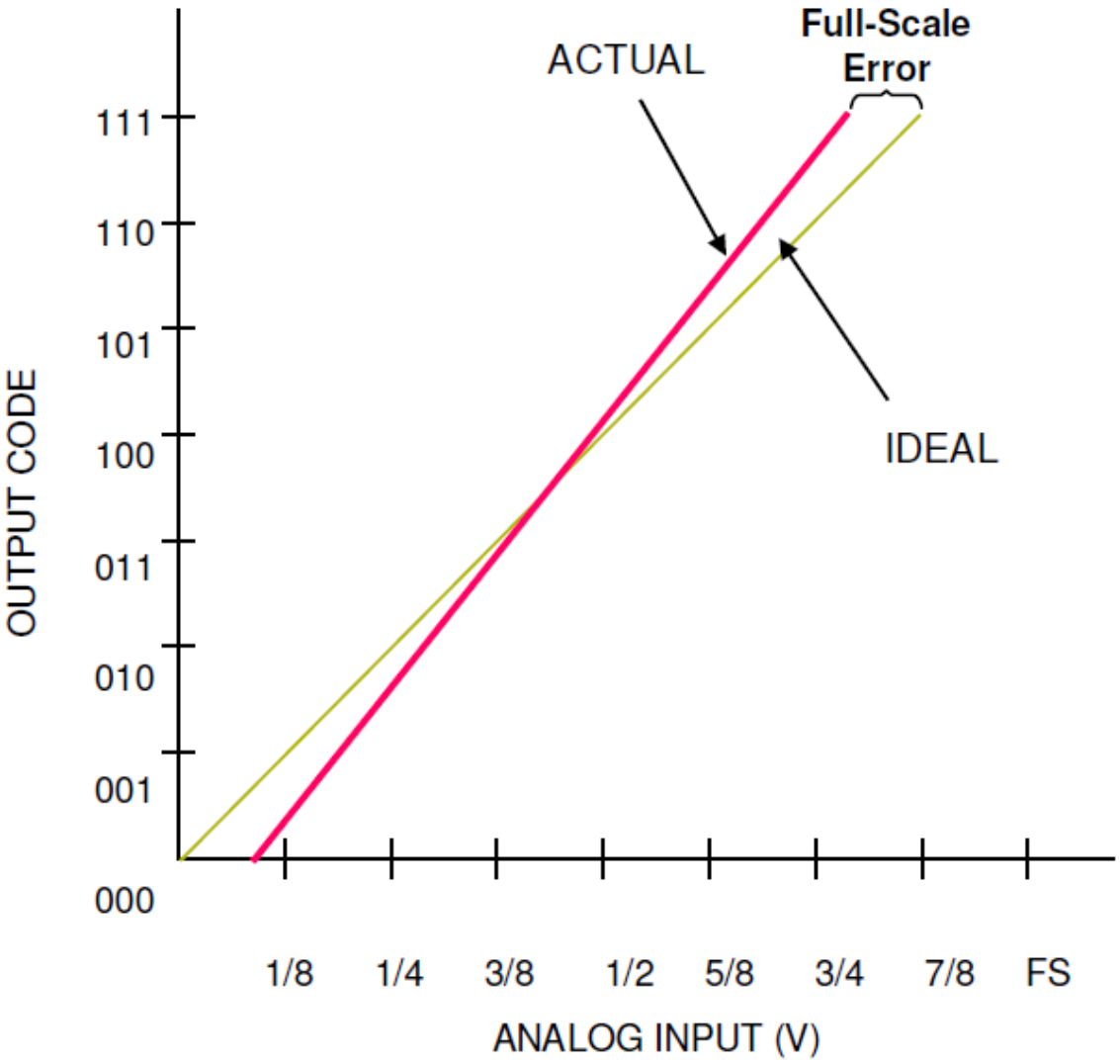


Image source: National Semiconductor ABCs of ADCs – Analog-to-Digital Converter Basics

Gain error

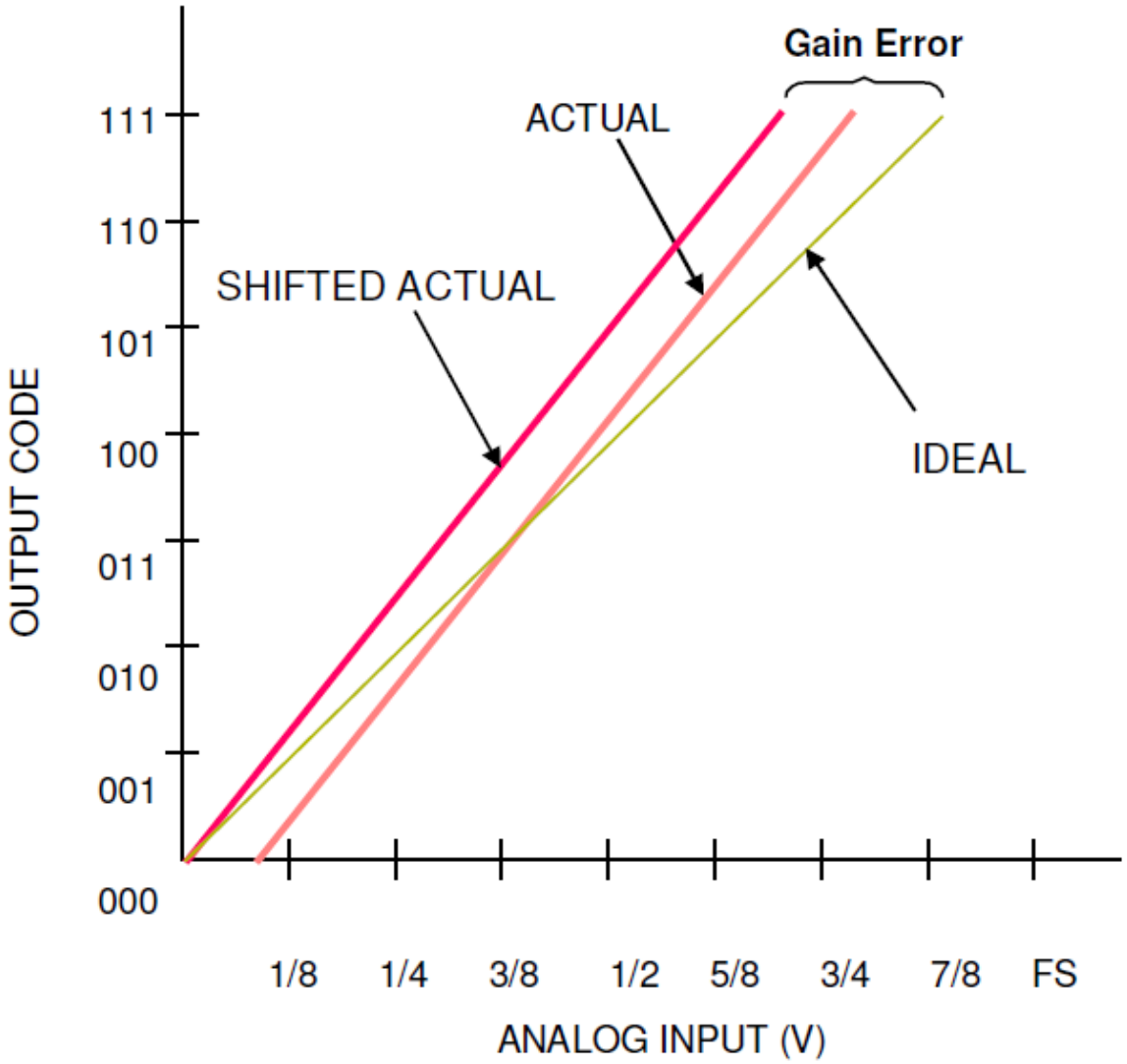
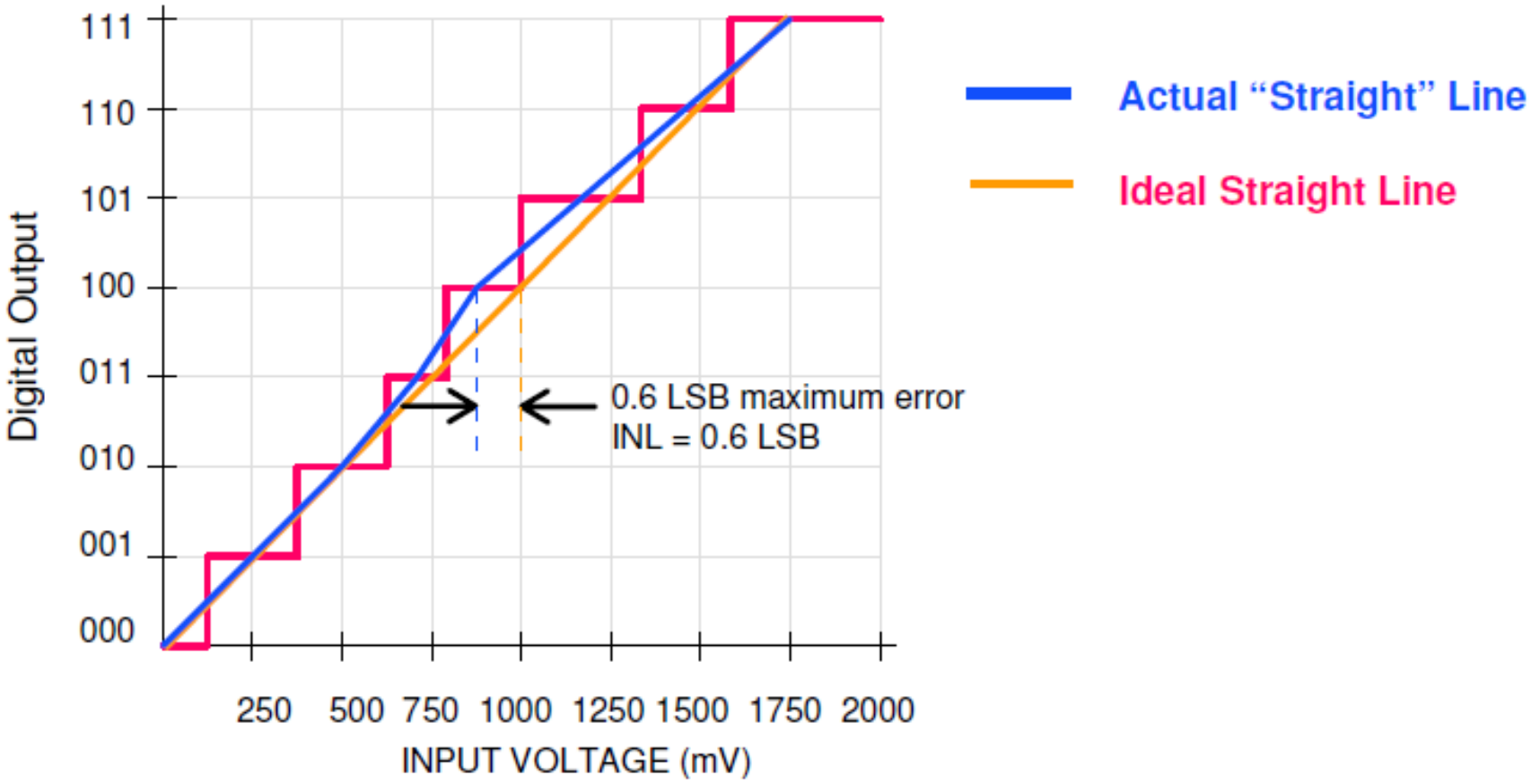


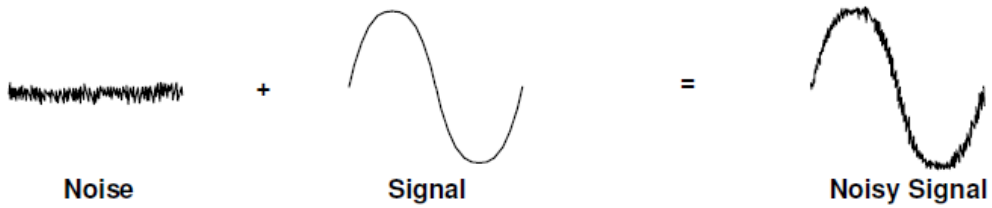
Image source: National Semiconductor ABCs of ADCs – Analog-to-Digital Converter Basics

Integral nonlinearity error – INL



Signal to noise ration - SNR

SNR is the ratio of the fundamental (PS) to the noise floor (PN), excluding the power at DC and in the first five harmonics. The first five harmonics are labeled 2 to 6 in Figure 3. The fundamental is technically the first harmonic, but is rarely called a harmonic. Some data sheets may exclude the first nine harmonics. Other names for the fundamental tone are signal or carrier. SNR is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full scale) when the power of the fundamental is extrapolated to the converter full-scale range.



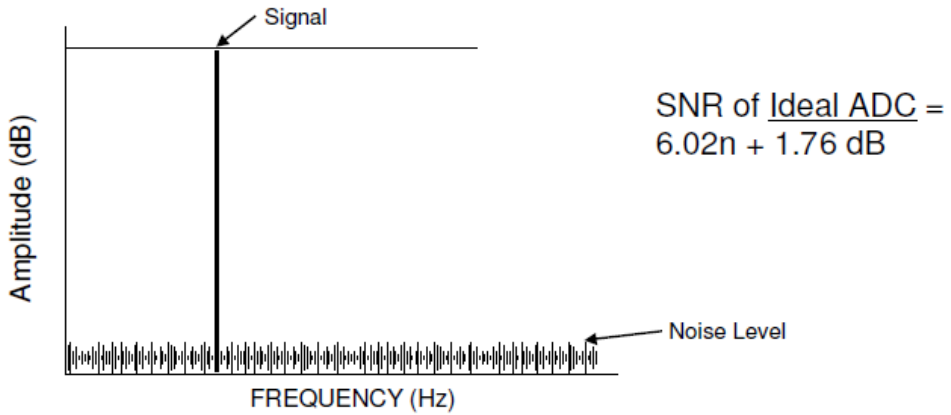
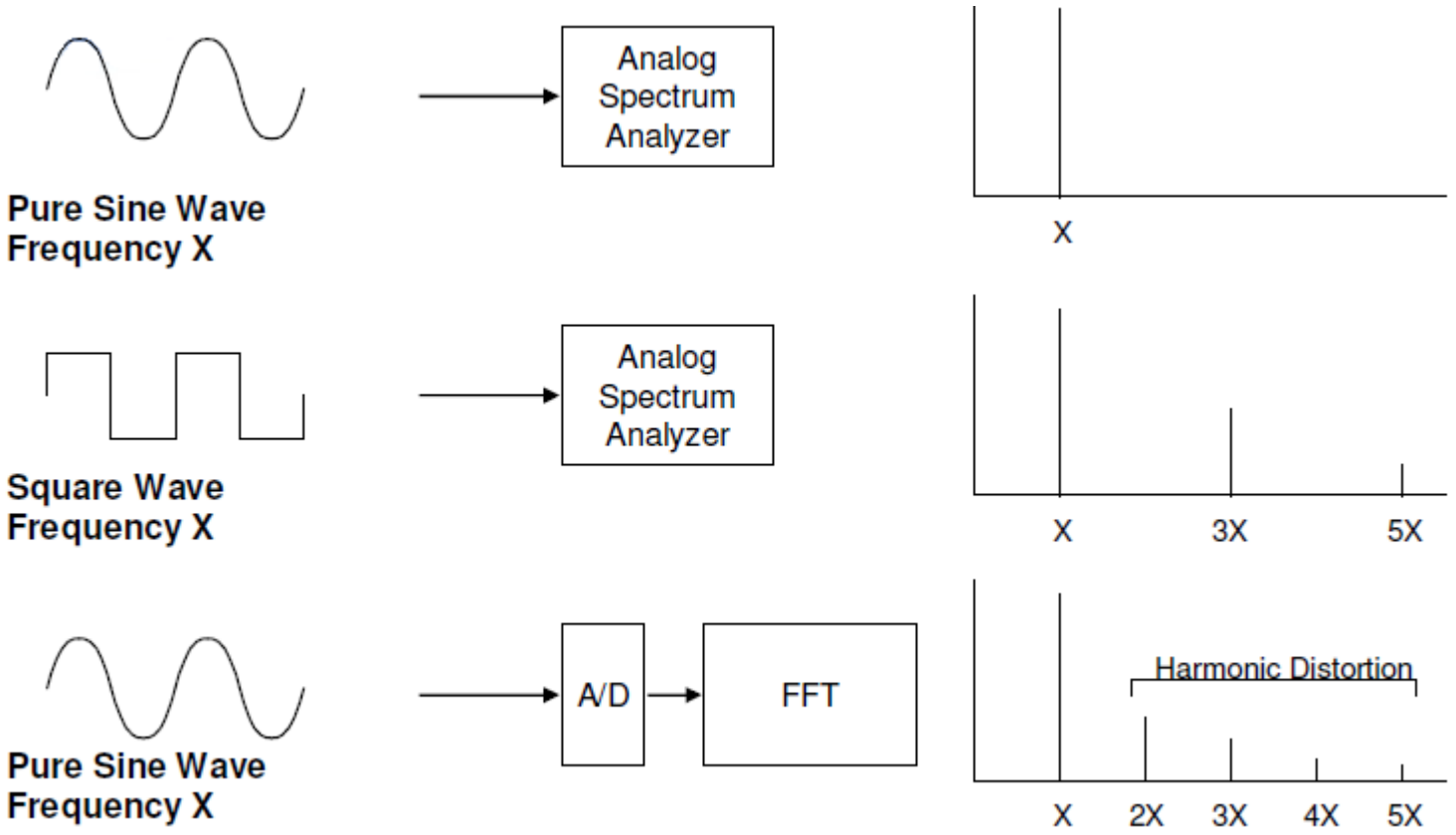


Image source: TI application report SLAA510

Total harmonic distortion - THD

THD is the ratio of the power of the fundamental (PS) to the power of the first five harmonics (PD). THD is typically given in units of dBc (dB to carrier).



Signal to noise and distortion - SINAD

SINAD is the ratio of the power of the fundamental (PS) to the power of all the other spectral components including (PN) and distortion (PD), but excluding dc. SINAD is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full scale)

$$SINAD = -20 * Log \sqrt{10^{\frac{-SNR}{10}} + 10^{\frac{THD}{10}}}$$

$$SINAD = 10 * Log \left[\frac{1}{10^{\frac{-SNR}{10}} + 10^{\frac{THD}{10}}} \right]$$

Image source: National Semiconductor ABCs of ADCs – Analog-to-Digital Converter Basics

Equivallent number of bits - ENOB

ENOB is a measure in units of bits of converter performance as compared to the theoretical ideal SNR limit based on quantization noise.

- **ENOB says that the ADC is equivalent to this (ENOB) number of bits as far as SINAD is concerned. That is, a converter with an ENOB of 7.0 has the same SINAD as a theoretically perfect 7-bit converter.**

$$\text{ENOB} = \frac{\text{SINAD} - 1.76}{6.02}$$

Image source: National Semiconductor ABCs of ADCs – Analog-to-Digital Converter Basics

Spurious free dynamic range - SFDR

FDR is the ratio of the power of the fundamental (PS) to the next highest spur (PH).

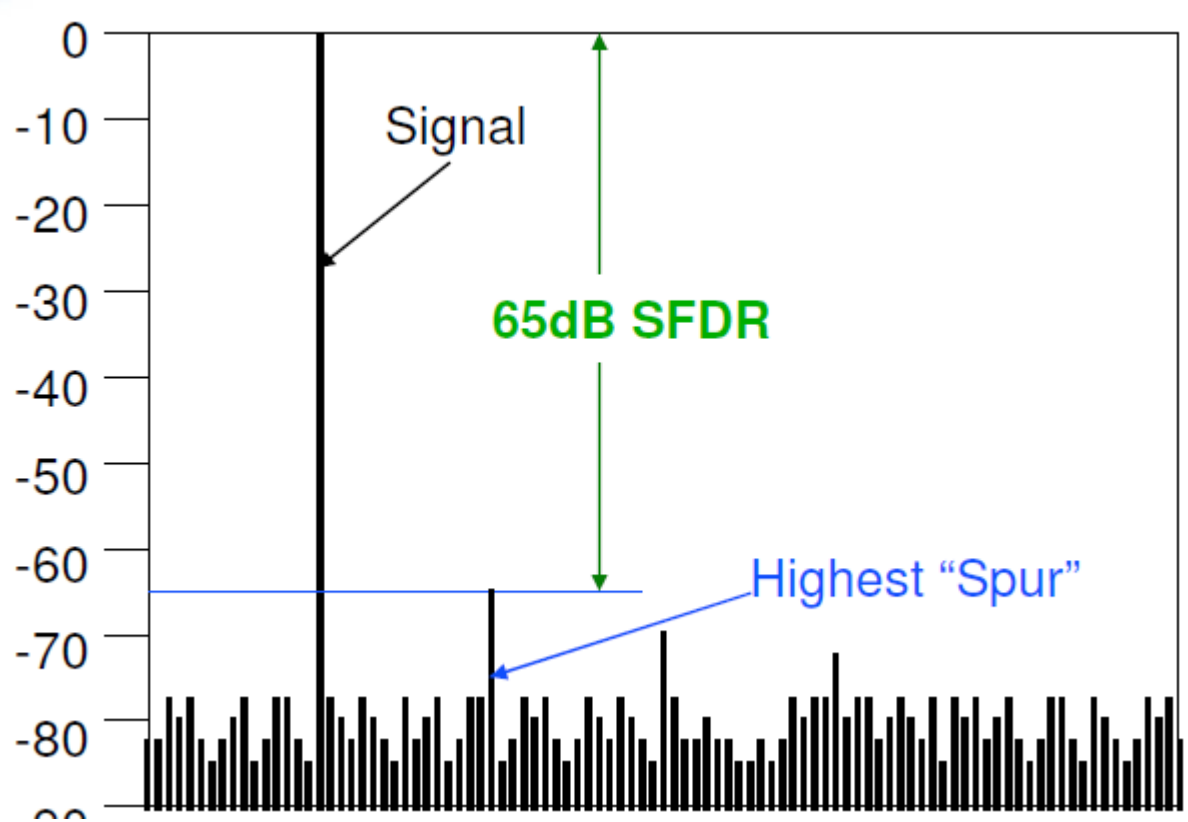


Image source: National Semiconductor ABCs of ADCs – Analog-to-Digital Converter Basics

Input dynamic range

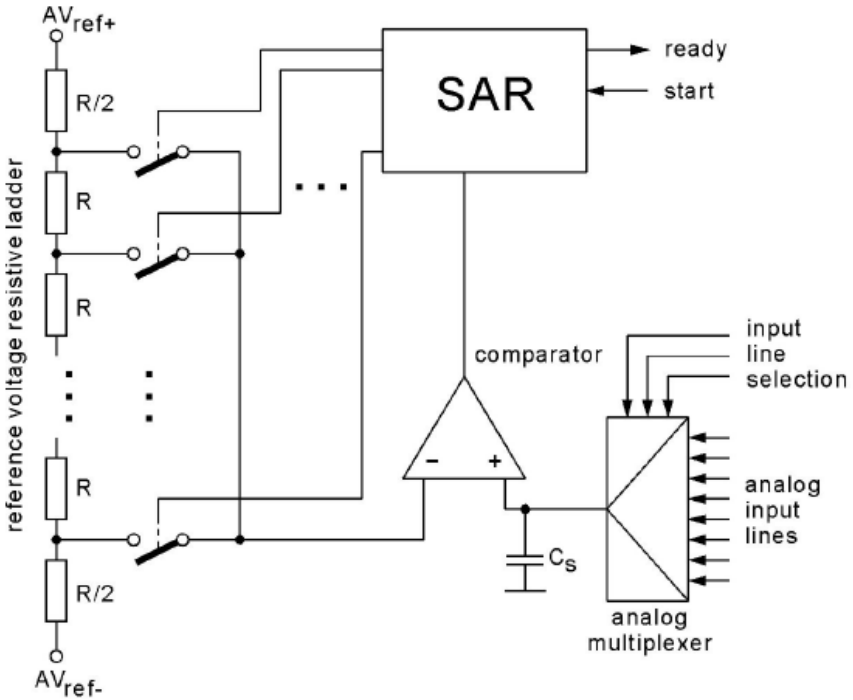
Dynamic Range is the ratio of the largest to the smallest possible signals that can be resolved. DO NOT confuse with Spurious Free Dynamic Range (SFDR).

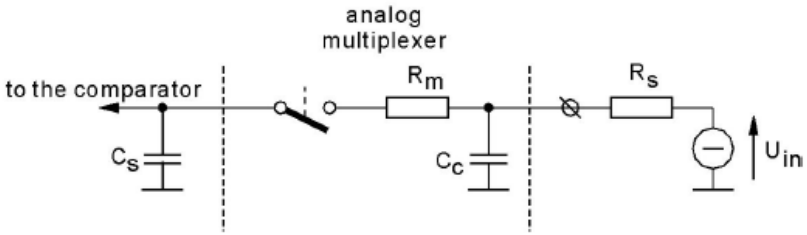
Resolution (Bits)	Dynamic Range (dB)
6	36.0
8	48.1
10	60.2
12	72.2
14	84.3
16	96.3
18	108.4
20	120.4

$$\text{Dynamic Range} = 20 * \text{Log}(2^n - 1)$$

Image source: National Semiconductor ABCs of ADCs – Analog-to-Digital Converter Basics

Internal ADCs in modern microcontrollers





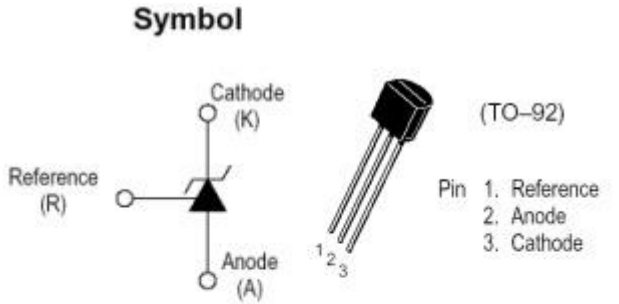
- successive approximation:
  kbps to Msps @ 8-16 bits
- sigma-delta:
  usually much slower (100-1000 times)
  but with higher resolution (16-24 bits)
- usually multiple (multiplexed) analog inputs

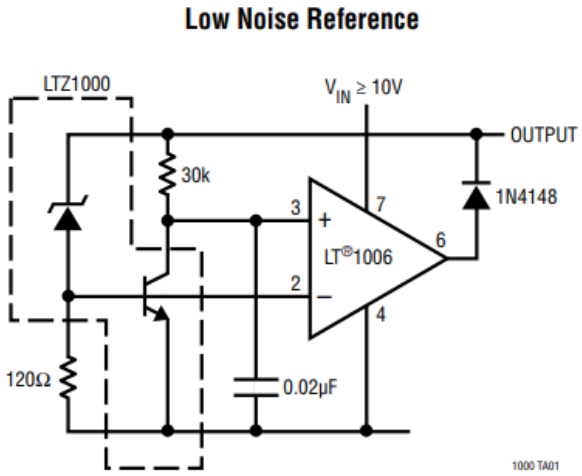
- usually higher errors in comparison to standalone ADCs
- usually unipolar input voltages only
- input impedance, slew rate, etc. may introduce strong limits or problems

- usually $(ADμC) < $(μC) + $(AD)
  similar relationship refers to size
- internal ADC increases reliability and simplifies firmware and debugging

Supporting circuits - Reference voltage source

- A voltage reference source is an electronic circuit that provides a fixed, precisely defined and stable in time (as much as possible) DC voltage that is used as a reference by A/D and D/A converters.
- The most important parameters of a good voltage reference are:
  - Initial accuracy – the difference between uncompensated value of measured output voltage of reference source and the same value stated in the datasheet
  - Temperature coefficient – the deviation of reference output voltage due to a change in the ambient or package temperature
  - Line regulation, load regulation – a measure of change of the output voltage caused by either a change of input voltage (line reg.) or change of load current (load reg.)
  - Long-term drift (stability) – a measure of change of output voltage value over time (days)
- Additional literature:
  http://www.ti.com/lit/ml/slyc147/slyc147.pdf
  https://www.maximintegrated.com/en/app-notes/index.mvp/id/719



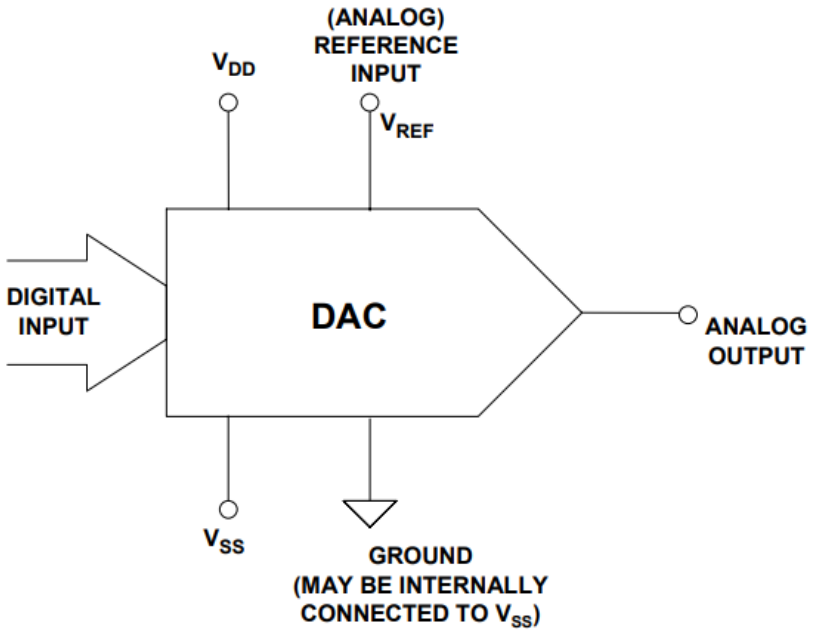


DAC

A digital-to-analog converter (also known as a DAC or a D/A converter) is an electronic circuit that converts a digital code (usually a binary code) into a corresponding discrete analog value (a voltage or current at the DAC's output). The word "discrete" is very important to understand, because a DAC cannot provide a continuous-voltage output signal. Rather, it provides analog steps. By increasing the resolution of the DAC, the number of discrete steps is increased and the step size is reduced (which reduces the quantization error). The steps can be lowpass filtered to obtain a signal that closer approximates a
continuous-time signal.

Basic DAC selection criteria

- Resolution
- INL and DNL, gain and offset errors
- output signal (current or voltage)
- bipolar or unipolar output
- output voltage/current range
- internal or external reference voltage
- bandwidth of the reference signal in the DAC is multiplying
- maximum output current
- speed
- number of channels
- microprocessor interface
- power consumption



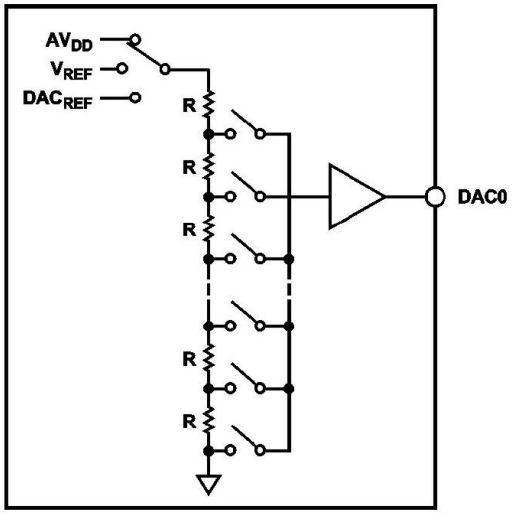


Image source: https://www.analog.com/media/en/training-seminars/design-handbooks/Data-Conversion-Handbook/Chapter3.pdf

DAC parameters and limitations

- SNR – the ratio of the RMS value of the fundamental (PS) output signal to the RMS sum of all other spectral components below the Nyquist frequency, including noise (PN), but excluding the first six harmonics and dc.
- SFDR - the ratio of the power of the fundamental (PS) to the next highest spur (PH).
- IMD3 – Inter Modulation Distortion – important in narrow or wide band signals – it tells what is the influence of DAC signal on other bandwidth channels, due to 3rd order product generation
- Dynamic range – output voltage range, usually from 0 to Vref
- Resolution – indicates the smalles increment of DAC output voltage
- Offset error, gain error, DNL, INL, – like in ADCs...
- Max conversion rate – the maximum input signal frequency that can be handled by the DAC

ADC and DAC application examples

Putting it all together

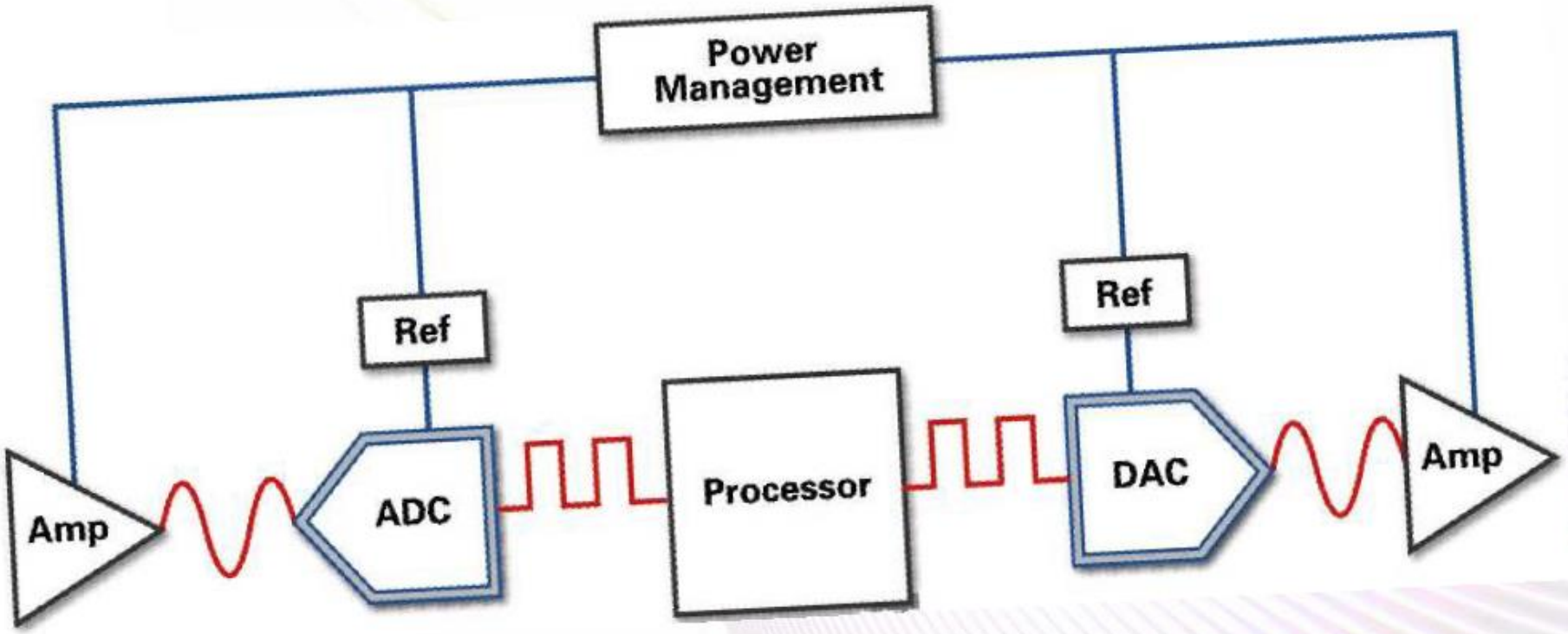


Image source: TI presentation – Data Converter Basics, how to use and test data-acquisition products, March 2007