Power consumption in microprocessor systems. Power saving issues Lecture 11

Semester 20L – Summer 2020

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Why should we reduce power consumption in microprocessor systems?

- Not every application runs with power supply coming from mains.
- Many modern applications require to be small, lightweight and efficient – power management is critical
  - Few microamperes of current savings may lead to few more **months** of battery time.
- Reducing power consumption in designed systems helps in:
  - System robustness
  - Operation time
  - Improving efficiency
  - Reduction of heat dissipated by the device
- Modern microcontrollers allow for special power saving modes
- Many external peripherals are designed to be energy-efficient – usually they have some power down or idle states or wake pins, etc.

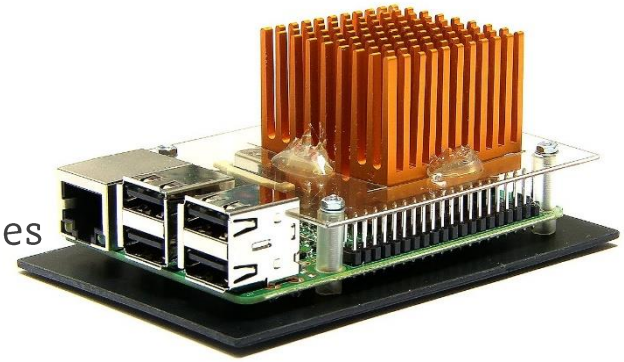


Image source: www.overclock.net

How to save power in microprocessor systems?

- There are few solutions to this problem:
  - Using special power down and sleep modes of the microcontrollers
  - Design of high efficiency clock distribution systems
    - Reducing master clock frequency (effect of frequency scaling)
    - Dynamic frequency scaling
      - Some microcontrollers (like STM32, AVR) allow for dynamic frequency scaling – clock frequency adjustment is possible via firmware
      - It is not obligatory to stay with only one clock frequency
    - $P = C \cdot V^2 \cdot f$ P – power consumption, C – capacitance switched per clock cycle
      f – clock frequency
  - Using interrupts, whenever possible
  - Using power down and sleep modes in external peripherals, whenever possible

Power down modes in 8051 family

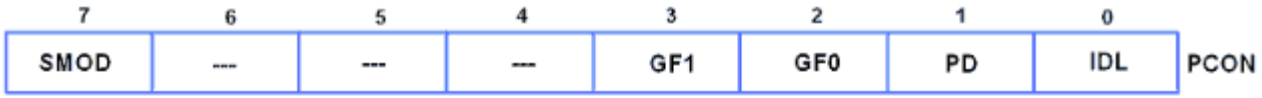
- 8051 microcontrollers have internal power saving features that should be used in applications where power consumption is a main constraint.
- 8051 has two power saving modes:
  - Power Down Mode
  - Idle Mode
- In Power Down mode the oscillator is off and thus the microcontroller is inactive, along with all internal peripherals
- In Idle mode only CPU is turned off (clock deactivated only for the CPU), peripherals remain active.
- This means that Idle state consumes more power than Power Down state

8051 model	f_{CLK}	Current in normal mode	Current in Idle mode	Current in Power down mode
AT89S51	12 MHz	25 mA	6.5 mA	50 uA
P89V51RD2	12 MHz	11.5 mA	8.5 mA	80-90 uA
DS80C323	18 MHz	10 mA	6 mA	0.1 uA

Source: https://www.electronicwings.com/8051/8051-power-down-and-idle-mode

Power down modes in 8051 family - configuration

- 8051 microcontrollers have special register PCON – Power Control register. It is used to force the 8051 microcontroller into power saving mode. Power control register contains serial port baud rate control bit and two power saving mode bits



Bit 7 – SMOD

1 = Baud rate is doubled in UART mode 1, 2 and 3.

0 = No effect on Baud rate.

Bit 3:2 – GF1 & GF0:

These are general purpose bit for user.

Bit 1 – PD: Power Down

1 = Enable Power Down mode. In this mode, Oscillator clock turned OFF and both CPU and peripherals clock stopped. Hardware reset can cancel this mode.

0 = Disable Power down mode.

Bit 0 – IDL: Idle

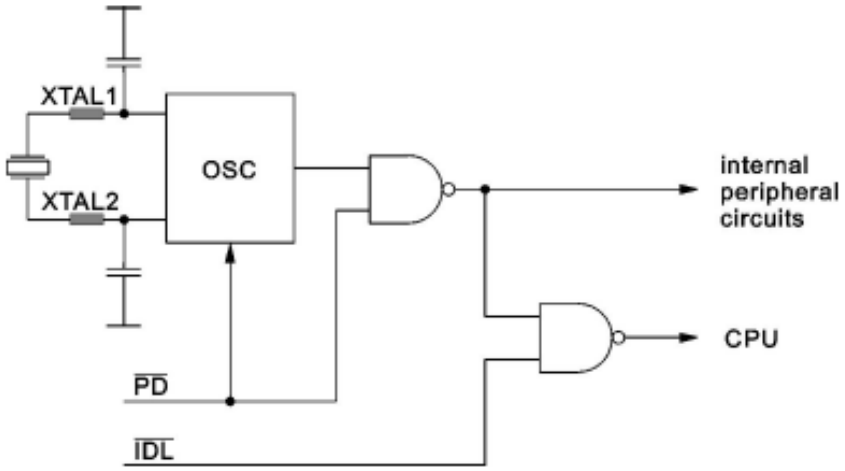
1 = Enable Idle mode. CPU clock turned off whereas internal peripheral module such as timer, serial port, interrupts works normally. Interrupt and H/W reset can cancel this mode.

0 = Disable Idle mode.

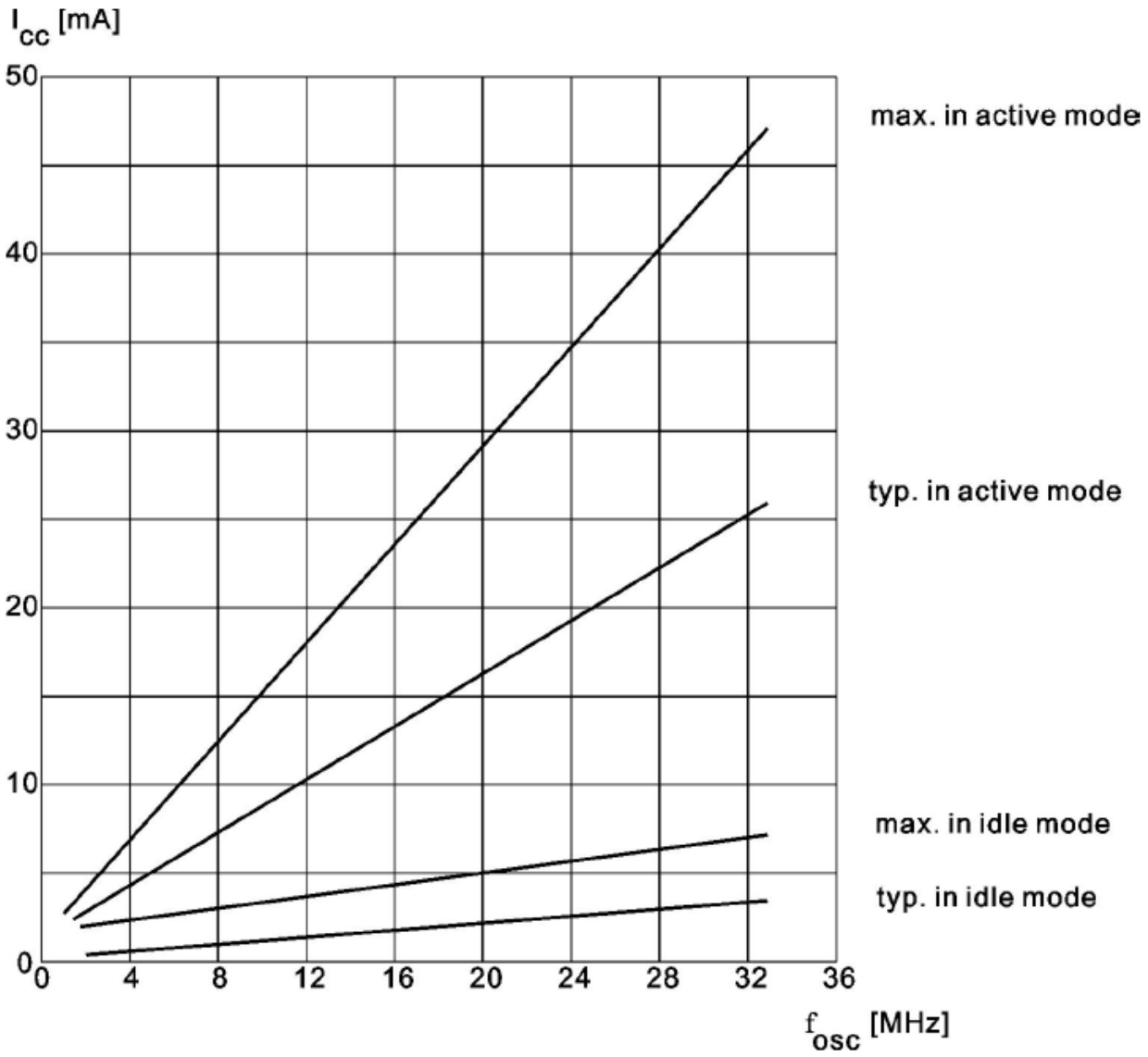
Source: https://www.electronicwings.com/8051/8051-power-down-and-idle-mode

Idle mode in 8051

- Idle is entered by setting appropriate control bit located in SFR area
- when Idle is entered the CPU is stopped
- peripheral circuits and interrupt system still work
- contents of the SFRs and internal memory is preserved
- I/O pins are held in the previous state, unless changed by working peripherals or forced externally
- in order to further reduce power consumption all the peripherals which are not needed should be switched off
- Idle mode can be terminated by an interrupt (external or internal) or reset
- during Idle mode power consumption is a few times lower than during normal active mode

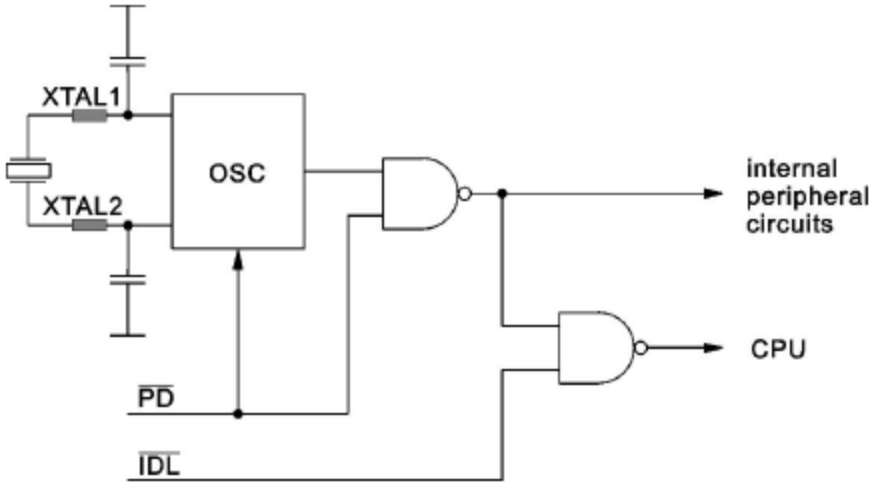


Power consumption vs. System clock frequency in active and idle modes of 8051

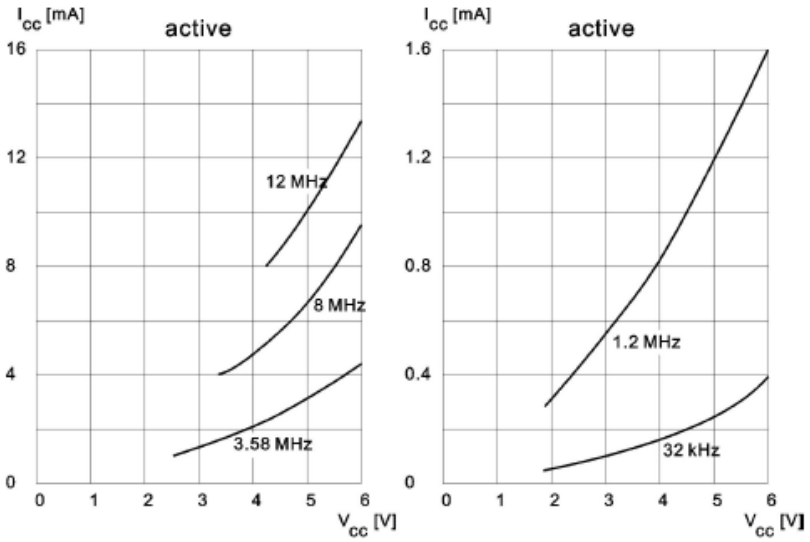


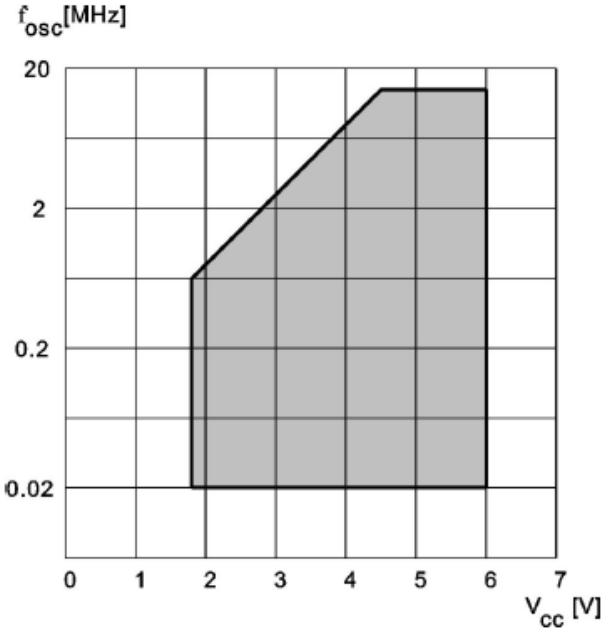
Power down mode in 8051

- Power Down is entered by setting appropriate control bit located in SFR area
- when Power Down is entered the clock is stopped
- as a result peripheral circuits don't work
- contents of the SFRs and internal memory is preserved
- I/O pins are held in the previous state, unless forced externally
- Power Down mode can be terminated by a hardware reset or (only in some cases) by an external interrupt (level-activated)
- during Power Down mode power consumption is reduced to the level of single microamperes and can be further reduced by lowering Vcc



Power consumption vs. Supply voltage of 8051





Slow down modes in 8051

- Slow Down is entered (quit) by setting (clearing) appropriate control bit located in SFR area
- when Slow Down is entered, frequency of the clock is substantially lowered
- changing of the clock frequency may be obtained by means of a clock prescaler (divider), selection of another clock source (eg. internal RC oscillator) or both
- as a result CPU and internal peripheral circuits work much slower, which may result in some side effects (eg. change of the serial port baudrate, frequency of the timer's overflow, etc.)
- Slow Down can be used independently from Idle or simultaneously with Idle mode

Slow down modes in 8051 – EFM8

Power Mode	Details	Mode Entry	Wake-Up Sources
Normal	Core and all peripherals clocked and fully operational	—	—
Idle	• Core halted • All peripherals clocked and fully operational • Code resumes execution on wake event	Set IDLE bit in PCON0	Any interrupt
Suspend	• Core and digital peripherals halted • Internal oscillators disabled • Code resumes execution on wake event	1. Switch SYSCLK to HFOSC0 or LPOSC0 2. Set SUSPEND bit in PMU0CF	• RTC0 Alarm Event • RTC0 Fail Event • Port Match Event • Comparator 0 Rising Edge
Stop	• All internal power nets shut down • Pins retain state • Exit on any reset source	Set STOP bit in PCON0	Any reset source
Sleep	• Most internal power nets shut down • Select circuits remain powered • Pins retain state • All RAM and SFRs retain state • Code resumes execution on wake event	1. Disable unused analog peripherals 2. Set SLEEP bit in PMU0CF	• RTC0 Alarm Event • RTC0 Fail Event • Port Match Event • Comparator 0 Rising Edge

Power down modes in AVR

- AVR microcontrollers include several sleep modes that enable the application to shut down unused modules in the MCU, thereby saving power

- There are five sleep modes in AVRs:
  - Idle Mode
  - Power Down
  - Power Save
  - Standby
  - Extended Standby

- To enter any of the sleep modes, the Sleep Enable bit in the Sleep Mode Control Register (SMCR.SE) must be written to '1'
- SLEEP instruction must be executed

Name: SMCR
Offset: 0x53
Reset: 0x00
Property: When addressing as I/O Register: address offset is 0x33

Bit	7	6	5	4	3	2	1	0
					SM2	SM1	SM0	SE
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit 3 – SM2: Sleep Mode Select 2
The SM[2:0] bits select between the five available sleep modes.

Table 14-2 Sleep Mode Select

SM2,SM1,SM0	Sleep Mode
000	Idle
001	
010	Power-down
011	Power-save
100	Reserved
101	Reserved
110	Standby(1)
111	Extended Standby(1)

Source: https://microchipdeveloper.com/8avr:avrsleep

Power down modes in AVR

- If an enabled interrupt occurs while the MCU is in a sleep mode, the microcontroller wakes up and after 4 cycles (halt) it executes interrupt procedure and then instructions following SLEEP command.
- When SM[2:0] are 000 the SLEEP instruction makes the MCU enter Idle mode – it stops the CPU, but not SPI, USART, analog comparator, timers, watchdog and interrupt system. Idle mode enables the MCU to wake up from external and internal interrupts
- When SM[2:0} are 010 the SLEEP instruction makes the MCU enter Power Down mode – the external Oscillator is stopped, but not 2-wire serial interface and watchdog. MCU can be woken up by external reset, watchdog reset or interrupt, brown-out reset, or external interrupt
- When SM[2:0] are 011 the SLEEP instruction makes the MCU enter Power Save mode – identical to Power Down, but Timer 2 is enabled
- When SM[2:0] are 110 the SLEEP instruction makes the MCU enter Standby mode – identical to Power Down mode, but the external Oscillator is working
- When SM[2:0] are 111 the SLEEP instruction makes the MCU enter extended Standby – identical to Power Save mode, but the Oscillator is running

Source: https://microchipdeveloper.com/8avr:avrsleep

Power down modes in STM32

- By default the microcontroller is in Run mode. STM32 feature three low-power modes:
  - Sleep mode
  - Stop mode
  - Standby mode

Table 1. Low-power mode summary

Mode name	Entry	Wakeup	Effect on 1.2 V domain clocks	Effect on V_{DD} domain clocks	Voltage regulator
Sleep (Sleep now or Sleep-on-exit)	WFI	Any interrupt	CPU CLK OFF no effect on other clocks or analog clock sources	None	ON
	WFE	Wakeup event			
Stop	PDDS and LPDS bits + SLEEPDEEP bit + WFI or WFE	Any EXTI line (configured in the EXTI registers, internal and external lines)	All 1.2 V domain clocks OFF	HSI and HSE oscillators OFF	ON or in low- power mode (depends on *PWR power control register (PWR_CR)*)
Standby	PDDS bit + SLEEPDEEP bit + WFI or WFE	WKUP pin rising edge, RTC alarm (Alarm A or Alarm B), RTC Wakeup event, RTC tamper event, RTC time stamp event, external reset in NRST pin, IWDG reset			OFF

For more information about low power modes, refer to RM0033 section “Low-power modes”.

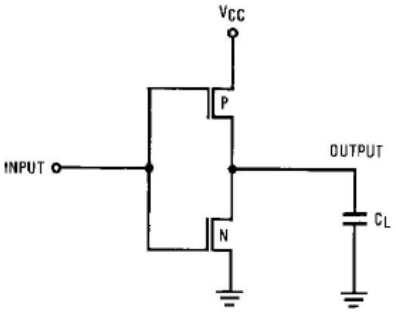
Power down modes - comparison

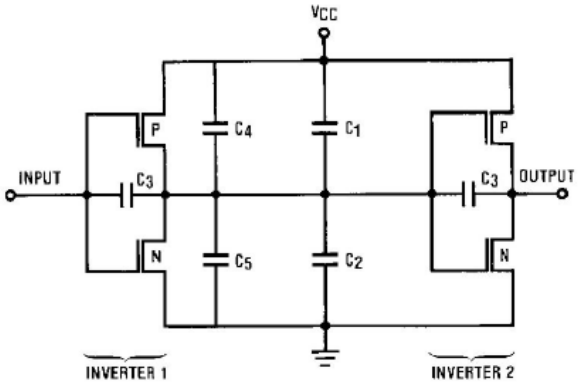
- common sensor node processors: AVR, 8051, StrongARM, XScale, ARM Thumb, SH Risc, MSP430, PIC
- exemplary values of power consumption:
  - 4 nJ/instr — ATMega128L @ 4 MHz, 3.0 V
  - 2 nJ/instr — AVR32 UC3A @ 66 MHz, 3.3 V
  - 2.1 nJ/instr — ARM Thumb @ 40 MHz, 3.0 V
  - 1.0 nJ/instr — Cygnal C8051F35x @ 50 MHz, 3.0 V
  - 0.5 nJ/instr — MSP430x20xx @ 1 MHz, 2.2 V
  - 0.11 nJ/instr — PIC16LF72X @ 4 MHz, 1.8 V
  - 0.8 nJ/instr — TMS320VC5510 @ 200 MHz, 1.5 V
  - 1.3 nJ/instr — IBM 405LP @ 380 MHz, 1.8 V
  - 0.35 nJ/instr — IBM 405LP @ 152 MHz, 1.0 V
  - 1.1 nJ/instr — Xscale PXA250 @ 400 MHz, 1.3 V
  - 1.9 nJ/instr — Xscale PXA250 @ 130 MHz, 0.85 V

Selecting energy-efficient components

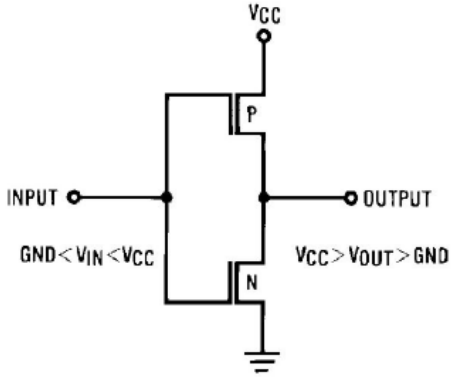
- eg. when looking for an ADC capable of working with the speed of 100 ksps
  - AD 7853 (12-bit; 200 ksps max) - 6.0 mW @ 3.0 V, 100 ksps; 6.5 - 12$
  - AD 7694 (16-bit; 250 ksps max) - 1.7 mW @ 3.0 V, 100 ksps; 6.1 - 7.6$
- modern solutions and higher level of integration usually result in lower power consumption
- display:
  - alphanumeric LCD: 0.5 - 1.0 mA (but the backlight can draw 30 mA!)
  - single LED: 1.0 - 2.0 mA
- all the peripherals which are not needed at the moment can be powered down or switched off (but care should be taken about the inputs of such components)
- resistor values should be increased if possible
- etc.

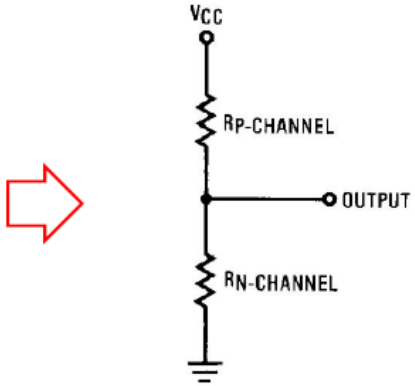
Selection of digital logic circuits – TTL vs LVTTL vs CMOS

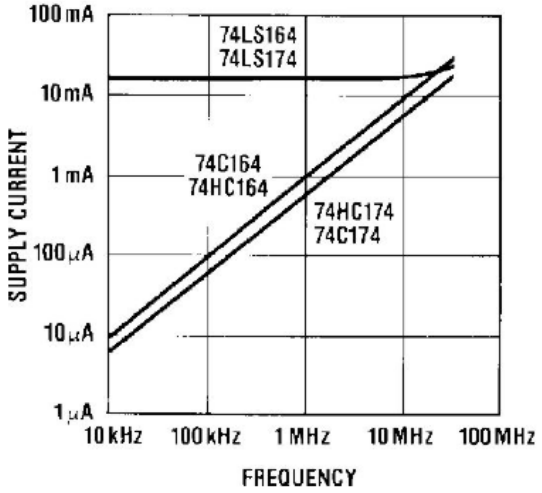




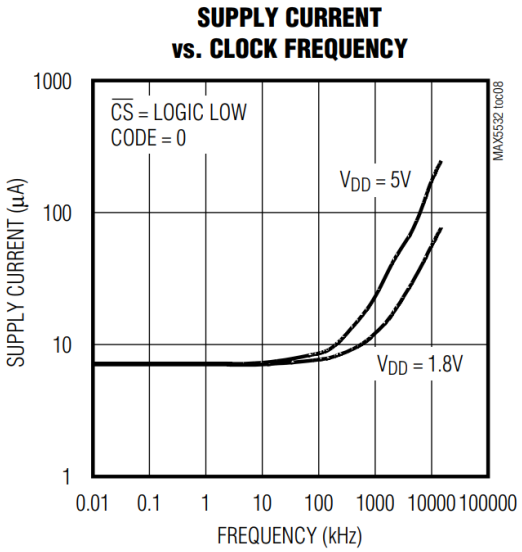
$$P \propto C \cdot V_{CC}^{\ 2} \cdot f$$







Peripherals in power saving modes - examples



MAXIM

Dual, Ultra-Low-Power, 12-Bit, Voltage-Output DACs

MAX5532–MAX5535

Features

- Ultra-Low 5µA Supply Current
- Shutdown Mode Reduces Supply Current to 0.18µA (max)
- Single +1.8V to +5.5V Supply
- Small 4mm x 4mm x 0.8mm Thin QFN Package
- Internal Reference Sources 8mA of Current (MAX5533/MAX5535)
- Flexible Force-Sense-Configured Rail-to-Rail Output Buffers
- Fast 16MHz, 3-Wire, SPI-/QSPI-/MICROWIRE-Compatible Serial Interface
- TTL- and CMOS-Compatible Digital Inputs with Hysteresis
- Glitch-Free Outputs During Power-Up

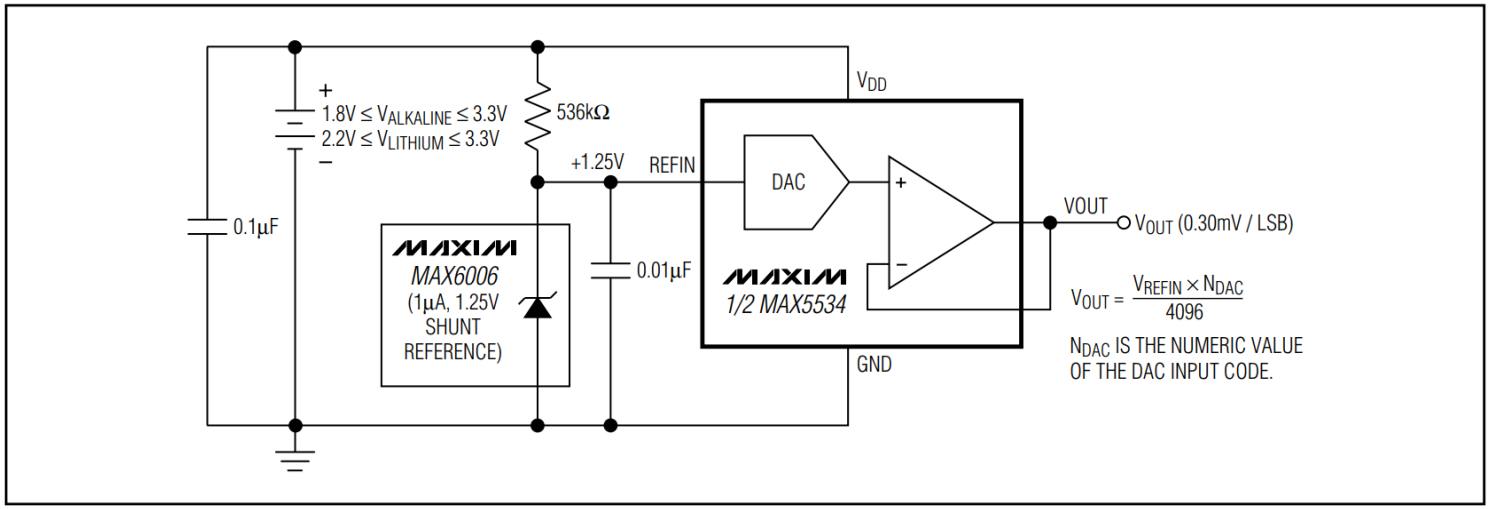


Figure 3. Portable Application Using Two Alkaline Cells or One Lithium Coin Cell

Source: https://pl.mouser.com/datasheet/2/256/MAX5533-1514746.pdf

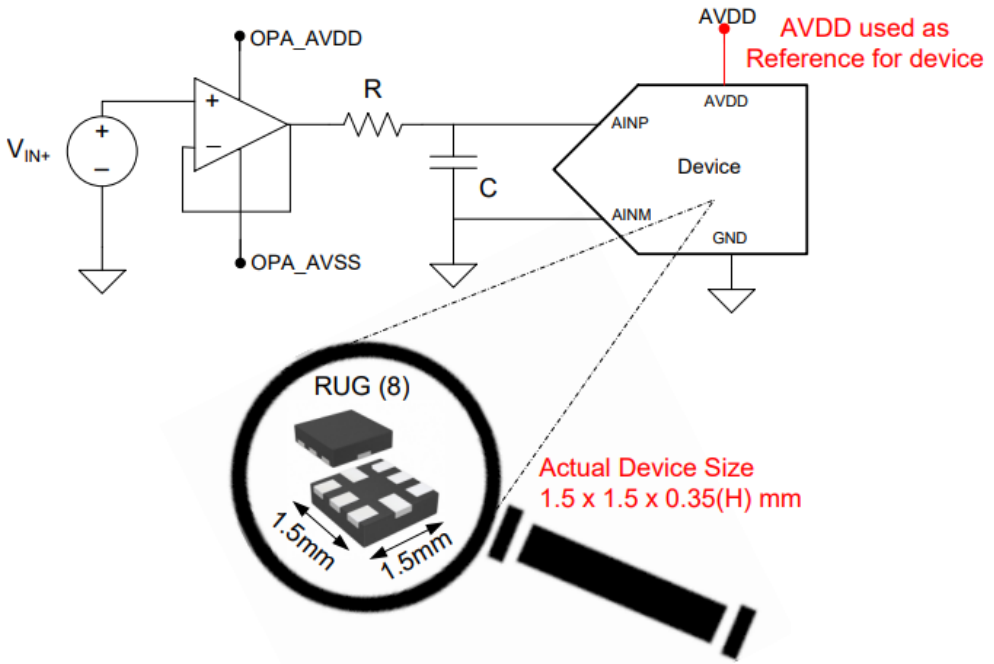
Peripherals in power saving modes - examples

ADS7042 Ultra-Low Power, Ultra-Small Size, 12-Bit, 1-MSPS, SAR ADC

1 Features

- Industry's First SAR ADC with Nanowatt Power Consumption:
  - 234 µW at 1 MSPS with 1.8-V AVDD
  - 690 µW at 1 MSPS with 3-V AVDD
  - 69 µW at 100 kSPS with 3-V AVDD
  - Less than 1 µW at 1 kSPS with 3-V AVDD
- Industry's Smallest SAR ADC:
  - X2QFN-8 Package with 2.25-mm^2 Footprint
- 1-MSPS Throughput with Zero Data Latency
- Wide Operating Range:
  - AVDD: 1.65 V to 3.6 V
  - DVDD: 1.65 V to 3.6 V (Independent of AVDD)
  - Temperature Range: –40°C to 125°C
- Excellent Performance:
  - 12-Bit Resolution with NMC
  - ±1-LSB (Max) DNL and INL
  - 70-dB SNR with 3-V AVDD
  - –80-dB THD with 3-V AVDD
- Unipolar Input Range: 0 V to AVDD
- Integrated Offset Calibration
- SPI™-Compatible Serial Interface: 16 MHz
- JESD8-7A Compliant Digital I/O

Typical Application



Modern power supply modules

LM7805C:

- output current in excess of 1A
- 2.5 V (typ) dropout voltage
- 50 mV (max) of line regulation
- 50 mV (max) of load regulation
- 8.5 mA quiescent current
- 40 μV_{RMS} output noise
- internal thermal overload protection
- no external components required
- internal short-circuit protection
- TO-3 and TO-220 packages

66% @ 5.0/7.5 V

MAX1793:

- guaranteed 1 A output current
- low 210 mV dropout @ 1 A
- up to ±1% output voltage accuracy
- preset at 1.5 V, 1.8 V, 2.0 V, 2.5 V, 3.3 V or 5.0 V
- adjustable from 1.25 V to 5.0 V
- low 125 µA ground current (200 µA @ 0.5 A output current)
- 0.1 µA shutdown
- low 115 μV_{RMS} output noise
- thermal overload protection
- output current limit
- TSSOP power package (1.5 W)

94% @ 3.3/3.51 V
66% @ 3.3/5.0 V

MAX8902:

- guaranteed 0.5 A output current
- 100mV (max) dropout @ 0.5 A
- ±1.5% output accuracy over load, line, and temperature
- 1.7 V to 5.5 V input voltage
- 0.6 V to 5.3 V output voltage
- 80 µA operating supply current
- < 1µA shutdown supply current
- 16 μV_{RMS} output noise
- 0.7 A short-circuit protection
- thermal-overload protection
- output-to-input reverse current protection

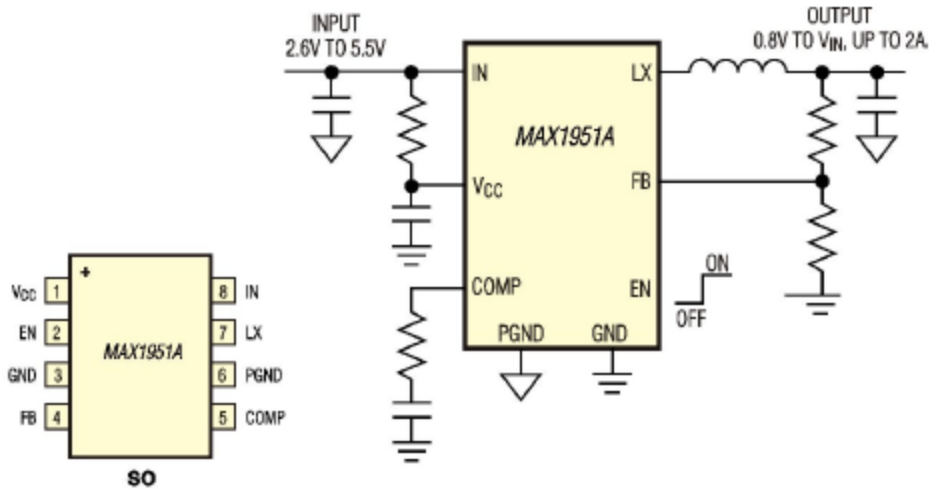
97% @ 3.3/3.4 V
66% @ 3.3/5.0 V

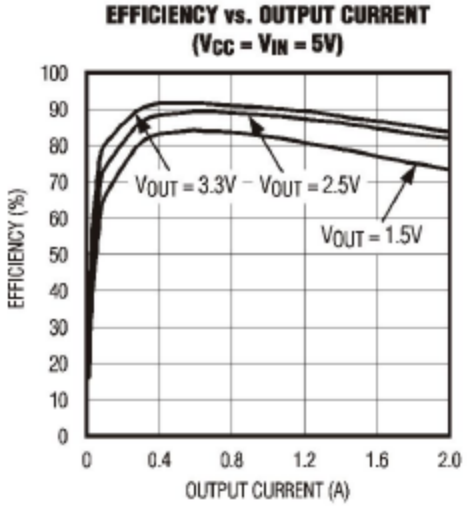
Modern power supply modules

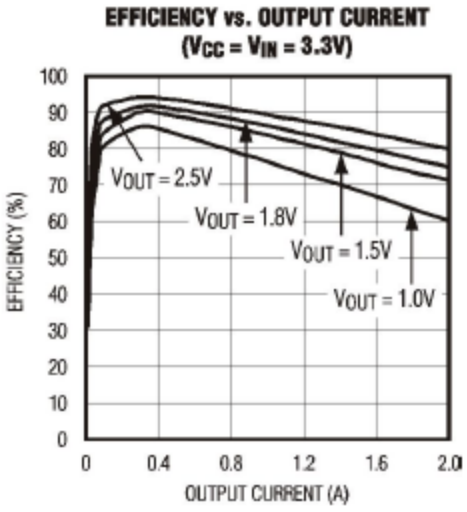
MAX1951A features:

- Efficiency Up to 94%
- 1.5% Output Accuracy Over Load, Line, and Temperature
- Guaranteed 2A Output Current
- Operates from 2.6V to 5.5V Supply
- Adjustable Output from 0.8V to VIN
- Internal Digital Soft-Soft
- Short-Circuit and Thermal-Overload Protection
- 1MHz Switching Frequency Reduces Component Size
- Enable Input Audio Shutdown for Reducing Power Consumption

92-93%@ 3.3/5.0 V

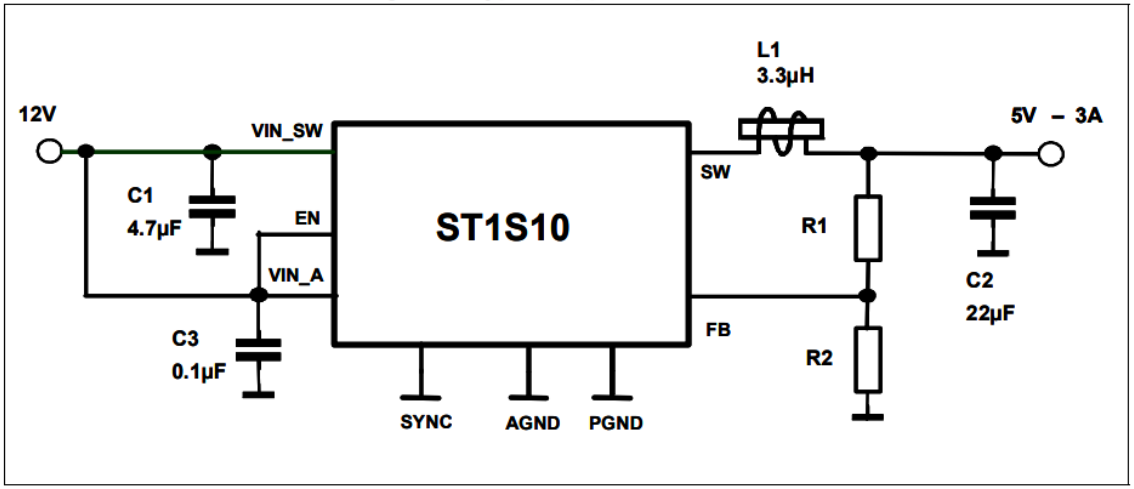






Modern power supply modules – ST1S10

Figure 1. Typical application circuit



Features

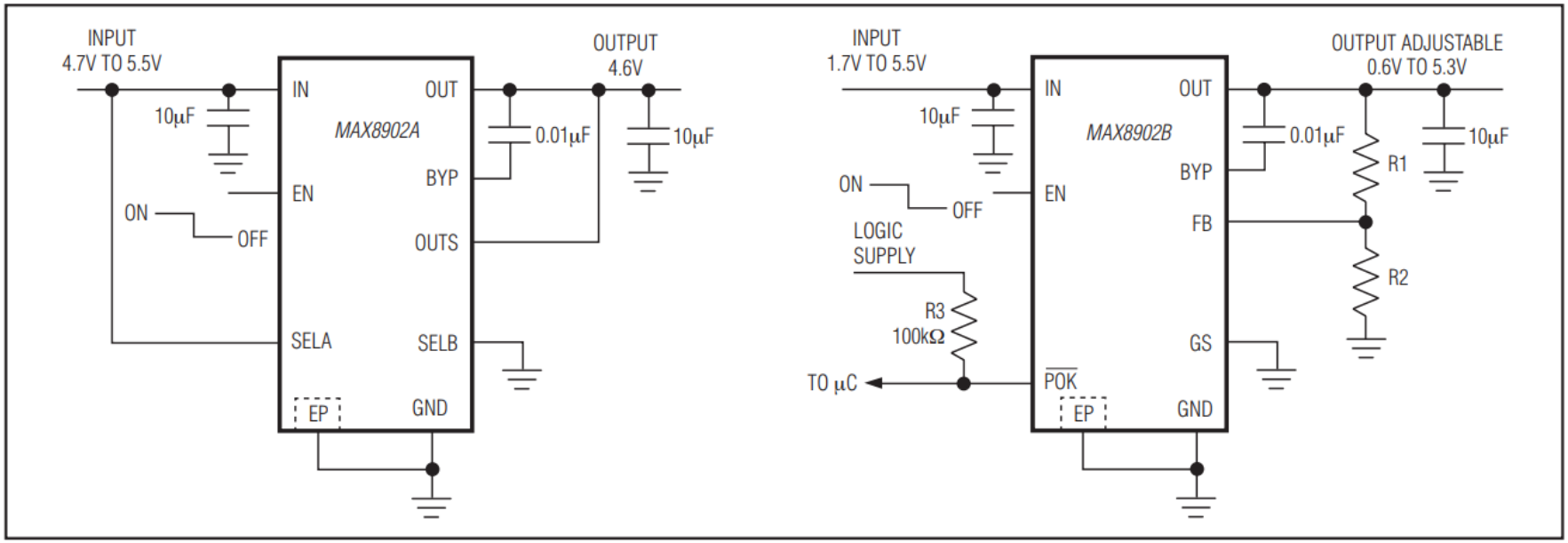
- Step-down current mode PWM regulator
- Output voltage adjustable from 0.8 V
- Input voltage from 2.5 V up to 18 V
- 2% DC output voltage tolerance
- Synchronous rectification
- Inhibit function
- Synchronizable switching frequency from 400 kHz up to 1.2 MHz
- Internal soft start
- Dynamic short-circuit protection
- Typical efficiency: 90%
- 3 A output current capability
- Standby supply current: max. 6 µA over temperature range
- Operative junction temp.: from -40 °C to 125 °C

Modern power supply modules – MAX8902

Features

- 1.7V to 5.5V Input Voltage Range
- 0.6V to 5.3V Output Voltage Range
- 16μV_{RMS} Output Noise, 10Hz to 100kHz
- 80μA Operating Supply Current
- 92dB PSRR at 5kHz
- Guaranteed 500mA Output Current
- ±1.5% Output Accuracy Over Load, Line, and Temperature
- 100mV (max) Dropout at 500mA Load
- < 1μA Shutdown Supply Current
- 700mA Short-Circuit Protection
- Thermal-Overload Protection
- Output-to-Input Reverse Current Protection
- 2mm x 2mm x 0.8mm TDFN Package

Typical Operating Circuits



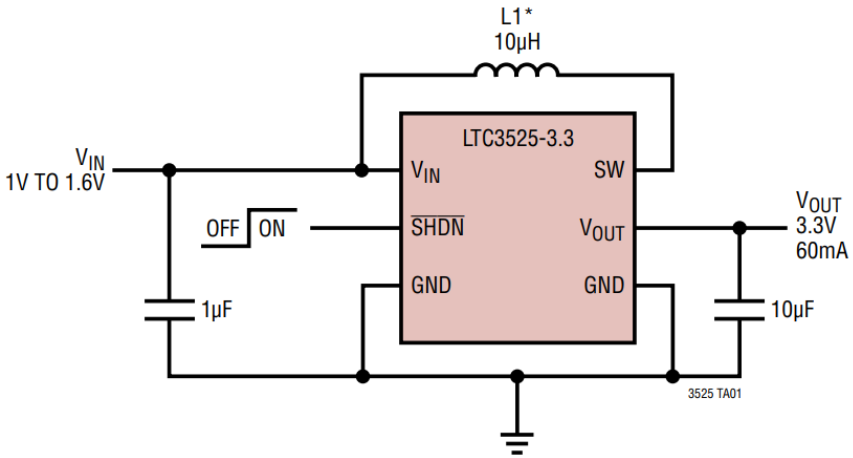
Pin Configurations appear at end of data sheet.

Modern power supply modules – battery example

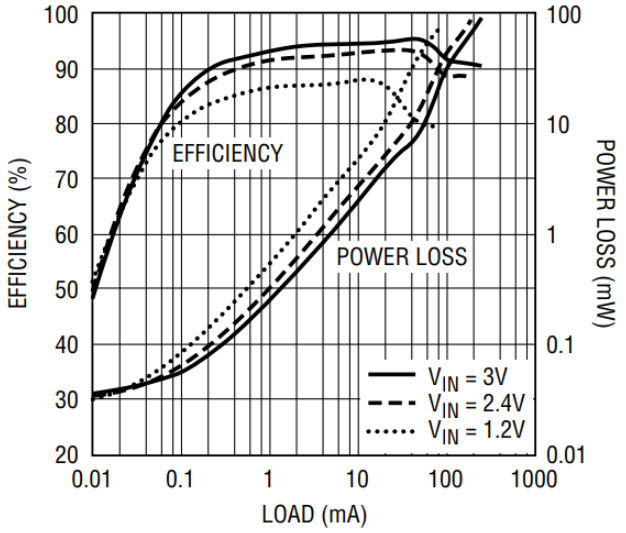
FEATURES

- **Up to 95% Efficiency**
- **Output Disconnect and Inrush Current Limit**
- **Fixed Output Voltages of 3V, 3.3V or 5V**
- **Delivers 65mA at 3V from a 1V Input**
- **Delivers 60mA at 3.3V from a 1V Input, or 140mA at 3.3V from a 1.8V Input**
- **Delivers 175mA at 5V from a 3V Input**
- **Burst Mode® Operation: I_Q = 7µA**
- Only Three External Components
- $V_{IN} > V_{OUT}$ Operation
- <1µA Shutdown Current
- Antiringing Control
- Short-Circuit and Overtemperature Protection
- Very Low Profile of 1mm
- Tiny 6-Lead SC70 Package

TYPICAL APPLICATION



LTC3525-3.3 Efficiency and Power Loss vs Load Current



More information: https://www.analog.com/media/en/technical-documentation/data-sheets/3525fc.pdf

General tips for power savings in microprocessor systems

- use CMOS whenever possible
- never leave CMOS inputs floating; connect unused inputs to GND or VCC
- use power saving modes efficiently
- use lower frequency of operation
- use lower supply voltage
- select energy-efficient components (in particular low-power microprocessor)
- switch off (power off) all the peripherals which you don't need at the moment
- use LCD instead of LEDs, don't use graphic LCD, neither backlight if it is not critical
- modern technology and higher level of integration usually result in lower power consumption
- remember that pull-ups, polarization resistors, etc. also draw current
- use high-efficiency DC/DC instead of linear regulators

Further reading

- https://www.analog.com/en/analog-dialogue/articles/designing-single-supply-low-power-battery.html
- http://ww1.microchip.com/downloads/en/appnotes/39610d.pdf
- http://www.ti.com/lit/ml/slyp088/slyp088.pdf