EDM1-IMX6

VER. 1.10

June 2, 2022

REVISION HISTORY

Revision	Date	Originator	Notes
1.00	November 14, 2019	TechNexion	Initial Public Release
1.10	June 2, 2022	TechNexion	Update LAN PHY to Realtek for continuous supply (PCB REV D1)

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1. Introduction

1.1. General Introduction

The EDM1-IMX6 is a high performance highly integrated EDM type 1 System-on-Module designed around the NXP i.MX6 Multicore ARM Cortex-A9. The EDM1-IMX6 provides an ideal building block that easily integrates with a wide range of target markets requiring rich multimedia functionality, powerful graphics and video capabilities, as well as high-processing power, compact, cost effective and with low power consumption.

The EDM1-IMX6 System-on-Module is typically being used as building blocks for portable and stationary embedded systems. The core CPU and support circuits, including DRAM, booth flash, power sequencing, CPU power supplies, Gigabit Ethernet and display interfaces are concentrated on the module. The modules are used with application specific carrier boards that implement other features such as audio CODECs, touch controllers, sensors and etcetera.

The modular approach offered by the EDM standard gives your project scalability, fast time to market and upgradability while reducing engineering risk and maintain a competitive total cost of ownership.

1.2. General Care and Maintenance

Your device is a product of superior design and craftsmanship and should be treated with care.

The following suggestions will help you.

- Keep the device dry. Precipitation, humidity, and all types of liquids or moisture can contain minerals that will corrode electronic circuits. If your device does get wet, allow it to dry completely.
- Do not use or store the device in dusty, dirty areas. Its moving parts and electronic components can be damaged.
- Do not store the device in hot areas. High temperatures can shorten the life of electronic devices, damage batteries, and warp or melt certain plastics.
- Do not store the device in cold areas. When the device returns to its normal temperature, moisture can form inside the device and damage electronic circuit boards.
- Do not attempt to open the device.
- Do not drop, knock, or shake the device. Rough handling can break internal circuit boards and fine mechanics.
- Do not use harsh chemicals, cleaning solvents, or strong detergents to clean the device.
- Do not paint the device. Paint can clog the moving parts and prevent proper operation.
- Unauthorized modifications or attachments could damage the device and may violate regulations governing radio devices.

These suggestions apply equally to your device, battery, charger, or any enhancement. If any device is not working properly, take it to the nearest authorized service facility for service.
Regulatory information

Disposal of Waste Equipment by Users in Private Household in the European Union
This symbol on the product or on its packaging indicates that this product must not be disposed of with your other household waste. Instead, it is your responsibility to dispose of your waste equipment by handing it over to a designated collection point for the recycling of waste electrical and electronic equipment. The separate collection and recycling of your waste equipment at the time of disposal will help to conserve natural resources and ensure that it is recycled in a manner that protects human health and the environment. For more information about where you can drop off your waste equipment for recycling, please contact your local city office, your household waste disposal service or the shop where you purchased the product.

We hereby declare that the product is in compliance with the essential requirements and other relevant provisions of European Directive 1999/5/EC (radio equipment and telecommunications terminal equipment Directive).

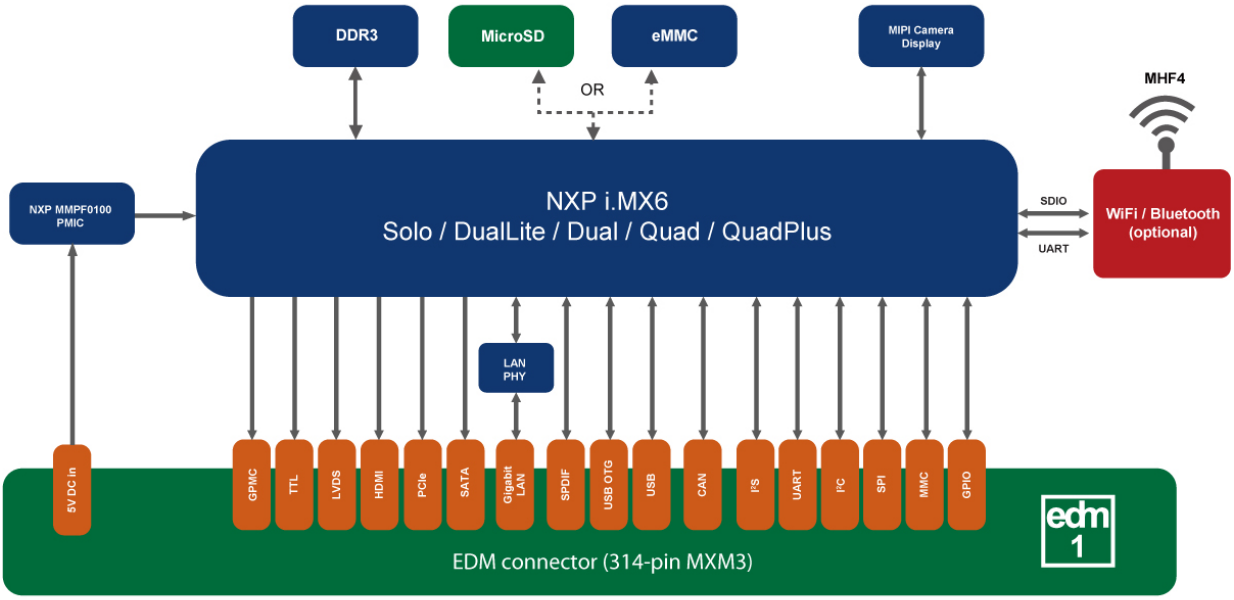
Federal Communications Commission (FCC) Unintentional emitter per FCC Part 15
This device has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio or television reception. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause interference to radio and television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna
- Increase the separation between the equipment and receiver
- Connect the equipment to an outlet on a different circuit from that to which the receiver is connected
- Consult the dealer or an experienced radio/TV technician for help.

WARNING! To reduce the possibility of heat-related injuries or of overheating the computer, do not place the computer directly on your lap or obstruct the computer air vents. Use the computer only on a hard, flat surface. Do not allow another hard surface, such as an adjoining optional printer, or a soft surface, such as pillows or rugs or clothing, to block airflow. Also, do not allow the AC adapter to contact the skin or a soft surface, such as pillows or rugs or clothing, during operation. The computer and the AC adapter comply with the user-accessible surface temperature limits defined by the International Standard for Safety of Information Technology Equipment (IEC 60950).

1.3. Block Diagram

Figure 1 - EDM1-IMX6 Block Diagram



1.4. EDM Compatibility

The EDM1-IMX6 is fully compatible with the EDM Type 1 Standard specifications.

For additional details, please refer to the “EDM Standard Specifications”.

Figure 2 – EDM Type 1 Compatibility Chart

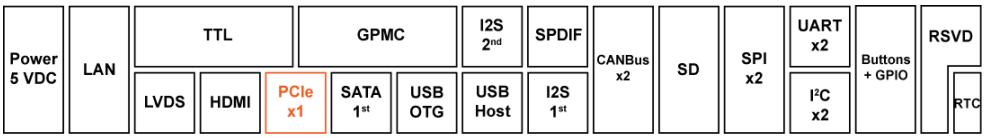


Table 1 - EDM Compatibility Overview

Interface	Description
LAN	1 Gigabit Ethernet
LVDS	1 single channel 18/24 bit
HDMI	1 HDMI ver.1.4 compatible
TTL Display	1 TTL 18/24 bit Display
PCIe	1 Lane PCIe 2.0
SATA	1 SATA II
USB Host	1 USB 2.0 Host port
USB OTG	1 USB 2.0 OTG port (possible to use in Host mode)
GPMC	8 bit localbus interface with 4 chip selects
I2S	2 Independent I^2S interfaces
SPDIF	1 S/P DIF interface
CAN Bus	2 FlexCAN CAN 2.0B protocol compliant interfaces
UART	2 UART 4 wire
SDIO	1 SDIO interface 4 bit
SPI	2 SPI interfaces with 2 chip selects
I^2C	2 independent general purpose interfaces 1 dedicated towards display/system functions
GPIO	10 dedicated GPIO’s available
RTC	On carrierboard

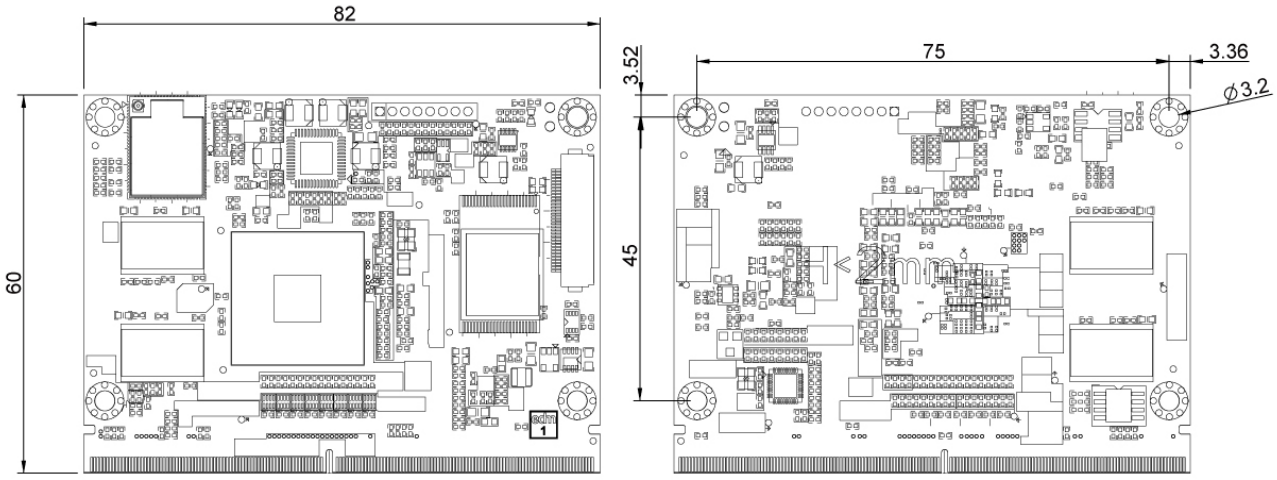
1.5. Dimensional Drawing

The EDM1-IMX6 is an EDM Type 1 Compact Form Factor System-on-Module and follows the EDM Standard Specifications in regards of dimensions and mounting options.

2D and 3D files can be obtained from the **www.technexion.com** homepage.

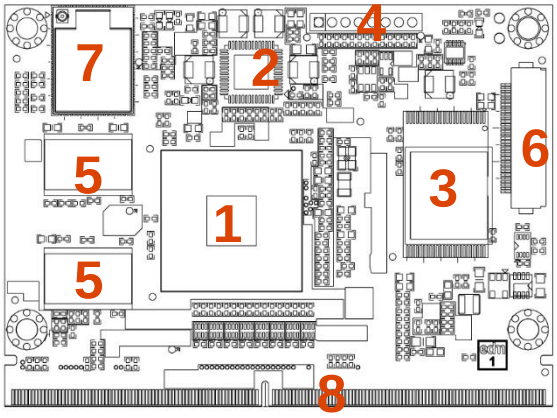
For additional details, please refer to the “EDM Standard Specifications”.

Figure 3 - EDM1-IMX6 Dimensional Drawing



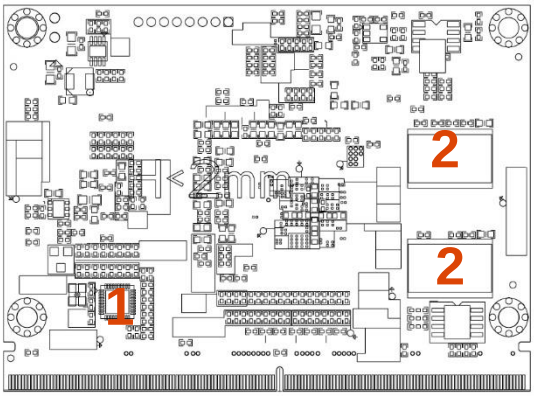
1.6. Component Location

Figure 4 - EDM1-IMX6 Top view



Item	Description	Item	Description
1	NXP i.MX6 Processor	5	Memory IC (2)
2	MMPF0100 Power Management IC	6	MIPI Camera / Display Connector
3	NAND Flash / eMMC (co-layout)	7	WiFi / BT Module
4	JTAG Interface	8	EDM Type 1 Connector

Figure 5 - EDM1-IMX6 Bottom view



Item	Description	Item	Description
1	Gigabit Ethernet PHY	2	Memory IC (2)

2. Core Components

2.1. NXP i.MX6 Cortex-A9 Multi-core Processor

The NXP i.MX6 processor is an implementation of the Single/Dual/Quad/Quadplus ARM Cortex™-A9 core, which operates at frequencies up to 1.2 GHz. The i.MX6 provides a variety of interfaces and supports the following main features:

- Single / Dual / Quad Core ARM Cortex™-A9. Core configuration is symmetric, where each core includes:
  - 32 KByte L1 Instruction Cache
  - 32 KByte L1 Data Cache
  - Private Timer and Watchdog
  - Cortex-A9 NEON MPE (Media Processing Engine) Co-processor
- Level 2 Cache—Unified instruction and data (up to 1 MByte)
- General Interrupt Controller (GIC) with 128 interrupt support
- Global Timer
- Snoop Control Unit (SCU)
- NEON MPE coprocessor:
  - SIMD Media Processing Architecture
  - NEON register file with 32x64-bit general-purpose registers
  - NEON Integer execute pipeline (ALU, Shift, MAC)
  - NEON dual, single-precision floating point execute pipeline (FADD, FMUL)
  - NEON load/store and permute pipeline
- Integrated Power Management unit:
  - Temperature Sensor for monitoring the die temperature
  - DVFS techniques for low power modes
  - Flexible clock gating control scheme
- Multimedia Hardware Accelerators

Figure 6 – NXP i.MX6 Processor Blocks

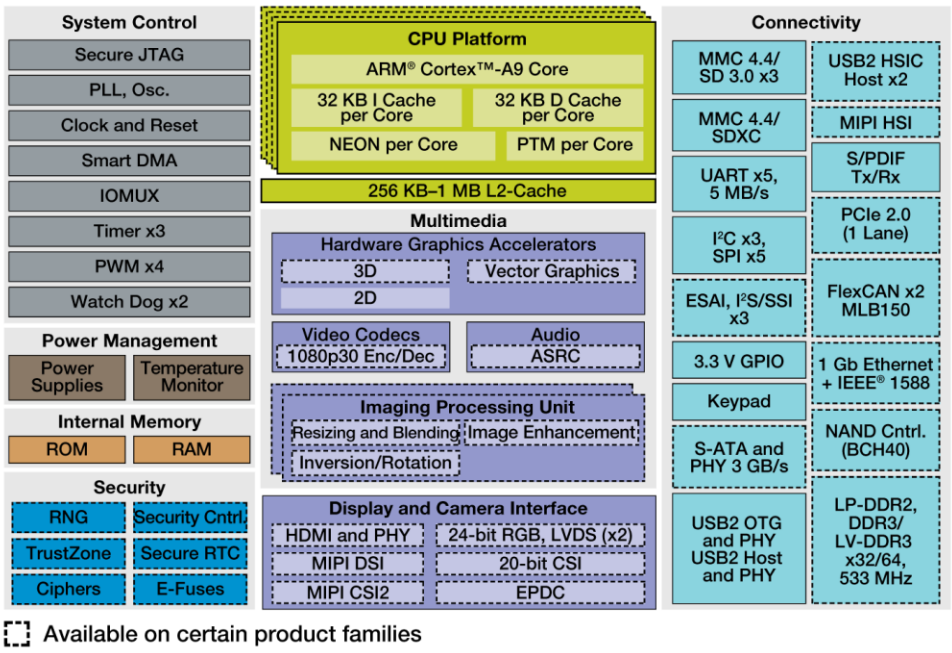
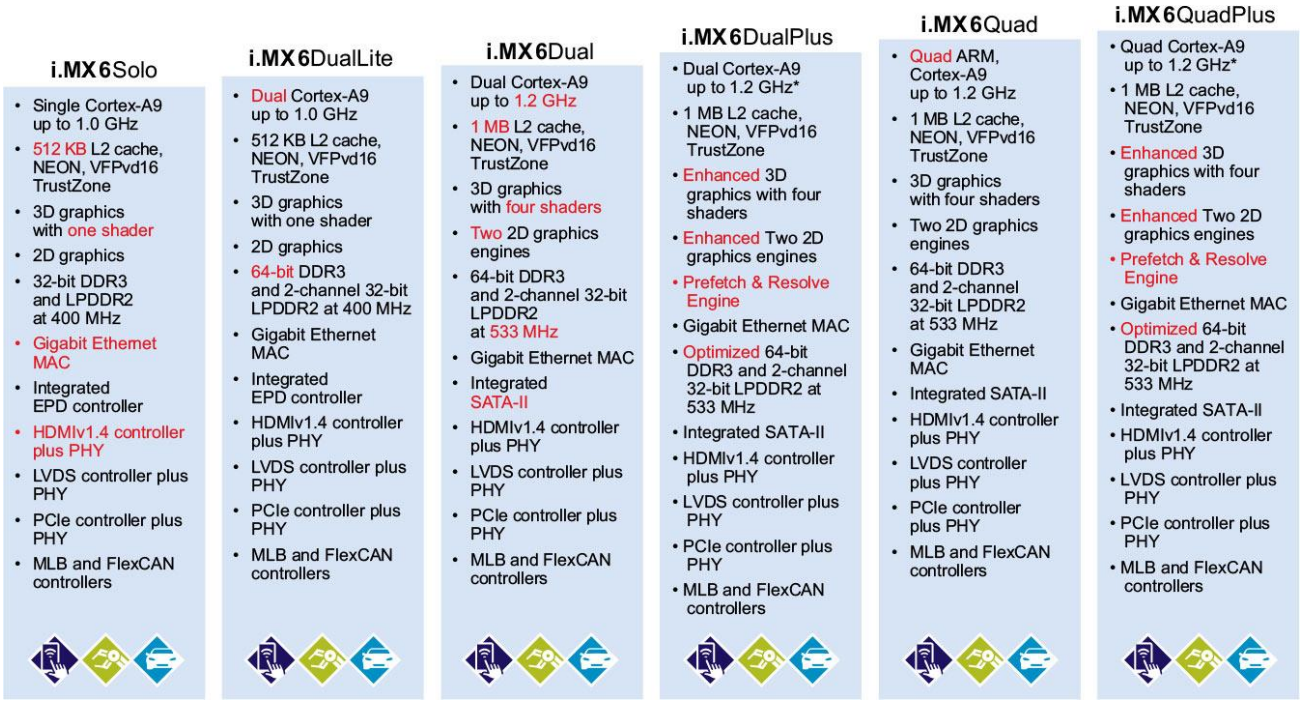


Figure 7 – NXP i.MX6 Processor Scalability Overview (Solo/Duallite/Dual/Quad/QuadPlus)



2.1.1. i.MX6 Memory Interfaces

- The memory system consists of the following components:
  - Level 1 Cache—32 KB Instruction, 32 KB Data cache per core
  - Level 2 Cache—Unified instruction and data (1 MByte)
- On-Chip Memory:
  - Boot ROM, including HAB (96 KB)
  - Internal multimedia / shared, fast access RAM (OCRAM, 256 KB)
  - Secure/non-secure RAM (16 KB)
- External memory interfaces:
  - 16-bit, 32-bit, and 64-bit DDR3-1066 and LV-DDR3-1066
  - 8-bit NAND-Flash, including support for Raw MLC/SLC, 2 KB, 4 KB, and 8 KB page size,
  - BA-NAND, PBA-NAND, LBA-NAND, OneNAND™ and others. BCH ECC up to 32 bit.

2.1.2. i.MX6 DMA Engine

The SDMA is multi-channel flexible DMA engine. It helps in maximizing system performance by off-loading the various cores in dynamic data routing. It has the following features:

- Powered by a 16-bit Instruction-Set micro-RISC engine
- Multi-channel DMA supporting up to 32 time-division multiplexed DMA channels
- 48 events with total flexibility to trigger any combination of channels
- Memory accesses including linear, FIFO, and 2D addressing
- Shared peripherals between ARM and SDMA
- Very fast Context-Switching with 2-level priority based preemptive multi-tasking
- DMA units with auto-flush and prefetch capability
- Flexible address management for DMA transfers (increment, decrement, and no address changes on source and destination address)
- DMA ports can handle unit-directional and bi-directional flows (copy mode)
- Up to 8-word buffer for configurable burst transfers
- Support of byte-swapping and CRC calculations
- Library of Scripts and API is available

2.1.3. i.MX6 Video and Graphics Subsystems

The EDM1-IMX6 video graphics subsystem consists of the following i.MX6 sub-blocks.

- VPU: A multi-standard high performance video codec engine supporting encode/decode operations of the following:
    - Decoding: H.264 BP/CBP/MP/HP, VC-1 SP/MP/AP, MPEG-4 SP/ASP, H.263 P0/P3, MPEG-1/2 MP, Divx (Xvid) HP/PP/HTP/HDP, VP8 (1280x720), AVS, H.264-MVC (1280x720), MJPEG BP (max. 8192x8192) up to full-HD 1920x1088 @30fps plus D1 @30fps.
    - Encoding: H.264 BP/CBP, MPEG-4 SP, H.263 P0/P3, MJPEG BP (max. 192x8192) up to full-HD 1920x1088@30fps.
- GPU2Dv2: Hardware acceleration of 2D graphics (Bit BLT and Stretch BLT). Based on the Vivante GC320 IP core.
- GPUVG: An OpenVG 1.1 Graphics Processing Unit providing hardware acceleration of vector graphics. Based on the Vivante GC355 IP core

Additionally the EDM1-IMX6 incorporates the following 3D GPU engine

The EDM1-IMX6 featuring an i.MX6 Solo or Duallite processor:

- GPU3Dv5: A 3D GPU (Vivante GC880), compliant with OpenGL ES2.0, OpenGL ES1.1 and OpenVG 1.1.

The EDM1-IMX6featuring an i.MX6 Dual or Quad processor:

- GPU3Dv4: A 3D GPU (Vivante GC2000), compliant with OpenGL ES2.0, OpenGL ES1.1 and OpenVG 1.1.

The EDM1-IMX6 featuring an i.MX6 DualPlus or QuadPlus processor:

- GPU3Dv4: A 3D GPU (Vivante GC2000+), compliant with OpenGL ES2.0, OpenGL ES1.1 and OpenVG 1.1.

2.2. Power Management IC (MMPF0100)

The EDM1-IMX6 has on onboard NXP MMPF0100 power management integrated circuit (PMIC) that features a configurable architecture supporting the numerous outputs with various current ratings as well as programmable voltage and sequencing required by the components on the EDM1-IMX6 module.

Table 2 - PMIC Signal Description

PMIC PIN	i.MX6 BALL	PAD NAME	Signal	V	I/O	Description
53	R2	GPIO_05	I2C3_SCL	3V3	I/O	I^2C bus clock line
54	R4	GPIO_16	I2C3_SDA	3V3	I/O	I^2C bus data line
56	D11	PMIC_ON_REQ	PMIC_ON_REQ	3V3	I	PMIC Power ON/OFF Input from processor
1	U20	PMIC_INT_B	PMIC_INT_B	3V3	I	PMIC Interupt Signal
3	C11	POR_B	POR_B	3V3	I	PMIC Reset Signal
4	F11	PMIC_STBY_REQ	PMIC_STBY_REQ	3V3	I	PMIC Standby Input Signal

For more information, please contact your TechNexion sales representative.

2.3. Memory

The EDM1-IMX6 integrates Double Data Rate III (DDR3) Synchronous DRAM in either a single (32 bit) or a dual (64 bit) channel configuration.

The following memory chips have been validated and tested on the EDM1-IMX6 System-on-Module:

- SKHynix
- Samsung
- ISSI
- Micron

NOTE : The i.MX6 Solo only support single (32 bit) channel configuration.

For more information, please contact your TechNexion sales representative.

2.4. eMMC Storage

The EDM1-IMX6 can be ordered with onboard eMMC storage in different configurations and capacity.

The onboard eMMC device is connected on the SD3 pins of the i.MX6 processor in a 8 bit width configuration.

The following eMMC chips have been validated and tested on the EDM1-IMX6 System-on-Module:

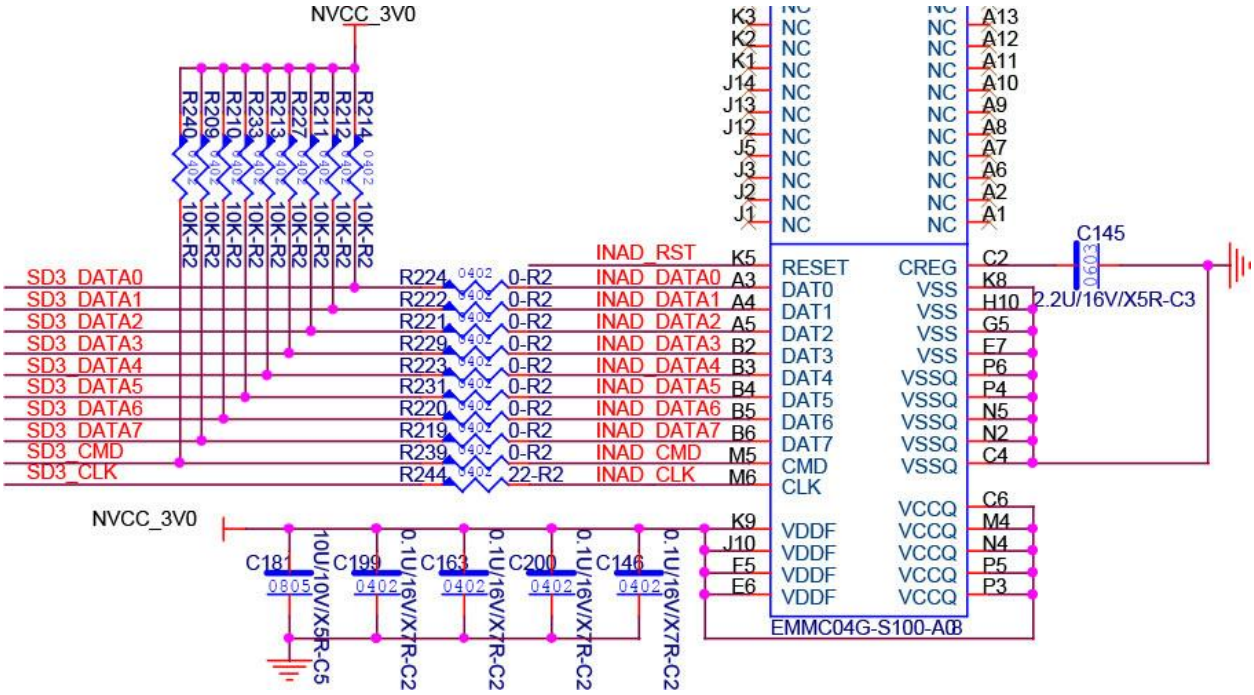
- Sandisk iNAND
- Kingston eMMC
- Micron eMMC

For more information, please contact your TechNexion sales representative.

Table 3 - eMMC Signal Description

i.MX6 BALL	PAD NAME	Signal	V	I/O	Description
E14	SD3_DAT0	eMMC_DATA0	3V3	I/O	MMC/SDIO Data bit 0
F14	SD3_DAT1	eMMC_DATA1	3V3	I/O	MMC/SDIO Data bit 1
A15	SD3_DAT2	eMMC_DATA2	3V3	I/O	MMC/SDIO Data bit 2
B15	SD3_DAT3	eMMC_DATA3	3V3	I/O	MMC/SDIO Data bit 3
D13	SD3_DAT4	eMMC_DATA4	3V3	I/O	MMC/SDIO Data bit 4
C13	SD3_DAT5	eMMC_DATA5	3V3	I/O	MMC/SDIO Data bit 5
E13	SD3_DAT6	eMMC_DATA6	3V3	I/O	MMC/SDIO Data bit 6
F13	SD3_DAT7	eMMC_DATA7	3V3	I/O	MMC/SDIO Data bit 7
B13	SD3_CMD	eMMC_CMD	3V3	I/O	MMC/SDIO Command
D14	SD3_CLK	eMMC_CLK	3V3	O	MMC/SDIO Clock

Figure 8 - eMMC Schematics



2.5. WiFi/Bluetooth SIP Module

The EDM1-IMX6 has an optional pre-certified high-performance TechNexion PIXI-9377 dual band 2.4/5Ghz Wi-Fi / Bluetooth 5 Qualcomm Atheros QCA9377 chipset based module on board.

The PIXI-9377 Wi-Fi / Bluetooth module is designed to operate with a single antenna for Wi-Fi and Bluetooth by using the MHF4 connector.

Key Features of the PIXI-9377 are:

- IEEE 802.11 ac/a/b/g/n 2.4 / 5Ghz
- Bluetooth 5
- MHF4 antenna connector
- Linux and Android drivers
- Wi-Fi / BT module board certifications with multiple antennas:
    - FCC (USA)
    - IC (Canada
    - ETSI (Europe)
    - Giteki / Telec (Japan)
    - RCM / C-tick (Australia / New Zealand).
- Industrial operation temperature range : -40°C to +85°C

The following pre-certified matching antennas are available with our distributors.

Partnumber	Description
ANTP180A138045D2450MHF4	4.5dBi dipole antenna
ANTP180A207070D2450MHF4	7dBi dipole antenna
ANTP150P232525D2450MHF4	2.5dBi PCB patch antenna

Figure 9 – EDM1-IMX6 Wi-Fi Module and Antenna Connector Location

Table 4 – Wi-Fi Signal Description

i.MX6 BALL	PAD NAME	Signal	I/O	Description
A22	SD2_DAT0	SD2_DAT0	I/O	MMC/SDIO Data bit 0
E20	SD2_DAT1	SD2_DAT1	I/O	MMC/SDIO Data bit 1
A23	SD2_DAT2	SD2_DAT2	I/O	MMC/SDIO Data bit 2
B22	SD2_DAT3	SD2_DAT3	I/O	MMC/SDIO Data bit 3
F19	SD2_CMD	SD2_CMD	I/O	MMC/SDIO Command
C21	SD2_CLK	SD2_CLK	O	MMC/SDIO Clock
W20	ENET_TXD1	GPIO1_IO29	O	Host wake up. Signal from the module to the host indicating that the module requires Attention. • Asserted: Host device must wake-up or remain awake. • Deserted: Host device may sleep when sleep criteria are met. The polarity of this signal is software configurable and can be asserted high or low.
W22	ENET_RXD1	GPIO1_IO26	O	Wi-Fi device wake-up: Signal from the host to the module indicating that the host requires attention. • Asserted: Wi-Fi device must wake-up or remain awake. • Deserted: Wi-Fi device may sleep when sleep criteria are met. The polarity of this signal is software configurable and can be asserted high or low.
N2	CSI0_VSYNC	GPIO5_IO21	O	SDIO Reset signal. For normal operation signal should be pull-high in software.

Table 5 – Bluetooth Signal Description

i.MX6 BALL	PAD NAME	Signal	I/O	Description
F22	EIM_D24	UART3_TXD	O	Bluetooth UART Serial Input. Serial data input for the HCI UART Interface
G22	EIM_D25	UART3_RXD	I	Bluetooth UART Serial Output. Serial data output for the HCI UART Interface.
D25	EIM_D23	UART3_CTS	I/O	Bluetooth UART Clear to Send. Active-low clear-to-send signal for the HCI UART interface.
F23	EIM_EB3	UART3_RTS	I/O	Bluetooth UART Request to Send. Active-low request-to-send signal for the HCI UART interface.
U6	KEY_ROW1	AUD5_RXD	I	Integrated Interchip Sound (I^2S) channel receive data line
V6	KEY_ROW0	AUD5_TXD	O	Integrated Interchip Sound (I^2S) channel transmit data line
W5	KEY_COL0	AUD5_TXC	O	Integrated Interchip Sound (I^2S) channel word clock signal
U7	KEY_COL1	AUD5_TXFS	O	Integrated Interchip Sound (I^2S) channel frame synchronization signal
P3	CSI0_DATA_EN	GPIO5_IO20	I	Host UART wake up. Signal from the module to the host indicating that the module requires Attention. • Asserted: Host device must wake-up or remain awake. • Deserted: Host device may sleep when sleep criteria are met. The polarity of this signal is software configurable and can be asserted high or low.
M2	CSI0_DAT12	GPIO5_IO30	O	Bluetooth device wake-up: Signal from the host to the module indicating that the host requires attention. • Asserted: Bluetooth device must wake-up or remain awake. • Deserted: Bluetooth device may sleep when sleep criteria are met. The polarity of this signal is software configurable and can be asserted high or low.

2.6. Gigabit LAN

The EDM1-IMX6 connects the i.MX6 processor RGMII interface to the gigabit Ethernet PHY chip.

The AR8035 supports IEEE 802.3az EEE standard (Energy Efficient Ethernet) and Atheros proprietary SmartEEE. SmartEEE allows legacy MAC/SoC devices without 802.3az support to function as a complete 802.3az system.

Features:

- 10/100/1000 BASE-T IEEE 802.3 compliant
- Supports 1000 BASE-T PCS and auto-negotiation with next page support
- RGMII timing modes support internal delay and external delay on Rx path
- Fully integrated digital adaptive equalizers, echo cancellers, and Near End Crosstalk (NEXT) cancellers
- Supports Synchronous Ethernet with selectable recovered clock output
- Robust Cable Discharge Event (CDE) protection of ±6 kV
- Error-free operation over up to 140 meters of CAT5 cable
- Automatic channel swap (ACS)
- Automatic MDI/MDIX crossover
- Automatic polarity correction
- IEEE 802.3u compliant Auto-Negotiation
- Jumbo Frame support up to 10KB (full duplex)
- Multiple loopback modes for diagnostics
- Robust Surge Protection with ±750 V/ differential mode and ±4 kV/common mode
- Cable Diagnostic Test (CDT)

For more information, please contact your TechNexion sales representative.

Table 6 - Gigabit Ethernet interconnect between i.MX6 and Gigabit Ethernet PHY

i.MX6 BALL	PAD NAME	Signal	Description
D21	RGMII_TXC	ETH_TXCLK	RGMII transmit clock
C22	RGMII_TD0	ETH_TXD0	RGMII transmit data 0
F20	RGMII_TD1	ETH_TXD1	RGMII transmit data 1
E21	RGMII_TD2	ETH_TXD2	RGMII transmit data 2
A24	RGMII_TD3	ETH_TXD3	RGMII transmit data 3
C23	RGMII_TX_CTL	ETH_TXEN	RGMII transmit enable
B25	RGMII_RXC	ETH_RXCLK	RGMII receive clock
C24	RGMII_RD0	ETH_RXD0	RGMII receive data 0
B23	RGMII_RD1	ETH_RXD1	RGMII receive data 1
B24	RGMII_RD2	ETH_RXD2	RGMII receive data 2
D23	RGMII_RD3	ETH_RXD3	RGMII receive data 3
D22	RGMII_RX_CTL	ETH_RXDV	RGMII receive data valid
V22	ENET_REF_CLK	CLK_25M	Synchronous Ethernet recovered clock
V21	ENET_TX_EN	INT	Ethernet interrupt output
J19	EIM_D29	RST	System reset
V20	ENET_MDC	MDC	Management data clock reference
V23	ENET_MDIO	MDIO	Management data

Table 7 – EDM Gigabit Ethernet Signal Description

EDM Pin	Signal	V	I/O	Description
E3_2	GBE_MDI2+	LAN	I/O	Gigabit Ethernet Media Dependent Interface (MDI) differential pair 2 positive signal
E4_2	GBE_MDI0+	LAN	I/O	Gigabit Ethernet Media Dependent Interface (MDI) differential pair 0 positive signal
E3_3	GBE_MDI2-	LAN	I/O	Gigabit Ethernet Media Dependent Interface (MDI) differential pair 2 negative signal
E4_3	GBE_MDI0-	LAN	I/O	Gigabit Ethernet Media Dependent Interface (MDI) differential pair 0 negative signal
E3_5	GBE_MDI3+	LAN	I/O	Gigabit Ethernet Media Dependent Interface (MDI) differential pair 3 positive signal
E4_5	GBE_MDI1+	LAN	I/O	Gigabit Ethernet Media Dependent Interface (MDI) differential pair 1 positive signal
E3_6	GBE_MDI3-	LAN	I/O	Gigabit Ethernet Media Dependent Interface (MDI) differential pair 3 negative signal
E4_6	GBE_MDI1-	LAN	I/O	Gigabit Ethernet Media Dependent Interface (MDI) differential pair 1 negative signal
E3_7	LED1_ACT	3V3	O	Gigabit Ethernet LED Activity indicator
E4_8	LED1_nLink100	3V3	O	Gigabit Ethernet 100Mbit/sec LED link indicator
E4_9	LED1_nLink1000	3V3	O	Gigabit Ethernet 1000Mbit/sec LED link indicator

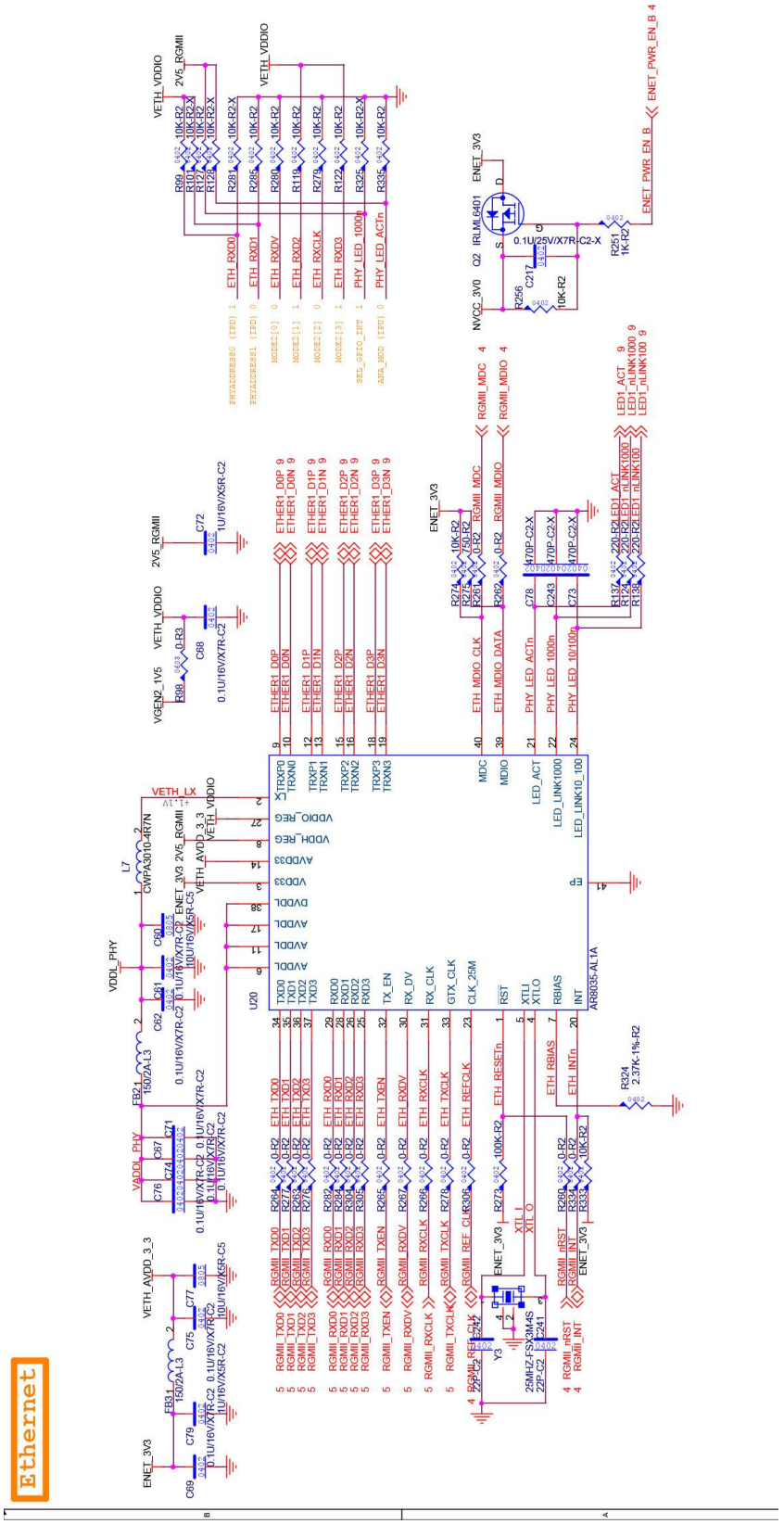
2.6.1. Gigabit Ethernet Magnetics

A Gigabit Ethernet coupling transformer either discrete or integrated inside a RJ45 jack should be integrated on the EDM carrier board.

The following table is a selection of compatible Ethernet PHY's available in the market that has been validated with the EDM1-IMX6.

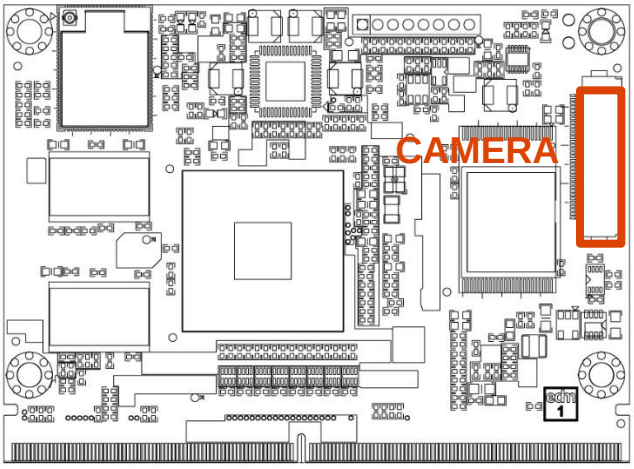
Manufacturer	Partnumber	Technology	Description
Pulse Engineering	H5007	10/100/1000BaseT	Discrete magnetics module
Pulse Engineering	JK0-0036	10/100/1000BaseT	RJ45 jack with integrated magnetics and activity LEDs
Bel Fuse	S558-5999–P3	10/100/1000BaseT	Discrete magnetics module
Pulse	JW0A1P01R-E	10/100/1000BaseT	RJ45 jack with integrated magnetics and USB jacks
Foxconn	UB11123-J51	10/100/1000BaseT	RJ45 jack with integrated magnetics and USB jacks

Figure 10 - Gigabit Ethernet Schematics



2.7 MIPI Camera and Display Connector

The EDM1-IMX6 expansion FPC connector carries the MIPI Serial Interface camera and display signals.



2.7.1 MIPI Camera

The MIPI CSI-2 Host Controller supports the following features:

- Compliant with MIPI Alliance Standard for Camera Serial Interface 2 (CSI-2), Version 1.00 – 29 November 2005
- Supports up to 4 Data Lanes
- Dynamically configurable multi-lane merging
- Long and Short packet decoding
- Timing accurate signaling of Frame and Line synchronization packets
- Supports all primary and secondary data formats:
- RGB, YUV and RAW color space definitions
- From 24-bit down to 6-bit per pixel
- Generic or user-defined byte-based data types

For additional details, please refer to the “MIPI - Camera Serial Interface Host Controller (MIPI_CSI)” chapter of the “i.MX6 Reference Manual”.

2.7.2 MIPI Display

The MIPI DSI Host Controller supports the following features:

IPU SIDE (input):

- Compliant with MIPI Alliance Specification for Display Serial Interface (DSI), Version 1.01.00 - 21 February 2008
- Fully Compliant with MIPI Alliance Standard for Display Pixel Interface (DPI-2), Version 2.00 15 September 2005 with Pixel Data bus width up to 24bits
- Compliant with MIPI Alliance Standard for Display Bus Interface (DBI-2) Version 2.00 - 29 November 2005.

Supported DBI types are:

- Type B
- 16bit, 9bit and 8bit Data bus width
- DBI and DPI interface can coexist (only one is operational at a time)
- Support all commands defined in MIPI Alliance Specification for Display Command Set (DCS), Version 1.02.00 - 23 July 2009

D-PHY side (output):

- Interface with MIPI D-PHY following PHY Protocol Interface (PPI), as defined in MIPI Alliance Specification for D-PHY, Version 1.00.00 - 14 May 2009
- Supports up to 2 D-PHY Data Lanes:
- Bidirectional Communication and Escape Mode Support through Data Lane 0.
- Programmable display resolutions, from 160x120(QQVGA) to 1024x768(XVGA).
- Multiple Peripheral Support capability, configurable Virtual Channels.
- Video Mode Pixel Formats, 16bpp(RGB565), 18bpp(RGB666) packed, 18bpp(RGB666) loosely, 24bpp(RGB888).

For additional details, please refer to the “MIPI DSI Host Controller” chapter of the “i.MX6 Reference Manual”.

Table 8 - MIPI Display and Camera Expansion Connector Signal Description

Pin #	i.MX6 PIN	PAD NAME	Signal	V	I/O	Description
1	F3	CSI_CLK0P	CSI_CLK0_P	2V5	I	MIPI Camera Serial Interface clock pair positive signal
2	F4	CSI_CLK0M	CSI_CLK0_M	2V5	I	MIPI Camera Serial Interface clock pair negative signal
3			GND	GND	P	Ground
4	E3	CSI_D0P	CSI_DATA0_P	2V5	I	MIPI Camera Serial Interface data pair 0 positive signal
5	E4	CSI_D0M	CSI_DATA0_M	2V5	I	MIPI Camera Serial Interface data pair 0 negative signal
6			GND	GND	P	Ground
7	D2	CSI_D1P	CSI_DATA1_P	2V5	I	MIPI Camera Serial Interface data pair 1 positive signal
8	D1	CSI_D1M	CSI_DATA1_M	2V5	I	MIPI Camera Serial Interface data pair 1 negative signal
9			GND	GND	P	Ground
10	E2	CSI_D2P	CSI_DATA2_P	2V5	I	MIPI Camera Serial Interface data pair 2 positive signal

Pin #	i.MX6 BALL	PAD NAME	Signal	V	I/O	Description
11	E1	CSI_D2M	CSI_DATA2_M	2V5	I	MIPI Camera Serial Interface data pair 2 negative signal
12			GND	GND	P	Ground
13	F1	CSI_D3P	CSI_DATA3_P	2V5	I	MIPI Camera Serial Interface data pair 3 positive signal
14	F2	CSI_D3M	CSI_DATA3_M	2V5	I	MIPI Camera Serial Interface data pair 3 negative signal
15			GND	GND	P	Ground
16	H1	DSI_D1P	DSI_DATA1_P		O	MIPI Display Serial Interface data pair 1 positive signal
17	H2	DSI_D1M	DSI_DATA1_M		O	MIPI Camera Serial Interface data pair 1 negative signal
18			GND	GND	P	Ground
19	G1	DSI_D0P	DSI_DATA0_P	2V5	O	MIPI Display Serial Interface data pair 0 positive signal
20	G2	DSI_D0M	DSI_DATA0_M	2V5	O	MIPI Camera Serial Interface data pair 0 negative signal
21			GND	GND	P	Ground
22	H4	DSI_CLK0P	DSI_CLK0_P	2V5	O	MIPI Display Serial Interface clock pair positive signal
23	H3	DSI_CLK0M	DSI_CLK0_M	2V5	O	MIPI Camera Serial Interface clock pair negative signal
24			GND	GND	P	Ground
25	U5	KEY_COL3	I2C2_SCL	3V3	I/O	I^2C bus clock line
26	T7	KEY_ROW3	I2C2_SDA	3V3	I/O	I^2C bus data line
27				3V3	P	Power Supply 3.3VDC
28				3V3	P	Power Supply 3.3VDC
29	R7	GPIO_3	GPIO1_IO03	3V3	I/O	General Purpose Input Output
30	T3	GPIO_6	GPIO1_IO06	3V3	I/O	General Purpose Input Output
31	R5	GPIO_8	GPIO1_IO08	3V3	I/O	General Purpose Input Output
32			VCC	5V	P	Power Supply 5VDC ± 5%
33			VCC	5V	P	Power Supply 5VDC ± 5%

NOTE: MIPI Camera Serial Interface data pair 2 and data pair 3 are NOT available on the i.MX6 Solo and i.MX6 Duallite processor.

2.8 JTAG Connector

The EDM1-IMX6 JTAG interface is derived from the i.MX6 processor integrated SJC module.

The SJC module implements and manages the daisy-chained topology consisting of its' own TAP and those of the SDMA, and the ARM Debug Access Port (DAP).

The SJC supports the following main features:

- IEEE P1149.1, 1149.6 (standard JTAG) interface to off-chip test and development equipment
- Debug-related control and status

For additional details, please refer to the SJC chapter of the "i.MX6 Reference Manual".

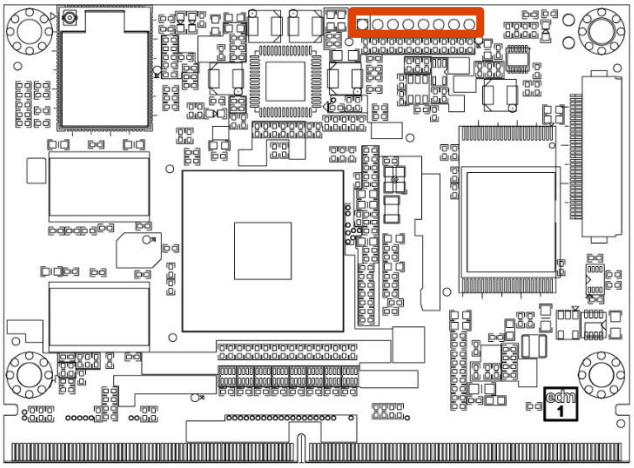


Table 9 - JTAG Expansion Header Signal Description

Pin #	i.MX6 BALL	Signal	V	I/O	Description
1		3.3V	3.3V	P	Power Supply 3.3VDC
2	C2	JTAG_nTRST		I	Test Reset (TRST). This is used to asynchronously initialize the test controller. The TRST pin has an internal pull-up resistor
3	C3	JTAG_TMS		I	Test Mode Select (TMS). This is used to sequence the test controller's state machine. TMS is sampled on the rising edge of TCK and includes an internal pull-up resistor
4	G5	JTAG_TDI		I	Test Data Input (TDI). Serial test instruction and data are received through the test data input (TDI) pin. TDI is sampled on the rising edge of TCK and includes an internal pull-up resistor
5	G6	JTAG_TDO		O	Test Data Output (TDO). The serial output for test instructions and data. TDO is tri-stat able and is actively driven in the shift-IR and shift-DR controller states. TDO changes on the falling edge of TCK
6	C11	JTAG_nSRST		I	System Reset (SRST). This is used to asynchronously initialize the test controller. The SRST pin has an internal pull-up resistor

7	H5	JTAG_TCK		I	Test Clock (TCK). This is used to synchronize the test logic and includes an internal pull-up resistor
8		GND	GND	P	Ground

3. EDM Type 1 Connector Interfaces

3.1 Gigabit Ethernet

The EDM1-IMX6 gigabit Ethernet Media Access Controller (MAC) is designed to support 10/100/1000 Mbps Ethernet/IEEE 802.3 networks.

Table 10 - EDM Gigabit Ethernet Signal Description

EDM Pin	Signal	V	I/O	Description
E3_2	GBE_MDI2+	LAN	I/O	Gigabit Ethernet Media Dependent Interface (MDI) differential pair 2 positive signal
E4_2	GBE_MDI0+	LAN	I/O	Gigabit Ethernet Media Dependent Interface (MDI) differential pair 0 positive signal
E3_3	GBE_MDI2-	LAN	I/O	Gigabit Ethernet Media Dependent Interface (MDI) differential pair 2 negative signal
E4_3	GBE_MDI0-	LAN	I/O	Gigabit Ethernet Media Dependent Interface (MDI) differential pair 0 negative signal
E3_5	GBE_MDI3+	LAN	I/O	Gigabit Ethernet Media Dependent Interface (MDI) differential pair 3 positive signal
E4_5	GBE_MDI1+	LAN	I/O	Gigabit Ethernet Media Dependent Interface (MDI) differential pair 1 positive signal
E3_6	GBE_MDI3-	LAN	I/O	Gigabit Ethernet Media Dependent Interface (MDI) differential pair 3 negative signal
E4_6	GBE_MDI1-	LAN	I/O	Gigabit Ethernet Media Dependent Interface (MDI) differential pair 1 negative signal
E3_7	LED1_ACT	3V3	O	Gigabit Ethernet LED Activity indicator
E4_8	LED1_nLink100	3V3	O	Gigabit Ethernet 100Mbit/sec LED link indicator
E4_9	LED1_nLink1000	3V3	O	Gigabit Ethernet 1000Mbit/sec LED link indicator

3.2. LVDS Interface

The EDM1-IMX6 is equipped with single LVDS Display interfaces. The LVDS Display Bridge (LDB) connects the IPU (Image Processing Unit) to an External LVDS Display Interface. The purpose of the LDB is to support flow of synchronous RGB data from the IPU to external display devices through LVDS interface.

The LDB output complies with the EIA-644-A standard and supports the following features:

- Connectivity to relevant devices - Displays with LVDS receivers.
- Arranging the data as required by the external display receiver and by LVDS display standards.
- Synchronization and control capabilities.
- Data input interface (inside the i.MX6 processor)
    - RGB Data of 18 or 24 bits
    - Pixel clock
    - Control signals: HSYNC, VSYNC, DE, and 1 additional optional general purpose control (I^2C)
- Single channel output data output interface
    - Total of up to 28 bits per data interface are transferred per pixel clock cycle.
- Data Rates
    - Overall: LDB supports rates needed by WUXGA 16:10 aspect ratio (1920 x 1200 @ 60 frames per second, data rate supported up to 170 MHz)
    - For single input data interface case: Up to 170 MHz pixel clock (WUXGA 1920x1200)
    - For dual input data interface case: Up to 85 MHz per interface. (WXGA 1366x768 @ 60 frames per second, 35% blanking).

For additional details, please refer to the “LVDS Display Bridge (LDB)” chapter of the “i.MX6 Reference Manual”.

Table 11 - LVDS Signal Description

EDM PIN	i.MX6 BALL	PAD NAME	Signal	V	I/O	Description
E3_9	U2	LVDS0_TX0_N	LVDS0_DATA0_N	2V5	O	LVDS primary channel differential pair 0 negative signal
E3_10	U1	LVDS0_TX0_P	LVDS0_DATA0_P	2V5	O	LVDS primary channel differential pair 0 positive signal
3	U4	LVDS0_TX1_N	LVDS0_DATA1_N	2V5	O	LVDS primary channel differential pair 1 negative signal
5	U3	LVDS0_TX1_P	LVDS0_DATA1_P	2V5	O	LVDS primary channel differential pair 1 positive signal
9	V2	LVDS0_TX2_N	LVDS0_DATA2_N	2V5	O	LVDS primary channel differential pair 2 negative signal
11	V1	LVDS0_TX2_P	LVDS0_DATA2_P	2V5	O	LVDS primary channel differential pair 2 positive signal
15	W2	LVDS0_TX3_N	LVDS0_DATA3_N	2V5	O	LVDS primary channel differential pair 3 negative signal
17	W1	LVDS0_TX3_P	LVDS0_DATA3_P	2V5	O	LVDS primary channel differential pair 3 positive signal
21	V4	LVDS0_CLK_N	LVDS0_CLK_N	2V5	O	LVDS primary channel clock negative signal
23	V3	LVDS0_CLK_P	LVDS0_CLK_P	2V5	O	LVDS primary channel clock positive signal
27	B19	SD4_DAT1	PWM3_OUT	3V3	O	LVDS primary channel panel backlight control
29	D18	SD4_DAT0	GPIO2_IO08	3V3	O	LVDS primary channel panel backlight enable
31	L1	CSI0_DAT13	GPIO5_IO31	3V3	O	LVDS primary channel panel power enable

The following pins can be used for LVDS panel detection.

Table 12 - LVDS Panel Detection Pins

EDM PIN	i.MX6 BALL	PAD NAME	Signal	V	I/O	Description
37	G23	EIM_D28	I2C1_SDA	3V3	I/O	Display ID DDC data line used for LVDS flat panel detection. If not used this can be assigned to General Purpose I^2C bus
39	H20	EIM_D21	I2C1_SCL	3V3	I/O	

NOTE: The I^2C signals for LVDS panel control are fully documented in chapter 3.14. I^2C Bus of this hardware manual.

3.3. HDMI (High Definition Multi-Media Interface)

The HDMI interface available with EDM1-IMX6 is based on the “HDMI transmitter” & “HDMI 3D Tx PHY” integrated into the i.MX6 processor. The “HDMI transmitter” combines video/display data from the IPU, Audio data from i.MX6 memory & control/status data from the ARM complex, into TMDS data & clock channels. The “HDMI 3D TX PHY” transmits the combined data by means of 3 TMDS data pairs and a TMDS clock pair together with the DDC/I^2C configuration signals to the EDM connector.

The HDMI 3D TX PHY integrated into the i.MX6 processor supports the following standards & features:

- High-Definition Multimedia Interface Specification, Version 1.4a
- Digital Visual Interface, Revision 1.0
- HDMI Compliance Test Specification, Version 1.4a
- Support for up to 720p at 100Hz and 720i at 200Hz or 1080p at 60Hz and 1080i/720i at 120Hz HDTV display resolutions and up to QXGA graphic display resolutions.
- Support for 4k x 2k and 3D video formats
- Support for up to 16-bit Deep Color modes

For additional details, please refer to the “Multimedia” chapter of the “i.MX6 Reference Manual”.

Table 13 - HDMI Signal Description

EDM PIN	i.MX6 BALL	PAD NAME	Signal	V	I/O	Description
43	J6	HDMI_CLKP	HDMI_TX_CLK_P	3V3	O	HDMI differential pair clock positive signal
45	J5	HDMI_CLKM	HDMI_TX_CLK_N	3V3	O	HDMI differential pair clock negative signal
49	K6	HDMI_D0P	HDMI_TX_DATA0_P	3V3	O	HDMI differential pair 0 positive signal
51	K5	HDMI_D0M	HDMI_TX_DATA0_N	3V3	O	HDMI differential pair 0 negative signal
55	J4	HDMI_D1P	HDMI_TX_DATA1_P	3V3	O	HDMI differential pair 1 positive signal
57	J3	HDMI_D1M	HDMI_TX_DATA1_N	3V3	O	HDMI differential pair 1 negative signal
61	K4	HDMI_D2P	HDMI_TX_DATA2_P	3V3	O	HDMI differential pair 2 positive signal
63	K3	HDMI_D2M	HDMI_TX_DATA2_N	3V3	O	HDMI differential pair 2 negative signal
67	K1	HDMI_HPD	HDMI_TX_HPD	3V3	I	HDMI/DP Hot plug detection signal that serves as an interrupt request
71	H19	EIM_A25	HDMI_TX_CEC_LINE	1V8	I/O	HDMI Consumer Electronics Control
73	H20	EIM_D21	I2C1_SCL	5V	I/O	Display ID DDC data line used for HDMI detection. If not used this can be assigned to General Purpose I^2C bus clock line
75	G23	EIM_D28	I2C1_SDA	5V	I/O	Display ID DDC data line used for HDMI detection. If not used this can be assigned to General Purpose I^2C bus data line

3.4. Digital Display Sub-System (DSS) or TTL Interface

The Parallel Display interface of EDM1-IMX6 is derived directly from the DI0 port of the IPU, effectively bypassing all the i.MX6 integrated display bridges.

Each DI port supports the following:

- Compatible with MIPI-DPI standard.
- Supports BT.656 (8-bit) and BT.1120 (16-bit) protocols.
- Supports HDTV standards SMPTE274 (1080i/p) and SMPTE296 (720p)
- Scan Order: progressive or interlaced
- Synchronization:
- Programmable horizontal and vertical synchronization output signals
- Data enabling output signal
- The combined data rate for the two DI ports is up to 240 MP/sec
- Supported pixel data formats:
- RGB - color depth fully configurable; up to 8 bits/value (color component)
- YUV 4:2:2, 8 bits/value
- All mandatory formats in MIPI DBI, DPI and DSI

For examples of valid mappings, please refer to the “IPU Display Interface Signal Mapping” chapter of the i.MX6 datasheet.

For detailed information please refer to the “Bus Mapping Unit” chapter of the “i.MX6 Reference Manual” and “EDM Standard Specifications”.

Table 14 - TTL Display Signal Description

EDM PIN	i.MX6 BALL	PAD NAME	Signal	V	I/O	Description
2	P24	DISP0_DAT0	IPU1_DISP0_DATA00	3V3	O	LCD Pixel Data bit 0
4	P22	DISP0_DAT1	IPU1_DISP1_DATA01	3V3	O	LCD Pixel Data bit 1
8	P23	DISP0_DAT2	IPU1_DISP1_DATA02	3V3	O	LCD Pixel Data bit 2
10	P21	DISP0_DAT3	IPU1_DISP1_DATA03	3V3	O	LCD Pixel Data bit 3
14	P20	DISP0_DAT4	IPU1_DISP0_DATA04	3V3	O	LCD Pixel Data bit 4
16	R25	DISP0_DAT5	IPU1_DISP0_DATA05	3V3	O	LCD Pixel Data bit 5
20	R23	DISP0_DAT6	IPU1_DISP0_DATA06	3V3	O	LCD Pixel Data bit 6
22	R24	DISP0_DAT7	IPU1_DISP0_DATA07	3V3	O	LCD Pixel Data bit 7
26	R22	DISP0_DAT8	IPU1_DISP0_DATA08	3V3	O	LCD Pixel Data bit 8
28	T25	DISP0_DAT9	IPU1_DISP0_DATA09	3V3	O	LCD Pixel Data bit 9
32	R21	DISP0_DAT10	IPU1_DISP0_DATA10	3V3	O	LCD Pixel Data bit 10
34	T23	DISP0_DAT11	IPU1_DISP0_DATA11	3V3	O	LCD Pixel Data bit 11
36	T24	DISP0_DAT12	IPU1_DISP0_DATA12	3V3	O	LCD Pixel Data bit 12
38	R20	DISP0_DAT13	IPU1_DISP0_DATA13	3V3	O	LCD Pixel Data bit 13
40	U25	DISP0_DAT14	IPU1_DISP0_DATA14	3V3	O	LCD Pixel Data bit 14
44	T22	DISP0_DAT15	IPU1_DISP0_DATA15	3V3	O	LCD Pixel Data bit 15
46	T21	DISP0_DAT16	IPU1_DISP0_DATA16	3V3	O	LCD Pixel Data bit 16
50	U24	DISP0_DAT17	IPU1_DISP0_DATA17	3V3	O	LCD Pixel Data bit 17
52	V25	DISP0_DAT18	IPU1_DISP0_DATA18	3V3	O	LCD Pixel Data bit 18
56	U23	DISP0_DAT19	IPU1_DISP0_DATA19	3V3	O	LCD Pixel Data bit 19
58	U22	DISP0_DAT20	IPU1_DISP0_DATA20	3V3	O	LCD Pixel Data bit 20
62	T20	DISP0_DAT21	IPU1_DISP0_DATA21	3V3	O	LCD Pixel Data bit 21
64	V24	DISP0_DAT22	IPU1_DISP0_DATA22	3V3	O	LCD Pixel Data bit 22
68	W24	DISP0_DAT23	IPU1_DISP0_DATA23	3V3	O	LCD Pixel Data bit 23
70	N19	DI0_DISP_CLK	IPU1_DI0_DISP_CLK	3V3	O	LCD Pixel Clock
72	N25	DI0_PIN2	IPU1_DI0_PIN02	3V3	O	LCD Horizontal Synchronization
74	N20	DI0_PIN3	IPU1_DI0_PIN03	3V3	O	LCD Vertical Synchronization
76	P25	DI0_PIN4	IPU1_DI0_PIN04	3V3	O	LCD backlight enable/disable
78	N21	DI0_PIN15	IPU1_DI0_PIN15	3V3	O	LCD dot enable pin signal
80	A20	SD4_DAT3	GPIO2_IO11	3V3	O	LCD Voltage On
82	F17	SD4_DAT2	PWM4_OUT	3V3	O	LCD Backlight brightness Control

3.5. Audio Interface

The EDM1-IMX6 incorporates two I^2S / AUDMUX signals, one S/P DIF interface and can as well provide surround audio over the HDMI data signals.

The AUDMUX provides flexible, programmable routing of the serial interfaces (SSI1 or SSI2) to and from off-chip devices. The AUDMUX routes audio data (and even splices together multiple time-multiplexed audio streams) but does not decode or process audio data itself. The AUDMUX is controlled by the ARM but can route data even when the ARM is in a low-power mode.

The ESAI (Enhanced Serial Audio Interface) provides a full-duplex serial port for serial communication with a variety of serial devices, including industry-standard codecs, SPDIF transceivers, and other processors. The ESAI consists of independent transmitter and receiver sections, each section with its own clock generator. The ESAI is connected to the IOMUX and to the ESAI_BIFIFO module.

The ESAI_BIFIFO (ESAI Bus Interface and FIFO) is the interface between the ESAI module and the shared peripheral bus. It contains the FIFOs used to buffer data to and from the ESAI, as well as providing the data word alignment and padding necessary to match the 24-bit data bus of the ESAI to the 32-bit data bus of the shared peripheral bus.

The SPDIF (Sony/Philips Digital Interface) audio module is a stereo transceiver that allows the processor to receive and transmit digital audio over it. The SPDIF receiver section includes a frequency measurement block that allows the precise measurement of incoming sampling frequency. A recovered clock is provided by the SPDIF receiver section and may be used to drive both internal and external components in the system. The SPDIF is connected to the shared peripheral bus.

The ASRC (Asynchronous Sample Rate Converter) converts the sampling rate of a signal associated to an input clock into a signal associated to a different output clock. The ASRC supports concurrent sample rate conversions of up to 10 channels of over 120dB THD+N. The sample rate conversion of each channel is associated to a pair of incoming and outgoing sampling rates. The ASRC supports up to three sampling rate pairs. The ASRC is connected to the shared peripheral bus.

Key features of the audio signal block include:

- Full 6-wire SSI interfaces for asynchronous receive and transmit
- Configurable 4-wire (synchronous) or 6-wire (asynchronous) peripheral interfaces
- Independent Tx/Rx frame sync and clock direction selection for host or peripheral
- Each host interface's capability to connect to any other host or peripheral interface in a point-to-point or point-to-multipoint (network mode)
- Transmit and receive data switching to support external network mode

Table 15 - Primary I²S Audio Signal Description

EDM PIN	i.MX6 BALL	PAD NAME	Signal	V	I/O	Description
187	N3	CSI0_DAT7	AUD3_RXD	3V3	I	Primary Integrated Interchip Sound (I²S) channel receive data line
189	N4	CSI0_DAT6	AUD3_TXFS	3V3	O	Primary Integrated Interchip Sound (I²S) channel frame synchronization signal
191	P2	CSI0_DAT5	AUD3_TXD	3V3	O	Primary Integrated Interchip Sound (I²S) channel transmit data line
193	N1	CSI0_DAT4	AUD3_TXC	3V3	O	Primary Integrated Interchip Sound (I²S) channel word clock signal
195	T5	GPIO_0	CCM_CLKO1	3V3	O	Primary Integrated Interchip Sound (I²S) channel master clock signal

Table 16 - Secondary I²S Audio Signal Description

EDM PIN	i.MX6 BALL	PAD NAME	Signal	V	I/O	Description
186	U6	KEY_ROW1	AUD5_RXD	3V3	I	Secondary Integrated Interchip Sound (I²S) channel receive data line
188	U7	KEY_COL1	AUD5_TXFS	3V3	O	Secondary Integrated Interchip Sound (I²S) channel frame synchronization signal
190	V6	KEY_ROW0	AUD5_TXD	3V3	O	Secondary Integrated Interchip Sound (I²S) channel transmit data line
192	W5	KEY_COL0	AUD5_TXC	3V3	O	Secondary Integrated Interchip Sound (I²S) channel word clock signal
194	T5	GPIO_0	CCM_CLKO1	3V3	O	Secondary Integrated Interchip Sound (I²S) channel master clock signal

NOTE: On EDM1-IMX6 System-on-Modules that feature WiFi / Bluetooth functionality. The Secondary I²S is routed to the onboard WiFi chip.

3.5.1. S/P DIF Audio

S/P DIF (Sony/Philips Digital Interconnect Format) is a type of digital audio interconnects cable used in consumer audio equipment to output audio over reasonably short distances. The signal is transmitted over either a coaxial cable with RCA connectors or a fibre optic cable with TOSLINK connectors. S/P DIF is based on the professional AES3 interconnect standard. S/P DIF can carry two channels of PCM audio or a multi-channel compressed surround sound format such as Dolby Digital or DTS.

The EDM1-IMX6 features an S/P DIF interface allowing EDM module to transmit digital audio data. The S/PDIF interface is implemented by means of the i.MX6 integrated S/P DIF transceiver.

For additional details, please refer to “Sony/Philips Digital Interface (SPDIF)” Chapter of the “i.MX6 Reference Manual”.

Table 17 - S/P DIF Audio Signal Description

EDM PIN	i.MX6 BALL	PAD NAME	Signal	V	I/O	Description
196	W21	ENET_RXD0	SPDIF_OUT	SPDIF	O	Sony / Philips Digital Interconnect Format Audio output

3.6. PCI Express

The EDM1-IMX6 is equipped with a single lane PCI Express interface, implemented in the i.MX6 processor.

The PCI Express interface complies with PCIe specification Gen 2.0 and supports the PCI Express 1.1/2.0 standards. The PCI Express module is a dual mode complex, supporting root complex operations and endpoint operations.

PCI Express PHY Features

- 5 Gbps data transmission rate
- Integrated PHY includes transmitter, receiver, PLL, digital core, and ESD.
- Programmable RX equalization
- Designed for excellent performance margin and receiver sensitivity
- Robust PHY architecture tolerates wide process, voltage and temperature variations
- Low-jitter PLL technology with excellent supply isolation
- IEEE 1149.6 (JTAG) boundary scan
- Built-in Self-Test (BIST) features for production, at-speed, testing on any digital tester
- 5Gb/s PCIe Gen 2 and 2.5Gb/s PCIe Gen 1.1 test modes supported
- Advanced built-in diagnostics including on-chip sampling scope for easy debug
- Visibility & controllability of hard macro functionality thru programmable registers in the design
- Over-rides on all ASIC side inputs for easy debug
- Access register space thru simple 16 bit parallel interface
- Access register space thru JTAG

For additional details, please refer to the “PCI Express (PCIe)” chapter of the “i.MX6 Reference Manual”.

Table 18 - PCI Express Signal Description

EDM PIN	i.MX6 BALL	PAD NAME	Signal	V	I/O	Description
85	D7	CLK1_P	XTALOSC_CLK1_P	2V5	O	PCI Express channel A clock differential pair positive signal
87	C7	CLK1_N	XTALOSC_CLK1_N	2V5	O	PCI Express channel A clock differential pair negative signal
91	B3	PCIE_TXP	PCIE_TX_P	2V5	O	PCI Express channel A Transmit output differential pair positive signal
93	A3	PCIE_TXM	PCIE_TX_N	2V5	O	PCI Express channel A Transmit output differential pair negative signal
97	B2	PCIE_RXP	PCIE_RX_P	2V5	I	PCI Express channel A Receive input differential pair positive signal
99	B1	PCIE_RXM	PCIE_RX_N	2V5	I	PCI Express channel A Receive input differential pair negative signal
119	H21	EIM_D31	GPIO3_IO31	3V3	O	PCI Express Reset signal for external devices

NOTE: The PCIE_RX pair has decoupling capacitors on the EDM module valued 10nF

3.7. Serial ATA Interface

The EDM-IMX6 incorporates a single SATA-II port implemented with the NXP i.MX6 integrated SATA controller and PHY.

The interface supports the following main features:

- The SATA block fully complies with AHCI specification version 1.10 and partially complies with AHCI specification version 1.3 (FIS-based switching is currently not supported).
- SATA 1.5 Gb/s and SATA 3.0 Gb/s speed.
- Power management features including automatic partial-to-slumber transition.
- eSATA (external analog logic also needs to support eSATA).
- Hardware-assisted Native Command Queuing (NCQ) for up to 32 entries.

For additional details, please refer to the “Serial Advanced Technology Attachment Controller (SATA)” chapter of the “i.MX6 Reference Manual”.

Table 19 - Serial ATA Signal Description

EDM PIN	i.MX6 BALL	PAD NAME	Signal	V	I/O	Description
123	B14	SATA_RXP	SATA_PHY_RX_P	2V5	I	Serial ATA channel 1 Receive differential pair positive signal
125	A14	SATA_RXM	SATA_PHY_RX_N	2V5	I	Serial ATA channel 1 Receive differential pair negative signal
133	M5	CSI0_DAT15	GPIO6_IO01	SATA	I/O	Serial ATA LED. Open collector output pin driven during SATA command activity
135	A12	SATA_TXP	SATA_PHY_TX_P	2V5	O	Serial ATA channel 1 Transmit differential pair positive signal
137	B12	SATA_TXM	SATA_PHY_TX_N	2V5	O	Serial ATA channel 1 Transmit differential pair negative signal

NOTE: SATA is not available on configurations that utilize the i.MX6 Solo and i.MX6 Duallite processor.

3.8. Universal Serial Bus (USB) Interface

The EDM-IMX6 incorporates a single USB Host controller and an additional USB Host/OTG controller.

Each of the USB controllers provides the following main features:
USB 2.0 Host/OTG Controller

- High-Speed/Full-Speed/Low-Speed OTG core
- HS/FS/LS UTMI compliant interface
- High Speed, Full Speed and Low Speed operation in Host mode (with UTMI transceiver)
- High Speed, and Full Speed operation in Peripheral mode (with UTMI transceiver)
- Hardware support for OTG signaling, session request protocol, and host negotiation protocol
- Up to 8 bidirectional endpoints
- Support charger detection

USB 2.0 Host Controller

- High-Speed/Full-Speed/Low-Speed Host-Only core
- HS/FS/LS UTMI compliant interface

For additional details, please refer to the “Universal Serial Bus Controller (USB)” chapter of the “i.MX6 Reference Manual”.

Table 20 - USB Host Signal Description

EDM PIN	i.MX6 BALL	PAD NAME	Signal	V	I/O	Description
139	R1	GPIO_17	GPIO7_IO12	USB	O	Universal Serial Bus carrier board hub reset pin
165	J20	EIM_D30	USB_H1_OC	3V3	I	Over current detect input pin to monitor USB power over current
179	F10	USB_H1_DN	USB_H1_DN	3V3	I/O	Universal Serial Bus differential pair negative signal
181	E10	USB_H1_DP	USB_H1_DP	3V3	I/O	Universal Serial Bus differential pair positive signal
183	D10	USB_H1_VBUS	USB_H1_VBUS	5V	I/O	Universal Serial Bus power

Table 21 - USB OTG Signal Description

EDM PIN	i.MX6 BALL	PAD NAME	Signal	V	I/O	Description
141	T2	GPIO_9	GPIO1_IO09	3V3	I	Over current detect input pin to monitor USB power over current
155	T4	GPIO_1	USB_OTG_ID	3V3	I	Universal Serial Bus On-The-Go detection signal
157	A6	USB_OTG_DP	USB_OTG_DP	3V3	I/O	Universal Serial Bus differential pair positive signal
159	B6	USB_OTG_DN	USB_OTG_DN	3V3	I/O	Universal Serial Bus differential pair negative signal
161	E9	USB_OTG_ VBUS	USB_OTG_ VBUS	5V	I/O	Universal Serial Bus power
163	E23	EIM_D22	USB_OTG_PWR	USB	O	Universal Serial Bus power enable

NOTE: While using USB OTG in USB HOST mode. The USB2_OTG_ID pin (EDM pin 155) should have a pull-down resistor to GND.

3.9. SDIO/MMC Interface

The EDM1-IMX6 features a MMC / SD / SDIO host interfaces connected to the NXP i.MX6 integrated "Ultra Secured Digital Host Controller" (uSDHC).

The following main features are supported by uSDHC:

- Compatible with the MMC System Specification version 4.2/4.3/4.4/4.5.
- Conforms to the SD Host Controller Standard Specification version 3.0.
- Compatible with the SD Memory Card Specification version 3.0 and supports the "Extended Capacity SD Memory Card".
- Compatible with the SDIO Card Specification version 3.0.
- Supports 1-bit / 4-bit SD and SDIO modes, 1-bit / 4-bit

The MMC/SD/SDIO host controller can support a single MMC / SD / SDIO card or device.

For additional details, please refer to the "Ultra Secured Digital Host Controller (uSDHC)" chapter of the "i.MX6 Reference Manual".

Table 22 - SDIO/MMC Interface Signal Description

EDM PIN	i.MX6 BALL	PAD NAME	Signal	V	I/O	Description
203	T1	GPIO_2	GPIO1_IO02	3V3	I/O	MMC/SDIO Card Detect
205	B21	SD1_CMD	SD1_CMD	3V3	I/O	MMC/SDIO Command
206	D20	SD1_CLK	SD1_CLK	3V3	O	MMC/SDIO Clock
207	N6	CSI0_DAT8	GPIO5_IO26	3V3	I/O	MMC/SDIO Write Protect
208	P4	CSI0_MCLK	GPIO5_IO19	3V3	O	MMC/SDIO LED
209	C20	SD1_DAT1	SD1_DATA1	3V3	I/O	MMC/SDIO Data bit 1
210	P1	CSI0_PIXCLK	GPIO5_IO18	3V3	O	MMC/SDIO Power Enable
211	F18	SD1_DAT3	SD1_DATA3	3V3	I/O	MMC/SDIO Data bit 3
212	A21	SD1_DAT0	SD1_DATA0	3V3	I/O	MMC/SDIO Data bit 0
214	E19	SD1_DAT2	SD1_DATA2	3V3	I/O	MMC/SDIO Data bit 2

3.10. General Purpose Memory Controller Bus (Local Bus)

The EDM1-IMX6 features a general-purpose media interface which is connected to the NXP i.MX6 GPMI controller.

The general-purpose media interface has several features to efficiently support NAND:

- Individual chip select pins and ganged ready/busy pin for up to four NANDs.
- Individual state machine and DMA channel for each chip select.
- Special command modes work with DMA controller to perform all normal NAND functions without CPU intervention.
- Configurable timing based on a dedicated clock allows optimal balance of high NAND performance and low system power.

GPMI and DMA have been designed to handle complex multi-page operations without CPU intervention. The DMA uses a linked descriptor function with branching capability to automatically handle all of the operations needed to read/write multiple pages:

- Data/Register Read/Write-The GPMI can be programmed to read or write multiple cycles to the NAND address, command or data registers.
- Wait for NAND Ready-The GPMI's Wait-for-Ready mode can monitor the ready/ busy signal of a single NAND flash and signal the DMA when the device has become ready. It also has a time-out counter and can indicate to the DMA that a time-out error has occurred. The DMAs can conditionally branch to a different descriptor in the case of an error.
- Check Status-The Read-and-Compare mode allows the GPMI to check NAND status against a reference. If an error is found, the GPMI can instruct the DMA to branch to an alternate descriptor, which attempts to fix the problem or asserts a CPU IRQ.

For additional details, please refer to the “General Purpose Media Interface (GPMI)” chapter of the “i.MX6 Reference Manual”.

Table 23 - GPMC / Local Bus Signal Description

EDM PIN	i.MX6 BALL	PAD NAME	Signal	V	I/O	Description
86	F15	NANDF_CS0	NAND_CE0_B	3V3	O	GPMC Chip Select bit A
90	C16	NANDF_CS1	NAND_CE1_B	3V3	O	GPMC Chip Select bit B
92	A17	NANDF_CS2	NAND_CE2_B	3V3	O	GPMC Chip Select bit C
96	D16	NANDF_CS3	NAND_CE3_B	3V3	O	GPMC Chip Select bit D
102	B16	NANDF_RB0	NAND_READY_B	3V3	I	External indication of wait
104	E15	NANDF_WP_B	NAND_WP_B	3V3	O	GPMC Write Protect / Enable
106	C15	NANDF_CLE	NAND_CLE	3V3	O	GPMC Lower Byte Enable. Also used for Command Latch Enable
108	A16	NANDF_ALE	NAND_ALE	3V3	O	GPMC Address Valid or Address Latch Enable
110	E16	SD4_CLK	NAND_WE_B	3V3	I	GPMC Write Enable
112	B17	SD4_CMD	NAND_RE_B	3V3	O	GPMC Read Enable
168	C18	NANDF_D7	NAND_DATA07	3V3	I/O	GPMC data bit 7
170	E17	NANDF_D6	NAND_DATA06	3V3	I/O	GPMC data bit 6
172	B18	NANDF_D5	NAND_DATA05	3V3	I/O	GPMC data bit 5
174	A19	NANDF_D4	NAND_DATA04	3V3	I/O	GPMC data bit 4
176	D17	NANDF_D3	NAND_DATA03	3V3	I/O	GPMC data bit 3
178	F16	NANDF_D2	NAND_DATA02	3V3	I/O	GPMC data bit 2
180	C17	NANDF_D1	NAND_DATA01	3V3	I/O	GPMC data bit 1
182	A18	NANDF_D0	NAND_DATA00	3V3	I/O	GPMC data bit 0

NOTE: On configurations where the NAND Flash IC is mounted instead of eMMC, EDM PIN# 86 is left un-connected.

3.11. CAN BUS Interface signals

The EDM1-IMX6 features two CAN bus interfaces. The CAN bus interfaces are implemented with the i.MX6 on chip “Flexible Controller Area Network” (FlexCAN) communication modules.

FlexCAN supports the following main features:

- Compliant with the CAN 2.0B protocol specification
- Programmable bit rate up to 1 Mb/sec

Integration of a CAN Bus transceiver and optional galvanic isolation should be incorporated on the EDM carrier board.

For additional details, please refer to the “Flexible Controller Area Network (FLEXCAN)” chapter of the “i.MX6 Reference Manual”.

Table 24 - Primary CAN Bus Signal Description

EDM PIN	i.MX6 BALL	PAD NAME	Signal	V	I/O	Description
200	W6	KEY_COL2	FLEXCAN1_TX	3V3	I/O	Primary CAN (controller Area Network) transmit signal
202	W4	KEY_ROW2	FLEXCAN1_RX	3V3	I/O	Primary CAN (controller Area Network) receive signal

Table 25 - Secondary CAN Bus Signal Description

EDM PIN	i.MX6 BALL	PAD NAME	Signal	V	I/O	Description
197	T6	KEY_COL4	FLEXCAN2_TX	3V3	I/O	Secondary CAN (controller Area Network) transmit signal
199	V5	KEY_ROW4	FLEXCAN2_RX	3V3	I/O	Secondary CAN (controller Area Network) receive signal

3.12. Universal Asynchronous Receiver/Transmitter (UART) Interface

The EDM1-IMX6 makes 2 UART ports available on the EDM connector and utilizes an additional UART on the module to connect to the WiFi/Bluetooth module.

The i.MX6 processor integrated UARTs support the following features:

- High-speed TIA/EIA-232-F compatible, up to 5.0 Mbit/s.
- Serial IR interface low-speed, IrDA-compatible (up to 115.2 Kbit/s).
- 9-bit or Multidrop mode (RS-485) support (automatic slave address detection).
- 7 or 8 data bits for RS-232 characters or 9 bit RS-485 format, 1 or 2 stop bits.
- Programmable parity (even, odd, and no parity).
- Hardware flow control support for request to send (RTS) and clear to send (CTS) signals
- RXD input and TXD output can be inverted respectively in RS-232/RS-485 mode
- RS-485 driver direction control via CTS signal
- Auto baud rate detection (up to 115.2 Kbit/s)
- Two independent, 32-entry FIFOs for transmit and receive

For additional details, please refer to the “Universal Asynchronous Receiver/Transmitter (UART)” chapter of the “i.MX6 Reference Manual”.

Table 26 - Primary UART Signal Description

EDM PIN	i.MX6 BALL	PAD NAME	Signal	V	I/O	Description
241	G21	EIM_D19	UART1_CTS_B	3V3	O	Universal Asynchronous Receive Transmit secondary channel clear to send signal
243	M1	CSI0_DAT10	UART1_TX_DATA	3V3	O	Universal Asynchronous Receive Transmit secondary channel transmit data signal
245	M3	CSI0_DAT11	UART1_RX_DATA	3V3	I	Universal Asynchronous Receive Transmit secondary channel receive data signal
247	G20	EIM_D20	UART1_RTS_B	3V3	O	Universal Asynchronous Receive Transmit secondary channel request to send signal

NOTE: it is recommended to use the UART1 interface as system debug where possible and use the UART2 signals in applications where one serial port is required.

Table 27 - Secondary UART Signal Description

EDM PIN	i.MX6 BALL	PAD NAME	Signal	V	I/O	Description
234	B20	SD4_DAT6	UART2_CTS_B	3V3	O	Universal Asynchronous Receive Transmit secondary channel clear to send signal
236	D19	SD4_DAT7	UART2_TX_DATA	3V3	O	Universal Asynchronous Receive Transmit secondary channel transmit data signal
238	E18	SD4_DAT4	UART2_RX_DATA	3V3	I	Universal Asynchronous Receive Transmit secondary channel receive data signal
240	C19	SD4_DAT5	UART2_RTS_B	3V3	O	Universal Asynchronous Receive Transmit secondary channel request to send signal

NOTE: UART3 is not listed in this section. This interface is connected from the i.MX6 processor towards the WiFi/Bluetooth interface present on EDM1-IMX6 and can be found in the WiFi/Bluetooth section of this manual.

3.13. Serial Peripheral Interface (SPI)

The EDM1-IMX6 features two Enhanced Configurable SPI ports, which are derived from the i.MX6 processor, integrated ECSPI IPs.

The following main features are supported:

- Full-duplex synchronous serial interface
- Master/Slave configurable
- Transfer continuation function allows unlimited length data transfers
- 32-bit wide by 64-entry FIFO for both transmit and receive data
- 32-bit wide by 16-entry FIFO for HT message data
- Polarity and phase of the Chip Select (SS) and SPI Clock (SCLK) are configurable Direct Memory Access (DMA) support

For additional details, please refer to the “Enhanced Configurable SPI (ECSPI)” chapter of the “i.MX6 Reference Manual”.

Table 28 - Primary SPI Channel Signal Description

EDM PIN	i.MX6 BALL	PAD NAME	Signal	V	I/O	Description
219	J23	EIM_CS1	ECSPI2_MOSI	3V3	O	Serial Peripheral Interface primary channel master output slave input signal
221	J24	EIM_OE	ECSPI2_MISO	3V3	I	Serial Peripheral Interface primary channel master input slave output signal
223	H24	EIM_CS0	ECSPI2_SCLK	3V3	O	Serial Peripheral Interface primary channel clock signal
225	K20	EIM_RW	ECSPI2_SS0	3V3	O	Serial Peripheral Interface primary channel Chip Select 0 signal
227	K22	EIM_LBA	ECSPI2_SS1	3V3	O	Serial Peripheral Interface primary channel Chip Select 1 signal. Do not use if only 1 SPI device is used

Table 29 - Secondary SPI Channel Signal Description

EDM PIN	i.MX6 BALL	PAD NAME	Signal	V	I/O	Description
222	D24	EIM_D18	ECSPI1_MOSI	3V3	O	Serial Peripheral Interface secondary channel master output slave input signal
224	F21	EIM_D17	ECSPI1_MISO	3V3	I	Serial Peripheral Interface secondary channel master input slave output signal
226	C25	EIM_D16	ECSPI1_SCLK	3V3	O	Serial Peripheral Interface secondary channel clock signal
228	E22	EIM_EB2	ECSPI1_SS0	3V3	O	Serial Peripheral Interface secondary channel Chip Select 0 signal
230	U21	ENET_CRS_DV	GPIO1_IO25	3V3	O	Serial Peripheral Interface secondary channel Chip Select 1 signal. Do not use if only 1 SPI device is used

3.14. I²C Bus

The EDM1-IMX6 I²C interfaces are implemented with the i.MX6 integrated I²C controller. There are two general purpose I²C interfaces and one I²C interface dedicated towards display and system management functions.

The following features are supported:

- Compliance with Philips I²C specification version 2.1
- Multiple-master operation
- Support for standard mode (up to 100K bits/s) and fast mode (up to 400K bits/s)
- Arbitration-lost interrupt with automatic mode switching from master to slave

For additional details, please refer to the “I2C Controller (I2C)” chapter of the “i.MX6 Reference Manual”.

3.14.1. Display and System Management Purpose I²C Bus

The I²C interface that manages display and system management functions is available at two instances.

Table 30 - Display and System Management Purpose I²C Bus Signal Description

EDM PIN	i.MX6 BALL	PAD NAME	Signal	V	I/O	Description
73	H20	EIM_D21	I2C1_SCL	5V	I/O	Display ID DDC data line used for HDMI detection. If not used this can be assigned to General Purpose I²C bus clock line
75	G23	EIM_D28	I2C1_SDA	5V	I/O	Display ID DDC data line used for HDMI detection. If not used this can be assigned to General Purpose I²C bus data line

NOTE: The 5.0V I²C signals are normally connected towards the external HDMI display interface and should not be connected to other parts of the system on an EDM carrier board if possible.

NOTE: The 5.0V I²C signals have an TX0102DCUR voltage level shift incorporated.

EDM PIN	i.MX6 BALL	PAD NAME	Signal	V	I/O	Description
37	G23	EIM_D28	I2C1_SDA	3V3	I/O	Display ID DDC data line used for LVDS flat panel detection. If not used this can be assigned to General Purpose I²C bus data line
39	H20	EIM_D21	I2C1_SCL	3V3	I/O	Display ID DDC clock line used for LVDS flat panel detection. If not used this can be assigned to General Purpose I²C bus clock line

NOTE: The 3.3V I²C signals are normally connected towards the LVDS display interface and smart battery solutions and should not be connected to other parts of the system on an EDM carrier board if possible.

3.14.2. General Purpose I²C Bus

The general purpose I²C interfaces are both independent and have no reserved addresses or devices on the EDM1-IMX6.

Table 31 – Primary General Purpose I²C Bus Signal Description

EDM PIN	i.MX6 BALL	PAD NAME	Signal	V	I/O	Description
231	U5	KEY_COL3	I2C2_SCL	3V3	I/O	I²C bus clock line
233	T7	KEY_ROW3	I2C2_SDA	3V3	I/O	I²C bus data line

Table 32 - Secondary General Purpose I²C Bus Signal Description

EDM PIN	i.MX6 BALL	PAD NAME	Signal	V	I/O	Description
235	R4	GPIO_5	I2C3_SCL	3V3	I/O	I²C bus clock line
237	R2	GPIO_16	I2C3_SDA	3V3	I/O	I²C bus data line

NOTE: All I²C bus data and clock lines for all I²C interfaces have 2.2K Ω pull-up to 3.3V resistors present on the EDM1-IMX6 module.

3.15. General Purpose Input/Output (GPIO)

The EDM Standard stipulates 10 dedicated GPIO pins. Many of the EDM1-IMX6 can be put in GPIO mode. Using the additional pins in GPIO mode however might break upgradability to other EDM modules.

The GPIO signals can be configured for the following applications:

- Data input / output
- Interrupt generation

For additional details, please refer to the “General Purpose Input/Output (GPIO)” chapter of the “i.MX6 Reference Manual”.

Table 33 - GPIO Signal Description

EDM PIN	i.MX6 BALL	PAD NAME	Signal	V	I/O	Description
255	L6	CSI0_DAT19	GPIO6_IO05	3V3	I/O	General Purpose Input Output
256	L4	CSI0_DAT16	GPIO6_IO02	3V3	I/O	General Purpose Input Output
257	M6	CSI0_DAT18	GPIO6_IO04	3V3	I/O	General Purpose Input Output
258	E25	EIM_D27	GPIO3_IO27	3V3	I/O	General Purpose Input Output
259	E24	EIM_D26	GPIO3_IO26	3V3	I/O	General Purpose Input Output
260	N22	EIM_BCLK	GPIO6_IO31	3V3	I/O	General Purpose Input Output
261	L3	CSI0_DAT17	GPIO6_IO03	3V3	I/O	General Purpose Input Output
262	W23	ENET_RX_ER	GPIO1_IO24	3V3	I/O	General Purpose Input Output
263	R6	GPIO_4	GPIO1_IO04	3V3	I/O	General Purpose Input Output
264	D15	SD3_RST	GPIO7_IO08	3V3	I/O	General Purpose Input Output

NOTE: It is suggested to use the GPIO’s connected to pin 263 and 264 for touch controller related functions.

3.16. Manufacturing and Boot Control

The EDM Standard reserves a number of pins for manufacturing purposes and boot behavior to override the default boot media present on the EDM1-IMX6 System-on-Module (eMMC or NAND Flash).

For additional details, please refer to “EDM Standard Specifications”

Table 34 - EDM MNF Pin Description

EDM PIN	i.MX6 BALL	PAD NAME	Signal	V	I/O	Description
267	M23	EIM_DA13	SRC_BOOT_CFG13		I	Pins for manufacturing and validation purposes
269	N23	EIM_DA14	SRC_BOOT_CFG14		I	Pins for manufacturing and validation purposes
271	L22	EIM_DA4	SRC_BOOT_CFG04		I	Pins for manufacturing and validation purposes
273	L23	EIM_DA5	SRC_BOOT_CFG05		I	Pins for manufacturing and validation purposes
275	K25	EIM_DA6	SRC_BOOT_CFG06		I	Pins for manufacturing and validation purposes
277	L25	EIM_DA7	SRC_BOOT_CFG07		I	Pins for manufacturing and validation purposes
278	M20	EIM_DA11	SRC_BOOT_CFG11		I	Pins for manufacturing and validation purposes
280	M24	EIM_DA12	SRC_BOOT_CFG12		I	Pins for manufacturing and validation purposes

The EDM1-IMX6 can boot from the following devices that are present on the carrier board.

Table 35 - EDM MNF Boot Configuration Option Overview

EDM PIN	SATA	SD Cardslot	eMMC on Carrier board
267	N.C.	HIGH	HIGH
269	N.C.	LOW	N.C.
271	LOW	HIGH	N.C.
273	HIGH	LOW	HIGH
275	LOW	HIGH	HIGH
277	LOW	LOW	LOW
278	N.C	LOW	LOW
280	N.C	LOW	LOW

NOTE: The signals that should be “HIGH” should have 10K Ω pull-up to 3.3V resistors.

When using EDM1-IMX6 on the TechNexion EDM1-FAIRY evaluation carrier board. You can simply configure the EDM-MNF-BOOT PCB that comes with the EDM1-FAIRY-START evaluation kit as follow:

Table 36 - EDM-MNF-BOOT Configuration for EDM1-FAIRY

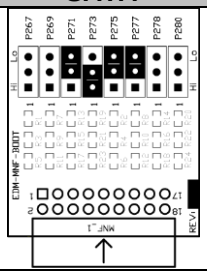
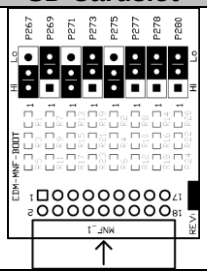
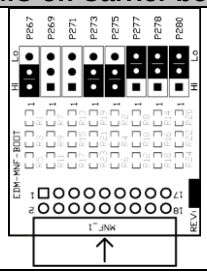
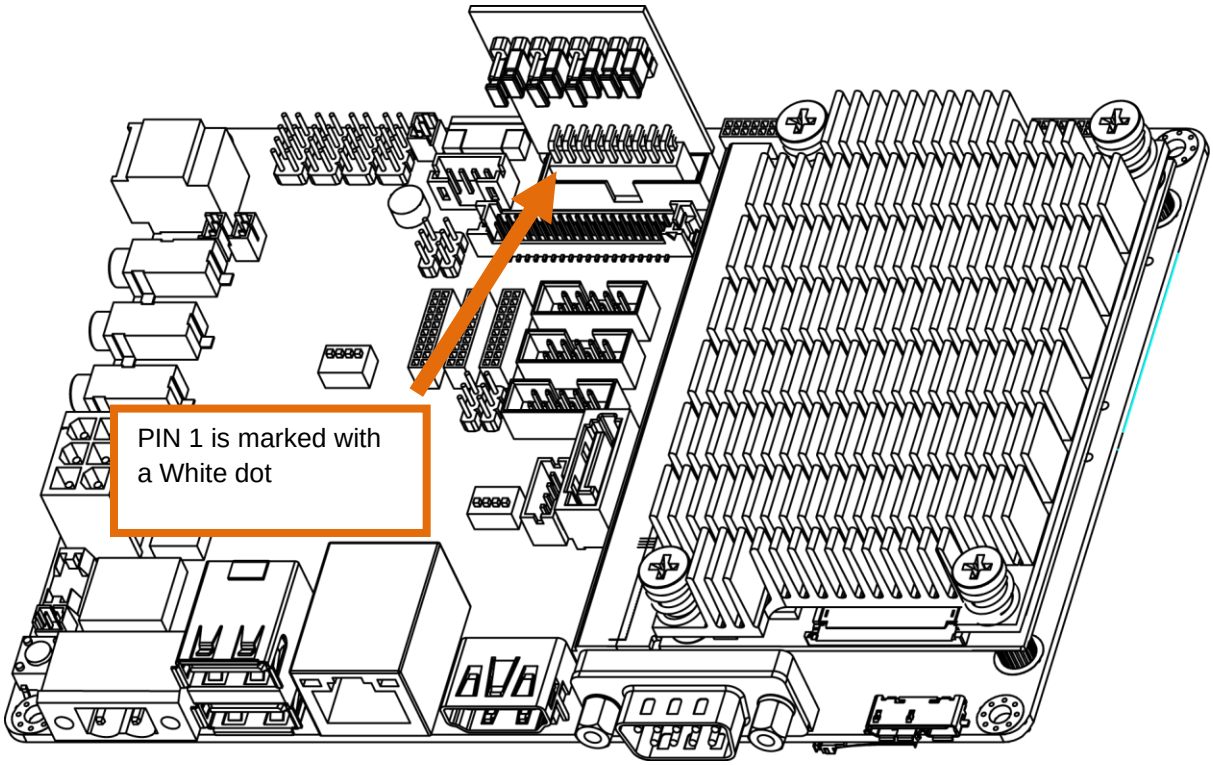
SATA	SD Cardslot	eMMC on Carrier board
		

Figure 11 - EDM1-FAIRY with EDM-MNF-BOOT



3.17. Input Power Requirements

The EDM1-IMX6 is designed to be driven with a single +5V input power rail.

The power domain pins have to be connected as follow:

- All GND pins have to be connected to the carrier board ground pane.
- All VCC pins should be connected to the +5V main power source.

If ATX functionality is desired the following power domains pin should also be connected (ATX mode only):

- All 5VSB pins should be connected to the +5VSB main power source.
- EDM PIN#251 should be connected to the ATX power circuit PWGIN circuit

Table 37 - Input Power Signals

Power Rail	Nominal Input	Input Range	Maximum Input Ripple
VCC (18 pin)	5V	+4.75V - +5.25V	±50 mV
5VSB (2 pin)	5VSB	+4.75V - +5.25V	±50 mV

3.17.1. Power Management Signals

The EDM1-IMX6 has the following set of signals to control the system power states such as the power-on and reset conditions. This enables the system designer to implement a fully ACPI compliant system supporting system states. The minimum hardware requirements for an ACPI compliant system are an EDM module supporting ACPI, ATX conforming power supply and a power button.

EDM PIN	i.MX6 BALL	PAD NAME	Signal	V	I/O	Description
251	5VSB with 10KΩ		S3	3V3	O	S3 signal shuts off power to all runtime system components that are not maintained during S3 state (suspend to RAM)
252	D12	ONOFF	SRC_ONOFF	3V3	I	Power ON button input signal
254	C11	POR_B	SRC_POR_B	3V3	I	Reset button input signal

3.17.2. Power Sequencing for AT based configurations

EDM1-IMX6 input power sequencing requirements for AT based configurations are as follow:

If a backup RealTime Clock (RTC) is required in the host system. We recommend to design an RTC circuit on the EDM carrier board. For example the Maxim Integrated DS1337+ connected over the general purpose I^2C can be used.

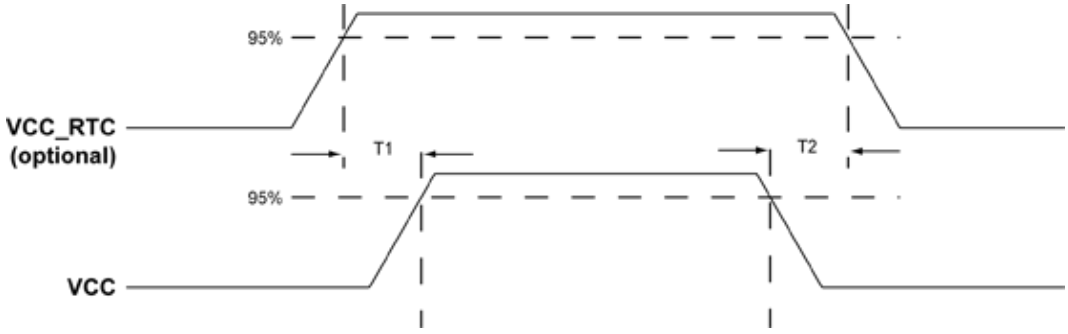
Start Sequence:
VCC_RTC must come up at the same time or before VCC comes up.

Stop Sequence:
VCC must go down at the same time or before VCC_RTC goes down

Table 38 - Input Power Sequencing for AT based configurations

Item	Description	Value
T1	VCC_RTC rise to VCC rise	≥ 0 ms
T2	VCC fall to VCC_RTC fall	≥ 0 ms

Figure 12 - Input Power sequence for AT based configurations



3.17.3. Power Sequencing for ATX based configurations

EDM1-IMX6 input power sequencing requirements for ATX based configurations are as follow:

If a backup RealTime Clock (RTC) is required in the host system. We recommend to design an RTC circuit on the EDM carrier board. For example the Maxim Integrated DS1337+ connected over the general purpose I^2C can be used.

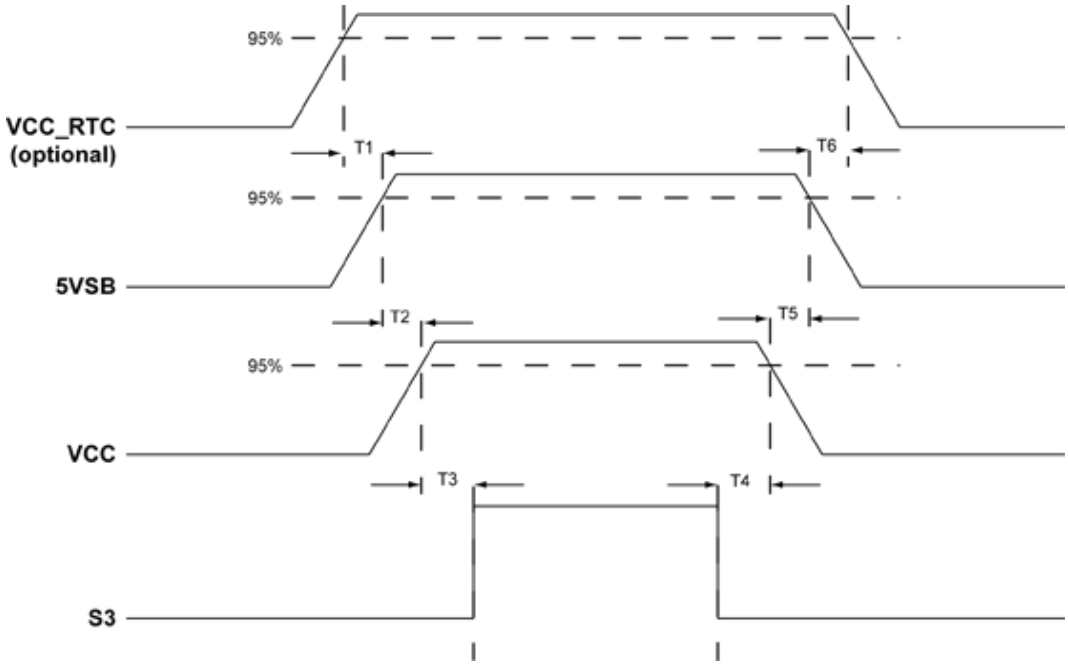
Start Sequence:
Optional VCC_RTC must come up at the same time or before 5VSB comes up.
5VSB must come up at the same time or before VCC comes up.
A 5V return signal is generated on EDM PIN# 251
PWGIN must be active at the same time or after VCC comes up.

Stop Sequence:
PWGIN must be inactive at the same time or before VCC goes down
VCC must go down at the same time or before 5VSB goes down
5VSB must go down at the same time or before VCC_RTC goes down

Table 39 - Input Power Sequencing for ATX based configurations

Item	Description	Value
T1	VCC_RTC rise to 5VSD rise	≥ 0 ms
T2	5VSB rise to VCC rise	≥ 0 ms
T3	VCC rise to PWGIN (S3) rise	≥ 0 ms
T4	PWGIN (S3) fall to VCC fall	≥ 0 ms
T5	VCC fall to 5VSB fall	≥ 0 ms
T6	5VSB fall to VCC_RTC fall	≥ 0 ms

Figure 13 - Input Power sequence for ATX based configurations



3.17.4. EDM1-IMX6 Power Option without Carrier Board

The EDM1-IMX6 provides support to be powered without a carrier board by mounting a power connector that provides +5V to the System-on-Module directly.

A Molex 43650-0200 connector should be mounted at the following location.

Figure 14 - EDM1-IMX6 Optional Power Connector Location

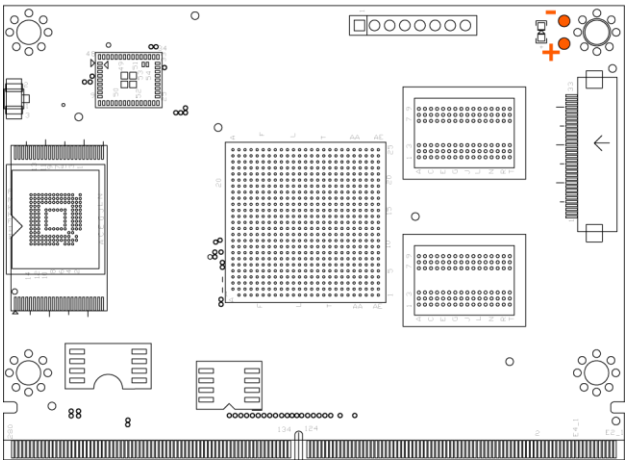
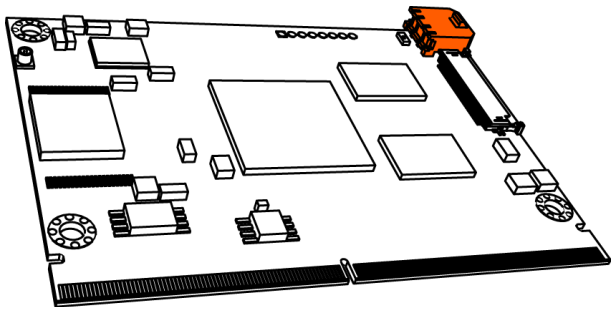
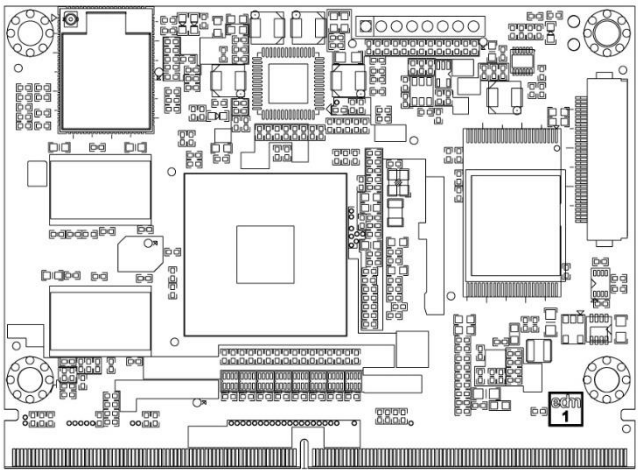


Figure 15 - EDM1-IMX6 with mounted Molex 43650-0200 Connector



4. EDM Connector Pin Assignment

The EDM1-IMX6 EDM connector 314 pin assignment is listed in the table below.



EDM PIN	CPU BALL	CPU PAD NAME	Signal	V	I/O	Description
E1_1			5VSB	5VSB	P	Standby Power Supply 5VDC ± 5%
E2_1			5VSB	5VSB	P	Standby Power Supply 5VDC ± 5%
E1_2			VCC	5V	P	Power Supply 5VDC ± 5%
E2_2			VCC	5V	P	Power Supply 5VDC ± 5%
E1_3			VCC	5V	P	Power Supply 5VDC ± 5%
E2_3			VCC	5V	P	Power Supply 5VDC ± 5%
E1_4			VCC	5V	P	Power Supply 5VDC ± 5%
E2_4			VCC	5V	P	Power Supply 5VDC ± 5%
E1_5			VCC	5V	P	Power Supply 5VDC ± 5%
E2_5			VCC	5V	P	Power Supply 5VDC ± 5%
E1_6			VCC	5V	P	Power Supply 5VDC ± 5%
E2_6			VCC	5V	P	Power Supply 5VDC ± 5%
E1_7			VCC	5V	P	Power Supply 5VDC ± 5%
E2_7			VCC	5V	P	Power Supply 5VDC ± 5%
E1_8			VCC	5V	P	Power Supply 5VDC ± 5%
E2_8			VCC	5V	P	Power Supply 5VDC ± 5%
E1_9			VCC	5V	P	Power Supply 5VDC ± 5%
E2_9			VCC	5V	P	Power Supply 5VDC ± 5%
E1_10			VCC	5V	P	Power Supply 5VDC ± 5%
E2_10			VCC	5V	P	Power Supply 5VDC ± 5%
E3_1			GND	GND	P	Ground
E4_1			GND	GND	P	Ground
E3_2			GBE_MDI2+	LAN	I/O	Gigabit Ethernet Media Dependent Interface (MDI) differential pair 2 positive signal

EDM PIN	i.MX6 BALL	PAD NAME	Signal	V	I/O	Description
E4_2			GBE_MDI0+	LAN	I/O	Gigabit Ethernet Media Dependent Interface (MDI) differential pair 0 positive signal
E3_3			GBE_MDI2-	LAN	I/O	Gigabit Ethernet Media Dependent Interface (MDI) differential pair 2 negative signal
E4_3			GBE_MDI0-	LAN	I/O	Gigabit Ethernet Media Dependent Interface (MDI) differential pair 0 negative signal
E3_4			GND	GND	P	Ground
E4_4			GND	GND	P	Ground
E3_5			GBE_MDI3+	LAN	I/O	Gigabit Ethernet Media Dependent Interface (MDI) differential pair 3 positive signal
E4_5			GBE_MDI1+	LAN	I/O	Gigabit Ethernet Media Dependent Interface (MDI) differential pair 1 positive signal
E3_6			GBE_MDI3-	LAN	I/O	Gigabit Ethernet Media Dependent Interface (MDI) differential pair 3 negative signal
E4_6			GBE_MDI1-	LAN	I/O	Gigabit Ethernet Media Dependent Interface (MDI) differential pair 1 negative signal
E3_7			LED1_ACT	3V3	O	Gigabit Ethernet LED Activity indicator
E4_7			GND	GND	P	Ground
E3_8			GND	GND	P	Ground
E4_8			LED1_nLink100	3V3	O	Gigabit Ethernet 100Mbit/sec LED link indicator
E3_9	U2	LVDS0_TX0_N	LVDS0_DATA0_N	2V5	O	LVDS primary channel differential pair 0 negative signal
E4_9			LED1_nLink1000	3V3	O	Gigabit Ethernet 1000Mbit/sec LED link indicator
E3_10	U1	LVDS0_TX0_P	LVDS0_DATA0_P	2V5	O	LVDS primary channel differential pair 0 positive signal
E4_10			GND	GND	P	Ground
1			GND	GND	P	Ground
2	P24	DISP0_DAT0	IPU1_DISP0_DATA00	3V3	O	LCD Pixel Data bit 0
3	U4	LVDS0_TX1_N	LVDS0_DATA1_N	2V5	O	LVDS primary channel differential pair 1 negative signal
4	P22	DISP0_DAT1	IPU1_DISP1_DATA01	3V3	O	LCD Pixel Data bit 1

EDM PIN	i.MX6 BALL	PAD NAME	Signal	V	I/O	Description
5	U3	LVDS0_TX1_P	LVDS0_DATA1_P	2V5	O	LVDS primary channel differential pair 1 positive signal
6			GND	GND	P	Ground
7			GND	GND	P	Ground
8	P23	DISP0_DAT2	IPU1_DISP1_DATA02	3V3	O	LCD Pixel Data bit 2
9	V2	LVDS0_TX2_N	LVDS0_DATA2_N	2V5	O	LVDS primary channel differential pair 2 negative signal
10	P21	DISP0_DAT3	IPU1_DISP1_DATA03	3V3	O	LCD Pixel Data bit 3
11	V1	LVDS0_TX2_P	LVDS0_DATA2_P	2V5	O	LVDS primary channel differential pair 2 positive signal
12			GND	GND	P	Ground
13			GND	GND	P	Ground
14	P20	DISP0_DAT4	IPU1_DISP0_DATA04	3V3	O	LCD Pixel Data bit 4
15	W2	LVDS0_TX3_N	LVDS0_DATA3_N	2V5	O	LVDS primary channel differential pair 3 negative signal
16	R25	DISP0_DAT5	IPU1_DISP0_DATA05	3V3	O	LCD Pixel Data bit 5
17	W1	LVDS0_TX3_P	LVDS0_DATA3_P	2V5	O	LVDS primary channel differential pair 3 positive signal
18			GND	GND	P	Ground
19			GND	GND	P	Ground
20	R23	DISP0_DAT6	IPU1_DISP0_DATA06	3V3	O	LCD Pixel Data bit 6
21	V4	LVDS0_CLK_N	LVDS0_CLK_N	2V5	O	LVDS primary channel clock negative signal
22	R24	DISP0_DAT7	IPU1_DISP0_DATA07	3V3	O	LCD Pixel Data bit 7
23	V3	LVDS0_CLK_P	LVDS0_CLK_P	2V5	O	LVDS primary channel clock positive signal
24			GND	GND	P	Ground
25			GND	GND	P	Ground
26	R22	DISP0_DAT8	IPU1_DISP0_DATA08	3V3	O	LCD Pixel Data bit 8
27	B19	SD4_DAT1	PWM3_OUT	3V3	O	LVDS primary channel panel backlight control
28	T25	DISP0_DAT9	IPU1_DISP0_DATA09	3V3	O	LCD Pixel Data bit 9
29	D18	SD4_DAT0	GPIO2_IO08	3V3	O	LVDS primary channel panel backlight enable
30			GND	GND	P	Ground
31	L1	CSI0_DAT13	GPIO5_IO31	3V3	O	LVDS primary channel panel power enable
32	R21	DISP0_DAT10	IPU1_DISP0_DATA10	3V3	O	LCD Pixel Data bit 10
33			NC			Not Connected
34	T23	DISP0_DAT11	IPU1_DISP0_DATA11	3V3	O	LCD Pixel Data bit 11
35			NC			Not Connected
36	T24	DISP0_DAT12	IPU1_DISP0_DATA12	3V3	O	LCD Pixel Data bit 12
37	G23	EIM_D28	I2C1_SDA	3V3	I/O	Display ID DDC data line used for LVDS flat panel detection. If not used this can be assigned to General Purpose I^2C bus data line

EDM PIN	i.MX6 BALL	PAD NAME	Signal	V	I/O	Description
38	R20	DISP0_DAT13	IPU1_DISP0_DATA13	3V3	O	LCD Pixel Data bit 13
39	H20	EIM_D21	I2C1_SCL	3V3	I/O	Display ID DDC clock line used for LVDS flat panel detection. If not used this can be assigned to General Purpose I^2C bus clock line
40	U25	DISP0_DAT14	IPU1_DISP0_DATA14	3V3	O	LCD Pixel Data bit 14
41			GND	GND	P	Ground
42			GND	GND	P	Ground
43	J6	HDMI_CLKP	HDMI_TX_CLK_P	3V3	O	HDMI differential pair clock positive signal
44	T22	DISP0_DAT15	IPU1_DISP0_DATA15	3V3	O	LCD Pixel Data bit 15
45	J5	HDMI_CLKM	HDMI_TX_CLK_N	3V3	O	HDMI differential pair clock negative signal
46	T21	DISP0_DAT16	IPU1_DISP0_DATA16	3V3	O	LCD Pixel Data bit 16
47			GND	GND	P	Ground
48			GND	GND	P	Ground
49	K6	HDMI_D0P	HDMI_TX_DATA0_P	3V3	O	HDMI differential pair 0 positive signal
50	U24	DISP0_DAT17	IPU1_DISP0_DATA17	3V3	O	LCD Pixel Data bit 17
51	K5	HDMI_D0M	HDMI_TX_DATA0_N	3V3	O	HDMI differential pair 0 negative signal
52	V25	DISP0_DAT18	IPU1_DISP0_DATA18	3V3	O	LCD Pixel Data bit 18
53			GND	GND	P	Ground
54			GND	GND	P	Ground
55	J4	HDMI_D1P	HDMI_TX_DATA1_P	3V3	O	HDMI differential pair 1 positive signal
56	U23	DISP0_DAT19	IPU1_DISP0_DATA19	3V3	O	LCD Pixel Data bit 19
57	J3	HDMI_D1M	HDMI_TX_DATA1_N	3V3	O	HDMI differential pair 1 negative signal
58	U22	DISP0_DAT20	IPU1_DISP0_DATA20	3V3	O	LCD Pixel Data bit 20
59			GND	GND	P	Ground
60			GND	GND	P	Ground
61	K4	HDMI_D2P	HDMI_TX_DATA2_P	3V3	O	HDMI differential pair 2 positive signal
62	T20	DISP0_DAT21	IPU1_DISP0_DATA21	3V3	O	LCD Pixel Data bit 21
63	K3	HDMI_D2M	HDMI_TX_DATA2_N	3V3	O	HDMI differential pair 2 negative signal
64	V24	DISP0_DAT22	IPU1_DISP0_DATA22	3V3	O	LCD Pixel Data bit 22
65			GND	GND	P	Ground
66			GND	GND	P	Ground
67	K1	HDMI_HPD	HDMI_TX_HPD	3V3	I	HDMI/DP Hot plug detection signal that serves as an interrupt request
68	W24	DISP0_DAT23	IPU1_DISP0_DATA23	3V3	O	LCD Pixel Data bit 23
69			NC			Not Connected
70	N19	DI0_DISP_CLK	IPU1_DI0_DISP_CLK	3V3	O	LCD Pixel Clock
71	H19	EIM_A25	HDMI_TX_CEC_LINE	1V8	I/O	HDMI Consumer Electronics Control
72	N25	DI0_PIN2	IPU1_DI0_PIN02	3V3	O	LCD Horizontal Synchronization

EDM PIN	i.MX6 BALL	PAD NAME	Signal	V	I/O	Description
73	H20	EIM_D21	I2C1_SCL	5V	I/O	Display ID DDC data line used for HDMI detection. If not used this can be assigned to General Purpose I²C bus clock line
74	N20	DI0_PIN3	IPU1_DI0_PIN03	3V3	O	LCD Vertical Synchronization
75	G23	EIM_D28	I2C1_SDA	5V	I/O	Display ID DDC data line used for HDMI detection. If not used this can be assigned to General Purpose I²C bus data line
76	P25	DI0_PIN4	IPU1_DI0_PIN04	3V3	O	LCD backlight enable/disable
77			GND	GND	P	Ground
78	N21	DI0_PIN15	IPU1_DI0_PIN15	3V3	O	LCD dot enable pin signal
79			NC			Not Connected
80	A20	SD4_DAT3	GPIO2_IO11	3V3	O	LCD Voltage On
81			NC			Not Connected
82	F17	SD4_DAT2	PWM4_OUT	3V3	O	LCD Backlight brightness Control
83			GND	GND	P	Ground
84			RSVD			Reserved
85	D7	CLK1_P	XTALOSC_CLK1_P	2V5	O	PCI Express channel A clock differential pair positive signal
86	F15	NANDF_CS0	NAND_CE0_B	3V3	O	GPMC Chip Select bit A
87	C7	CLK1_N	XTALOSC_CLK1_N	2V5	O	PCI Express channel A clock differential pair negative signal
88			GND	GND	P	Ground
89			GND	GND	P	Ground
90	C16	NANDF_CS1	NAND_CE1_B	3V3	O	GPMC Chip Select bit B
91	B3	PCIE_TXP	PCIE_TX_P	2V5	O	PCI Express channel A Transmit output differential pair positive signal
92	A17	NANDF_CS2	NAND_CE2_B	3V3	O	GPMC Chip Select bit C
93	A3	PCIE_TXM	PCIE_TX_N	2V5	O	PCI Express channel A Transmit output differential pair negative signal
94			GND	GND	P	Ground
95			GND	GND	P	Ground
96	D16	NANDF_CS3	NAND_CE3_B	3V3	O	GPMC Chip Select bit D
97	B2	PCIE_RXP	PCIE_RX_P	2V5	I	PCI Express channel A Receive input differential pair positive signal
98			NC			Not Connected
99	B1	PCIE_RXM	PCIE_RX_N	2V5	I	PCI Express channel A Receive input differential pair negative signal
100			GND	GND	P	Ground

EDM PIN	i.MX6 BALL	PAD NAME	Signal	V	I/O	Description
101			GND	GND	P	Ground
102	B16	NANDF_RB0	NAND_READY_B	3V3	I	External indication of wait
103			NC			Not Connected
104	E15	NANDF_WP_B	NAND_WP_B	3V3	O	GPMC Write Protect / Enable
105			NC			Not Connected
106	C15	NANDF_CLE	NAND_CLE	3V3	O	GPMC Lower Byte Enable. Also used for Command Latch Enable
107			NC			Not Connected
108	A16	NANDF_ALE	NAND_ALE	3V3	O	GPMC Address Valid or Address Latch Enable
109			NC			Not Connected
110	E16	SD4_CLK	NAND_WE_B	3V3	I	GPMC Write Enable
111			NC			Not Connected
112	B17	SD4_CMD	NAND_RE_B	3V3	O	GPMC Read Enable
113			NC			Not Connected
114			NC			Not Connected
115			NC			Not Connected
116			NC			Not Connected
117			NC			Not Connected
118			NC			Not Connected
119	H21	EIM_D31	GPIO3_IO31	3V3	O	PCI Express Reset signal for external devices
120			NC			Not Connected
121			GND	GND	P	Ground
122			NC			Not Connected
123	B14	SATA_RXP	SATA_PHY_RX_P	2V5	I	Serial ATA channel 1 Receive differential pair positive signal
124			GND	GND	P	Ground
125	A14	SATA_RXM	SATA_PHY_RX_N	2V5	I	Serial ATA channel 1 Receive differential pair negative signal
126			KEY			
127			KEY			
128			KEY			
129			KEY			
130			KEY			
131			KEY			
132			KEY			
133	M5	CSI0_DAT15	GPIO6_IO01	SATA	I/O	Serial ATA LED. Open collector output pin driven during SATA command activity
134			NC			Not Connected
135	A12	SATA_TXP	SATA_PHY_TX_P	2V5	O	Serial ATA channel 1 Transmit differential pair positive signal
136			NC			Not Connected
137	B12	SATA_TXM	SATA_PHY_TX_N	2V5	O	Serial ATA channel 1 Transmit differential pair negative signal
138			NC			Not Connected

EDM PIN	i.MX6 BALL	PAD NAME	Signal	V	I/O	Description
139	R1	GPIO_17	GPIO7_IO12	USB	O	Universal Serial Bus carrier board hub reset pin
140			NC			Not Connected
141	T2	GPIO_9	GPIO1_IO09	3V3	I	Over current detect input pin to monitor USB power over current
142			NC			Not Connected
143			NC			Not Connected
144			NC			Not Connected
145			NC			Not Connected
146			NC			Not Connected
147			NC			Not Connected
148			GND	GND	P	Ground
149			NC			Not Connected
150			NC			Not Connected
151			NC			Not Connected
152			NC			Not Connected
153			GND	GND	P	Ground
154			GND	GND	P	Ground
155	T4	GPIO_1	USB_OTG_ID	3V3	I	Universal Serial Bus On-The-Go detection signal
156			NC			Not Connected
157	A6	USB_OTG_DP	USB_OTG_DP	3V3	I/O	Universal Serial Bus differential pair positive signal
158			NC			Not Connected
159	B6	USB_OTG_DN	USB_OTG_DN	3V3	I/O	Universal Serial Bus differential pair negative signal
160			NC			Not Connected
161	E9	USB_OTG_ VBUS	USB_OTG_ VBUS	5V	I/O	Universal Serial Bus power
162			NC			Not Connected
163	E23	EIM_D22	USB_OTG_PWR	USB	O	Universal Serial Bus power enable
164			NC			Not Connected
165	J20	EIM_D30	USB_H1_OC	3V3	I	Over current detect input pin to monitor USB power over current
166			GND	GND	P	Ground
167			NC			Not Connected
168	C18	NANDF_D7	NAND_DATA07	3V3	I/O	GPMC data bit 7
169			NC			Not Connected
170	E17	NANDF_D6	NAND_DATA06	3V3	I/O	GPMC data bit 6
171			NC			Not Connected
172	B18	NANDF_D5	NAND_DATA05	3V3	I/O	GPMC data bit 5
173			NC			Not Connected
174	A19	NANDF_D4	NAND_DATA04	3V3	I/O	GPMC data bit 4
175			NC			Not Connected
176	D17	NANDF_D3	NAND_DATA03	3V3	I/O	GPMC data bit 3
177			GND	GND	P	Ground
178	F16	NANDF_D2	NAND_DATA02	3V3	I/O	GPMC data bit 2

EDM PIN	i.MX6 BALL	PAD NAME	Signal	V	I/O	Description
179	F10	USB_H1_DN	USB_H1_DN	3V3	I/O	Universal Serial Bus differential pair negative signal
180	C17	NANDF_D1	NAND_DATA01	3V3	I/O	GPMC data bit 1
181	E10	USB_H1_DP	USB_H1_DP	3V3	I/O	Universal Serial Bus differential pair positive signal
182	A18	NANDF_D0	NAND_DATA00	3V3	I/O	GPMC data bit 0
183	D10	USB_H1_VBUS	USB_H1_VBUS	5V	I/O	Universal Serial Bus power
184			GND	GND	P	Ground
185			GND	GND	P	Ground
186	U6	KEY_ROW1	AUD5_RXD	3V3	I	Secondary Integrated Interchip Sound (I^2S) channel receive data line
187	N3	CSI0_DAT7	AUD3_RXD	3V3	I	Primary Integrated Interchip Sound (I^2S) channel receive data line
188	U7	KEY_COL1	AUD5_TXFS	3V3	O	Secondary Integrated Interchip Sound (I^2S) channel frame synchronization signal
189	N4	CSI0_DAT6	AUD3_TXFS	3V3	O	Primary Integrated Interchip Sound (I^2S) channel frame synchronization signal
190	V6	KEY_ROW0	AUD5_TXD	3V3	O	Secondary Integrated Interchip Sound (I^2S) channel transmit data line
191	P2	CSI0_DAT5	AUD3_TXD	3V3	O	Primary Integrated Interchip Sound (I^2S) channel transmit data line
192	W5	KEY_COL0	AUD5_TXC	3V3	O	Secondary Integrated Interchip Sound (I^2S) channel word clock signal
193	N1	CSI0_DAT4	AUD3_TXC	3V3	O	Primary Integrated Interchip Sound (I^2S) channel word clock signal
194	T5	GPIO_0	CCM_CLKO1	3V3	O	Secondary Integrated Interchip Sound (I^2S) channel master clock signal
195	T5	GPIO_0	CCM_CLKO1	3V3	O	Primary Integrated Interchip Sound (I^2S) channel master clock signal
196	W21	ENET_RXD0	SPDIF_OUT	SPDIF	O	Sony / Philips Digital Interconnect Format Audio output
197	T6	KEY_COL4	FLEXCAN2_TX	3V3	I/O	Secondary CAN (controller Area Network) transmit signal
198			GND	GND	P	Ground
199	V5	KEY_ROW4	FLEXCAN2_RX	3V3	I/O	Secondary CAN (controller Area Network) receive signal
200	W6	KEY_COL2	FLEXCAN1_TX	3V3	I/O	Primary CAN (controller Area Network) transmit signal
201			GND	GND	P	Ground
202	W4	KEY_ROW2	FLEXCAN1_RX	3V3	I/O	Primary CAN (controller Area Network) receive signal
203	T1	GPIO_2	GPIO1_IO02	3V3	I/O	MMC/SDIO Card Detect

EDM PIN	i.MX6 BALL	PAD NAME	Signal	V	I/O	Description
204			GND	GND	P	Ground
205	B21	SD1_CMD	SD1_CMD	3V3	I/O	MMC/SDIO Command
206	D20	SD1_CLK	SD1_CLK	3V3	O	MMC/SDIO Clock
207	N6	CSI0_DAT8	GPIO5_IO26	3V3	I/O	MMC/SDIO Write Protect
208	P4	CSI0_MCLK	GPIO5_IO19	3V3	O	MMC/SDIO LED
209	C20	SD1_DAT1	SD1_DATA1	3V3	I/O	MMC/SDIO Data bit 1
210	P1	CSI0_PIXCLK	GPIO5_IO18	3V3	O	MMC/SDIO Power Enable
211	F18	SD1_DAT3	SD1_DATA3	3V3	I/O	MMC/SDIO Data bit 3
212	A21	SD1_DAT0	SD1_DATA0	3V3	I/O	MMC/SDIO Data bit 0
213			NC			Not Connected
214	E19	SD1_DAT2	SD1_DATA2	3V3	I/O	MMC/SDIO Data bit 2
215			NC			Not Connected
216			NC			Not Connected
217			GND	GND	P	Ground
218			NC			Not Connected
219	J23	EIM_CS1	ECSPI2_MOSI	3V3	O	Serial Peripheral Interface primary channel master output slave input signal
220			GND	GND	P	Ground
221	J24	EIM_OE	ECSPI2_MISO	3V3	I	Serial Peripheral Interface primary channel master input slave output signal
222	D24	EIM_D18	ECSPI1_MOSI	3V3	O	Serial Peripheral Interface secondary channel master output slave input signal
223	H24	EIM_CS0	ECSPI2_SCLK	3V3	O	Serial Peripheral Interface primary channel clock signal
224	F21	EIM_D17	ECSPI1_MISO	3V3	I	Serial Peripheral Interface secondary channel master input slave output signal
225	K20	EIM_RW	ECSPI2_SS0	3V3	O	Serial Peripheral Interface primary channel Chip Select 0 signal
226	C25	EIM_D16	ECSPI1_SCLK	3V3	O	Serial Peripheral Interface secondary channel clock signal
227	K22	EIM_LBA	ECSPI2_SS1	3V3	O	Serial Peripheral Interface primary channel Chip Select 1 signal. Do not use if only 1 SPI device is used
228	E22	EIM_EB2	ECSPI1_SS0	3V3	O	Serial Peripheral Interface secondary channel Chip Select 0 signal
229			GND	GND	P	Ground
230	U21	ENET_CRS_DV	GPIO1_IO25	3V3	O	Serial Peripheral Interface secondary channel Chip Select 1 signal. Do not use if only 1 SPI device is used
231	U5	KEY_COL3	I2C2_SCL	3V3	I/O	I^2C bus clock line
232			GND	GND	P	Ground
233	T7	KEY_ROW3	I2C2_SDA	3V3	I/O	I^2C bus data line

EDM PIN	i.MX6 BALL	PAD NAME	Signal	V	I/O	Description
234	B20	SD4_DAT6	UART2_CTS_B	3V3	O	Universal Asynchronous Receive Transmit secondary channel clear to send signal
235	R4	GPIO_5	I2C3_SCL	3V3	I/O	I²C bus clock line
236	D19	SD4_DAT7	UART2_TX_DATA	3V3	O	Universal Asynchronous Receive Transmit secondary channel transmit data signal
237	R2	GPIO_16	I2C3_SDA	3V3	I/O	I²C bus data line
238	E18	SD4_DAT4	UART2_RX_DATA	3V3	I	Universal Asynchronous Receive Transmit secondary channel receive data signal
239			GND	GND	P	Ground
240	C19	SD4_DAT5	UART2_RTS_B	3V3	O	Universal Asynchronous Receive Transmit secondary channel request to send signal
241	G21	EIM_D19	UART1_CTS_B	3V3	O	Universal Asynchronous Receive Transmit secondary channel clear to send signal
242			NC			Not Connected
243	M1	CSI0_DAT10	UART1_TX_DATA	3V3	O	Universal Asynchronous Receive Transmit secondary channel transmit data signal
244			NC			Not Connected
245	M3	CSI0_DAT11	UART1_RX_DATA	3V3	I	Universal Asynchronous Receive Transmit secondary channel receive data signal
246			NC			Not Connected
247	G20	EIM_D20	UART1_RTS_B	3V3	O	Universal Asynchronous Receive Transmit secondary channel request to send signal
248			NC			Not Connected
249			GND	GND	P	Ground
250			GND	GND	P	Ground
251	5VSB with 10KΩ		S3	3V3	O	S3 signal shuts off power to all runtime system components that are not maintained during S3 state (suspend to RAM)
252	D12	ONOFF	SRC_ONOFF	3V3	I	Power ON button input signal
253			NC			Not Connected
254	C11	POR_B	SRC_POR_B	3V3	I	Reset button input signal
255	L6	CSI0_DAT19	GPIO6_IO05	3V3	I/O	General Purpose Input Output
256	L4	CSI0_DAT16	GPIO6_IO02	3V3	I/O	General Purpose Input Output
257	M6	CSI0_DAT18	GPIO6_IO04	3V3	I/O	General Purpose Input Output
258	E25	EIM_D27	GPIO3_IO27	3V3	I/O	General Purpose Input Output
259	E24	EIM_D26	GPIO3_IO26	3V3	I/O	General Purpose Input Output
260	N22	EIM_BCLK	GPIO6_IO31	3V3	I/O	General Purpose Input Output
261	L3	CSI0_DAT17	GPIO6_IO03	3V3	I/O	General Purpose Input Output
262	W23	ENET_RX_ER	GPIO1_IO24	3V3	I/O	General Purpose Input Output
263	R6	GPIO_4	GPIO1_IO04	3V3	I/O	General Purpose Input Output

EDM PIN	i.MX6 BALL	PAD NAME	Signal	V	I/O	Description
264	D15	SD3_RST	GPIO7_IO08	3V3	I/O	General Purpose Input Output
265			GND	GND	P	Ground
266			GND	GND	P	Ground
267	M23	EIM_DA13	SRC_BOOT_CFG13		I	Pins for manufacturing and validation purposes
268			NC			Not Connected
269	N23	EIM_DA14	SRC_BOOT_CFG14		I	Pins for manufacturing and validation purposes
270			NC			Not Connected
271	L22	EIM_DA4	SRC_BOOT_CFG04		I	Pins for manufacturing and validation purposes
272			NC			Not Connected
273	L23	EIM_DA5	SRC_BOOT_CFG05		I	Pins for manufacturing and validation purposes
274			NC			Not Connected
275	K25	EIM_DA6	SRC_BOOT_CFG06		I	Pins for manufacturing and validation purposes
276			NC			Not Connected
277	L25	EIM_DA7	SRC_BOOT_CFG07		I	Pins for manufacturing and validation purposes
278	M20	EIM_DA11	SRC_BOOT_CFG11		I	Pins for manufacturing and validation purposes
279	NC		Watchdog	3V3	O	Watchdog event indication signal
280	M24	EIM_DA12	SRC_BOOT_CFG12		I	Pins for manufacturing and validation purposes
281	NC		VCC_RTC	3V3	I	Input power for RTC clock

5. EDM Pinmux Overview

Many signals on the EDM1-IMX6 can be configured to support other interfaces. The table below gives an overview of all pins that can be modified.

The default operation mode which is compatible with other EDM Type 1 Modules has been highlighted.

PIN	CPU BALL	PADNAME	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
2	P24	DISP0_DAT0	IPU1_DISP0_DATA00	IPU2_DISP0_DATA00	ECSPI3_SCLK			GPIO4_IO21		
4	P22	DISP0_DAT1	IPU1_DISP0_DATA01	IPU2_DISP0_DATA01	ECSPI3_MOSI			GPIO4_IO22		
8	P23	DISP0_DAT2	IPU1_DISP0_DATA02	IPU2_DISP0_DATA02	ECSPI3_MISO			GPIO4_IO23		
10	P21	DISP0_DAT3	IPU1_DISP0_DATA03	IPU2_DISP0_DATA03	ECSPI3_SS0			GPIO4_IO24		
14	P20	DISP0_DAT4	IPU1_DISP0_DATA04	IPU2_DISP0_DATA04	ECSPI3_SS1			GPIO4_IO25		
16	R25	DISP0_DAT5	IPU1_DISP0_DATA05	IPU2_DISP0_DATA05	ECSPI3_SS2	AUD6_RXFS		GPIO4_IO26		
20	R23	DISP0_DAT6	IPU1_DISP0_DATA06	IPU2_DISP0_DATA06	ECSPI3_SS3	AUD6_RXC		GPIO4_IO27		
22	R24	DISP0_DAT7	IPU1_DISP0_DATA07	IPU2_DISP0_DATA07	ECSPI3_RDY			GPIO4_IO28		
26	R22	DISP0_DAT8	IPU1_DISP0_DATA08	IPU2_DISP0_DATA08	PWM1_OUT	WDOG1_B		GPIO4_IO29		
27	B19	SD4_DAT1		SD4_DATA1	PWM3_OUT			GPIO2_IO09		
28	T25	DISP0_DAT9	IPU1_DISP0_DATA09	IPU2_DISP0_DATA09	PWM2_OUT	WDOG2_B		GPIO4_IO30		
29	D18	SD4_DAT0		NAND_DQS				GPIO2_IO08		
31	L1	CSI0_DAT13	IPU1_CSI0_DATA13	EIM_DATA09		UART4_RX_DATA		GPIO5_IO31		ARM_TRACE10
32	R21	DISP0_DAT10	IPU1_DISP0_DATA10	IPU2_DISP0_DATA10				GPIO4_IO31		
34	T23	DISP0_DAT11	IPU1_DISP0_DATA11	IPU2_DISP0_DATA11				GPIO5_IO05		
36	T24	DISP0_DAT12	IPU1_DISP0_DATA12	IPU2_DISP0_DATA12				GPIO5_IO06		
37	G23	EIM_D28	EIM_DATA28	I2C1_SDA	ECSPI4_MOSI	IPU2_CSI1_DATA12	UART2_CTS_B	GPIO3_IO28	IPU1_EXT_TRIG	IPU1_DI0_PIN13
38	R20	DISP0_DAT13	IPU1_DISP0_DATA13	IPU2_DISP0_DATA13		AUD5_RXFS		GPIO5_IO07		
39	H20	EIM_D21	EIM_DATA21	ECSPI4_SCLK	IPU1_DI0_PIN17	IPU2_CSI1_DATA11	USB_OTG_OC	GPIO3_IO21	I2C1_SCL	SPDIF_IN
40	U25	DISP0_DAT14	IPU1_DISP0_DATA14	IPU2_DISP0_DATA14		AUD5_RXC		GPIO5_IO08		
44	T22	DISP0_DAT15	IPU1_DISP0_DATA15	IPU2_DISP0_DATA15	ECSPI1_SS1	ECSPI2_SS1		GPIO5_IO09		
46	T21	DISP0_DAT16	IPU1_DISP0_DATA16	IPU2_DISP0_DATA16	ECSPI2_MOSI	AUD5_TXC	SDMA_EXT_EVENT0	GPIO5_IO10		
50	U24	DISP0_DAT17	IPU1_DISP0_DATA17	IPU2_DISP0_DATA17	ECSPI2_MISO	AUD5_TXD	SDMA_EXT_EVENT1	GPIO5_IO11		
52	V25	DISP0_DAT18	IPU1_DISP0_DATA18	IPU2_DISP0_DATA18	ECSPI2_SS0	AUD5_TXFS	AUD4_RXFS	GPIO5_IO12		EIM_CS2_B
56	U23	DISP0_DAT19	IPU1_DISP0_DATA19	IPU2_DISP0_DATA19	ECSPI2_SCLK	AUD5_RXD	AUD4_RXC	GPIO5_IO13		EIM_CS3_B
58	U22	DISP0_DAT20	IPU1_DISP0_DATA20	IPU2_DISP0_DATA20	ECSPI1_SCLK	AUD4_TXC		GPIO5_IO14		
62	T20	DISP0_DAT21	IPU1_DISP0_DATA21	IPU2_DISP0_DATA21	ECSPI1_MOSI	AUD4_TXD		GPIO5_IO15		
64	V24	DISP0_DAT22	IPU1_DISP0_DATA22	IPU2_DISP0_DATA22	ECSPI1_MISO	AUD4_TXFS		GPIO5_IO16		
68	W24	DISP0_DAT23	IPU1_DISP0_DATA23	IPU2_DISP0_DATA23	ECSPI1_SS0	AUD4_RXD		GPIO5_IO17		
70	N19	DI0_DISP_CLK	IPU1_DI0_DISP_CLK	IPU2_DI0_DISP_CLK				GPIO4_IO16		
71	H19	EIM_A25	EIM_ADDR25	ECSPI4_SS1	ECSPI2_RDY	IPU1_DI1_PIN12	IPU1_DI0_D1_CS	GPIO5_IO02	HDMI_TX_CEC_LINE	
72	N25	DI0_PIN2	IPU1_DI0_PIN02	IPU2_DI0_PIN02	AUD6_TXD			GPIO4_IO18		
73	H20	EIM_D21	EIM_DATA21	ECSPI4_SCLK	IPU1_DI0_PIN17	IPU2_CSI1_DATA11	USB_OTG_OC	GPIO3_IO21	I2C1_SCL	SPDIF_IN
74	N20	DI0_PIN3	IPU1_DI0_PIN03	IPU2_DI0_PIN03	AUD6_TXFS			GPIO4_IO19		
75	G23	EIM_D28	EIM_DATA28	I2C1_SDA	ECSPI4_MOSI	IPU2_CSI1_DATA12	UART2_CTS_B	GPIO3_IO28	IPU1_EXT_TRIG	IPU1_DI0_PIN13
76	P25	DI0_PIN4	IPU1_DI0_PIN04	IPU2_DI0_PIN04	AUD6_RXD	SD1_WP		GPIO4_IO20		
78	N21	DI0_PIN15	IPU1_DI0_PIN15	IPU2_DI0_PIN15	AUD6_TXC			GPIO4_IO17		
80	A20	SD4_DAT3	SD4_DATA3					GPIO2_IO11		
82	F17	SD4_DAT2	SD4_DATA2	PWM4_OUT				GPIO2_IO10		
86	F15	NANDF_CS0	NAND_CE0_B					GPIO6_IO11		
90	C16	NANDF_CS1	NAND_CE1_B	SD4_VSELECT	SD3_VSELECT			GPIO6_IO14		
92	A17	NANDF_CS2	NAND_CE2_B	IPU1_SISG0	ESAI_TX0	EIM_CRE	CCM_CLKO2	GPIO6_IO15	IPU2_SISG0	
96	D16	NANDF_CS3	NAND_CE3_B	IPU1_SISG1	ESAI_TX1	EIM_ADDR26		GPIO6_IO16	IPU2_SISG1	
102	B16	NANDF_RB0	NAND_READY_B	IPU2_DI0_PIN01				GPIO6_IO10		
104	E15	NANDF_WP_B	NAND_WP_B	IPU2_SISG5				GPIO6_IO09		
PIN	CPU BALL	PADNAME	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7

PIN	CPU BALL	PADNAME	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
106	C15	NANDF_CLE	NAND_CLE	IPU2_SISG4				GPIO6_IO07		
108	A16	NANDF_ALE	NAND_ALE	SD4_RESET				GPIO6_IO08		
110	E16	SD4_CLK	SD4_CLK	NAND_WE_B	UART3_RX_DATA			GPIO7_IO10		
112	B17	SD4_CMD	SD4_CMD	NAND_RE_B	UART3_TX_DATA			GPIO7_IO09		
119	H21	EIM_D31	EIM_DATA31	IPU1_DISP1_DATA20	IPU1_DI0_PIN12	IPU1_CSI0_DATA02	UART3_RTS_B	GPIO3_IO31	USB_H1_PWR	
133	M5	CSI0_DAT15	IPU1_CSI0_DATA15	EIM_DATA11		UART5_RX_DATA		GPIO6_IO01		ARM_TRACE12
139	R1	GPIO_17	ESAI_TX0	ENET_1588_EVENT3_IN	CCM_PMIC_READY	SDMA_EXT_EVENT0	SPDIF_OUT	GPIO7_IO12		
141	T2	GPIO_9	ESAI_RX_FS	WDOG1_B	KEY_COL6	CCM_REF_EN_B	PWM1_OUT	GPIO1_IO09	SD1_WP	
155	T4	GPIO_1	ESAI_RX_CLK	WDOG2_B	KEY_ROW5	USB_OTG_ID	PWM2_OUT	GPIO1_IO01	SD1_CD_B	
163	E23	EIM_D22	EIM_DATA22	ECSPI4_MISO	IPU1_DI0_PIN01	IPU2_CSI1_DATA10	USB_OTG_PWR	GPIO3_IO22	SPDIF_OUT	
165	J20	EIM_D30	EIM_DATA30	IPU1_DISP1_DATA21	IPU1_DI0_PIN11	IPU1_CSI0_DATA03	UART3_CTS_B	GPIO3_IO30	USB_H1_OC	
168	C18	NANDF_D7	NAND_DATA07	SD2_DATA7				GPIO2_IO07		
170	E17	NANDF_D6	NAND_DATA06	SD2_DATA6				GPIO2_IO06		
172	B18	NANDF_D5	NAND_DATA05	SD2_DATA5				GPIO2_IO05		
174	A19	NANDF_D4	NAND_DATA04	SD2_DATA4				GPIO2_IO04		
176	D17	NANDF_D3	NAND_DATA03	SD1_DATA7				GPIO2_IO03		
178	F16	NANDF_D2	NAND_DATA02	SD1_DATA6				GPIO2_IO02		
180	C17	NANDF_D1	NAND_DATA01	SD1_DATA5				GPIO2_IO01		
182	A18	NANDF_D0	NAND_DATA00	SD1_DATA4				GPIO2_IO00		
186	U6	KEY_ROW1	ECSPI1_SS0	ENET_COL	AUD5_RXD	KEY_ROW1	UART5_RX_DATA	GPIO4_IO09	SD2_VSELECT	
187	N3	CSI0_DAT7	IPU1_CSI0_DATA07	EIM_DATA05	ECSPI1_SS0	KEY_ROW6	AUD3_RXD	GPIO5_IO25		ARM_TRACE04
188	U7	KEY_COL1	ECSPI1_MISO	ENET_MDIO	AUD5_TXFS	KEY_COL1	UART5_TX_DATA	GPIO4_IO08	SD1_VSELECT	
189	N4	CSI0_DAT6	IPU1_CSI0_DATA06	EIM_DATA04	ECSPI1_MISO	KEY_COL6	AUD3_TXFS	GPIO5_IO24		ARM_TRACE03
190	V6	KEY_ROW0	ECSPI1_MOSI	ENET_TX_DATA3	AUD5_TXD	KEY_ROW0	UART4_RX_DATA	GPIO4_IO07	DCIC2_OUT	
191	P2	CSI0_DAT5	IPU1_CSI0_DATA05	EIM_DATA03	ECSPI1_MOSI	KEY_ROW5	AUD3_TXD	GPIO5_IO23		ARM_TRACE02
192	W5	KEY_COL0	ECSPI1_SCLK	ENET_RX_DATA3	AUD5_TXC	KEY_COL0	UART4_TX_DATA	GPIO4_IO06	DCIC1_OUT	
193	N1	CSI0_DAT4	IPU1_CSI0_DATA04	EIM_DATA02	ECSPI1_SCLK	KEY_COL5	AUD3_TXC	GPIO5_IO22		ARM_TRACE01
194	T5	GPIO_0	CCM_CLKO1		KEY_COL5	ASRC_EXT_CLK	EPIT1_OUT	GPIO1_IO00	USB_H1_PWR	SNVS_VIO_5
195	T5	GPIO_0	CCM_CLKO1		KEY_COL5	ASRC_EXT_CLK	EPIT1_OUT	GPIO1_IO00	USB_H1_PWR	SNVS_VIO_5
196	W2	ENET_RXD0	XTALOSC_OSC32K_32K_OUT	ENET_RX_DATA0	ESAI_TX_HF_CLK	SPDIF_OUT		GPIO1_IO27		
197	T6	KEY_COL4	FLEXCAN2_TX	IPU1_SISG4	USB_OTG_OC	KEY_COL4	UART5_RTS_B	GPIO4_IO14		
199	V5	KEY_ROW4	FLEXCAN2_RX	IPU1_SISG5	USB_OTG_PWR	KEY_ROW4	UART5_CTS_B	GPIO4_IO15		
200	W6	KEY_COL2	ECSPI1_SS1	ENET_RX_DATA2	FLEXCAN1_TX	KEY_COL2	ENET_MDC	GPIO4_IO10	USB_H1_PWR_CTL_WAKE	
202	W4	KEY_ROW2	ECSPI1_SS2	ENET_TX_DATA2	FLEXCAN1_RX	KEY_ROW2	SD2_VSELECT	GPIO4_IO11	HDMI_TX_CEC_LINE	
203	T1	GPIO_2	ESAI_TX_FS		KEY_ROW6			GPIO1_IO02	SD2_WP	MLB_DATA
205	B21	SD1_CMD	SD1_CMD	ECSPI5_MOSI	PWM4_OUT	GPT_COMPARE1		GPIO1_IO18		
206	D20	SD1_CLK	SD1_CLK	ECSPI5_SCLK	XTALOSC_OSC32K_32K_OUT	GPT_CLKIN		GPIO1_IO20		
207	N6	CSI0_DAT8	IPU1_CSI0_DATA08	EIM_DATA06	ECSPI2_SCLK	KEY_COL7	I2C1_SDA	GPIO5_IO26		ARM_TRACE05
208	P4	CSI0_MCLK	IPU1_CSI0_HSYNC			CCM_CLKO1		GPIO5_IO19		ARM_TRACE_CTL
209	C20	SD1_DAT1	SD1_DATA1	ECSPI5_SS0	PWM3_OUT	GPT_CAPTURE2		GPIO1_IO17		
210	P1	CSI0_PIXCLK	IPU1_CSI0_PIXCLK					GPIO5_IO18		ARM_EVENTO
211	F18	SD1_DAT3	SD1_DATA3	ECSPI5_SS2	GPT_COMPARE3	PWM1_OUT	WDOG2_B	GPIO1_IO21	WDOG2_RESET_B_DEB	
212	A21	SD1_DAT0	SD1_DATA0	ECSPI5_MISO		GPT_CAPTURE1		GPIO1_IO16		
214	E19	SD1_DAT2	SD1_DATA2	ECSPI5_SS1	GPT_COMPARE2	PWM2_OUT	WDOG1_B	GPIO1_IO19	WDOG1_RESET_B_DEB	
219	J23	EIM_CS1	EIM_CS1_B	IPU1_DI1_PIN06	ECSPI2_MOSI			GPIO2_IO24		
221	J24	EIM_OE	EIM_OE_B	IPU1_DI1_PIN07	ECSPI2_MISO			GPIO2_IO25		
222	D24	EIM_D18	EIM_DATA18	ECSPI1_MOSI	IPU1_DI0_PIN07	IPU2_CSI1_DATA17	IPU1_DI1_D0_CS	GPIO3_IO18	I2C3_SDA	
223	H24	EIM_CS0	EIM_CS0_B	IPU1_DI1_PIN05	ECSPI2_SCLK			GPIO2_IO23		
224	F21	EIM_D17	EIM_DATA17	ECSPI1_MISO	IPU1_DI0_PIN06	IPU2_CSI1_PIXCLK	DCIC1_OUT	GPIO3_IO17	I2C3_SCL	
225	K20	EIM_RW	EIM_RW	IPU1_DI1_PIN08	ECSPI2_SS0			GPIO2_IO26		SRC_BOOT_CFG29
226	C25	EIM_D16	EIM_DATA16	ECSPI1_SCLK	IPU1_DI0_PIN05	IPU2_CSI1_DATA18	HDMI_TX_DDC_SDA	GPIO3_IO16	I2C2_SDA	
PIN	CPU BALL	PADNAME	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7

PIN	CPU BALL	PADNAME	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
227	K22	EIM_LBA	EIM_LBA_B	IPU1_DI1_PIN17	ECSPI2_SS1			GPIO2_IO27		SRC_BOOT_CFG26
228	E22	EIM_EB2	EIM_EB2_B	ECSPI1_SS0		IPU2_CSI1_DATA19	HDMI_TX_DDC_SCL	GPIO2_IO30	I2C2_SCL	SRC_BOOT_CFG30
230	U21	ENET_CRS_DV		ENET_RX_EN	ESAI_TX_CLK	SPDIF_EXT_CLK		GPIO1_IO25		
231	U5	KEY_COL3	ECSPI1_SS3	ENET_CRS	HDMI_TX_DDC_SCL	KEY_COL3	I2C2_SCL	GPIO4_IO12	SPDIF_IN	
233	T7	KEY_ROW3	XTALOSC_OSC32K_32K_OUT	ASRC_EXT_CLK	HDMI_TX_DDC_SDA	KEY_ROW3	I2C2_SDA	GPIO4_IO13	SD1_VSELECT	
234	B20	SD4_DAT6		SD4_DATA6	UART2_CTS_B			GPIO2_IO14		
235	R4	GPIO_5	ESAI_TX2_RX3		KEY_ROW7	CCM_CLKO1		GPIO1_IO05	I2C3_SCL	ARM_EVENTI
236	D19	SD4_DAT7		SD4_DATA7	UART2_TX_DATA			GPIO2_IO15		
237	R2	GPIO_16	ESAI_TX3_RX2	ENET_1588_EVENT2_IN	ENET_REF_CLK	SD1_LCTL	SPDIF_IN	GPIO7_IO11	I2C3_SDA	JTAG_DE_B
238	E18	SD4_DAT4		SD4_DATA4	UART2_RX_DATA			GPIO2_IO12		
240	C19	SD4_DAT5		SD4_DATA5	UART2_RTS_B			GPIO2_IO13		
241	G21	EIM_D19	EIM_DATA19	ECSPI1_SS1	IPU1_DI0_PIN08	IPU2_CSI1_DATA16	UART1_CTS_B	GPIO3_IO19	EPIT1_OUT	
243	M1	CSI0_DAT10	IPU1_CSI0_DATA10	AUD3_RXC	ECSPI2_MISO	UART1_TX_DATA		GPIO5_IO28		ARM_TRACE07
245	M3	CSI0_DAT11	IPU1_CSI0_DATA11	AUD3_RXFS	ECSPI2_SS0	UART1_RX_DATA		GPIO5_IO29		ARM_TRACE08
247	G20	EIM_D20	EIM_DATA20	ECSPI4_SS0	IPU1_DI0_PIN16	IPU2_CSI1_DATA15	UART1_RTS_B	GPIO3_IO20	EPIT2_OUT	
255	L6	CSI0_DAT19	IPU1_CSI0_DATA19	EIM_DATA15		UART5_CTS_B		GPIO6_IO05		
256	L4	CSI0_DAT16	IPU1_CSI0_DATA16	EIM_DATA12		UART4_RTS_B		GPIO6_IO02		ARM_TRACE13
257	M6	CSI0_DAT18	IPU1_CSI0_DATA18	EIM_DATA14		UART5_RTS_B		GPIO6_IO04		ARM_TRACE15
258	E25	EIM_D27	EIM_DATA27	IPU1_DI1_PIN13	IPU1_CSI0_DATA00	IPU2_CSI1_DATA13	UART2_RX_DATA	GPIO3_IO27	IPU1_SISG3	IPU1_DISP1_DATA23
259	E24	EIM_D26	EIM_DATA26	IPU1_DI1_PIN11	IPU1_CSI0_DATA01	IPU2_CSI1_DATA14	UART2_TX_DATA	GPIO3_IO26	IPU1_SISG2	IPU1_DISP1_DATA22
260	N22	EIM_BCLK	EIM_BCLK	IPU1_DI1_PIN16				GPIO6_IO31		
261	L3	CSI0_DAT17	IPU1_CSI0_DATA17	EIM_DATA13		UART4_CTS_B		GPIO6_IO03		ARM_TRACE14
262	W23	ENET_RX_ER	USB_OTG_ID	ENET_RX_ER	ESAI_RX_HF_CLK	SPDIF_IN	ENET_1588_EVENT2_OU	GPIO1_IO24		
263	R6	GPIO_4	ESAI_TX_HF_CLK		KEY_COL7			GPIO1_IO04	SD2_CD_B	
PIN	CPU BALL	PADNAME	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7

6. Ordering information, Evaluation Components and Accessories

TechNexion provides a complete product portfolio for the EDM1-IMX6 to assist our customers to evaluate, proto-type, integrate and mass produce solutions with our EDM System on Modules.

6.1. Product Ordering Part Numbers

The EDM1-IMX6 is available in a number of standard configurations. Custom tailored versions with other memory configuration, de-population of interfaces or extended and industrial temperature options are available upon request.

6.1.1 Standard Part Numbers

Standard part numbers can be easily found on the EDM1-IMX6 product page on the TechNexion corporate homepage.

6.1.2. Custom Part Number Creation Rules

The EDM1-IMX6 can be ordered in custom tailored to meet special application requirements and conditions according to the following custom part number creation rules.

Custom part numbers carry minimum order quantities. Please connect with your TechNexion representative for conditions and availability.

Part number format:

EDM1-IMX6Q10-R20-E04-BW-xx-xxxx

Interface	Code	Description
Processor	S	i.MX6 Solo
	U	i.MX6 Duallite
	D	i.MX6 Dual
	Q	i.MX6 Quad
	QP	i.MX6 QuadPlus
CPU Speed	10	1Ghz
Memory	R05	512 MB DDR3
	R10	1GB DDR3
	R20	2GB DDR3
Storage	E16	eMMC 16GB (Default)
	Exx	Other capacities of eMMC are possible (32GB, 64GB)
Wireless Networking	-	No
	9377	Qualcomm QCA9377 802.11a/b/g/n/ac (2.4 + 5GHz) + Bluetooth 5
Temperature Range	-	Commercial Temperature range (0~60°C) (Default)
	TE	Extended Temperature range (-20~70°C)
	TI	Industrial Temperature range (-40~85°C)
Custom ID	XXXX	Custom Partnumber ID for customized software loader and special component (BOM)

7. Important Notice

TechNexion reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TechNexion terms and conditions of sale supplied at the time of order acknowledgment.

TechNexion warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TechNexion's standard warranty. Testing and other quality control techniques are used to the extent TechNexion deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TechNexion assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TechNexion components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

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TechNexion products are not authorized for use in safety-critical applications (such as life support) where a failure of the TechNexion product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TechNexion products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TechNexion. Further, Buyers must fully indemnify TechNexion and its representatives against any damages arising out of the use of TechNexion products in such safety-critical applications.

TechNexion products are neither designed nor intended for use in military/aerospace applications or environments unless the TechNexion products are specifically designated by TechNexion as military grade or "enhanced plastic." Only products designated by TechNexion as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TechNexion products which TechNexion has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TechNexion products are neither designed nor intended for use in automotive applications or environments unless the specific TechNexion products are designated by TechNexion as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TechNexion will not be responsible for any failure to meet such requirements.

8. DISCLAIMER

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