Arun Subramaniyan

Research interests: Computer Architecture, Bioinformatics

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Education

- **University of Michigan** — Ann Arbor, MI
  PhD. Candidate, Computer Science and Engineering; GPA: 4.0 — *Aug. 2016 – present*
- **Birla Institute of Technology and Science** — Pilani, India
  B.E.(Hons) in Electrical and Electronics; GPA: 9.62/10.0 — *Aug. 2011 – July. 2015*

Experience

- **University of Michigan** — Ann Arbor, MI
  Graduate Student Research Assistant, Advisor: Reetuparna Das — *Aug 2016 - present*
  - **Hardware Acceleration of FASTQ to VCF pipeline**: The goal of this project is to enable FPGA-accelerated variant calling in the cloud (e.g., AWS EC2 F1) while retaining accuracy. Towards, this end we propose hardware-software co-designed solutions to accelerate the key time consuming computations in the BWA-GATK pipeline: seeding, seed-extension and variant calling for short reads. For seeding we propose a string index structure called *enumerated radix trees* that trades off memory space for memory bandwidth while improving locality of access. Seed extension uses a novel String Independent Local Levenshtein Automata (*Silla*). We are currently investigating pruning techniques to reduce computation in the Haplotype Caller.
  - **In-Memory Automata Processing**: In this project we leverage enumerative parallelization techniques to accelerate finite state automata computation on Micron's Automata Processor. Further, we developed techniques to re-purpose the last level caches in general purpose processors for automata processing using novel SRAM-based interconnects. To support parsing of recursively nested data, we also developed a custom datapath for deterministic pushdown automata computation in cache.
  - **Bit-Serial Arithmetic in Caches**: In this work, we leverage bitline computing techniques to transform the passive last-level cache real-estate in modern processors into massive bit-serial computational units. One of the key insights from this work was that caches can compute at a much higher frequency, since in-situ computation requires only SRAM lookups and does not incur the overheads of a traditional cache access.
- **Nvidia Graphics Pvt Ltd.** — Bangalore, IN
  Architect, Manager: Jay Gupta — *Aug 2015 - Aug 2016*
  - **Tegra SoC Memory Controller Architecture**: My focus was on designing high-throughput QoS-aware arbitration schemes for the various crossbars in the Xavier SoC memory controller and developing performance models for these crossbars. I was also involved in post-silicon memory subsystem performance studies and parameter tuning.
- **Karlsruhe Institute of Technology** — Karlsruhe, DE
  Student Research Assistant, Advisor: Muhammad Shafique — *Jan 2015 - Jul 2015*
  - **Reliability Adaptive Cache Hierarchies in Multi-Cores**: In this work, I showed that soft error vulnerability of the cache hierarchy is highly dependent on the access patterns of applications and the parameters of different cache levels. Towards this end, I developed cache vulnerability models considering vulnerability interdependencies among cache levels and applied these models to simultaneously reconfigure multiple cache levels to improve their reliability against soft errors.

Publications

- **GenAx: A Genome Sequencing Accelerator**: Daichi Fujiki*, Arun Subramaniyan*, Tianjun Zhang*, Yu Zeng, Reetuparna Das, David Blaauw, Satish Narayanasamy, ISCA'18. *equal contribution
- **Neural Cache: Bit-Serial In-Cache Acceleration of Deep Neural Networks**: Charles Eckert, Xiaowei Wang, Jingcheng Wang, Arun Subramaniyan, Ravi Iyer, Dennis Sylvester, David Blaauw, Reetuparna Das, ISCA'18
- **ASPEN: A Scalable In-SRAM Architecture for Pushdown Automata**: Kevin Angstadt, Arun Subramaniyan, Elaheh Sadredini, Reza Rahimi, Kevin Skadron, Westley Weimer, Reetuparna Das, MICRO'18
- **Parallel Automata Processor**: Arun Subramaniyan, Reetuparna Das, ISCA'17
- **Cache Automaton**: Arun Subramaniyan, Jingcheng Wang, Ezhil R.M. Balasubramanian, David Blaauw, Dennis Sylvester, Reetuparna Das, MICRO'17
- **Compute Caches**: Shaizeen Aga, Supreet Jeloka, Arun Subramaniyan, Satish Narayanasamy, David Blaauw, Reetuparna Das, HPCA'17
- **Soft Error-Aware Architectural Exploration for Designing Reliability Adaptive Cache Hierarchies in Multi-Cores**: Arun Subramaniyan, Semeen Rehman, Muhammad Shafique, Akash Kumar, Jörg Henkel, DATE'17
- **R^{2}Cache: Reliability-Aware Reconfigurable Last-Level Cache Architecture for Multi-Cores**: Florian Kriebel, Arun Subramaniyan, Semeen Rehman, Segnon Jean Bruno Ahandagbe, Muhammad Shafique, Jörg Henkel, CODES+ISSS'15, *Best Paper Award*

Awards

- **UM Precision Health Scholar Award, 2018.** One of 12 recipients of university-wide precision health initiative.
- **Rackham International Student Fellowship, 2017.** This is a university-wide award given to 25 international graduate students for outstanding academic performance.
- **CFAR Annual Review Workshop Demo Winner, 2016.** Awarded as co-author of Compute Caches which enables in-place computation in caches. This workshop showcased nearly 50 projects in computer architecture related topics from several leading institutions..

Service

- **CS KickStart:** Co-organizer for the CS KickStart hardware lab (2017, 2018), a workshop aimed at improving gender diversity in computer science through increased female enrollments.

Technical Skills

- **Languages:** C, C++, Java, Python, Verilog HDL
- **Software tools:** BWA-MEM, Picard Tools, GATK, Murphi, LLVM
- **Architectural simulators:** gem5, Snipersim
- **Version Control:** git, Perforce