Term Project MPI
Group 2: Microwave Oven

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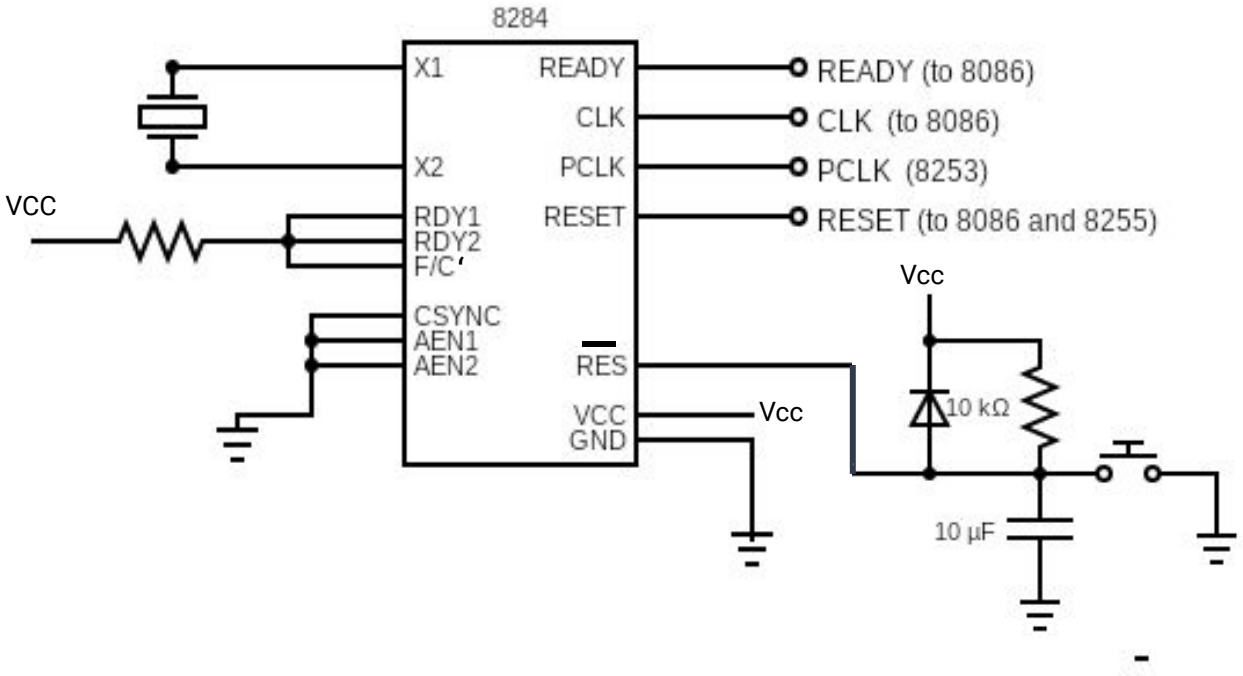
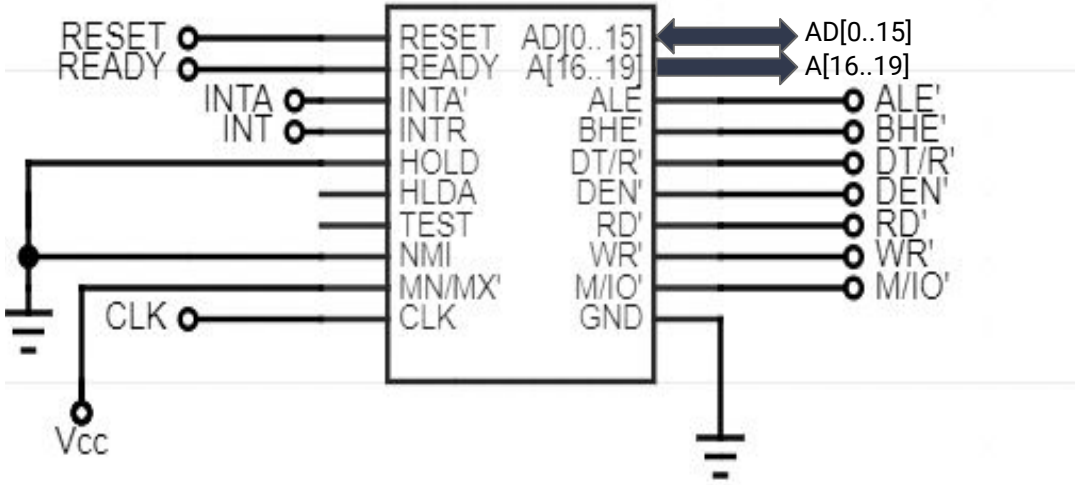
8284: Timing Signal Generator



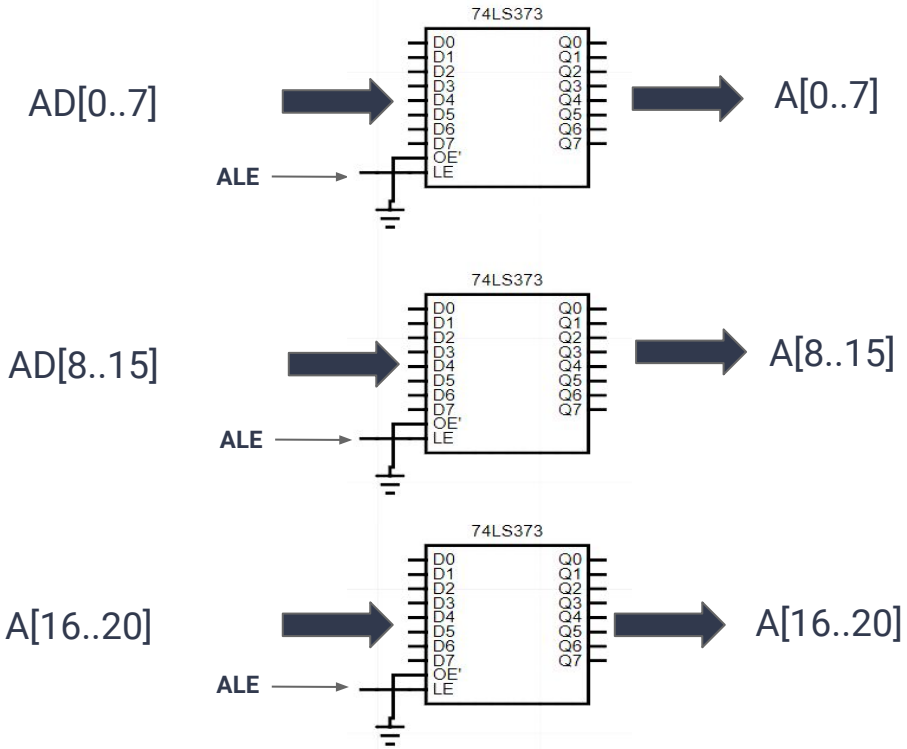
- The Crystal used is of 15 MHz.
- The pins ASYNC, EFI and OSC have not been depicted as they are not required for our design.

8086 pin out



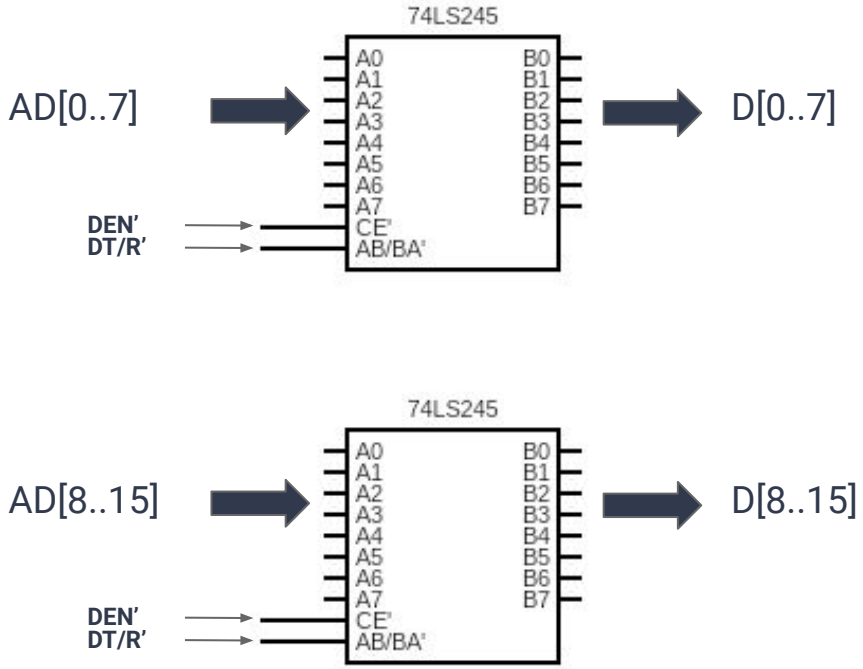
- Reset and Ready are given by the 8284
- The CLK signal also comes from the 8284 at 5 MHz
- We are not using NMIs and the INTR and INTA’ are connected to the 8259
- VCC and VDD are not depicted here, but are both connected to +5V.
- HLDA and TEST don’t have any connections

ADDRESS LINE DEMULTIPLEXING



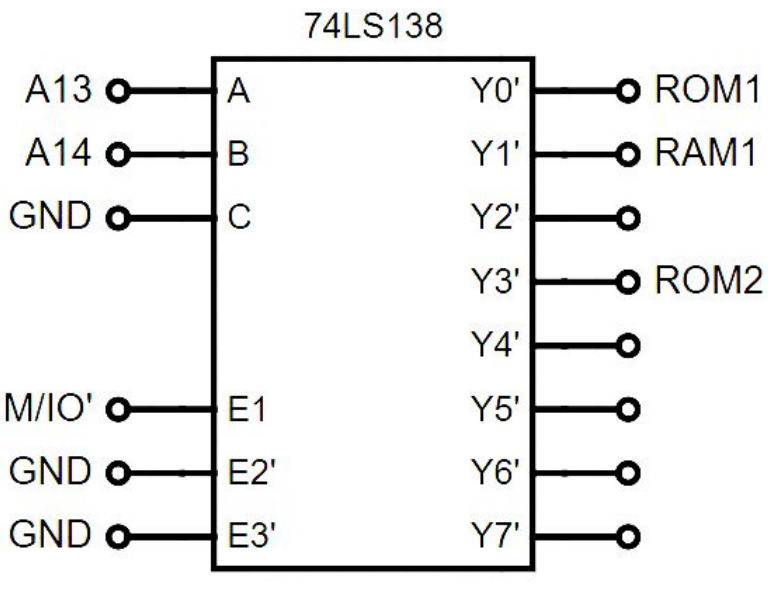
- The ALE signal comes from the 8086
- ⇨ Coming in from the 8086
- ⇨ Going out from the octal latch to be used in MEM and I/O access.

DATA LINE DEMULTIPLEXING

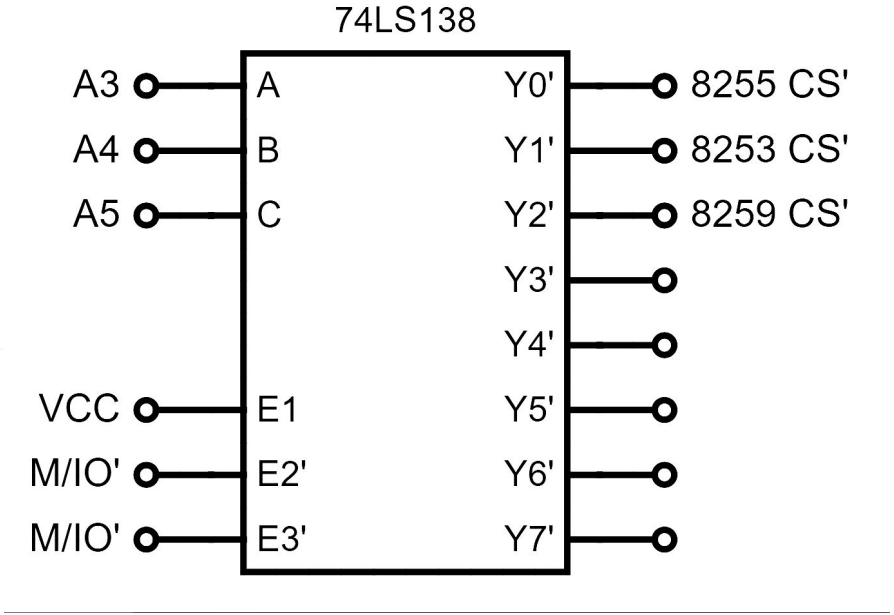


- The DEN' and DT/R' signals comes from the 8086
- ⇒ Coming in from the 8086
- ⇒ Going out from the octal latch to be used in MEM and I/O operations.

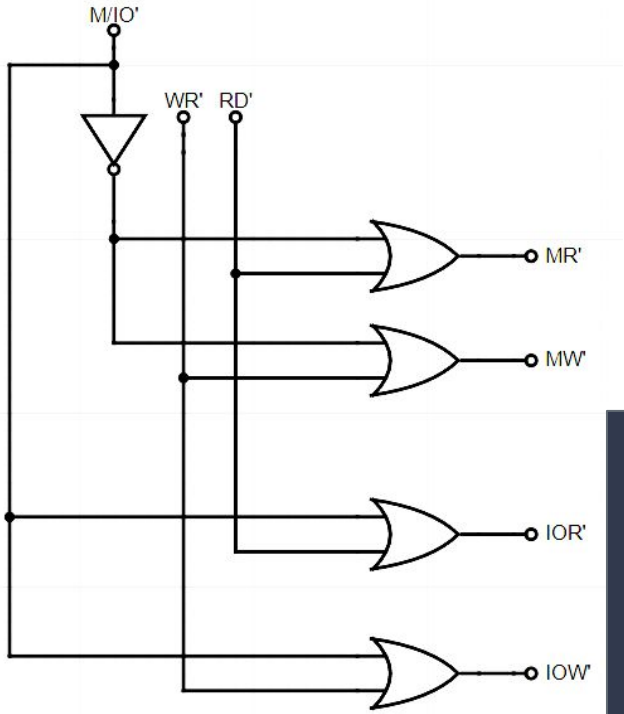
Memory Decoder

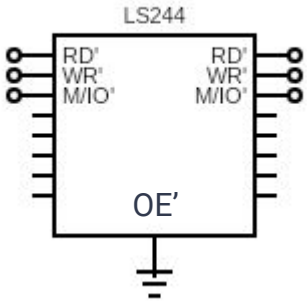


I/O Decoder



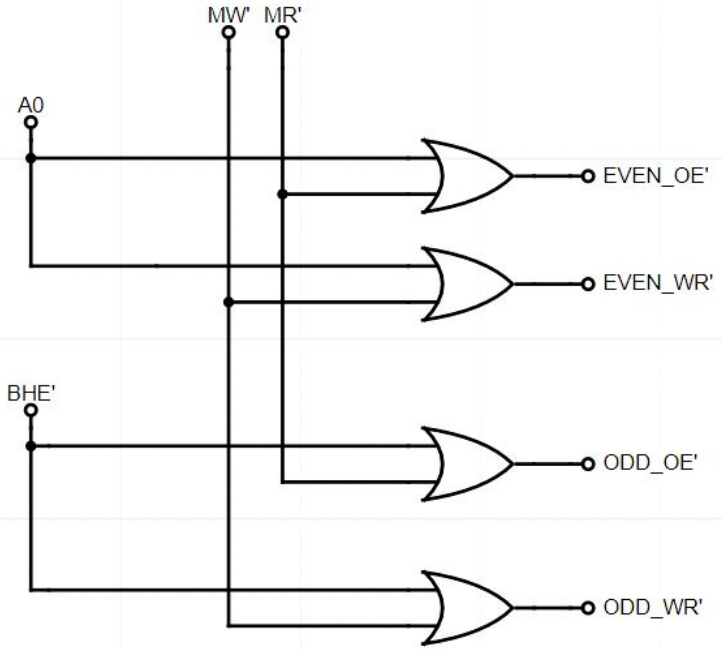
Control Signals



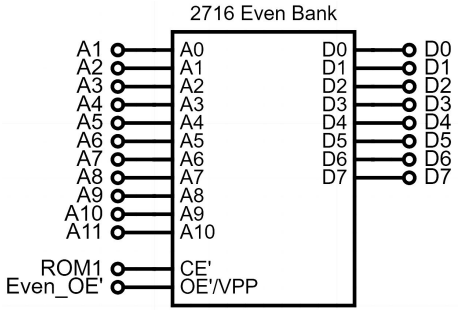


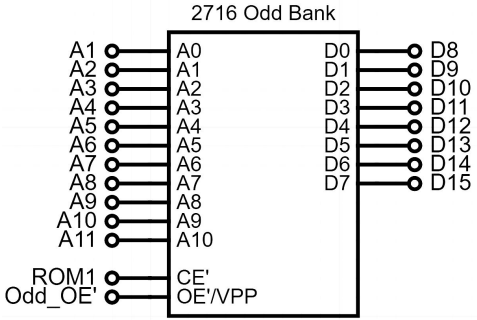
The LS244 buffer does not alter the signal and is always active

Bank Signals

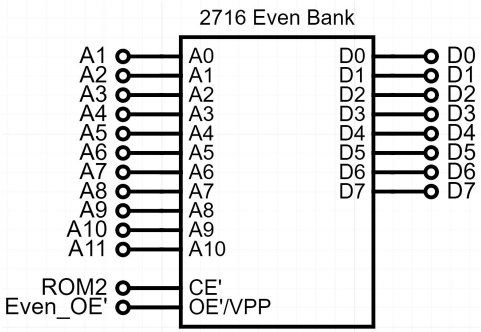


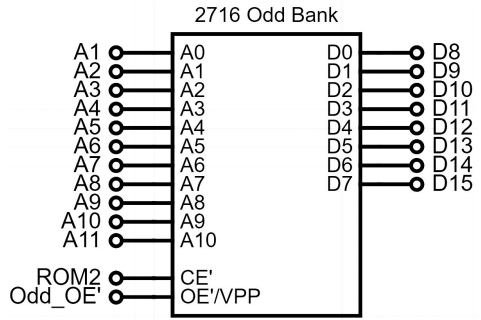
ROM 1


2716 Even Bank
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
ROM1
Even_OE'
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
CE'
OE'/VPP
D0
D1
D2
D3
D4
D5
D6
D7
D0
D1
D2
D3
D4
D5
D6
D7

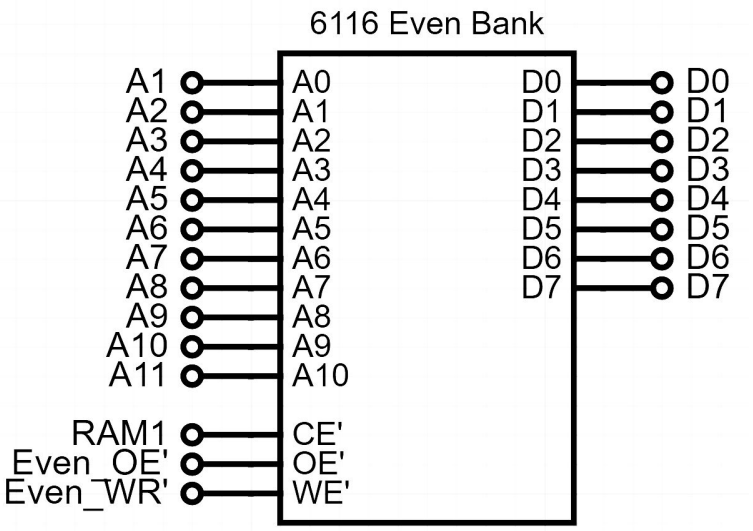

2716 Odd Bank
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
ROM1
Odd_OE'
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
CE'
OE'/VPP
D0
D1
D2
D3
D4
D5
D6
D7
D8
D9
D10
D11
D12
D13
D14
D15

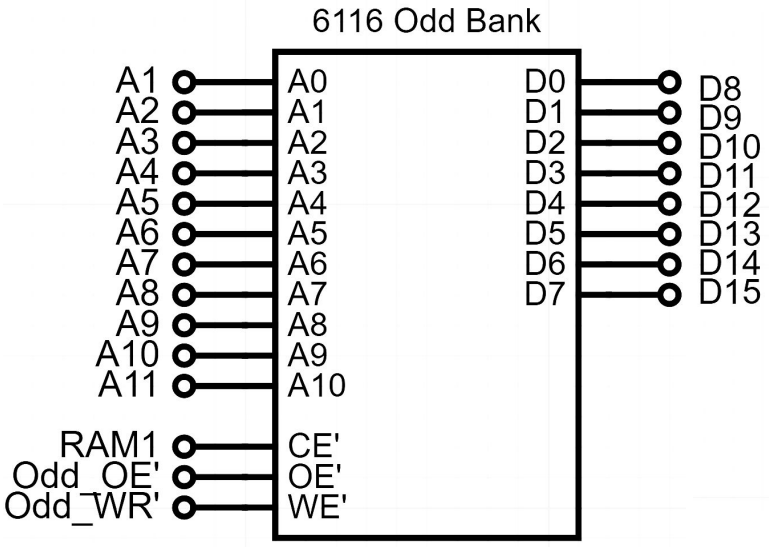
ROM 2


2716 Even Bank
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
ROM2
Even_OE'
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
CE'
OE'/VPP
D0
D1
D2
D3
D4
D5
D6
D7
D0
D1
D2
D3
D4
D5
D6
D7

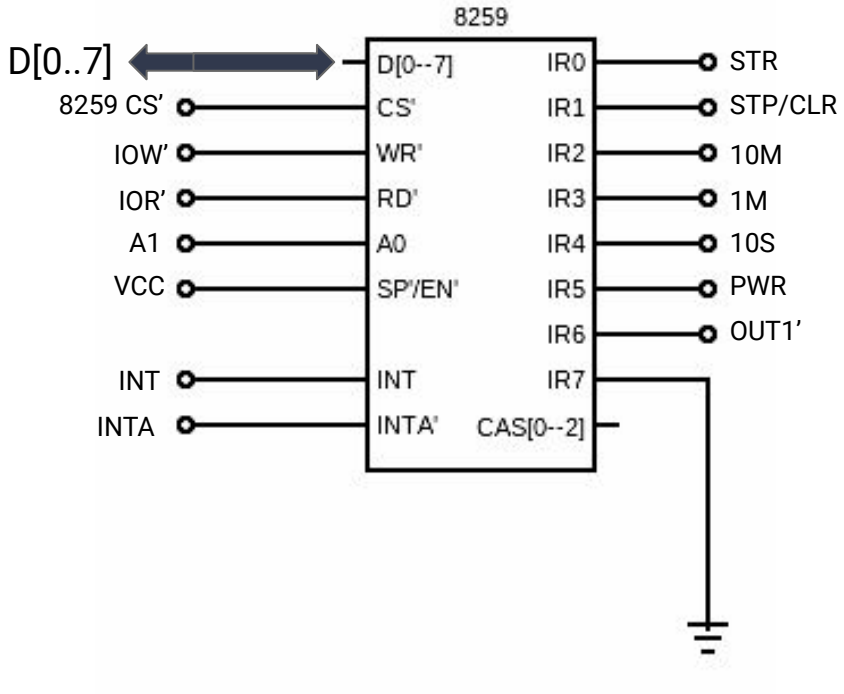

2716 Odd Bank
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
ROM2
Odd_OE'
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
CE'
OE'/VPP
D0
D1
D2
D3
D4
D5
D6
D7
D8
D9
D10
D11
D12
D13
D14
D15

RAM


6116 Even Bank
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
RAM1
Even_OE'
Even_WR'
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
CE'
OE'
WE'
D0
D1
D2
D3
D4
D5
D6
D7
D0
D1
D2
D3
D4
D5
D6
D7

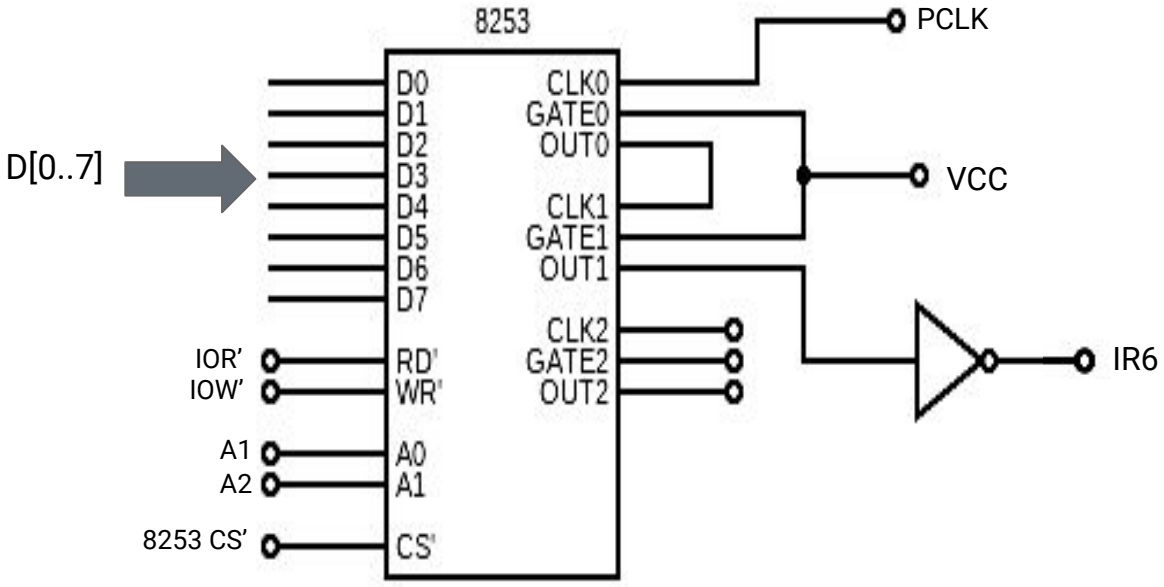

6116 Odd Bank
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
RAM1
Odd_OE'
Odd_WR'
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
CE'
OE'
WE'
D0
D1
D2
D3
D4
D5
D6
D7
D8
D9
D10
D11
D12
D13
D14
D15

8259 interfacing



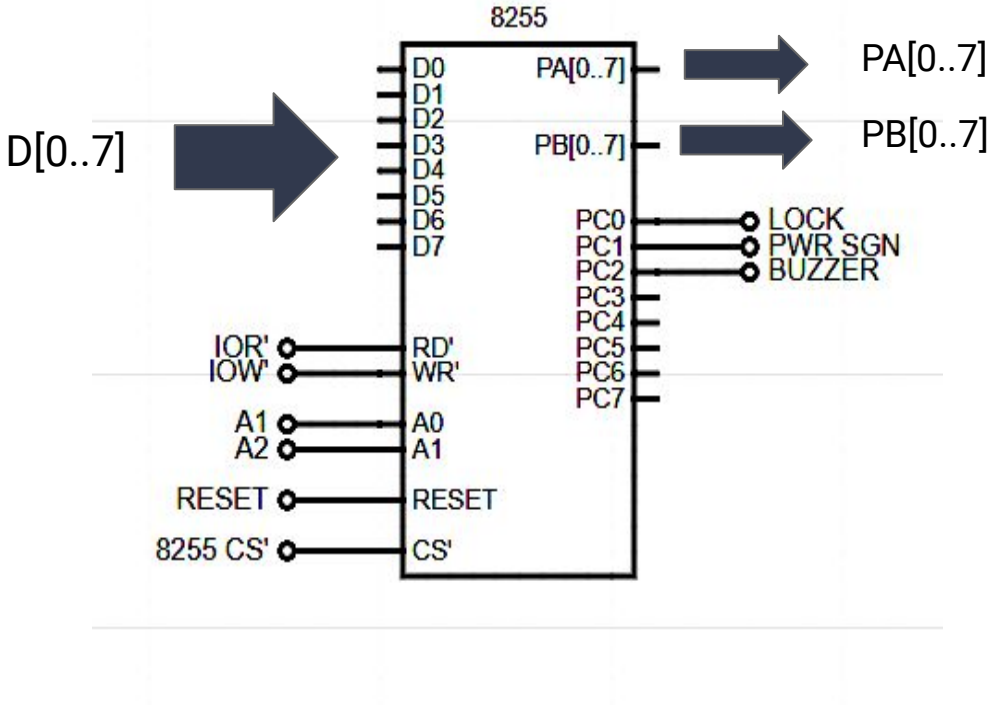
- The CS' is coming from the I/O decoder circuitry
- INT and INTA' are directly connected to the 8086
- CAS[0..2] is not used as there is only 1 8259 in the system
- IR0-5 are connected to their respective buttons
- IR6 is the OUT1' from the 8253 acts as the 1HZ signal for the timer ISR
- IR7 is not used, hence Grounded and masked

8253 interfacing



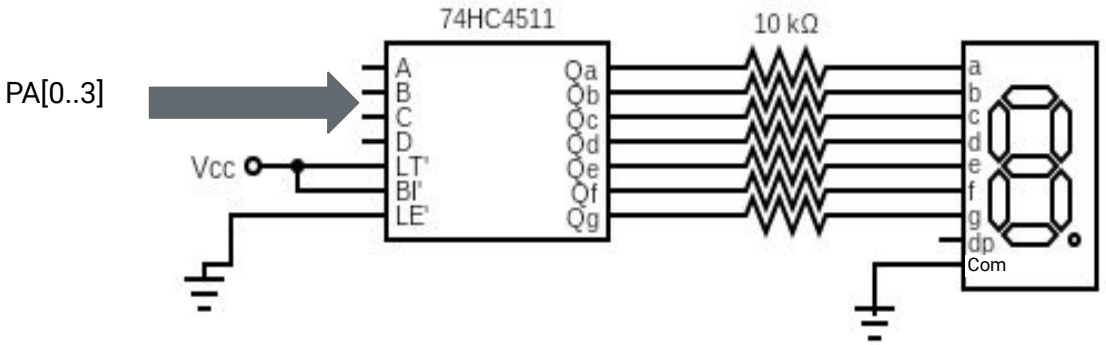
- The CS' is coming from the I/O decoder circuitry
- The PCLK is the 2.5 MHz signal from the 8284
- The IR6 is going to the 8259
- CLK2 and its respective gate and output are not in use

8255



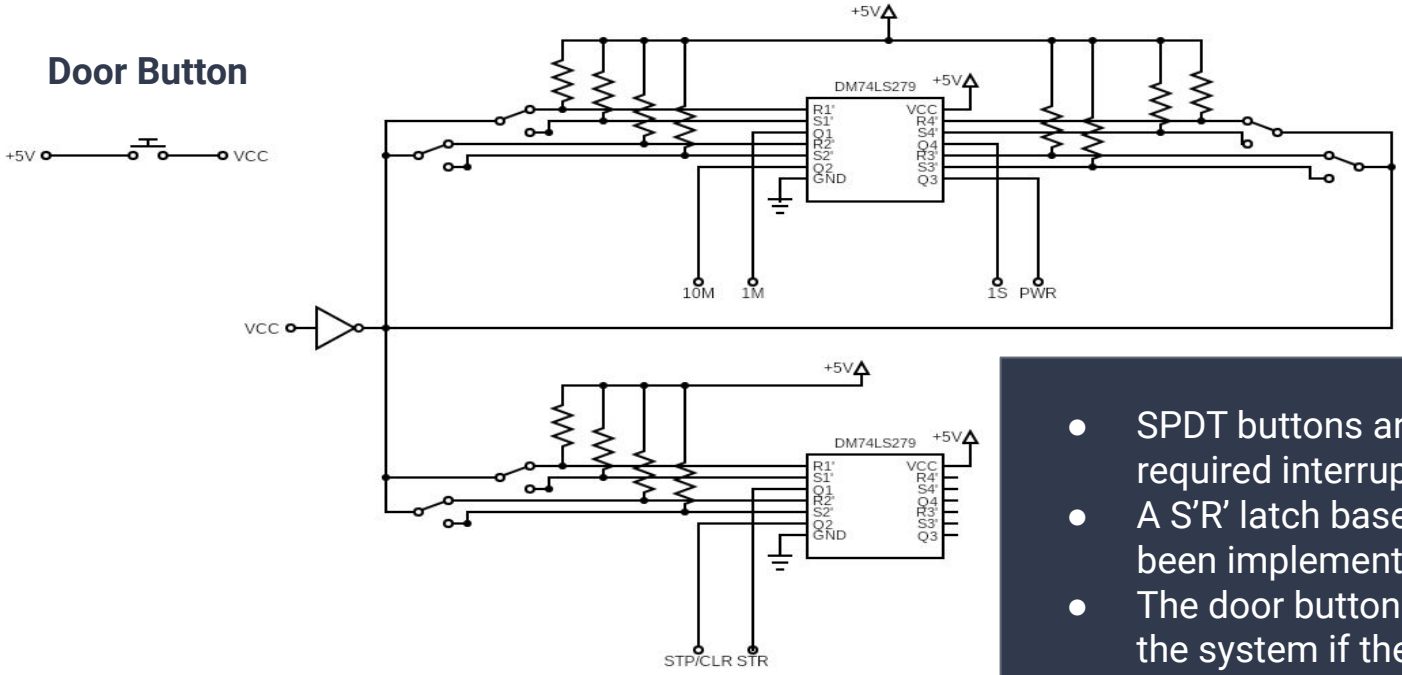
- The CS' is coming from the I/O decoder circuitry
- RESET is coming from 8284
- Port A and Port B are connected to the 7 Seg displays
- Port C is being used in BSR mode
- PC0 is controlling the lock
- PC1 is providing the signal at the requested Power Level
- PC2 is controlling the buzzer when required.

7 SEG



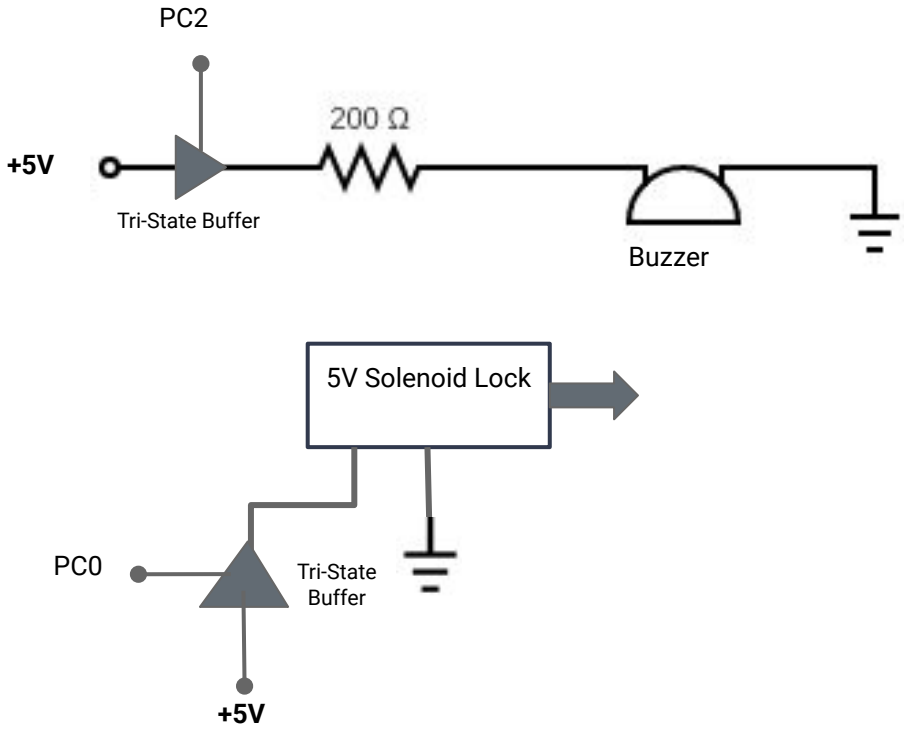
- This is the MSB of the timer/power level display
- The other 7 Seg displays are connected similarly with PA[4..7], PB[0..3] and PB[4..7]
- The Ports A and B are always active and and controlled in the MAIN loop
- The decimal point(dp) pin is not connected to anything

Command Buttons & Door Check Button



- SPDT buttons are being used to raise the required interrupts to the 8259
- A S'R' latch based debounce circuitry has been implemented for the buttons.
- The door button connects the powerline to the system if the door is closed and contact is made.

Buzzer & Lock



- The SN74AUC1G126 Tri State buffer is used to provide the required voltage to the output devices
- The Buzzer power is controlled by the PC2 port of 8255
- The Lock power is controlled by the PC0 port of 8255