all_fanin

NAME

all_fanin

Reports pins, ports, or cells in the fanin of specified sinks.

SYNTAX

```
collection all_fanin
    -to sink_list
    [-startpoints_only]
    [-exclude_bboxes]
    [-break_on_bboxes]
    [-only_cells]
    [-flat]
    [-levels count]
    [-trace_arcs arc_type]
```

Data Types

sink_list	list
count	int

ARGUMENTS

-to *sink_list*

Reports a list of sink pins, ports, or nets in the design and a timing fanin of each sink in the *sink_list*. If you specify a net, the effect is the same as listing all driver pins on the net.

-startpoints_only

Returns only the timing startpoints.

-exclude_bboxes

Excludes black boxes from the final result.

-break_on_bboxes

Stops timing fanin traversal on black boxes.

-only_cells

Results in a set of all cells in the timing fanin of the *sink_list*.

-flat

Specifies to function in the flat mode of operation. The two major modes in which **all_fanin** functions are

hierarchical (the default) and flat. When in hierarchical mode, only objects from the same hierarchy level as the current sink are returned. Thus, pins within a level of hierarchy lower than that of the sink are used for traversal but are not reported.

-levels ***count***

Stops traversal when reaching the perimeter of the search of *count* hops, where counting is performed over the layers of cells that are equidistant from the sink.

-trace_arcs ***arc_type***

Specifies the type of combinational arcs to trace during the traversal. Allowed values are **timing**, which permits the tracing only of valid timing arcs (arcs that are neither disabled nor invalid due to case analysis), and **all**, which permits tracing of all combinational arcs regardless of either case analysis or arc disabling. The default in Design Compiler (both in topographical mode and non-topographical mode) is **timing**. The default in DC Explorer is **all**. You can change the default by setting the **fanin_fanout_trace_arcs** variable to the desired value.

DESCRIPTION

The **all_fanin** command reports the timing fanin of specified sink pins, ports, or nets in the design. A pin is considered to be in the timing fanin of a sink if there is a timing path through combinational logic from the pin to that sink. The fanin report stops at the clock pins of registers (sequential cells).

Multicorner-Multimode Support

Depending on the options used, this command either uses the current scenario or has no dependency on scenario-specific information.

EXAMPLES

The following examples show the timing fanin of a port in the design. The design comprises three inverters in a chain named *iv1*, *iv2*, and *iv3*. The *iv1* and *iv2* inverters are hierarchically combined in a larger cell named *ii2*.

```
prompt> all_fanin -to tout
{ii2/hin iv3/in iv3/out tin ii2/hout tout}

prompt> all_fanin -to tout -flat
{ii2/iv1/U1/a ii2/iv2/U1/z tin iv3/U1/a ii2/iv1/U1/z
ii2/iv2/U1/a iv3/U1/z tout}
```

SEE ALSO

all_fanout(2)
report_transitive_fanin(2)