dft_drc

NAME

dft_drc

Checks the current design against test design rules.

SYNTAX

```
status dft_drc
    [-pre_dft]
    [-verbose]
    [-coverage_estimate]
    [-sample percentage]
```

ARGUMENTS

-pre_dft

Specifies that only pre-DFT rules (D rules) are checked. By default, the state of the design determines the rules that are checked. The state of the design is automatically determined using attributes. For scan-routed designs, post-DFT rules are checked; otherwise pre-DFT rules are checked.

-verbose

Controls the amount of detail when displaying violations. If specified, every violation instance is displayed. By default, only the first instance and the number of instances are displayed.

-coverage_estimate

Generates a test coverage estimate at the end of design rule checking.

-sample *percentage*

Specifies a sample percent of faults to be considered when estimating test coverage. This option must be used in conjunction with the **-coverage_estimate** option.

DESCRIPTION

This command checks the current design against the test design rules of the scan test implementation specified by the **set_scan_configuration -style** command. If there are unconnected test modes and functional Autofix clocks, they are constrained as needed.

If design rule violations are found, the appropriate messages are generated.

Perform test design rule checking on a design before performing any other DFT Compiler operations, such as **insert_dft**.

This command requires the existence of a valid test protocol. The test protocol can be generated using the

create_test_protocol command or read using the **read_test_protocol** command.

The severity of violations falls under one of the following categories:

- Information indicates no action is required.
- Warning indicates that you should analyze the violations. These might violate sequential cells resulting in their exclusion from scan chains. However, they do not prevent you from running certain DFT Compiler commands.
- Fatal violations stop you from proceeding. Certain DFT Compiler commands cannot be run.

If you start with a design with pre-existing scan structures, the scan information for inference must be specified with **-view** as **existing_dft** for the **set_dft_signal** and **set_scan_path** commands and run the **create_test_protocol** command.

The \fb-coverage option generates test coverage statistics for the current design. The option does not allow you to save or write out test patterns. The number generated is only an estimate and might be different from the one generated by an ATPG tool.

If you are running the command in the Design Vision environment, you can use the violation browser to analyze violations.

EXAMPLES

The following command performs test design-rule checking for the current design, and illustrates the types of messages that are printed:

```
prompt> current_design des1

prompt> set_scan_configuration -methodology full_scan \
        -style multiplexed_flip_flop

prompt> set_dft_signal -view existing_dft -type Constant \
        -port TM1 -active_state
Accepted dft signal specification.
1

prompt> set_dft_signal -view existing_dft -type Constant \
        -port TM2 -active_state
Accepted dft signal specification.
1

prompt> set_dft_signal -view existing_dft -type MasterClock \
        -port CLK1 -timing [list 45 55]
Accepted dft signal specification.
1

prompt> create_test_protocol -infer_asynch
In all_dft mode...

Information: Starting test protocol creation. (TEST-219)
  ...reading user specified clock signals...
Information: Identified system clock port CLK1 (45.0,55.0). (TEST-265)
  ...inferring asynchronous signals...
Information: Inferred active low asynchronous control port as1. (TEST-261)
Information: Inferred active low asynchronous control port as2. (TEST-261)
1

prompt> dft_drc -ver
In all_dft mode...
  Loading test protocol
  Pre-DFT DRC enabled

Information: Starting test design rule checking. (TEST-222)
  ...basic checks...
  ...basic sequential cell checks...
        ...checking for scan equivalents...
  ...checking vector rules...
```

```
  ...checking pre-dft rules...

-------------------------------------------------------------------
Begin Pre-DFT violations...

 Warning: Clock input CP of DFF ff2 was not controlled. (D1-1)

Pre-DFT violations completed...
-------------------------------------------------------------------

-------------------------------------------------------------------
  DRC Report

  Total violations: 1

-------------------------------------------------------------------

1 PRE-DFT VIOLATION
     1 Uncontrollable clock input of flip-flop violation (D1)

Warning: Violations occurred during test design rule checking. (TEST-124)

-------------------------------------------------------------------
  Sequential Cell Report

  1 out of 2 sequential cells have violations

-------------------------------------------------------------------

SEQUENTIAL CELLS WITH VIOLATIONS
      *   1 cell has test design rule violations
          ff2
SEQUENTIAL CELLS WITHOUT VIOLATIONS
      *   1 cell is a valid scan cell
          ff1

Information: Test design rule checking completed. (TEST-123)
```

SEE ALSO

create_test_protocol(2)
current_design(2)
insert_dft(2)
preview_dft(2)
read_test_protocol(2)
set_dft_signal(2)
set_scan_path(2)
target_library(3)