set_clock_latency

NAME
SYNTAX
ARGUMENTS
DESCRIPTION
EXAMPLES
SEE ALSO

NAME

set_clock_latency

Specifies the clock latency for clocks, ports, or pins.

SYNTAX

```
status set_clock_latency
    [-rise]
    [-fall]
    [-min]
    [-max]
    [-source]
    [-early]
    [-late]
    [-dynamic jitter]
    [-clock clock_list]
    delay
    object_list
```

Data Types

jitter	float
clock_list	list
delay	float
object_list	collection

ARGUMENTS

-rise

Applies the specified latency value only to rising transitions at register clock pins. By default, the latency value applies to both rising and falling transitions at register clock pins.

-fall

Applies the specified latency value only to falling transitions at register clock pins.

-min

Applies the specified latency value only to the minimum operating condition. By default, the latency value applies to both the minimum and maximum operating conditions.

-max

Applies the specified latency value only to the maximum operating condition.

-source

Specifies the source (instead of network) latency. Source latency is the amount of delay from the ideal waveform to the source object in the design, as defined by the **create_clock** command.

By default, the delay value applies to the network latency, the amount of delay from the source object in the design to the register clock pin of the sequential device. The total latency is source latency plus network latency.

-early

Applies the specified delay value only to early source latency, for example, to calculate the clock delay to the capture register in a setup check. This option can be used only with the **-source** option. By default, when you use the **-source** option, the specified delay value applies to both early and late source latency.

-late

Applies the specified delay value only to late source latency, for example, to calculate the clock delay to the capture register in a hold check. This option can be used only with the **-source** option.

-dynamic *jitter*

Specifies the dynamic component of the clock latency, which represents the amount of jitter in the original clock source. This option can be used only with the **-source** option.

-clock *clock_list*

Applies the latency value with respect to the specified clock. This option lets you specify the relevant clock when you set the latency on a port or pin, and multiple clocks pass through the port or pin.

delay

Specifies the clock latency value, either network latency by default, or source latency if you use the **-source** option.

object_list

Specifies the clocks, ports, and pins on which to set the delay value.

DESCRIPTION

This command specifies clock latency, which is the amount of delay for a clock signal reaching the clock pin of a sequential device. You can specify two types of clock latency: network latency (the default) and source latency (by using the **-source** option).

Clock network latency is the time it takes a clock signal to propagate from the clock definition point (as defined by the **create_clock** command) to a register clock pin. The rise and fall latencies are the latencies for rising and falling transitions at the register clock pin, respectively. The tool considers inversion of the clock waveform, if present in the clock network, to determine the rising or falling sense at the register clock pin .

Clock source latency (also called insertion delay) is the time it takes for a clock signal to propagate from its actual ideal waveform origin point to the clock definition point in the design. You can use it to model off-chip clock latency when a clock generation circuit is not part of the current design. For generated clocks, you can use clock source latency to model the delay from the master clock to the generated clock definition point. You can use the **-early** and **-late** options to specify early and late clock source latencies, respectively.

The dynamic component of clock latency is the amount of jitter in the original clock source, which leads to a reduction in timing slack equal to the specified amount of time. You specify this amount by using the **-dynamic** option, which can be used only with the **-source** option. In the case of a zero-cycle path, in which the same clock edge both launches and captures data in the path, jitter does not reduce the slack; the tool takes this into account in any clock reconvergence pessimism removal adjustment performed on the path.

If multiple clocks are allowed per object, you can specify the clock latency with respect to specific clocks by using the **-clock** option. By using multiple **set_clock_latency** commands, you can specify different latency values for different clocks that pass through the same ports or pins.

By default, the tool assumes ideal clocking, which means clocks have a specified network latency (from the

set_clock_latency command) or zero network latency by default. Propagated clock network latency (from the **set_propagated_clock** command) is normally used after layout and final clock tree generation. Specifying the ideal clock network latency provides an estimate of the clock tree delay for before layout.

You can specify clock source latency using the **-source** option for both ideal and propagated clocks. The total clock latency at a register clock pin is the sum of the source latency and network latency.

When you apply the **set_clock_latency** command to pins or ports, it affects all register clock pins in the transitive fanout of the specified pins or ports. You can apply source latency only to clocks and clock source pins.

To undo the effects of the **set_clock_latency** command, use the **remove_clock_latency** command.

To report the clock network latency and clock source latency information, use the **report_clock -skew** command.

Multicorner-Multimode Support

This command applies to the current scenario only.

EXAMPLES

The following example specifies a rise latency of 1.2 and a fall latency of 0.9 for the clock named CLK1:

```
prompt> set_clock_latency 1.2 -rise [get_clocks CLK1]
prompt> set_clock_latency 0.9 -fall [get_clocks CLK1]
```

The next example specifies an early rise and an early fall source latency of 0.8, and a late rise and a late fall source latency of 0.9 for the clock named CLK1:

```
prompt> set_clock_latency 0.8 -source -early [get_clocks CLK1]
prompt> set_clock_latency 0.9 -source -late  [get_clocks CLK1]
```

The next example specifies an early and late source latency of 3 and 5 respectively with dynamic components of 0.5.

```
prompt> set_clock_latency 3 -source -early -dynamic 0.5 [get_clocks CLK1]
prompt> set_clock_latency 5 -source -late  -dynamic 0.5 [get_clocks CLK1]
```

SEE ALSO

create_clock(2)
current_design(2)
remove_clock_latency(2)
report_clock(2)
set_clock_gate_latency(2)
set_clock_transition(2)
set_clock_uncertainty(2)
set_input_delay(2)
set_propagated_clock(2)