report_power

NAME

report_power

Calculates and reports dynamic and static power for the design or instance.

SYNTAX

```
status report_power
    [-net]
    [-cell]
    [-only cell_or_net_list]
    [-hierarchy]
    [-levels level_value]
    [-verbose]
    [-flat]
    [-exclude_boundary_nets]
    [-include_input_nets]
    [-analysis_effort low | medium | high]
    [-nworst number]
    [-sort_mode mode]
    [-histogram [-exclude_leq le_val
     | -exclude_geq ge_val]]
    [-nosplit]
    [-scenarios scenario_list]
    [-groups group_list]
```

Data Types

cell_or_net_list	object_list
level_value	integer
number	integer
mode	string
le_val	float
ge_val	float
scenario_list	list
group_list	list

ARGUMENTS

-net

Reports the power consumption of nets. Use the **-net** option alone, or use it with the **-cell** option. By default, only the design's summary power information is reported when neither option is specified.

-cell

Reports the power consumption of cells. If there are physical-only cells in a hierarchical module, the physical-only cells and the nonphysical-only cells are listed separately.

When you use the **-cell** option, some entries in the power report might not apply to certain cells. The column entry for such cells is annotated with N/A. Use the **-cell** option alone or with the **-net** option to report the cells and nets. By default, only the design's summary power information is reported when neither option is specified.

In Design Compiler topographical mode, when you specify the **-cell** option, the power report includes estimated clock tree power numbers, if you do not use the **-only** option and if the power prediction was turned on in the previous run of the **compile_ultra** command. This entry is marked *CLOCK_TREE_EST* in the cell column.

-only *cell_or_net_list*

Specifies a list of cells and nets to display with the **-net** or **-cell** options. With this option, only the cells and nets in the *cell_or_net_list* are listed in the power report. If both **-net** and **-only** options are specified, the *cell_or_net_list* must contain at least one net. Similarly, if both **-cell** and **-only** options are specified, the *cell_or_net_list* must contain at least one cell.

If the **-net**, **-cell**, and **-only** options are specified together, the *cell_or_net_list* must contain at least one net and one cell. Physical-only cells in a hierarchical module are not reported unless they are explicitly specified in the cell list as shown in the following example:

```
report_power -cell -only [get_cells  hier_module/* -all]
```

-hierarchy

Specifies that the report be in a hierarchical format, with power information reported on a block-by-block basis. Use the **-levels** option to limit the number of levels of hierarchy shown in the report. The **-sort** and **-nworst** options are ignored for this report. The switching, internal, and leakage power numbers are reported for each hierarchical block. The hierarchy is shown through indentations.

In Design Compiler topographical mode, when you specify the **-hierarchy** option, the power report includes estimated clock-tree power numbers if power prediction was turned on in the last run of the **compile_ultra** command. This entry is marked *CLOCK_TREE_EST*.

-levels *level_value*

Specifies the number of levels of hierarchy to display, in the hierarchical report. You can specify a positive integer, greater than 1, with this option. Hierarchy levels deeper than those specified in this option are not shown in the hierarchical report. This option is only used for the hierarchical report and is ignored for all other types of reports.

-verbose

If the **-net** or **-cell** option is specified, it displays additional detailed information about the power information of the cells and nets. With the **report_power -verbose** specified, the power group summary displays the cell counts of the power groups.

-flat

Specifies that the power report traverse the hierarchy and report objects at all lower levels (assumes a flat design hierarchy). The default behavior is to report objects at only the current level of hierarchy. For cell report, if the **-flat** option is not specified, the power reported for a subdesign is the total power estimated for that subdesign, including all of its contents.

-exclude_boundary_nets

Specifies an option that is now obsolete.

-include_input_nets

Includes the switching power of primary input nets in the power report. The default is to exclude boundary input nets. This option affects the nets that are chosen to be displayed in the net-specific report as well as the value of the total switching power. This option does not affect the cell leakage and internal power values. When this option is specified, the sum of the power values of different power groups might be different with the summary report.

-analysis_effort low | medium | high

Provides a trade off between runtime and accuracy. The default is **low**. Specifying **low** effort results in the fastest runtime and the lowest accuracy of power estimates. Specifying **medium** or **high** effort results in a longer run with increased levels of accuracy. The analysis effort is considered only during the estimation of switching activity information, and therefore, has an effect only when the design is not fully annotated with switching activity.

-nworst *number*

Filters the report so that it displays only the highest *number* power objects. This option is valid only if either **-net** or **-cell** or both the options are specified.

-sort_mode *mode*

Determines the sorting mode for report order and **-nworst** selection. The valid sorting modes for the **-net** or **-cell** options are as follows:

-net option	**-cell** option
name	name
net_static_probability	cell_internal_power
net_switching_power	cell_leakage_power
net_toggle_rate	dynamic_power
total_net_load	

When using both **-net** and **-cell** and specifying a sorting mode, you must select a sorting mode that is valid for both options. The mode is used for both the cell and the net reports.

If you do not explicitly set the sorting mode, a default is chosen based on the mode of the **report_power** command:

Mode	Implicit default
-net	net_switching_power
-cell	cell_internal_power
-net -cell	dynamic_power

-histogram -exclude_leq *le_val* | -exclude_geq *ge_val*

Displays a histogram-style report showing the number of nets in each power range. The **-exclude_leq** and **-exclude_geq** arguments are used to exclude data values less than *le_val* or greater than *ge_val*, respectively. Useful for displaying the range and variation of power in the design. This option displays the histogram report only if either **-net** or **-cell** is specified.

-nosplit

Prevents line splitting and facilitates writing applications to extract information from the report output. Most of the design information is listed in fixed-width columns. If the information for a given field exceeds its column's width, the next field begins on a new line, starting in the correct column.

-scenarios *scenario_list*

Reports power for the specified scenarios of a multicorner-multimode design. Each scenario is reported separately. Inactive scenarios are skipped in the report. If you do not specify this option, only the current scenario is reported.

-groups *group_list*

Reports power for the specified power groups. By default all instances are placed in only 1 power group, so the sum of the predefined groups power equals the total power consumption of the design. The valid power groups of the group_list are: io_pad, memory, black_box, clock_network, register, sequential, combinational.

io_pad	cells defined as part of the pad_cell group in the library
memory	cells defined as part of the memory group in the library

```
black_box             cells with no functional description in
                      the library
clock_network         cells in the clock network excluding
                      io_pad cells
register              latches and flip-flops driven by the
                      clock network excluding io_pads and
                      black_boxes
sequential            latches and flip-flops clocked by
                      signals other than those in the clock
                      network
combinational         nonsequential cells with a functional
                      description
```

DESCRIPTION

The **report_power** command calculates and reports power for a design. The command uses the user-annotated switching activity to calculate the net switching power, cell internal power, and cell leakage power, and displays the calculated values in a power report. The **report_power** command needs switching activity information on all design nets, and uses a switching activity propagation mechanism to estimate switching activity information on nonannotated design objects.

The options enable you to specify cells and nets for reporting. The default operation is to display the summary of power values for only the current design. If a current instance is specified, the **report_power** command displays the summary power values for that instance. The power of an instance is estimated in the context of the higher-level design, which means using the switching activity and load of the higher-level design.

The **-verbose** option reports more details of the power information. The **-flat**, **-exclude_boundary_nets**, **-nworst**, and **-sort_mode** options enable the filtering of objects that are selected by the **report_power** command. The **-sort_mode** option also affects the formatting of the power reports by modifying the order of nets and cells that are displayed by the **report_power** command.

The **-histogram** option causes additional sections to be displayed in the power reports. The power histogram classifies the nets or cells into groups of power values, allowing for easier visual analysis of the range of power values and of the distribution of the nets and cells across that range. The **-histogram** option enables the pruning of objects in the histogram by excluding values greater than or less than specified values.

Power analysis uses the current tool's mechanism to obtain the loads. For example, for synthesis in nontopographical mode without parasitic back-annotation, the tool uses wire load models; it uses back-annotated capacitance information when available, and so on.

The standalone **report_power** command does not update extraction information, so it is recommended to use **extract_rc** before using **report_power**.

When you run the **report_power** command it checks-out a Power Compiler license. If a license is not available, the command terminates with an error message. Otherwise, the command proceeds normally. At the completion of the command, the Power Compiler license is released. To keep the license checked-out after the completion of the **report_power** command, set the **power_keep_license_after_power_commands** variable to **true**.

In topographical mode, if power prediction is enabled, **report_power** reports the correlated power. The reported power numbers include the power consumption by design components as well as the predicted power of missing components, such as clock tree. The correlated power is not reported if any option of the **report_power** is used.

When the leakage power model is set to **channel_width**, using the set_leakage_power_model command, the total design power reported by the **report_power** command includes the total weighted sum of the channel widths for the design.

Creation and use of scenarios is supported in Design Compiler Graphical.

Multicorner-Multimode Support

By default, this command uses information from the current scenario. You can select different scenarios by using the **-scenarios** option.

EXAMPLES

The following example shows a summary report of the **report_power** command. A medium-effort analysis is performed to estimate the design's power values.

```
prompt> report_power -analysis_effort medium

****************************************
Report : power
        -analysis_effort low
Design : ChipTop
Version: F-2011.09
Date   : Thu Jun 30 10:12:49 2011
****************************************

Library(s) Used:

    power_lib.db (File: /remote/libraries/power_lib.db)

Operating Conditions: WCCOM   Library: power_lib
Wire Load Model Mode: segmented

Design        Wire Load Model            Library
------------------------------------------------
ChipTop                ZeroWireload      power_lib.db
InstructionDecoder     ZeroWireload      power_lib.db
GeneralPurposeRegisters
                       ZeroWireload      power_lib.db

Global Operating Voltage = 0.99
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000pf
    Time Units = 1ns
    Dynamic Power Units = 1mW    (derived from V,C,T units)
    Leakage Power Units = 1uW

  Cell Internal Power  =   9.4997 mW   (81%)
  Net Switching Power  =   2.2525 mW   (19%)
                         ---------
Total Dynamic Power    =  11.7522 mW  (100%)

Cell Leakage Power     =   7.7869 uW

                 Internal        Switching          Leakage            Total
Power Group      Power           Power              Power              Power      (       %)  Attrs
--------------------------------------------------------------------------------------------------
io_pad             0.0000           0.0000           0.0000           0.0000      (   0.00%)
memory             0.0000           0.0000           0.0000           0.0000      (   0.00%)
black_box          0.0000           0.0000           0.0000           0.0000      (   0.00%)
clock_network      0.0000           0.0000           0.0000           0.0000      (   0.00%)
register           6.4008           0.2053           1.5931           6.6076      (  56.19%)
sequential         0.0000           0.0000           0.0000           0.0000      (   0.00%)
combinational      3.0989           2.0472           6.1938           5.1524      (  43.81%)
--------------------------------------------------------------------------------------------------
Total              9.4997 mW        2.2525 mW        7.7869 uW       11.7678 mW
```

The following example shows a net power report sorted by the **net_switching_power** option and filtered to display only five nets with the highest switching power. A low-effort analysis is performed to estimate the design's power values.

```
prompt> report_power -net -flat -nworst 5

****************************************
Report : power
        -net
        -analysis_effort low
        -nworst 5
        -flat
        -sort_mode net_switching_power
Design : ALARM_BLOCK
```

```
Version: v3.2a
Date   : Sun Jun 19 15:45:26 1994
****************************************

Library(s) Used:

    power_lib.db (File: /remote/libraries/power_lib.db)

Operating Conditions:
Wire Loading Model Mode: enclosed

Design           Wire Loading Model      Library
------------------------------------------------
ALARM_BLOCK            0.5K_TLM          power_lib.db
ALARM_STATE_MACHINE    0.5K_TLM          power_lib.db
ALARM_COUNTER          0.5K_TLM          power_lib.db
ALARM_COUNTER_DW01_inc_6_0
                       0.5K_TLM          power_lib.db

Global Operating Voltage = 4.75
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 50.029999ff
    Time Units = 1ns
    Dynamic Power Units = 10uW    (derived from V,C,T units)
    Leakage Power Units = 1nW

                      Total      Static   Toggle   Switching
Net                   Net Load   Prob.    Rate     Power       Attrs
--------------------------------------------------------------------------
ACOUNT/CLK              20.467     0.500   0.1000    115.5149
ACOUNT/n493             23.193     0.985   0.0250     32.7255
ASM/n225                 9.165     0.985   0.0250     12.9314
ACOUNT/HRS_OUT[3]        6.365     0.537   0.0303     10.8763
ACOUNT/HRS_OUT[2]        5.161     0.537   0.0303      8.8202
--------------------------------------------------------------------------
Total (5 nets)                                        18.0868 uW
```

The following example shows a **report_power** summary report in topographical mode with power prediction on. Note the PWR-620 information message that mentions that it is the correlated power.

```
prompt> set_power_prediction
prompt> compile_ultra -incremental
prompt> report_power -analysis_effort medium

Information: Updating design information... (UID-85)
Performing probabilistic propagation through design.

****************************************
Report : power
        -analysis_effort medium
Design : ALARM_BLOCK
Version: v3.2a
Date   : Sun Jun 19 15:45:24 1994
****************************************

Library(s) Used:

    power_lib.db (File: /remote/libraries/power_lib.db)

Operating Conditions:
Wire Loading Model Mode: enclosed

Design           Wire Loading Model      Library
------------------------------------------------
ALARM_BLOCK            0.5K_TLM          power_lib.db
ALARM_STATE_MACHINE    0.5K_TLM          power_lib.db
ALARM_COUNTER          0.5K_TLM          power_lib.db
ALARM_COUNTER_DW01_inc_6_0
                       0.5K_TLM          power_lib.db

Global Operating Voltage = 4.75
```

```
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 50.029999ff
    Time Units = 1ns
    Dynamic Power Units = 1mW    (derived from V,C,T units)
    Leakage Power Units = 1nW

 Information: Reporting correlated power. (PWR-620)

  Cell Internal Power  = 157.0383 nW   (86%)
  Net Switching Power  =  26.1555 nW   (14%)
                         ---------
Total Dynamic Power    = 183.1938 nW  (100%)

Cell Leakage Power     =   1.0225 mW
```

SEE ALSO

propagate_switching_activity(2)
set_power_prediction(2)
set_switching_activity(2)
extract_rc(2)
power_keep_license_after_power_commands(3)