all_registers

NAME

all_registers

Returns a collection of sequential cells or pins in the current design.

SYNTAX

```
collection all_registers
    [-no_hierarchy]
    [-clock clock_name]
    [-rise_clock rise_clock_name]
    [-fall_clock fall_clock_name]
    [-cells]
    [-data_pins]
    [-clock_pins]
    [-slave_clock_pins]
    [-output_pins]
    [-level_sensitive | -edge_triggered]
    [-master_slave]
```

Data Types

```
clock_name          string
rise_clock_name     string
fall_clock_name     string
```

ARGUMENTS

-no_hierarchy

Limits the search to only the current level of hierarchy. Subdesigns are not searched.

By default, the entire hierarchy is searched.

-clock *clock_name*

Considers only sequential cells clocked by the specified clock.

By default, all sequential cells in the current design are considered.

-rise_clock *rise_clock_name*

Considers only sequential cells triggered by the rising edge of the specified clock.

By default, all sequential cells in the current design are considered.

-fall_clock *fall_clock_name*

Considers only sequential cells triggered by the falling edge of the specified clock.

By default, all sequential cells in the current design are considered.

-cells

Returns a collection of sequential cells that meet the search criteria.

If you do not specify any of the object type options, the command returns a collection of sequential cells.

-data_pins

Returns a collection of data pins of the sequential cells that meet the search criteria.

-clock_pins

Returns a collection of clock pins of the sequential cells that meet the search criteria.

-slave_clock_pins

Returns a collection of slave clock pins of master-slave registers that meet the search criteria. Slave clock pins are specified as clocked_on_also in the library.

-output_pins

Returns a collection of output pins of the sequential cells that meet the search criteria.

-level_sensitive

Limits the search to level-sensitive cells.

-edge_triggered

Limits the search to edge-triggered cells.

-master_slave

Limits search to master_slave cells.

DESCRIPTION

The **all_registers** command returns a collection of sequential cells or pins in the current design, filtered as specified by the options. By default, the command returns a collection of all sequential cells in the design. If you specify *clock_name*, it considers only the sequential cells in the transitive fanout of the sources of the clock.

You can use one or more of the **-cells**, **-data_pins**, **-clock_pins**, **-slave_clock_pins**, and **-output_pins** options to return a collection containing the respective types of objects. For example, if you use **-data_pins**, the command returns a collection containing the only the data pins of the sequential cells that meet the search criteria. If you use both **-cells** and **-data_pins**, the command returns a collection containing both the sequential cells and their data pins.

Multicorner-Multimode Support

This command uses information from the current scenario only.

EXAMPLES

The following example sets max_delay targets for timing paths leading to data pins of all registers clocked by *PHI2*:

```
prompt> set_max_delay 10.0 -to [all_registers -clock PHI2 -data_pins]
```

The following example returns a list of data pins for all master-slave registers clocked by *clockB*:

```
prompt> all_registers -master_slave -data_pins -clock clockB
```

The following example returns a list of all level-sensitive cells and their clock (enable) pins:

```
prompt> all_registers -level_sensitive -cells -clock_pins
```

The following example shows how to push into an instance named *U1* and find level-sensitive cells without searching subdesigns of that instance:

```
prompt> current_instance U1

prompt> all_registers -no_hierarchy
```

SEE ALSO

create_clock(2)
current_design(2)
current_instance(2)
remove_clock(2)
set_max_delay(2)