all_fanout

NAME

all_fanout

Returns a set of pins, ports, or cells in the fanout of the specified sources.

SYNTAX

```
collection all_fanout
    -clock_tree
    -from source_list
    [-endpoints_only]
    [-exclude_bboxes]
    [-break_on_bboxes]
    [-only_cells]
    [-flat]
    [-levels count]
    [-trace_arcs arc_type]
```

Data Types

```
source_list     list
count           int
```

ARGUMENTS

-clock_tree

Uses all clock source pins and/or ports in the design as the list of sources. Clock sources are specified by using the **create_clock** command. If there are no clocks, or if the clocks have no sources, the report is empty. Use the **report_clock** command to list the sources for all clocks in the design. The **-clock_tree** option generates a report that displays the clock trees or networks in the design. The **-clock_tree** and **-from** options are mutually exclusive.

-from *source_list*

Specifies a list of source pins, ports, or nets in the design. The timing fanout of each source in the *source_list* is reported. If a net is specified, the effect is the same as listing all load pins on the net. The **-clock_tree** and **-from** options are mutually exclusive.

-endpoints_only

Returns only timing endpoints as a result.

-exclude_bboxes

Excludes black boxes from the final result.

-break_on_bboxes

Stops timing fanout traversal on black boxes.

-only_cells

Results in a set of all cells in the timing fanout of the *source_list*, rather than a set of pins or ports.

-flat

Specifies to function in the flat mode of operation. The two major modes in which **all_fanout** functions are hierarchical (the default) and flat. When in hierarchical mode, only objects from the same hierarchy level as the current source are returned. Thus, pins within a level of hierarchy lower than that of the source are used for traversal but are not reported.

-levels ***count***

Stops traversal when reaching the perimeter of the search of *count* hops, where counting is performed over the layers of cells that are equidistant from the source.

-trace_arcs ***arc_type***

Specifies the type of combinational arcs to trace during the traversal. Allowed values are **timing**, which permits the tracing only of valid timing arcs (arcs that are neither disabled nor invalid due to case analysis), and **all**, which permits tracing of all combinational arcs regardless of either case analysis or arc disabling. The default in IC Compiler and Design Compiler (both in topographical mode and non-topographical mode) is **timing**. The default in DC Explorer is **all**. The default can be changed by setting the **fanin_fanout_trace_arcs** variable to the desired value.

DESCRIPTION

The **all_fanout** command reports the timing fanout of specified source pins, ports, or nets in the design. A pin is considered to be in the timing fanout of a sink if there is a timing path through combinational logic from that source to the pin. The fanout report stops at the inputs to registers (sequential cells). The source pins or ports are specified by using the **-clock_tree** or **-from source_list** option.

Multicorner-Multimode Support

Depending on the options used, this command either uses the current scenario or has no dependency on scenario-specific information.

EXAMPLES

The following example shows the timing fanout of a port in the design. The design comprises the following three inverters in a chain named *iv1*, *iv2*, and *iv3*. The *iv1* and *iv2* inverters are hierarchically combined in a larger cell named ii2.

```
prompt> all_fanout -from tin
{iv3/out tout iv3/in ii2/hin ii2/hout tin}

prompt> all_fanout -from tin -flat
{tout ii2/iv2/U1/z ii2/iv1/U1/a iv3/U1/z iv3/U1/a
ii2/iv2/U1/a ii2/iv1/U1/z tin}

prompt> all_fanout -from tin -levels 1 -only_cells
{iv3 ii2}
```

SEE ALSO

all_fanin(2)
create_clock(2)
report_clock(2)
report_transitive_fanout(2)