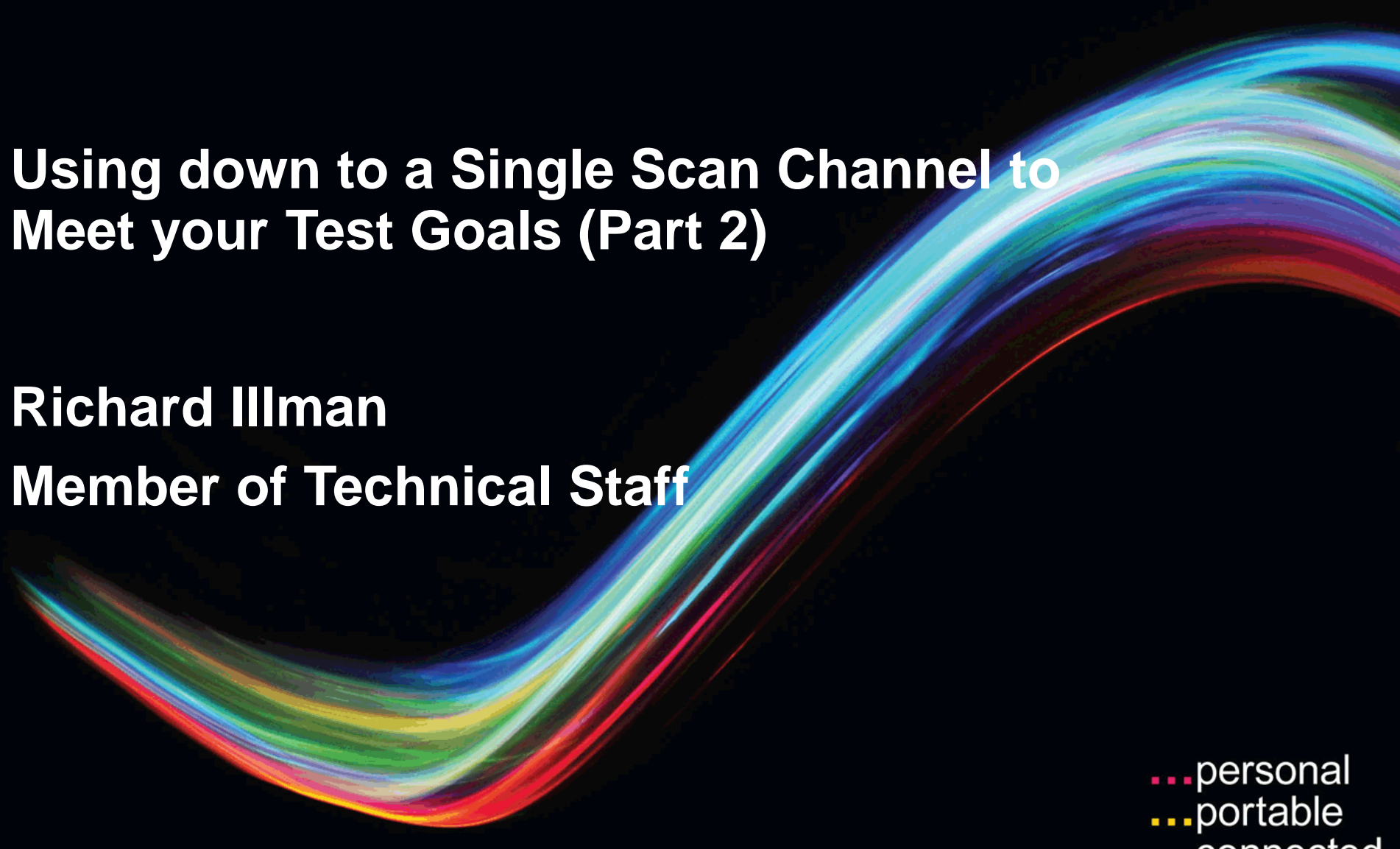


# Using down to a Single Scan Channel to Meet your Test Goals (Part 2)

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**Member of Technical Staff**

A series of vibrant, multi-colored wavy lines (red, orange, yellow, green, blue, purple) that sweep across the lower half of the slide from left to right.

...personal  
...portable  
...connected

“Dialog Semiconductor creates energy-efficient, highly integrated, mixed signal circuits optimised for smartphones, tablets, ULTRABOOKS™ and other portable devices.”

### Implications:

- Low pin count devices

- Large volumes (10s millions to 100s millions)

- Price competitive

# Reducing Pin Count – Example Audio Design

Limited digital pins available:

- Clock input/output 3 pins

- I2C interface 2 pins

- I2S interface 4 pins

Typically limited 3 or 4 pairs scan in/out pads

# Dual use of audio analogue input pads



Analogue audio input pads can be as digital inputs in scan mode.

Issues:

- Typically must be level shifted in the chip to the digital supply levels.
- Load board must support both analogue and digital channels for the same pad.
- Mixes the analogue/digital design environments.

# Requirement for high X-tolerance



Large amounts of non-scan elements latches

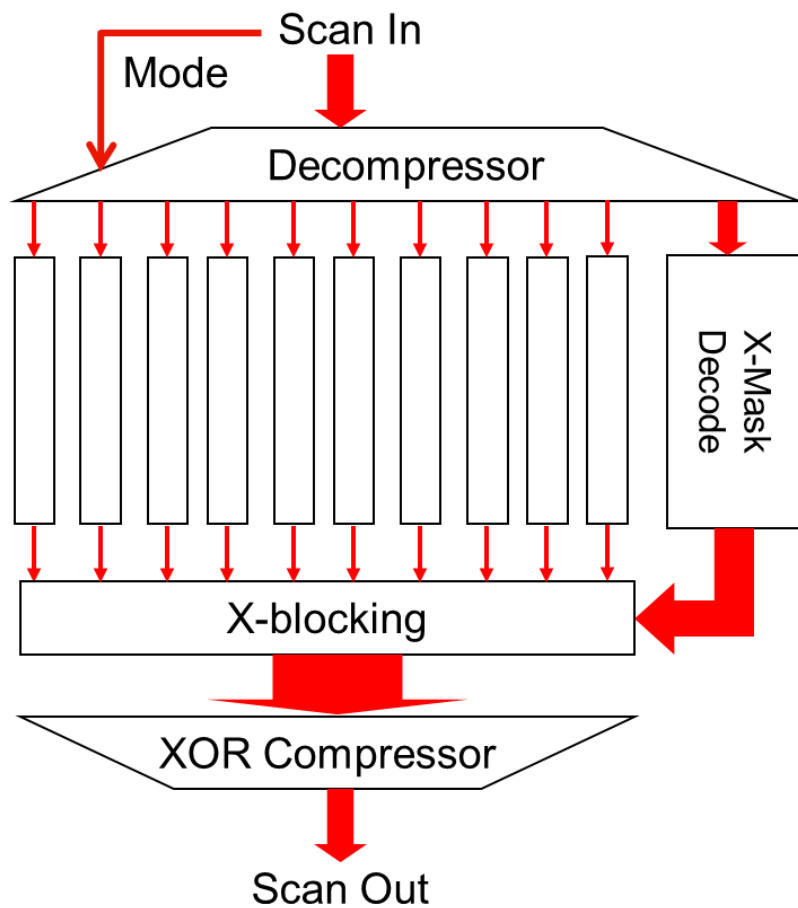
Ratio 2:1 of scan to non-scan elements

Register files, filter blocks etc.

Tolerance to problems in sub-chains in analogue blocks

Real Time Counter, PLL

# High X tolerance DFTMAX architecture



Number of scan-in and scan-out pins	Maximum internal chains
2	4
3	12
4	32
5	80
6	192

3875 scan patterns

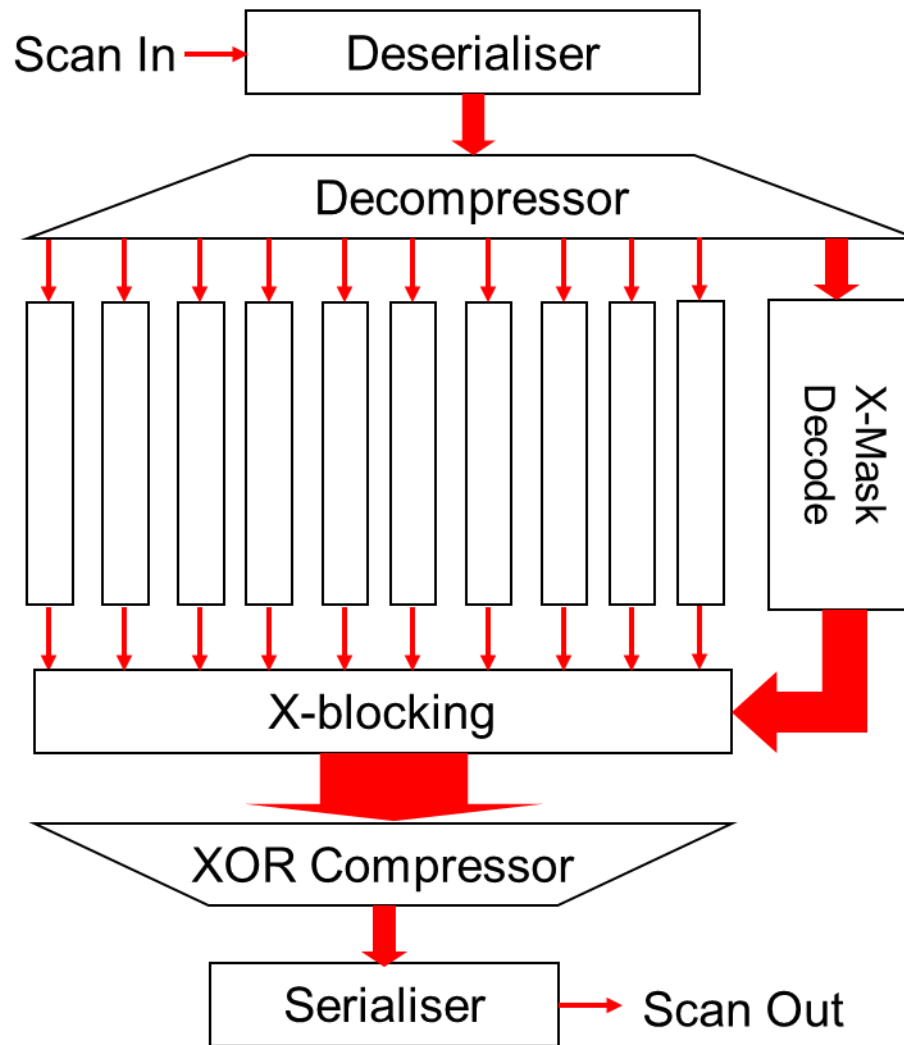
302 mask-only patterns

230 patterns without X-masking (~6%)

3342 patterns with X-masking

Average 55 mask bits (chain length 181 bits)

# High X tolerance DFTMAX with Serialiser

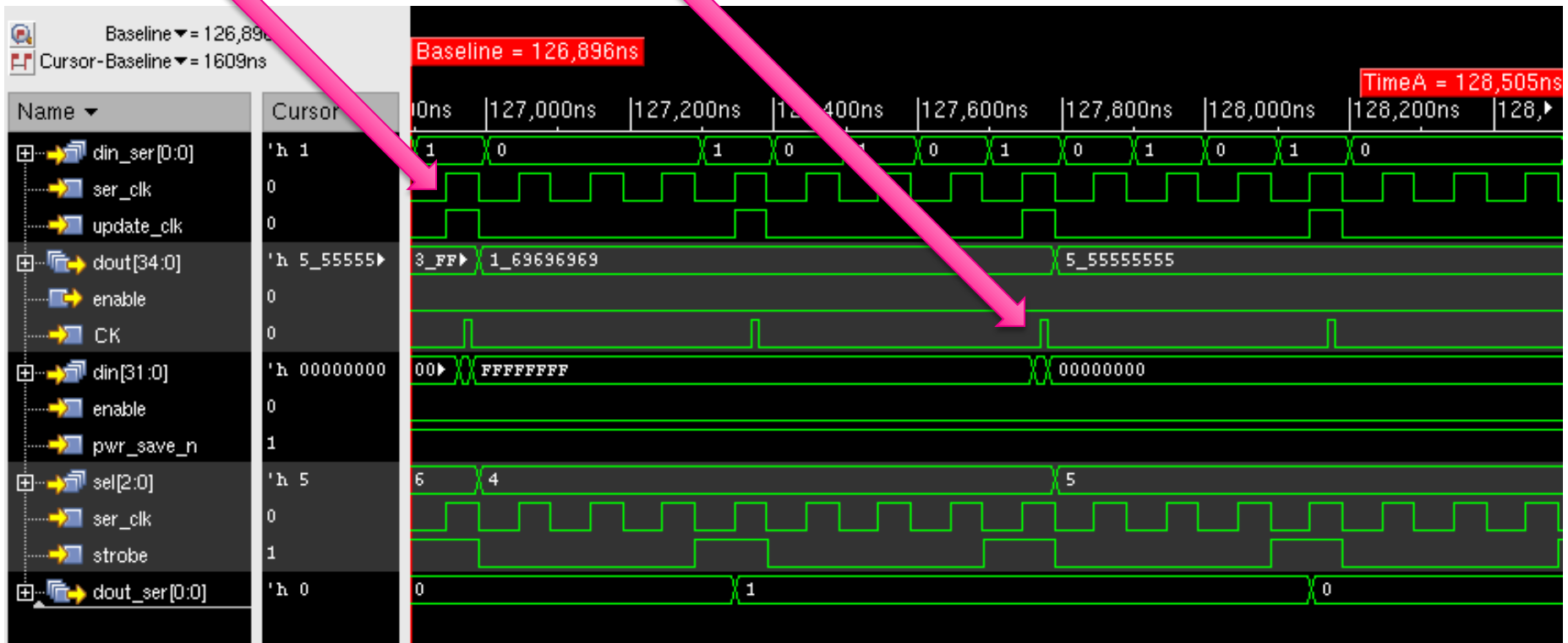




# Serialiser Shift Clock Ratios

External  
Shift

Internal  
Shift



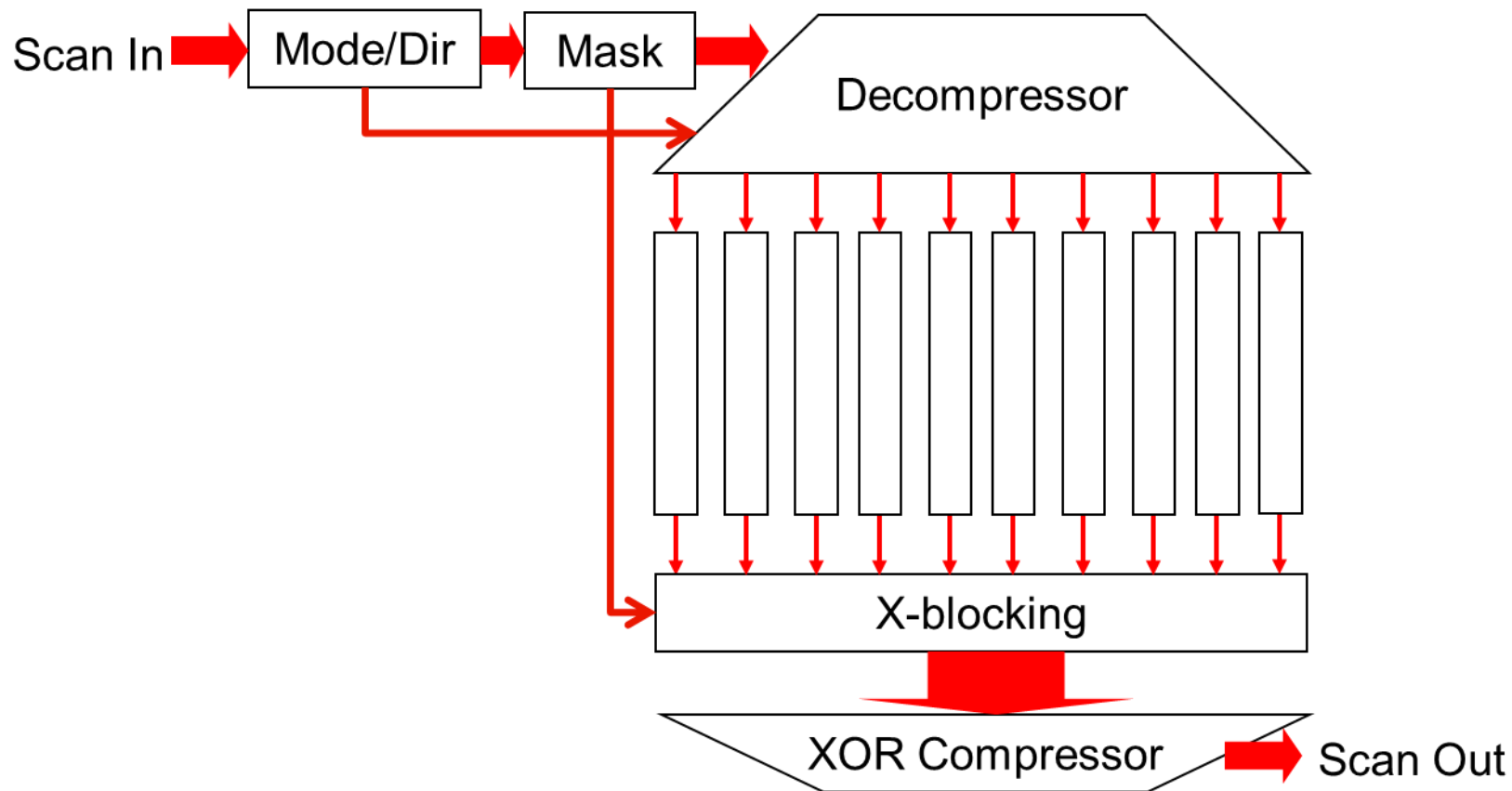
# Compression – Goldilocks type problem?

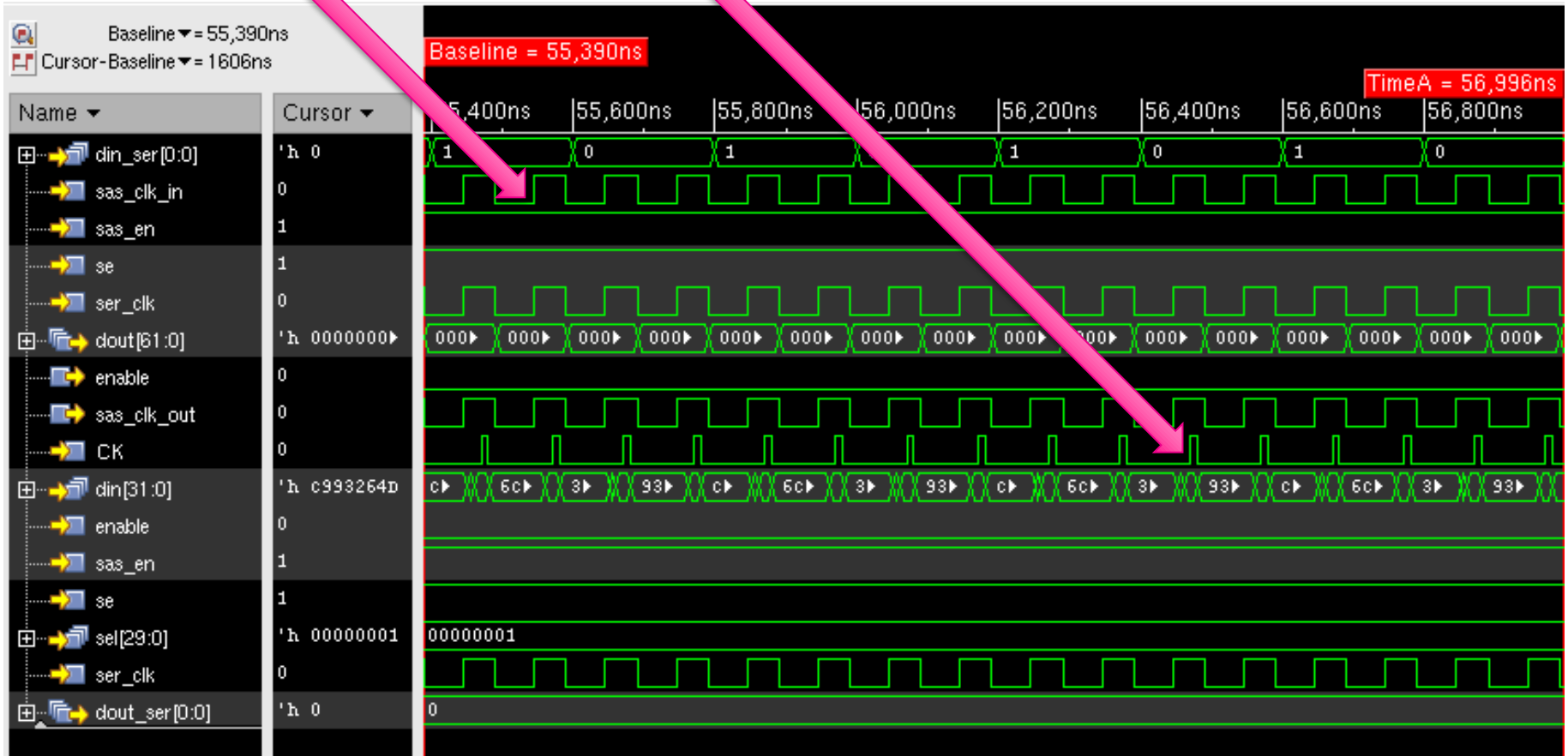
DFTMAX – “too many pins”

DFTMAX Serialiser – “too slow, too much data”

DFTMAX Ultra – “baby bear” solution - just right?

# DFTMAX Ultra Architecture





# Change to the Design Compiler Synthesis Flow

```
set_dft_configuration -scan_compression enable
```

```
set_scan_compression_configuration \  
  -xtolerance high \  
  -chain_count 32 -inputs 4 -outputs 4 \  
  -min_power true
```

```
report_scan_compression_configuration
```

```
set_dft_configuration -streaming_compression enable
```

```
set_streaming_compression_configuration \  
  -chain_count 120 -inputs 4 -outputs 4
```

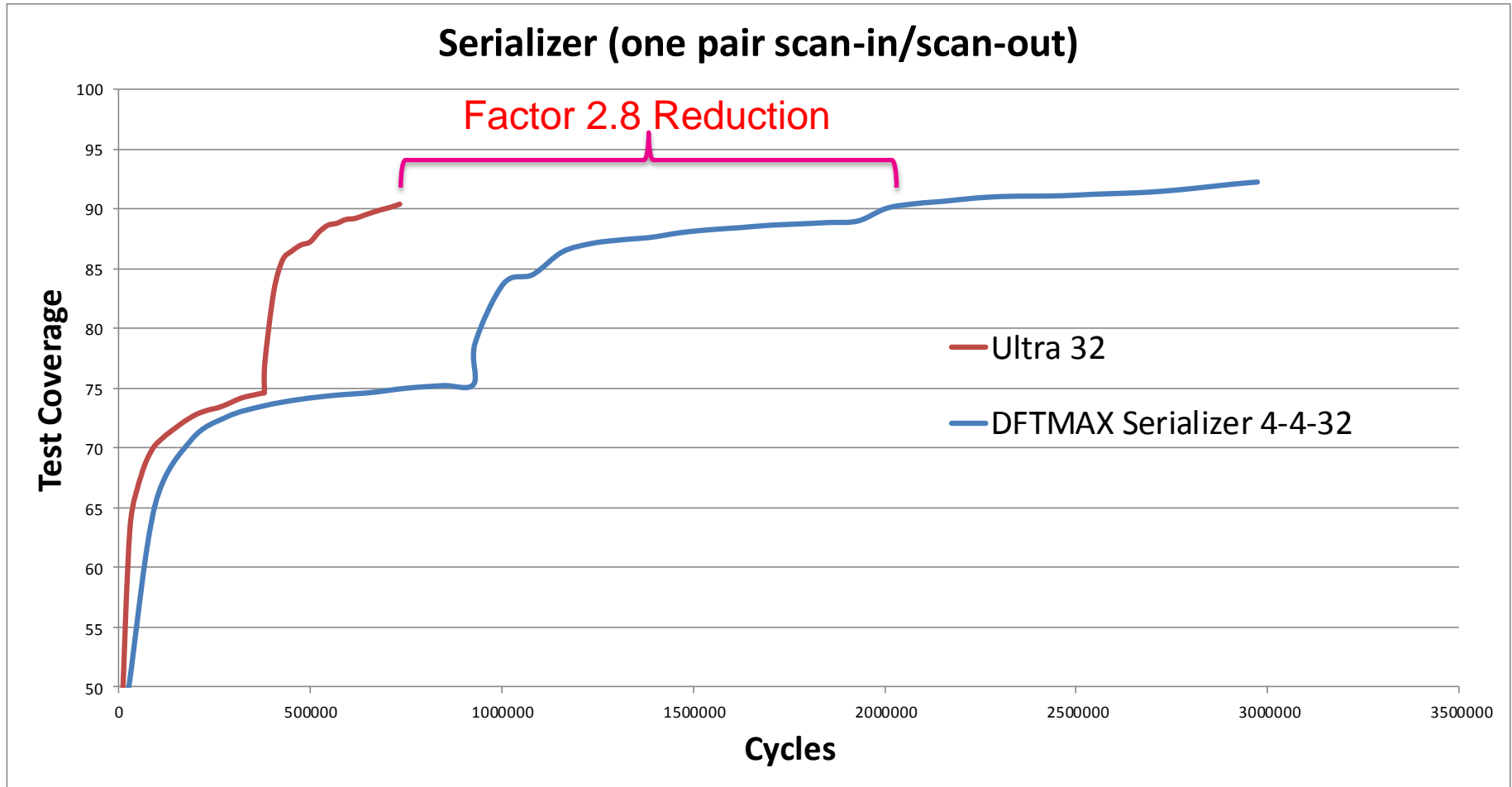
```
report_streaming_compression_configuration
```

# DFTMax Ultra overhead

(Design has 6,300 scan flops and 3,500 non-scan latches)

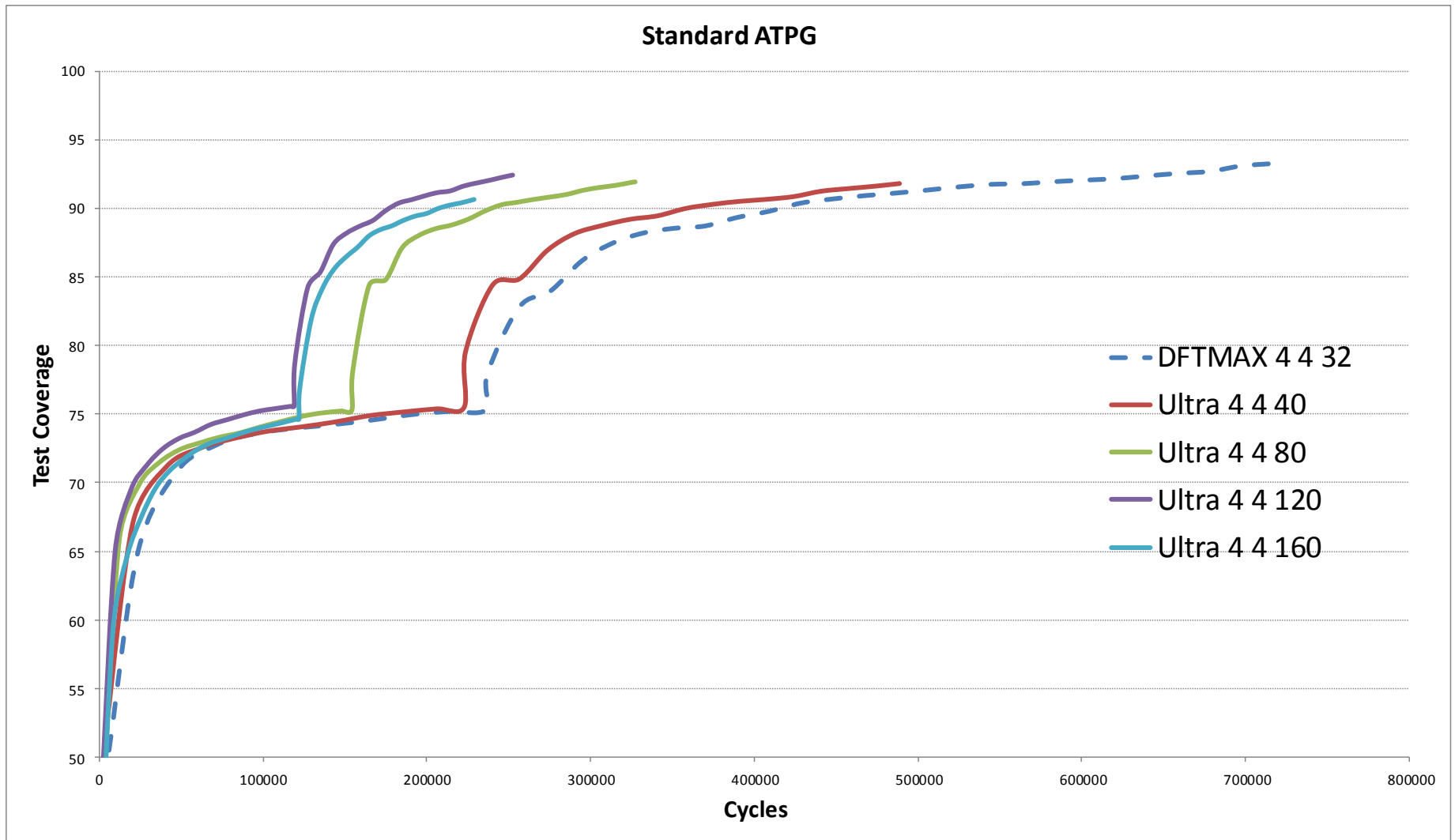
Architecture	#si/so pins	Internal Chains	Latches added	DFF added	Seq. element overhead*	Fault list overhead**
DFTMAX	4	32	0	0	0	0.23%
DFTMAX Ultra	4	40	38	84	1.3%	1.06%
DFTMAX Ultra	4	80	62	136	2.2%	2.05%
DFTMAX Ultra	4	120	78	168	2.7%	3.31%
DFTMAX Ultra	4	160	86	188	3.0%	4.25%
DFTMAX serializer	1	32	4	16	0.2%	0.29%
DFTMAX Ultra	1	32	36	72	1.2%	0.90%

# Single SI/SO results



With “Minimum Detect” ATPG the reduction is 3.4

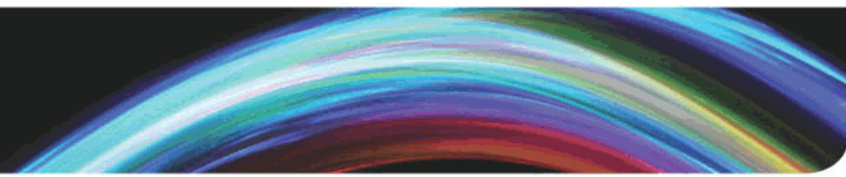
# 4 SI/SO test case





# DFTMAX Ultra Budgeter

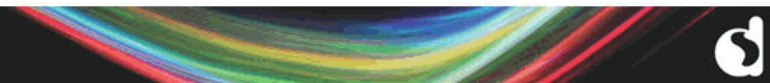
A	B	C	D	E	F	G	H	I	J
<b>DFTMAX Ultra Budgeter v1.0</b>									
<b>INPUT DATA (to be filled in by the user)</b>									
SCAN In/Out PORT pairs (Choose value from dropdown menu)	<b>AND</b>	Number of flip flops [#DFFs]	<b>AND/OR</b>	Target Compression Ratio (Choose value from dropdown menu)	<div style="border: 1px solid black; padding: 10px; margin: 10px;"> <div style="border: 1px solid black; padding: 5px; text-align: center; margin-bottom: 10px;">Start Feasibility Analysis</div> <div style="border: 1px solid black; padding: 5px; text-align: center;">Clear Data</div> </div>				
4		6000		10					
4		6000		20					
4		6000		30					
4		6000		40					
<b>OUTPUT DATA</b>									
SCAN In/Out PORT pairs	Number of flip flops [#DFFs]	Compression Ratio		# Internal Scan Chains (ScanCompression_mode)		# External Cycles		Internal Scan Chain length (ScanCompression_mode)	
		User Target	Max Target	User Target	Max Target	User Target	Max Target	User Target	Max Target
4	6000	10	20	40	80	12	19	150	75
4	6000	20	20	80	80	19	19	75	75
4	6000	30	20	120	80	23	19	50	75
4	6000	40	20	160	80	26	19	38	75



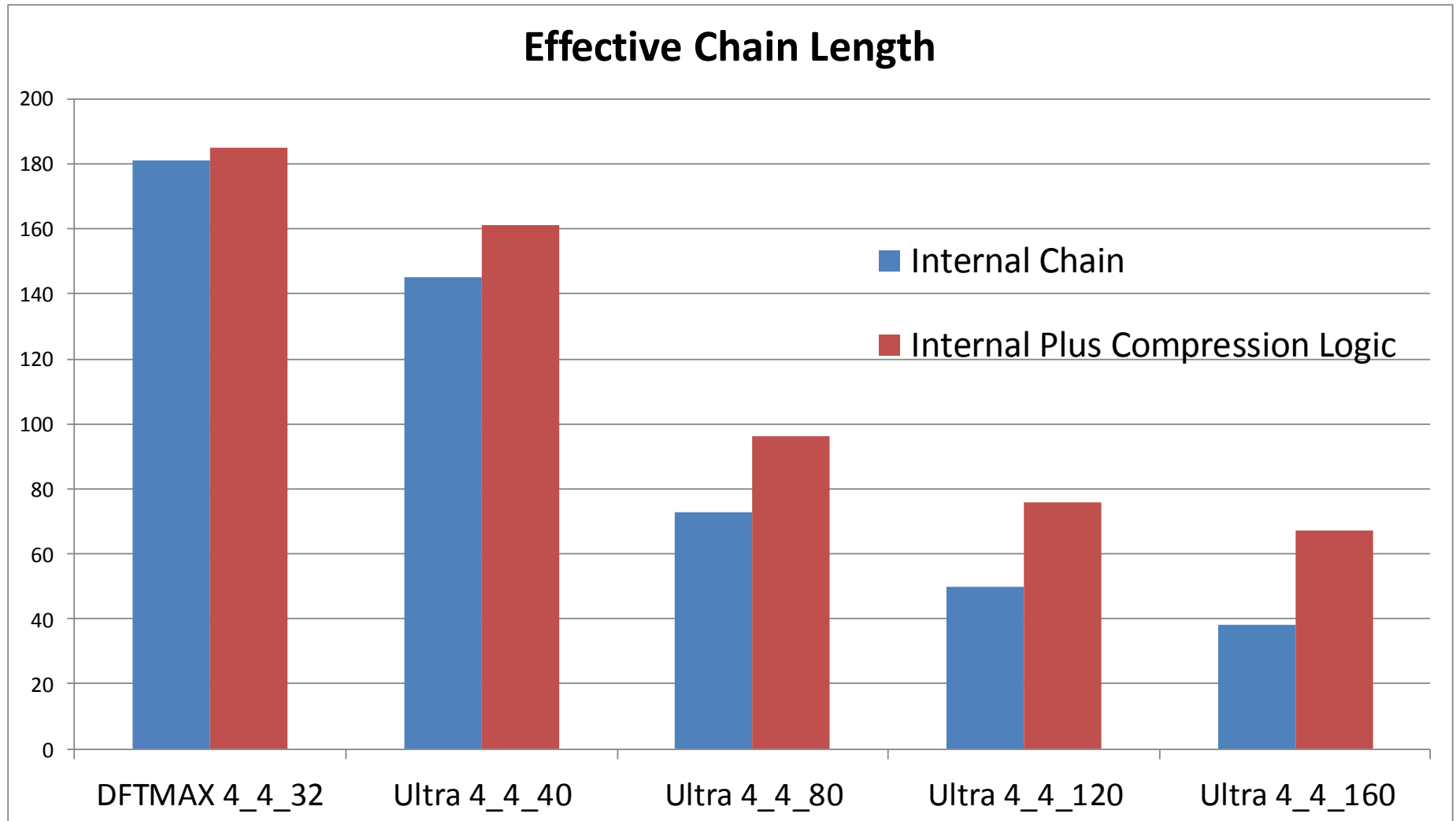
OUTPUT DATA				
Number of flip flops [#DFFs]	Compression Ratio		# Internal Scan Chains (ScanCompression_mode)	
	User Target	Max Target	User Target	Max Target
6000	10	20	40	80
6000	20	20	80	80
6000	30	20	120	80
6000	40	20	160	80

`And thirdly, the ~~Pirate Code~~ DFTMAX Ultra Budgeter is more what you'd call "guidelines" than actual rules.`

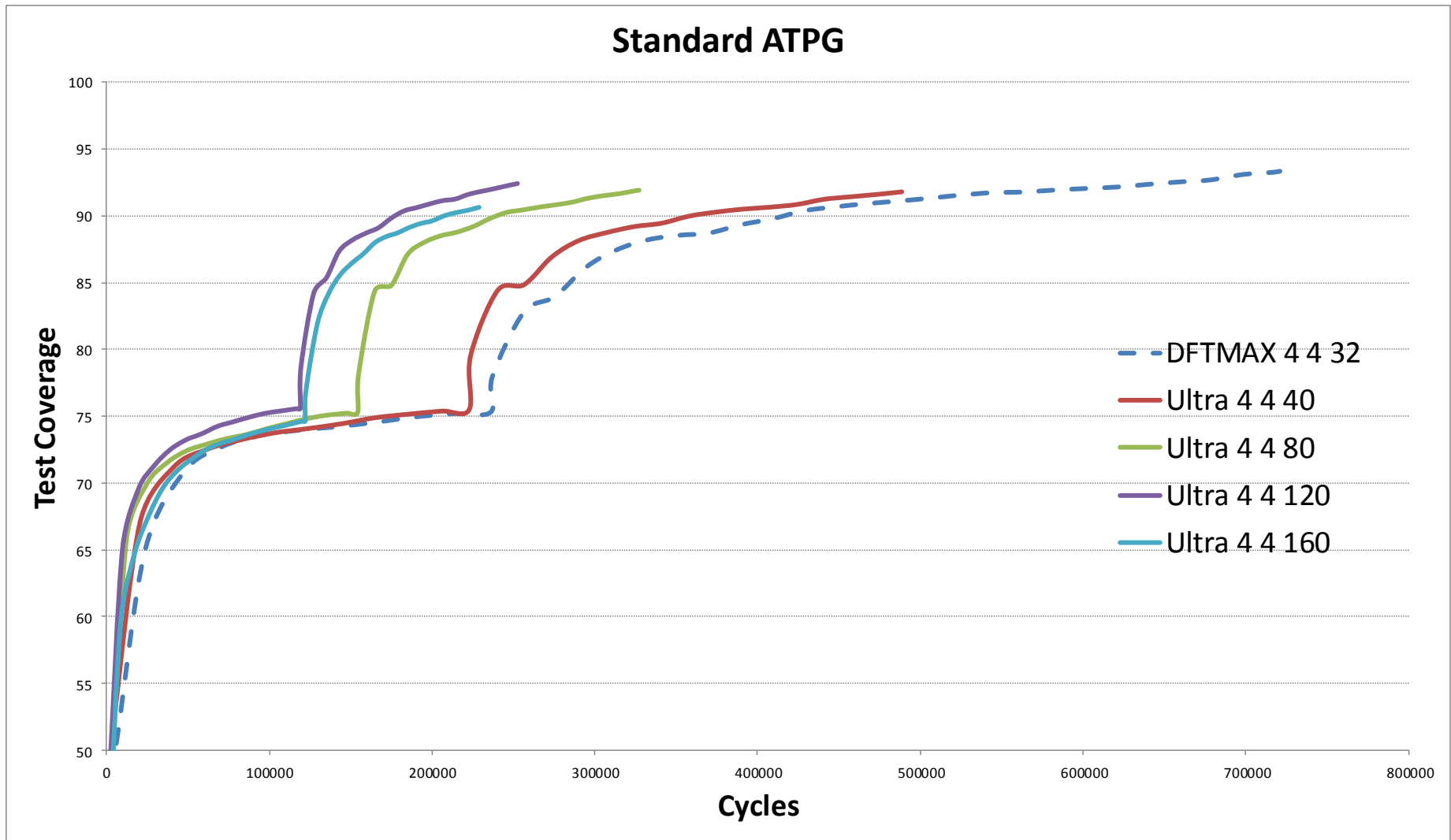
Captain Barbossa, "Pirates of the Caribbean"



# Effective Chain Lengths



# 4 SI/SO test case



## DFTMAX

- Mask data for the unload of the ***previous*** pattern
- Decompressor mode for the current pattern
- Data is encoded on a cycle basis through the whole pattern

## DFTMAX Ultra

- Mask data and compressor direction for the ***current*** pattern
- Decompressor mode and direction for the next pattern
- Data is encoded in separate dedicated bits

High X-tolerance DFTMAX patterns *which utilise X-masking* cannot be individually manipulated, DFTMAX Ultra patterns can.

```
set_atpg -basic_min_detects_per_pattern { d d } \  
        -fast_min_detects_per_pattern { d d }
```

parameters

minimum number of fault detects

limit on consecutive rejected patterns

```
set i 8192  
while { $i > 2 } { set i [expr $i/2] ;  
            set_atpg -fast_min_detect [list $i 20];  
            run_atpg fast -auto }
```

# DFTMAX Ultra Pattern Reordering Command

## Post ATPG (Beta status)

```
reorder_patterns -coverage \  
                  -sort partial \  
                  -group_size <d> \  
                  -number_of_patterns <d>
```

```
reorder_patterns -coverage -sort full \  
                  -first_pattern <d> \  
                  -last_pattern <d>
```

# Pattern reordering – fault simulation based

## Extracting fault detections for each pattern

```
set limit [expr [sizeof_collection [get_patterns -all ]] -1 ]  
  
for { set i 0 } { $i < $limit } { incr i } {  
    run_fault_sim -first $i -last $i }
```

Very slow and inefficient

```
run_fault_sim -detected_pattern_storage  
  
write_patterns filename -all
```

Fault list contains the first pattern where the fault is detected  
Not available with multi-processor



# DFTMAX Ultra Pattern Reordering Command

## User defined list

```
reorder_patterns -remove {  
1932 1972 2207 2229 2231 2249 2250 2266 2605 2696 2697 1923 1945  
1951 1954 1957 44 71 39 53 67 6 30 43 35 12 23 19 26 29 27 24 16  
}  
-insert {  
X X X X 1355 1355 1355 1355 1355 1355 1355 1355 1355 1355 1355  
1355 X X X X 5 5 5 5 5 5 5 5 5 5 5 5 }  
}
```

The first list is the patterns to be removed. The corresponding item in the second list is the position it is to be placed.

If the item in the second list is “X” the pattern is deleted.

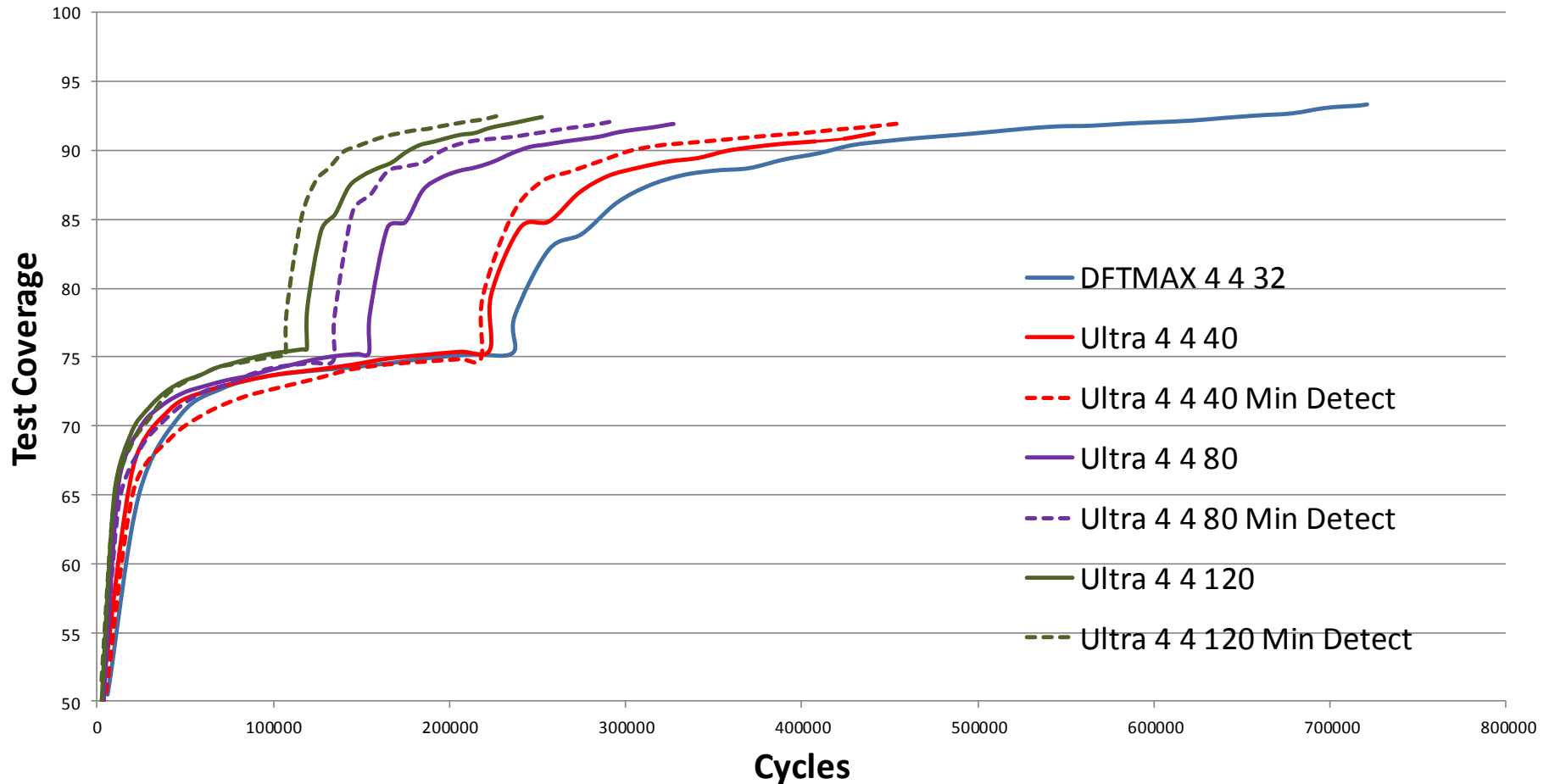
Over 50,000 patterns successfully reordered with a single command.

Legacy patterns reordered with:

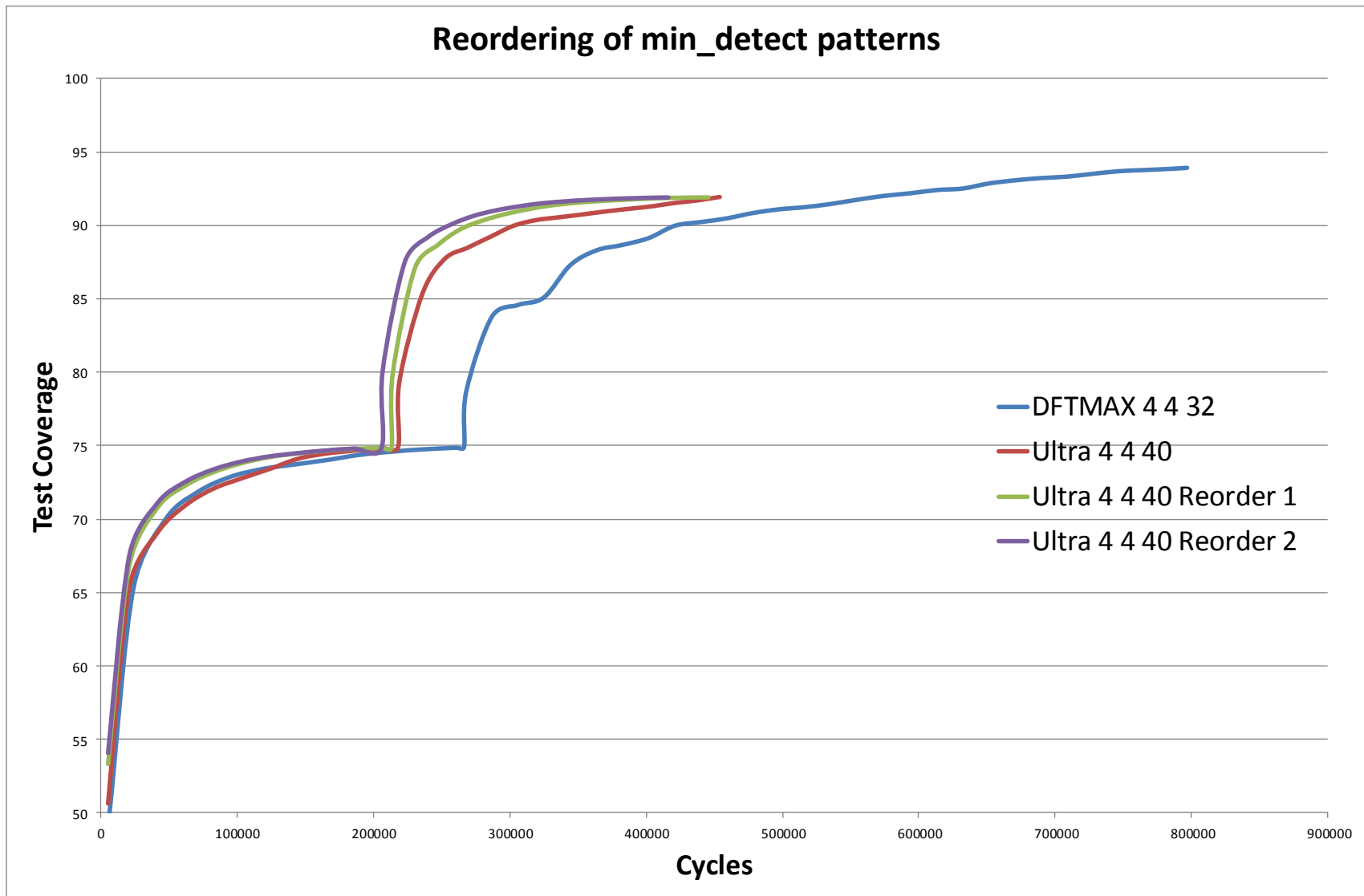
```
write_patterns filename -reorder file
```

# DFTMAX Ultra with “minimum detect” 20 rejected pattern limit

## Minimum Detect ATPG

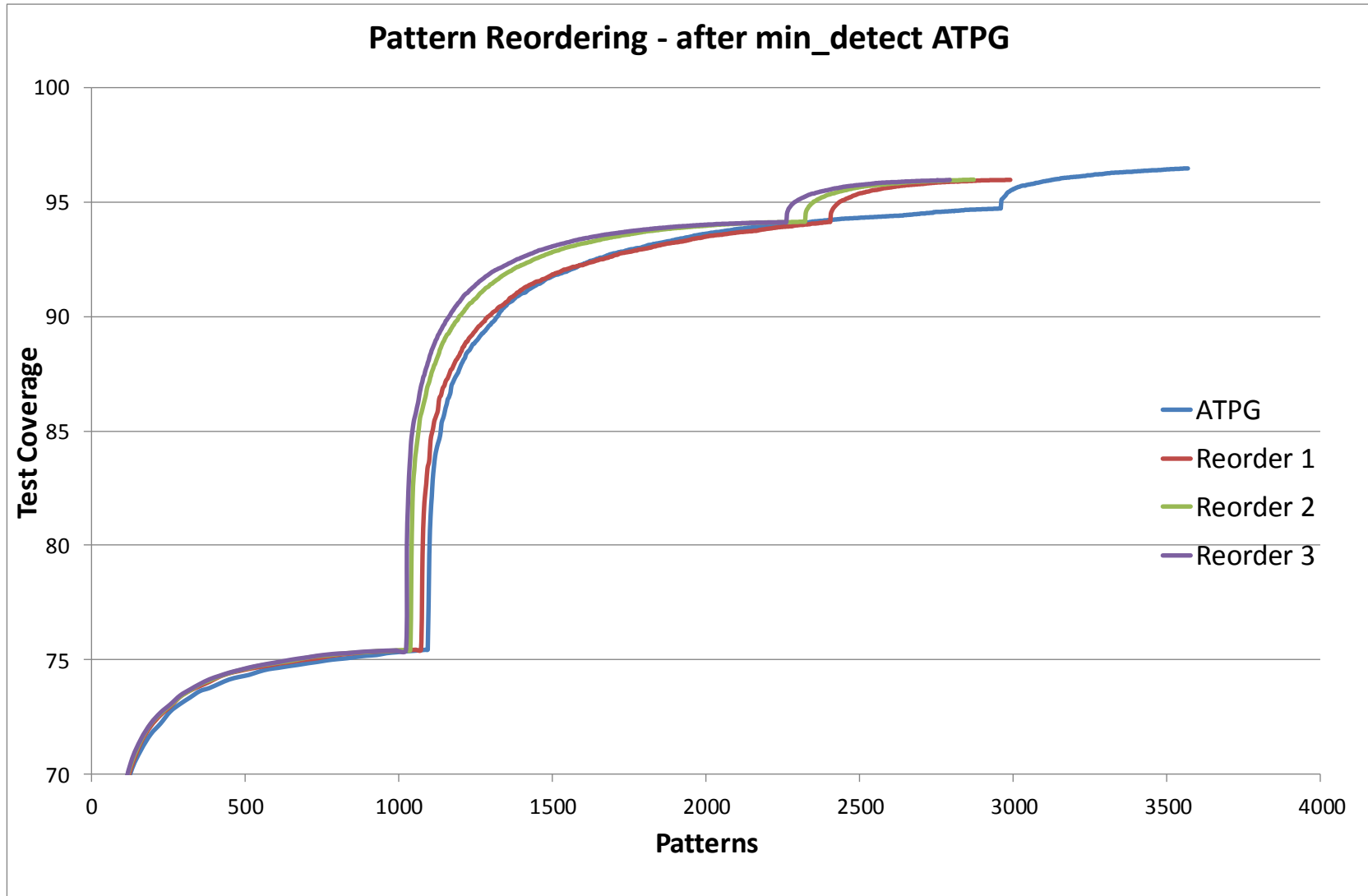


# Reordering of “minimum detect” patterns

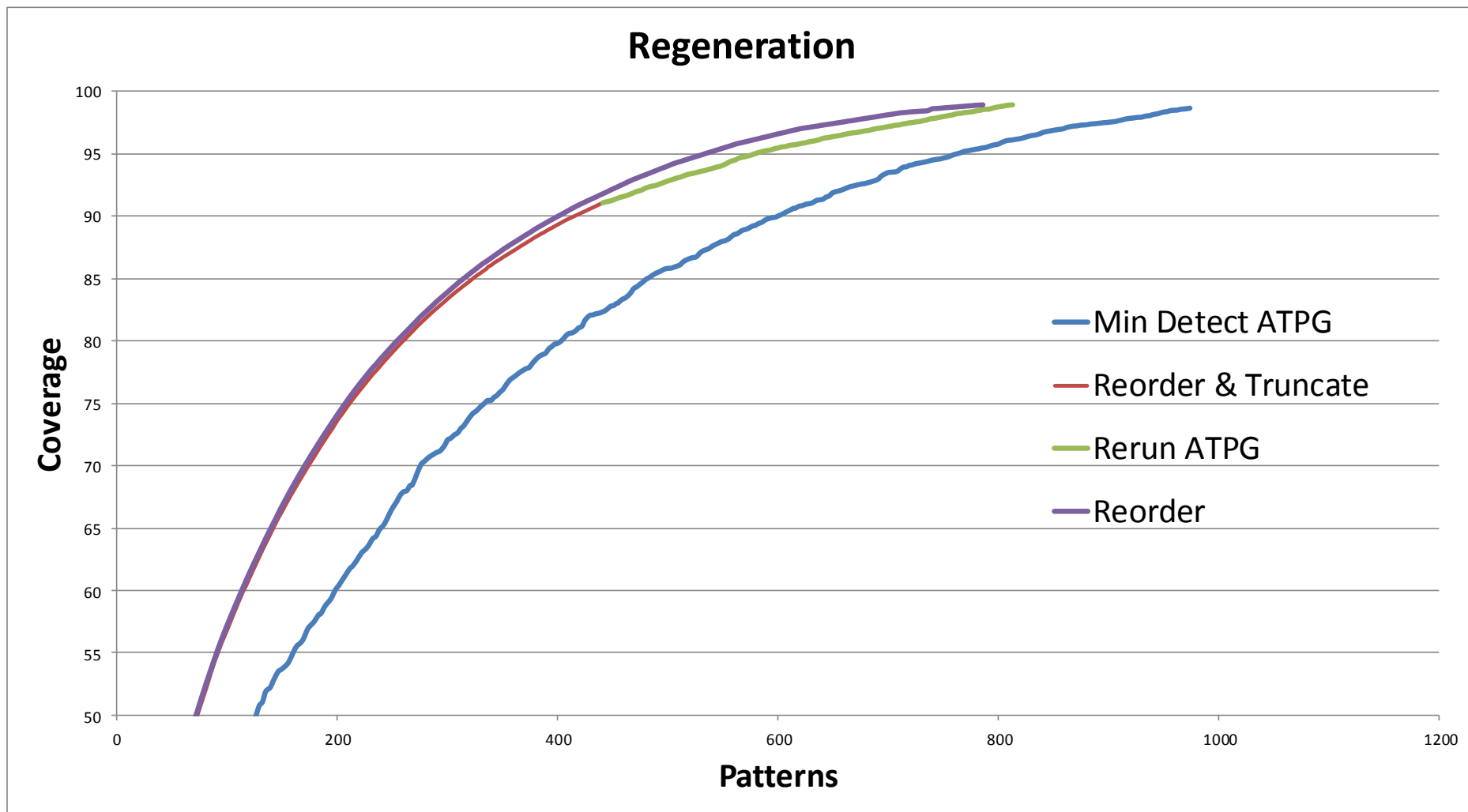


# “Legacy” design reordering

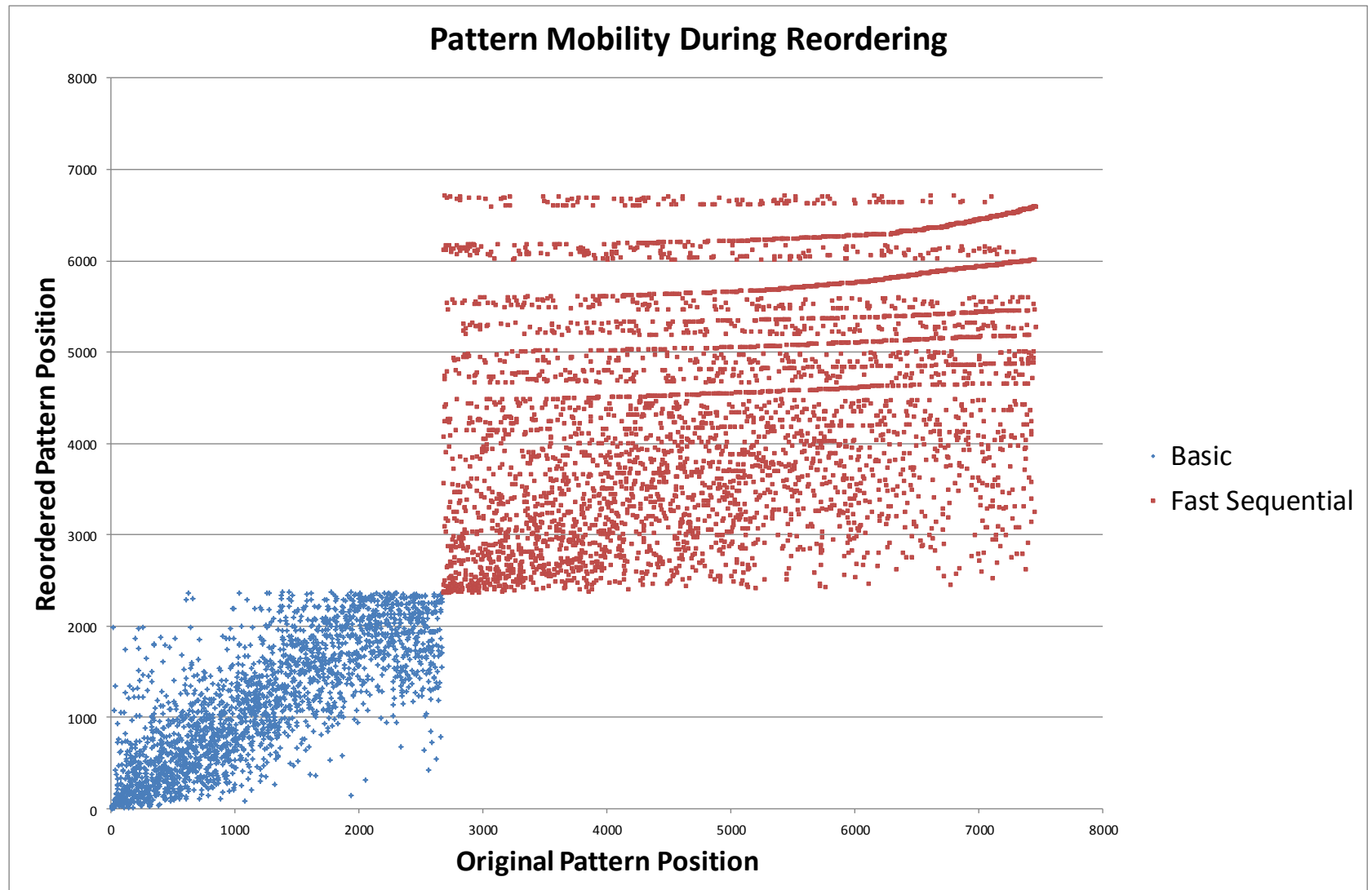
## Basic, single load sequential, multi load sequential



# Regeneration of Patterns



# Pattern Reordering



- Easy transition of the synthesis/ATPG flow
- Dramatically improved results for the single scan in/out implementation.
- Higher compression achieved when pin counts are limited (or achieve the same compression with reduced pin access on the ATE).
- More compact pattern sets can be generated
  - “minimum detect” and pattern reordering available even with High X tolerance

# The power to be...

...personal  
...portable  
...connected