Analog Circuits (Formula Notes/Short Notes)

- Energy gap $\left.\begin{matrix} E_{G/si}=1.21-3.6\times10^{-4}.T \ \text{ev} \\ E_{G/Ge}=0.785-2.23\times10^{-4}.T \ \text{ev}\end{matrix}\right\}$ Energy gap depending on temperature
- $E_F = E_C - KT \ln\left(\frac{N_C}{N_D}\right) = E_v + KT \ln\left(\frac{N_v}{N_A}\right)$
- No. of electrons $n = N_c \, e^{-(E_c - E_f)/RT}$ (KT in ev)
- No. of holes $p = N_v \, e^{-(E_f - E_v)/RT}$
- Mass action law $n_p = n_i^2 = N_c N_v \, e^{-EG/KT}$
- Drift velocity $v_d = \mu E$ (for si $v_d \leq 10^7$ cm/sec)
- Hall voltage $v_H = \frac{B.I}{w_e}$. Hall coefficient $R_H = 1/\rho$. $\rho \rightarrow$ charge density = qN_0 = ne …
- Conductivity $\sigma = \rho\mu$; $\mu = \sigma R_H$.
- Max value of electric field @ junction $E_0 = -\frac{q}{\epsilon_{si}} N_d . n_{n0} = -\frac{q}{\epsilon_{si}} N_A . n_{p0}$.
- Charge storage @ junction $Q_+ = - Q_- = qA \, x_{n0} N_D = qA \, x_{p0} N_A$
- Diffusion current densities $J_p = - q \, D_p \frac{dp}{dx}$ $J_n = - q \, D_n \frac{dn}{dx}$
- Drift current Densities $= q(p \, \mu_p + n\mu_n)E$
- μ_p , μ_n decrease with increasing doping concentration .
- $\frac{D_n}{\mu_n} = \frac{D_p}{\mu_p} = KT/q \approx 25$ mv @ 300 K
- Carrier concentration in N-type silicon $n_{n0} = N_D$; $p_{n0} = n_i^2 / N_D$
- Carrier concentration in P-type silicon $p_{p0} = N_A$; $n_{p0} = n_i^2 / N_A$
- Junction built in voltage $V_0 = V_T \ln\left(\frac{N_A N_D}{n_i^2}\right)$
- Width of Depletion region $W_{dep} = x_p + x_n = \sqrt{\frac{2\varepsilon_s}{q}\left(\frac{1}{N_A} + \frac{1}{N_D}\right)(V_0 + V_R)}$

  $* \left(\frac{2\varepsilon_{ft}}{q} = 12.93m \ for \ si\right)$
- $\frac{x_n}{x_p} = \frac{N_A}{N_D}$
- Charge stored in depletion region $q_J = \frac{q.N_A N_D}{N_A + N_D} . A . W_{dep}$
- Depletion capacitance $C_j = \frac{\varepsilon_s A}{W_{dep}}$; $C_{j0} = \frac{\varepsilon_s A}{W_{dep}/V_R=0}$

  $C_j = C_{j0} / \left(1 + \frac{V_R}{V_0}\right)^m$

  $C_j = 2C_{j0}$ (for forward Bias)
- Forward current $I = I_p + I_n$; $I_p = Aq \, n_i^2 \frac{D_p}{L_p N_D}\left(e^{V/V_T} - 1\right)$

  $I_n = Aq \, n_i^2 \frac{D_n}{L_n N_A}\left(e^{V/V_T} - 1\right)$
- Saturation Current $I_s = Aq \, n_i^2 \left(\frac{D_p}{L_p N_D} + \frac{D_n}{L_n N_A}\right)$
- Minority carrier life time $\tau_p = L_p^2 / D_p$; $\tau_n = L_n^2 / D_n$

- Minority carrier charge storage $Q_p = \tau_p I_p$, $Q_n = \tau_p I_n$
  $Q = Q_p + Q_n = \tau_T I$ τ_T = mean transist time
- Diffusion capacitance $C_d = \left(\frac{\tau_T}{\eta V_T}\right) I = \tau.g \Rightarrow C_d \propto I$.
  $\tau \rightarrow$ carrier life time , g = conductance = I / ηV_T
- $I_{02} = 2^{(T_2-T_1)/10}\, I_{01}$
- Junction Barrier Voltage $V_j = V_B = V_r$ (open condition)
  $= V_r - V$ (forward Bias)
  $= V_r + V$ (Reverse Bias)
- Probability of filled states above 'E' $f(E) = \frac{1}{1+e^{(E-E_f)/KT}}$
- Drift velocity of e^- $v_d \leq 10^7$ cm/sec
- Poisson equation $\frac{d^2V}{dx^2} = \frac{-\rho_v}{\epsilon} = \frac{-nq}{\epsilon} \Rightarrow \frac{dv}{dx} = E = \frac{-nqx}{\epsilon}$

Transistor :-

- $I_E = I_{DE} + I_{nE}$
- $I_C = I_{Co} - \alpha\, I_E$ $\rightarrow$ Active region
- $I_C = -\alpha\, I_E + I_{Co}\,(1- e^{V_C/V_T})$

Common Emitter :-

- $I_C = (1+\beta)\, I_{Co} + \beta I_B$ $\beta = \frac{\alpha}{1-\alpha}$
- $I_{CEO} = \frac{I_{Co}}{1-\alpha}$ $\rightarrow$ Collector current when base open
- I_{CBO} $\rightarrow$ Collector current when $I_E = 0$ $I_{CBO} > I_{Co}$.
- $V_{BE,sat}$ or $V_{BC,sat} \rightarrow$ - 2.5 mv /^{0} C ; $V_{CE,sat} \rightarrow \frac{V_{BE,sat}}{10}$ = - 0.25 mv /^{0}C
- Large signal Current gain $\beta = \frac{I_C - I_{CBo}}{I_B + I_{CBo}}$
- D.C current gain $\beta_{dc} = \frac{I_C}{I_B} = h_{FE}$
- $(\beta_{dc} = h_{FE}) \approx \beta$ when $I_B > I_{CBo}$
- Small signal current gain $\beta' = \left.\frac{\partial I_C}{\partial I_R}\right|_{V_{CE}} = h_{fe} = \frac{h_{FE}}{1-(I_{CBo}+I_B)\frac{\partial h_{FE}}{\partial I_C}}$
- Over drive factor = $\frac{\beta_{active}}{\beta_{forced} \rightarrow \text{under saturation}}$ $\because I_{C\,sat} = \beta_{forced}\, I_{B\,sat}$

Conversion formula :-

CC $\leftrightarrow$ CE

- $h_{ic} = h_{ie}$; $h_{rc} = 1$; $h_{fc} = -(1+h_{fe})$; $h_{oc} = h_{oe}$

CB $\leftrightarrow$ CE

- $h_{ib} = \frac{h_{ie}}{1+h_{fe}}$; $h_{ib} = \frac{h_{ie}\, h_{oe}}{1+h_{fe}} - h_{re}$; $h_{fb} = \frac{-h_{fe}}{1+h_{fe}}$; $h_{ob} = \frac{h_{oe}}{1+h_{fe}}$

CE parameters in terms of CB can be obtained by interchanging B & E .

Specifications of An amplifier :-

- $A_I = \frac{-h_f}{1+h_o Z_L}$ $Z_i = h_i + h_r A_I Z_L$ $A_{vs} = \frac{A_v . Z_i}{Z_i + R_s} = \frac{A_I . Z_L}{Z_i + R_s} = \frac{A_{I_S} . Z_L}{R_s}$

  $A_V = \frac{A_I \; Z_L}{Z_i}$ $Y_0 = h_o - \frac{h_f \, h_r}{h_i + R_s}$ $A_{Is} = \frac{A_v . R_s}{Z_i + R_s} = \frac{A_{vs} . R_s}{Z_L}$

Choice of Transistor Configuration :-

- For intermediate stages CC can't be used as $A_V < 1$
- CE can be used as intermediate stage
- CC can be used as o/p stage as it has low o/p impedance
- CC/CB can be used as i/p stage because of i/p considerations.

Stability & Biasing :- (Should be as min as possible)

- For $S = \frac{\Delta I_C}{\Delta I_{Co}}\Big|_{V_{B0,\beta}}$ $S' = \frac{\Delta I_C}{\Delta V_{BE}}\Big|_{I_{C0,\beta}}$ $S'' = \frac{\Delta I_C}{\Delta \beta}\Big|_{V_{BE,I_{Co}}}$

  $\Delta I_C = S.\, \Delta I_{Co} + S'\, \Delta V_{BE} + S''\, \Delta\beta$

- For fixed bias $S = \frac{1+\beta}{1-\beta\frac{dI_B}{dI_C}} = 1 + \beta$

- Collector to Base bias $S = \frac{1+\beta}{1+\beta\frac{R_C}{R_C+R_B}}$ $0 < s < 1+\beta = \frac{1+\beta}{1+\beta\left(\frac{R_C+R_E}{R_C+R_E+R_B}\right)}$

- Self bias $S = \frac{1+\beta}{1+\beta\frac{R_E}{R_E+R_{th}}} \approx 1+\frac{R_{th}}{R_e}$ $\beta R_E > 10\, R_2$

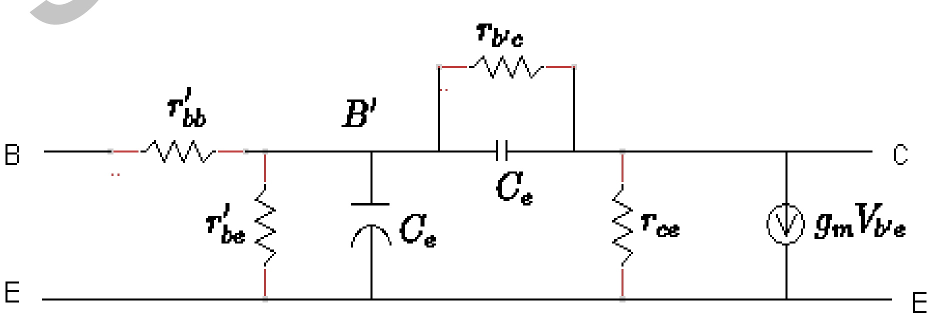
- $R_1 = \frac{V_{cc}\, R_{th}}{V_{th}}$; $R_2 = \frac{V_{cc}\, R_{th}}{V_{cc} - V_{th}}$

- For thermal stability $[\, V_{cc} - 2I_c\, (R_C + R_E)]\, [\, 0.07\, I_{co} \,.\, S] < 1/\theta$; $V_{CE} < \frac{V_{CC}}{2}$

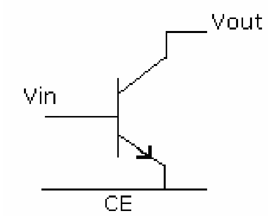
Hybrid –pi(π)- Model :-

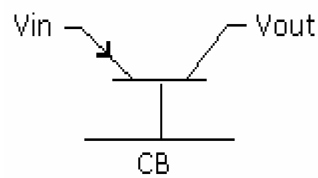
$g_m = |I_C| / V_T$

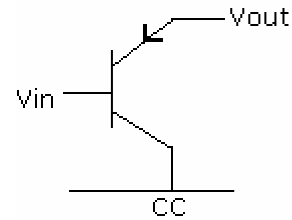
$r_{b'e} = h_{fe} / g_m$
$r_{b'b} = h_{ie} - r_{b'e}$
$r_{b'c} = r_{b'e} / h_{re}$
$g_{ce} = h_{oe} - (1+ h_{fe}\,)\, g_{b'c}$

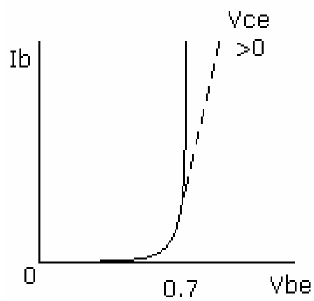


- 3 Configurations are used on BJT, CE, CB & CC

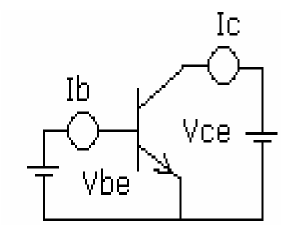


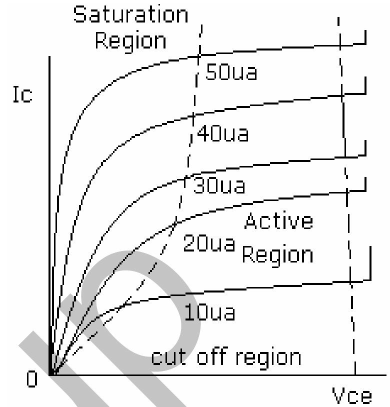






$$\beta = \frac{I_C}{I_B}\bigg|_{V_{CE}}$$





COMPARISON		
	BE	BC
SATURATION	f/b	f/b
ACTIVE	f/b	r/b
CUT OFF	r/b	r/b

AMPLIFIER COMPARISON			
	CB	CE	CF
R_i	LOW	MED	HIGH
A_I	A_I	β	$\beta+1$
A_V	High	High	<1
R_o	High	High	low

For CE :-

- $f_\beta = \frac{g_{b'e}}{2\pi(C_e + C_c)} = \frac{g_m}{h_{fe} 2\pi(C_e + C_c)}$

- $f_T = h_{fe}\, f_\beta$; $f_H = \frac{1}{2\pi\, r_{b'e}\, C} = \frac{g_{b'e}}{2\pi C}$ $C = C_e + C_c\,(1 + g_m R_L)$

  f_T = S.C current gain Bandwidth product
  f_H = Upper cutoff frequency

For CC :-

- $f_H = \frac{1+g_m R_L}{2\pi C_L R_L} \approx \frac{g_m}{2\pi C_L} = \frac{f_T\, C_e}{C_L} = \frac{g_m + g_{b'e}}{2\pi(C_L + C_e)}$

For CB:-

- $f_\alpha = \frac{1+h_{fe}}{2\pi r_{b'e}(C_C + C_e)} = (1+h_{fe})\, f_\beta = (1+\beta)\, f_\beta$

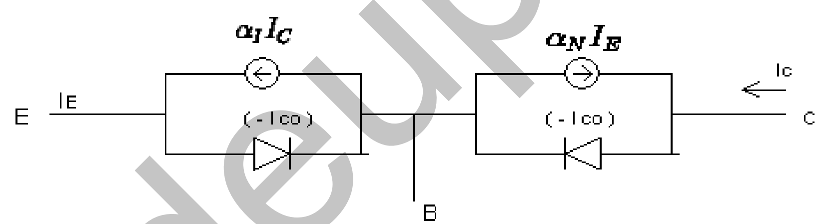
- $f_T = \frac{\beta}{1+\beta} f_\alpha$ $f_\alpha > f_T > f_\beta$

Ebress moll model :-

$I_C = -\alpha_N I_E + I_{Co}\,(1 - e^{V/V_T})$

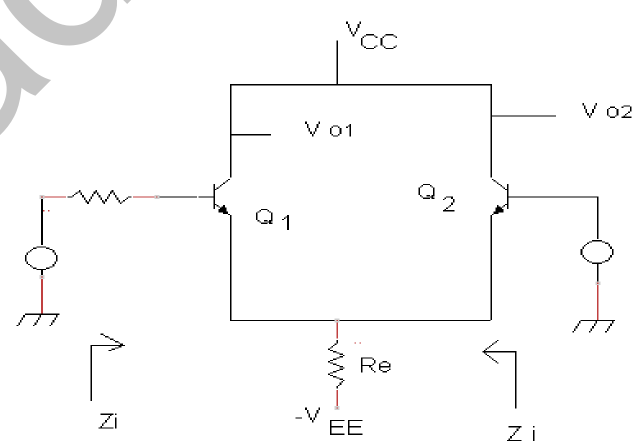
$I_E = -\alpha_I I_C + I_{Eo}\,(1 - e^{V/V_T})$

$\alpha_I I_{Co} = \alpha_N I_{Eo}$



Multistage Amplifiers :-

- $f_H^* = f_H \sqrt{2^{1/n} - 1}$; $f_L^* = \frac{f_L}{\sqrt{2^{1/n}-1}}$
- Rise time $t_r = \frac{0.35}{f_H} = \frac{0.35}{B.W}$
- $t_r^* = 1.1\sqrt{t_{r1}^2 + t_{r2}^2 + \cdots}$
- $f_L^* = 1.1\sqrt{f_{L_1}^2 + f_{L_2}^2 + \cdots}$
- $\frac{1}{f_H^*} = 1.1\sqrt{\frac{1}{f_{H_1}^2} + \frac{1}{f_{H_2}^2} + \cdots}$



Differential Amplifier :-

- $Z_i = h_{ie} + (1 + h_{fe})\, 2R_e = 2\, h_{fe}\, R_e \approx 2\beta R_e$

- $g_m = \frac{\alpha_0 |I_{EE}|}{4V_T} = \frac{I_C}{4V_T} = g_m$ of BJT/4 $\alpha_0 \rightarrow$ DC value of α

- $CMRR = \frac{h_{fe} R_e}{R_s + h_{ie}}$; $R_e \uparrow, \rightarrow Z_i \uparrow, A_d \uparrow$ & $CMRR \uparrow$

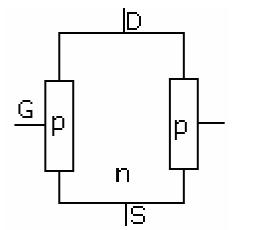
Darlington Pair :-

- $A_I = (1 + \beta_1)(1 + \beta_2)$; $A_v \approx 1$ (< 1)
- $Z_i = \frac{(1+h_{fe})^2 R_{e2}}{1+h_{fe} h_{oc} R_{e2}}$ Ω   [if Q_1 & Q_2 have same type] $= A_I R_{e2}$
- $R_o = \frac{R_s}{(1+h_{fe})^2} + \frac{2 h_{ie}}{1+h_{fe}}$
- $g_m = (1 + \beta_2) g_{m1}$

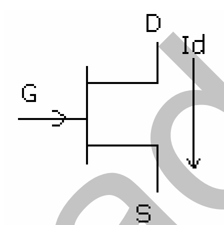
Tuned Amplifiers : (Parallel Resonant ckts used) :

- $f_0 = \frac{1}{2\pi\sqrt{LC}}$ Q → 'Q' factor of resonant ckt which is very high
- B.W = f_0 /Q
- $f_L = f_0 - \frac{\Delta BW}{2}$
- $f_H = f_0 + \frac{\Delta BW}{2}$
- For double tuned amplifier 2 tank circuits with same f_0 used . $f_0 = \sqrt{f_L f_H}$.

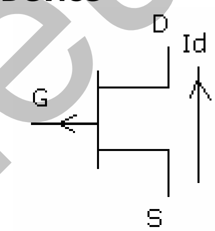
FIELD EFFECT TRANSISTOR, FET is Unipolar Device



Construction

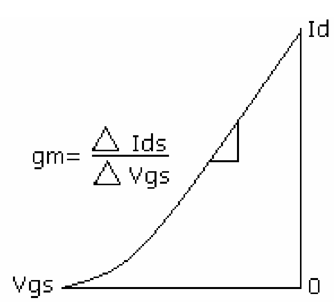


n-Channel

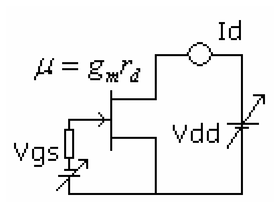


p-Channel

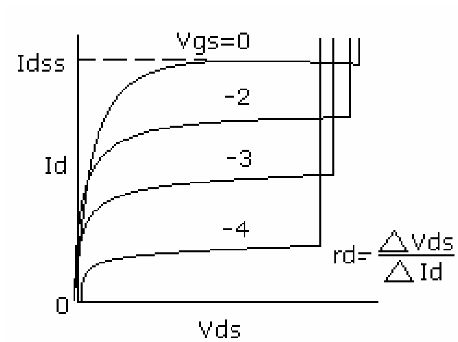
- ➢ S=Source, G=Gate, D=Drain
- ➢ GS Junction in Reverse Bias Always
- ➢ V_{gs} Controls Gate Width
- ➢ VI CHARACTERSTICS



Transfer Characteristics



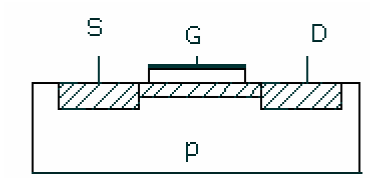
Circuit

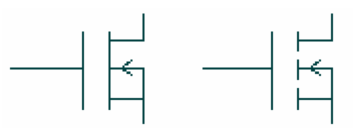


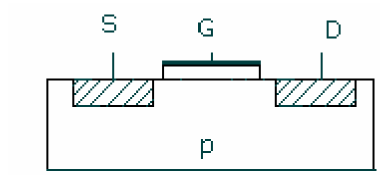
Forward Characteristics

- Shockley Equation
- $I_d = I_{dss}\left(1-\frac{V_{gs}}{V_p}\right)^2$, $g_m = g_{m0}\left(1-\frac{V_{gs}}{V_p}\right)$

MOSFET (Metal Oxide Semiconductor FET, IGFET)







Depletion Type Mosfet **Symbols** **Enhancement Mosfet**

- Depletion Type MOSFET can work width $V_{gs} > 0$ and $V_{gs} < 0$
- Enhancement MOSFET operates with, $V_{gs} > V_t$, $V_t = Threshold\ Voltage$

- NMOSFET formed in p-substrate
- If $V_{GS} \geq V_t$ channel will be induced & i_D (Drain → source)
- $V_t \rightarrow$ +ve for NMOS
- $i_D \propto (V_{GS} - V_t)$ for small V_{DS}
- $V_{DS} \uparrow \rightarrow$ channel width @ drain reduces .

  $V_{DS} = V_{GS} - V_t$ channel width $\approx 0 \rightarrow$ pinch off further increase no effect
- For every $V_{GS} > V_t$ there will be $V_{DS,sat}$
- $i_D = K_n' \left[(V_{GS} - V_t) V_{DS} - \frac{1}{2} V_{DS}^2 \right] \left(\frac{W}{L}\right) \rightarrow$ triode region ($V_{DS} < V_{GS} - V_t$)

  $$K_n' = \mu_n C_{ox}$$
- $i_D = \frac{1}{2} K_n' \left(\frac{W}{L}\right) [V_{DS}^2] \rightarrow$ saturation
- $r_{DS} = \frac{1}{K_n' \left(\frac{W}{L}\right)(V_{GS} - V_t)} \rightarrow$ Drain to source resistance in triode region

PMOS :-

- Device operates in similar manner except V_{GS} , V_{DS}, V_t are –ve
- i_D enters @ source terminal & leaves through Drain .

$V_{GS} \le V_t$ → induced channel $V_{DS} \ge V_{GS} - V_t$ → Continuous channel

$i_D = K_p' \left(\frac{W}{L}\right) [(V_{GS} - V_t)^2 - \frac{1}{2} V_{DS}^2]$ $K_p' = \mu_p C_{ox}$

$V_{DS} \le V_{GS} - V_t$ → Pinched off channel .
- NMOS Devices can be made smaller & thus operate faster . Require low power supply .
- Saturation region → Amplifier
- For switching operation Cutoff & triode regions are used

- **NMOS**   **PMOS**

NMOS	PMOS	
$V_{GS} \ge V_t$	$V_{GS} \le V_t$	→ induced channel
$V_{GS} - V_{DS} > V_t$	$V_{GS} - V_{DS} < V_t$	→ Continuous channel(Triode region)
$V_{DS} \ge V_{GS} - V_t$	$V_{DS} \le V_{GS} - V_t$	→ Pinchoff (Saturation)

Depletion Type MOSFET :- [channel is physically implanted . i_0 flows with $V_{GS} = 0$]

- For n-channel V_{GS} → +ve → enhances channel .
  → -ve → depletes channel
- i_D - V_{DS} characteristics are same except that V_t is –ve for n-channel
- Value of Drain current obtained in saturation when $V_{GS} = 0 \Rightarrow I_{DSS}$.

$\therefore I_{DSS} = \frac{1}{2} K_n' \left(\frac{W}{L}\right) V_t^2$.

MOSFET as Amplifier :-

- For saturation $V_D > V_{GS} - V_t$
- To reduce non linear distortion $v_{gs} << 2(V_{GS} - V_t)$
- $i_d = K_n' \left(\frac{W}{L}\right)(V_{GS} - V_t)\, v_{gs} \Rightarrow$ $g_m = K_n' \left(\frac{W}{L}\right)(V_{GS} - V_t)$
- $\frac{v_d}{v_{gs}} = - g_m R_D$
- Unity gain frequency $f_T = \frac{g_m}{2\pi(C_{gs}+C_{gd})}$

JFET :-

- $V_{GS} \le V_p \Rightarrow i_D = 0 \rightarrow$ Cut off
- $V_p \le V_{GS} \le 0, \; V_{DS} \le V_{GS} - V_p$

$$i_D = I_{DSS}\left[2\left(1-\frac{V_{GS}}{V_p}\right)\left(\frac{V_{DS}}{-V_p}\right) - \left(\frac{V_{DS}}{V_p}\right)^2\right] \Bigg\} \rightarrow \text{Triode}$$

- $V_p \le V_{GS} \le 0 \;, \; V_{DS} \ge V_{GS} - V_p$

$$\left.\begin{aligned} i_D = I_{DSS}\left(1-\frac{V_{GS}}{V_p}\right)^2 &\Rightarrow V_{GS} = V_p\left(1-\sqrt{\frac{I_D}{I_{DSS}}}\right) \\ g_m = \frac{2I_{DSS}}{|V_p|}\left(1-\frac{V_{GS}}{V_p}\right) &= \frac{2I_{DSS}}{|V_p|}\sqrt{\frac{I_D}{I_{DSS}}} \end{aligned}\right\} \rightarrow \text{Saturation}$$

Zener Regulators :-

- For satisfactory operation $\frac{V_i - V_z}{R_s} \ge I_{Z_{min}} + I_{L_{max}}$
- $R_{S_{max}} = \frac{V_{s_{min}} - V_{z_0} - I_{Z_{min}} r_z}{I_{Z_{min}} + I_{L_{max}}}$
- Load regulation $= -(r_z \parallel R_s)$
- Line Regulation $= \frac{r_z}{R_s + r_z}$.
- For finding min R_L take $V_{s\,min}$ & V_{zk} , I_{zk} (knee values (min)) calculate according to that .

Operational Amplifier:- (VCVS)

- Fabricated with VLSI by using epitaxial method
- High i/p impedance , Low o/p impedance , High gain , Bandwidth , slew rate .
- FET is having high i/p impedance compared to op-amp .
- Gain Bandwidth product is constant .
- Closed loop voltage gain $A_{CL} = \frac{A_{OL}}{1 \pm \beta A_{OL}}$ $\beta \rightarrow$ feed back factor
- $\Rightarrow V_0 = \frac{-1}{RC}\int V_i \; dt \rightarrow$ LPF acts as integrator ;
- $\Rightarrow V_0 = \frac{-R}{L}\int V_i \; dt$; $V_0 = \frac{-L}{R}\frac{dv_i}{dt}$ (HPF)
- For Op-amp integrator $V_0 = \frac{-1}{\tau}\int V_i \; dt$; Differentiator $V_0 = -\tau\frac{dv_i}{dt}$
- Slew rate SR $= \frac{\Delta V_0}{\Delta t} = \frac{\Delta V_0}{\Delta t} \cdot \frac{\Delta V_i}{\Delta t} = A. \frac{\Delta V_i}{\Delta t}$
- Max operating frequency $f_{max} = \frac{\text{slew rate}}{2\pi .\, \Delta V_0} = \frac{\text{slew rate}}{2\pi \times \Delta V_i \times A}$.

- In voltage follower Voltage series feedback
- In non inverting mode voltage series feedback
- In inverting mode voltage shunt feed back
- $V_0 = -\eta\ V_T \ln\left(\frac{V_i}{RI_0}\right)$
- $V_0 = -\ V_{BE}$

  $= -\ \eta\ V_T \ln\left(\frac{V_s}{RI_{C0}}\right)$
- Error in differential % error = $\frac{1}{\text{CMRR}}\left(\frac{V_c}{V_d}\right) \times 100\ \%$

Power Amplifiers :-

- Fundamental power delivered to load $P_1 = \left(\frac{B_1}{\sqrt{2}}\right)^2 R_L = \frac{B_1^2}{2} R_L$
- Total Harmonic power delivered to load $P_T = \left[\frac{B_1^2}{2} + \frac{B_2^2}{2} + \cdots\ldots\right] R_L$

$$= P_1\left[1 + \left(\frac{B_2}{B_1}\right)^2 + \left(\frac{B_3}{B_1}\right)^2 + \ \ldots\ldots\right]$$
$$= [\ 1 + D^2\ ]\ P_1$$

Where $D = \sqrt{+D_2^2 + \cdots\ldots + D_n^2}$ $\quad D_n = \frac{B_n}{B_1}$

D = total harmonic Distortion .

Class A operation :-

- o/p I_C flows for entire 360^0
- 'Q' point located @ centre of DC load line i.e., $V_{ce} = V_{cc} / 2$; $\eta = 25\ \%$
- Min Distortion , min noise interference , eliminates thermal run way
- Lowest power conversion efficiency & introduce power drain
- $P_T = I_C V_{CE} - i_c V_{ce}$ if $i_c = 0$, it will consume more power
- P_T is dissipated in single transistors only (single ended)

Class B:-

- I_C flows for 180^0 ; 'Q' located @ cutoff ; $\eta = 78.5\%$; eliminates power drain
- Higher Distortion , more noise interference , introduce cross over distortion
- Double ended . i.e ., 2 transistors . $I_C = 0$ [transistors are connected in that way] $P_T = i_c V_{ce}$
- $P_T = i_c V_{ce} = 0.4\ P_0$ $\quad P_T \rightarrow$ power dissipated by 2 transistors .

Class AB operation :-

- I_C flows for more than 180^0 & less than 360^0
- 'Q' located in active region but near to cutoff ; η = 60%
- Distortion & Noise interference less compared to class 'B' but more in compared to class 'A'
- Eliminates cross over Distortion

Class 'C' operation :-

- I_C flows for < 180 ; 'Q' located just below cutoff ; η = 87.5%
- Very rich in Distortion ; noise interference is high .

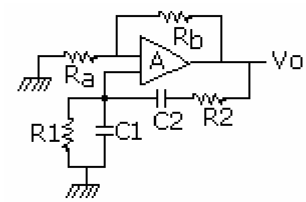
Oscillators :-

- For RC-phase shift oscillator $f = \frac{1}{2\pi RC\sqrt{6+4K}}$ $h_{fe} \geq 4k + 23 + \frac{29}{k}$ where $k = R_c/R$

$$f = \frac{1}{2\pi RC\sqrt{6}} \qquad \mu > 29$$

- For op-amp RC oscillator $f = \frac{1}{2\pi RC\sqrt{6}}$ $|A_f| \geq 29 \Rightarrow R_f \geq 29 R_1$

Wein Bridge Oscillator :-



$$f = \frac{1}{2\pi\sqrt{R_1R_2C_1C_2}},$$

if R1=R2=R, C1=C2=C , $f = \frac{1}{2\pi RC}$; $A = \frac{1}{\beta} = 3$

Hartley Oscillator :-

$f = \frac{1}{2\pi\sqrt{(L_1+L_2)C}}$

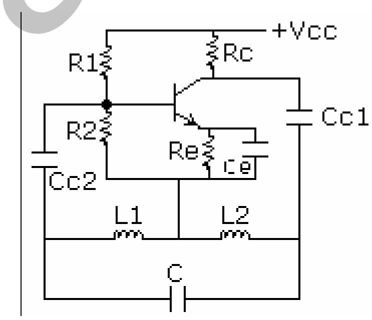
$|h_{fe}| \geq \frac{L_2}{L_1}$

$|\mu| \geq \frac{L_2}{L_1}$

$|A| \geq \frac{L_2}{L_1}$

↓

$\frac{R_f}{R_1}$



Colpits Oscillator :-

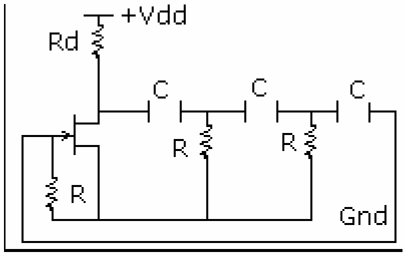
$f = \frac{1}{2\pi\sqrt{L\frac{C_1C_2}{C_1+C_2}}}$

$|h_{fe}| \geq \frac{C_1}{C_2}$

$|\mu| \geq \frac{C_1}{C_2}$

$|A| \geq \frac{C_1}{C_2}$

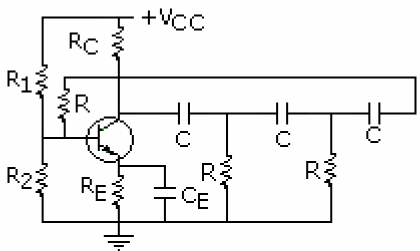
Phase shift oscillator:-



FET MODEL

$$f = \frac{1}{2\pi\sqrt{6}RC}, \quad A = 29,$$

Minimum RC sections 3



BJT MODEL

$$f = \frac{1}{2\pi RC\sqrt{6+\left(\frac{4R_C}{R}\right)}}, A = 29,$$

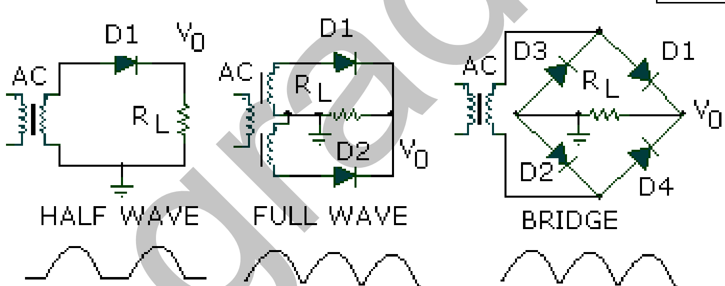
Minimum RC sections 3

Comparisons:

BJT	FET
Current controlled	Voltage controlled
High gain	Med gain
Bipolar	Unipolar
Temp sensitive	Little effect of T
High GBWP	Low GBWP

MOSFET	JPET
High $R_i = 10^{10}$	-10^{8}
$R_0 = 50\ k\Omega$	$\geq 1 m\Omega$
Depletion Enhancement Mode	Depletion Mode
Delicate	Rugged

Rectifiers:



Comparisons:

	HW	FW CT	FW BR
V_{DC}	V_m/π	$2V_m/\pi$	$2V_m/\pi$
V_{rms}	$V_m/2$	$V_m/\sqrt{2}$	$V_m/\sqrt{2}$
γ Ripple factor	1.21	0.482	0.482
η Rectification efficiency	40.6%	81%	81%
PIV Peak Inverse Voltage	V_m	$2V_m$	V_m