TYPE OF QUESTION: MCQ

Semi Design

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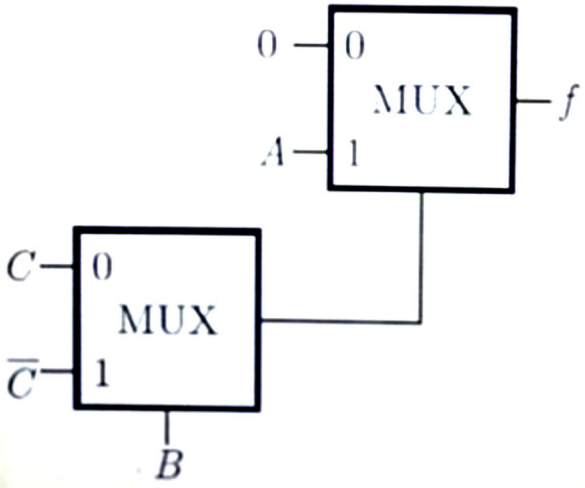
No.of Questions : 10

QUESTION 1:

The boolean function f implemented in the figure using two input multiplexes is :



–

A. A(~B)C + AB(~C)

B. ABC + A~(BC)

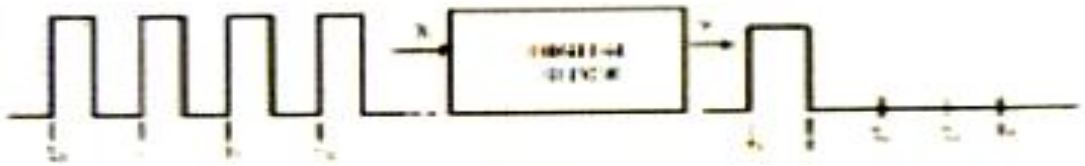
C. (~A)BC +~(ABC)

D. (~AB)C + (~A)B(~C)

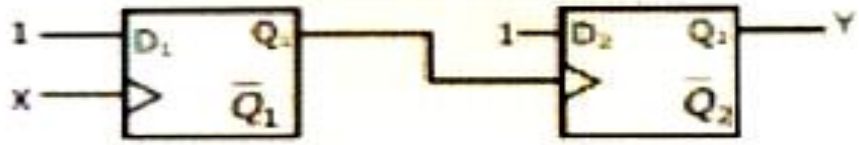
QUESTION 2:

The digital block shown in the figure below is realized using 2 positive edge triggered flipflops. Assume that for t<t0, Q1=Q2=0.

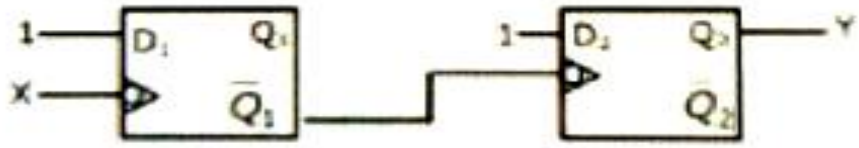
The circuit in the digital block is given by:



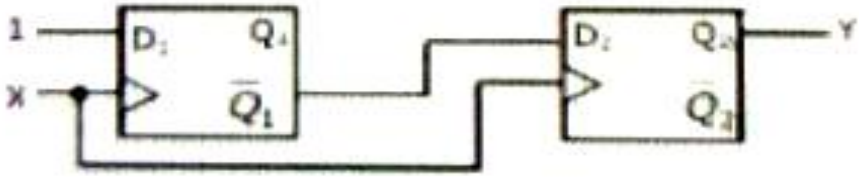
A



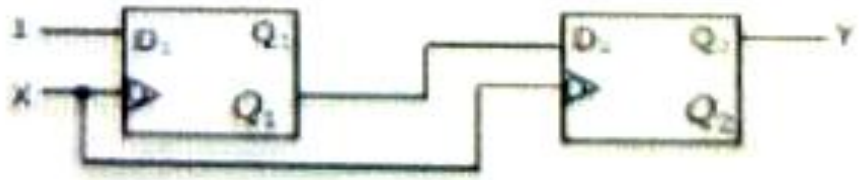
B



C

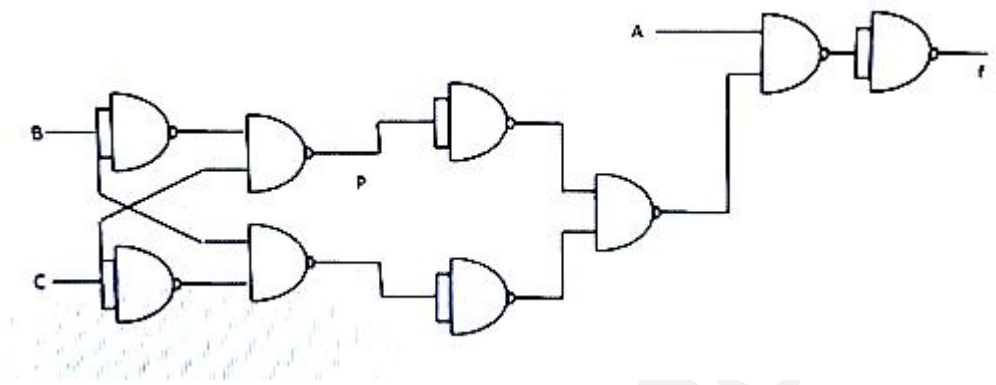


D



QUESTION 3:

In the following figure, if a net Y and W are being driven as shown, what is the resultant strength value on:



E. ~(AB(~C))

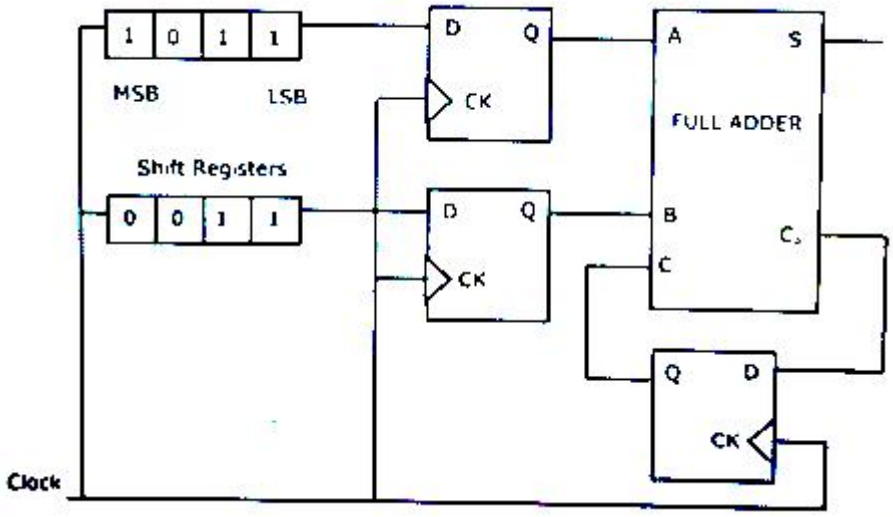
F. ~A

G. AB(~C)

H. A

QUESTION 4:

For the circuit shown in figure below, two parallel-in serial-outshift registers loaded with the data shown are used to feed the data to a full adder. Initially all the the flip flops are in clear state. After applying two clock cycles, the outputs of the full adder should be :



I. S=0, C_0=0

J. S=0, C_0=1

K. S=1, C_0=0

L. S=1, C_0=1

QUESTION 5:

A boolean function f of two variables x and y is defined as follows :

f(0, 0) = f(0, 1) = f(1, 1) = 1; f(1, 0) = 0;

Assuming complements of x and y are not available, a minimum cost solution for realizing f usign only 2- input NOR gates and 2-input OR gates(each having unit cost) would have a total cost

M. 1 unit

N. 4 units

O. 3 units

P. 2 units

QUESTION 6:

Analyze the code segment and choose the right answer.

```
module top;

assign out=a&b|c;

initial begin

#50 force out=a&b&c;
#50 release out;

end
endmodule
```

Q. Expression a&b&c is assigned to net from 50 to 100

R. a&b&c overrides assignment of a&b|c completely throughout the simulation time

S. All of the above

T. None of the above

QUESTION 7:

Analyze the code below and choose the right options?

```
reg clock;
initial begin
clock=1'b0;
forever #10 clock=~clock;
end
```

A. The forever loop will execute the statement infinitely

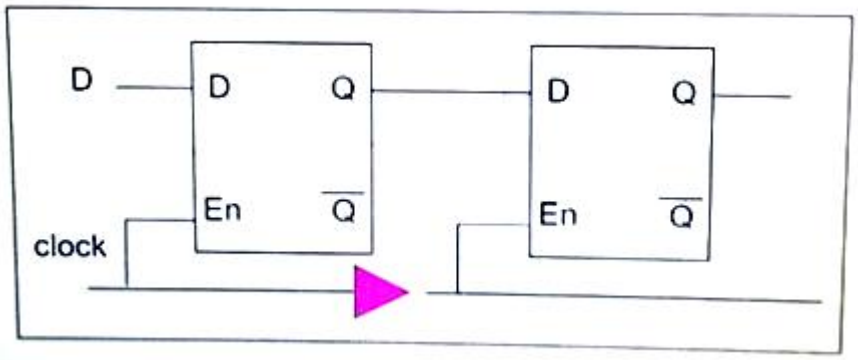
B. Timing control construct is optional in forever

C. All of the above

D. None of the above

QUESTION 8:

A master slave flipflop has the characteristic that :



A. Change in the input immediately reflected in the output

B. Change in the output occurs when the state of master is affected

C. Change in the output occurs when the state of slave is affected

D. Both master and slave states are affected at same time

QUESTION 9:

What is the order of execution of below code?

```
module zero;
reg a,b,c;

//initial block with zero delay

initial
begin
#0 a=1;
#0 b=1;
#0 c=1;
$display("zero delay control a=%b, b=%b, c=%b", a,b,c);
end

//initial block without zero dealy

initial c=0;
initial
begin
a=0;
b=0;
$display("zero delay control a=%b, b=%b, c=%b", a,b,c);
end

endmodule
```

A. zero dealy control statement is executed first

B. zero dealy control statement is executed only after all other statements

C. zero dealy control statement is non-deterministic

D. None of the above

QUESTION 10:

What is missing in top module of below code segment

```
module my_verilog;
parameter p1 = 5;
initial $display("displaying my_verilog=%d",p1);
endmodule

module top;
defparam q1.p1=6,q2.p1=4;
endmodule
```

A. Initial statement

B. One module instance of my_verilog

C. Two module instance of my_verilog

D. All of the above

*****END*****