TEST 2 (QUEST SEASON 3)

*****NEGATIVE MARKING IS THERE*****

Name: class Total questions: 25 Time: 40min

1. Verilog HDL originated at

   A. AT&T Bell Laboratories
   B. Defence Advanced Research Projects Agency (DARPA)
   C. Gateway Design Automation
   D. Institute of Electrical and Electronics Engineers (IEEE)

2. Verilog is an IEEE standard

   A. IEEE 1346

   B. IEEE 1364

   C. IEEE 1394

   D. IEEE 1349

3. Which level of abstraction level is available in Verilog but not in VHDL?

   A. Behavioral level

   B. Dataflow level

   C. Gate level

   D. Switch level

4. In verilog `h1234 is a

   A. 16 bit hexadecimal number

   B. 32 bit hexadecimal number

   C. 4 bit hexadecimal number

   D. It is invalid notation

5. Which logic level is not supported by verilog?

   A. U

   B. X

   C. Z

   D. None of the above

6. If a *net* has no driver, it gets the value

   A. 0

   B. X

   C. Z

   D. U

7. Default value of *reg* is

A. 0

B. X

C. Z

D. U

8. The task *$stop* is provided to

A. End simulation

B. Suspend simulation

C. Exit simulator

D. None of the above

9. Externally, a output port must always connected to a

A. net only

B. a reg only

C. either net or reg

D. None of the above

10. If A= 4`b011 and B= 4b`0011, then the result of A**B will be

A. 6

B. 9

C. 27

D. Invalid expression

11. If A= 4b`001x and B= 4b`1011, then result of A+B will be

A. 110x

B. 1100

C. xxxx

D. None of the above

12. If A= 4`1xxz and B= 4`b1xxx, then A= = =B will return

A. 1

B. X

C. Z

D. 0

13. Result of 9% -2 will be

A. 4

B. 4.5

C. -1

D. +1

14. Initial value of a=1 and b=2, then what will be final value if

```
always @ (posedge clock)
        a=b;
always @ (posedge clock)
        b=a;
```

A. a= 2, b=1

B. a= 1, b=2

C. Both a and b will have same value either 0 or 1

D. None of the above

15. Initial value of a=1 and b=2, then what will be final value if

```
always @ (posedge clock)
        a<=b;
always @ (posedge clock)
        b<=a;
```

A. a= 2, b=1

B. a= 1, b=2

C. Both a and b will have same value either 0 or 1

D. None of the above

16. Given the following Verilog code, what value of "a" is displayed?

```
always @ (clock) begin
a = 0;
a <= 1;
$display(a);
end
```

A. 0

B. 1

C. either 0 or 1 depending on depending on simulator implementation

D. None of the above

17. In a pure combinational circuit is it necessary to mention all the inputs in sensitivity list?

A. No

B. Yes

C. It depends on the coding style

D. None of these

18. How many flops will be synthesized by the given code?

```
always @ (posedge clock) begin
Q1<=d;
Q2<=q1;
Q3<=q2;
end
```

A. 1

B. 2

C. 3

D. None of the above

19. Which is not a correct method of specifying time scale in verilog?

A. 1ns/1ps

B. 10ns/1ps

C. 100ns/100ps

D. 100ns/110ps

20. If time scale is defined as `timescale 10ns/1ns and #1.55 a = b; then 'a' gets 'b' after

A. 10ns

B. 11 ns

C. 15.5ns

D. 16ns

21. A task can have arguments of type

A. Input only

B. Output only

C. Both input and output

D. All input, output and inout

22. If a recursive function is called concurrently from two locations, then

A. Recursive function can have multiple calls concurrently

B. It will result give ambiguous results

C. It will result in an error

D. Simulation will hang up

23. Which operators has highest precedence in verilog

A. Unary

B. Multiplication

C. Addition

D. Conditional

24. In the given code snippet, statement 2 will executed at

```
initial
begin
        #5 x= 1'b0;       // statement 1
        # 15 y= 1b'1;    //statement 2
End
```

A. 15

B. **20**

C. 5

D. Current simulation time

25. Variable and signal which will be updated first?

A. Variable

B. **Signal**

C. Can't say

D. None of the above