OP AMP Reading Material Part 1

OP AMPS

Add a note on LIC

1. What is an op amp?

It is essentially a voltage amplifier with very high gain, very high input resistance, very low output resistance, and moderate bandwidth. It has a balanced dual input stage (a difference amplifier), and single ended output. In other words, input at one input terminal produces an in phase output, whereas input at the other input terminal produces out of phase output.

The op amp can be found in diverse applications and it derives its name from amplifier circuits that were used to perform mathematical operations in analogue computers. It can be easily designed into circuits for various operations like summing, subtraction, differentiation, and integration, in addition to normal amplifier functions. We will see some of the circuit applications later.

2. Symbol and brief description

See figure 1.

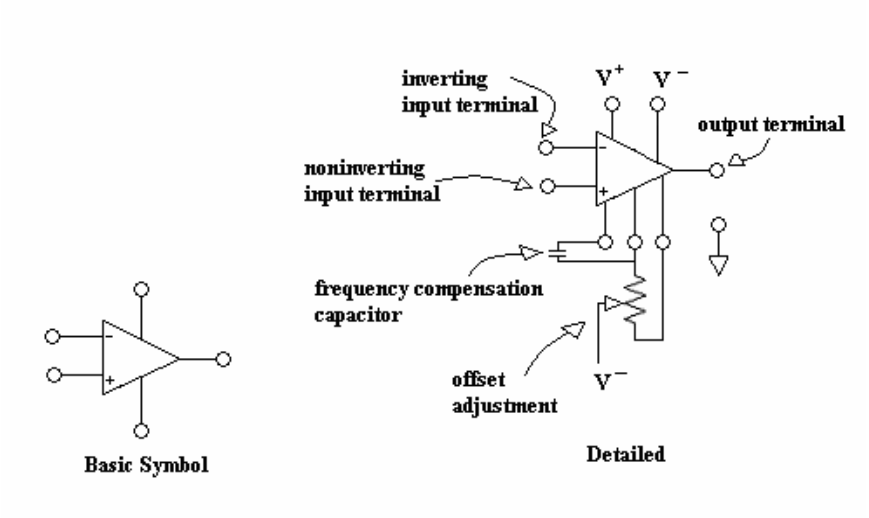

Figure1. Op amp symbol and details.

Two input terminals: inverting input terminal and noninverting input terminal.
One output terminal: Output is in phase with the signal at the noninverting input terminal, and is out of phase with the signal at the inverting input terminal. (Please do not say negative terminal and positive terminal.)
Two terminals are provided for supplying the bias voltages. Generally, positive and negative supplies are required. There are op amps which need only single supply. Reference for output is the common of the two power supplies.
Three additional terminals may be provided as shown: for offset voltage adjustment and for control of frequency response. (We will see more details on these later.)

3. Packages
Opamps are available in different packages like the metal can (TO), dual-in-line package (DIP), and the flat package. [Refer any standard text book for more details.]

4. Op Amp Terminals
Op amps have five basic terminals as shown in the top view of a can package in figure 2.

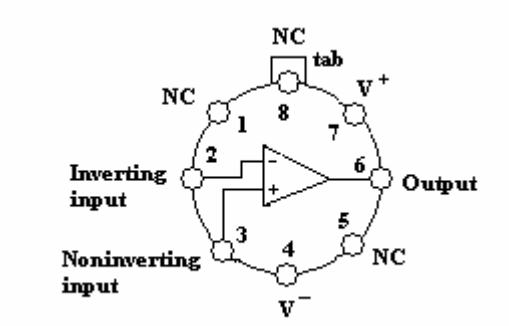

Figure 2: Connection diagram for a can package; terminal numbers as seen from top.
The can has 8 pins. Pin number 8 is identified by a tab as shown. The other pins are numbered counterclockwise, from 8, beginning with pin 1. The basic terminals are the two input terminals (pins 2 and 3), the output terminal (pin 6), and the power supply terminals (pins 4 and 7). The power supply terminals are labeled V^- and V^+ in the figure. The terminals marked NC are shown with regard to the normal 741 op amp, and these need no external connection, for normal applications. In many op amps these terminals find use in connecting external circuits for offset and frequency compensation (details to be seen later). Remember that the pins which do not need any external connections are also to be firmly soldered to the pcb so that the whole ic gets well supported.
Figure 3 shows the connection diagram for an 8-pin DIP package and figure 4, for a 14-pin DIP package. (Both are top views.)

Pin configuration

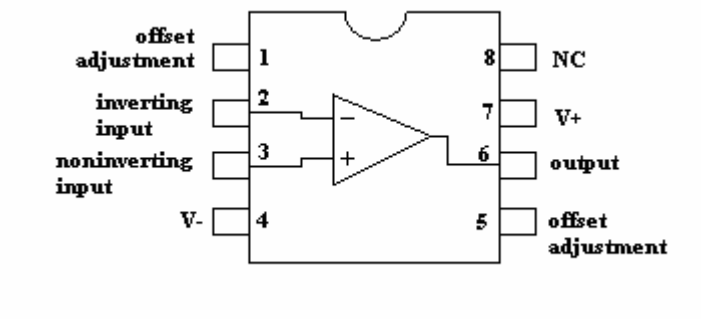

Figure 3: Connection diagram for 8-pin DIP; as seen from top.

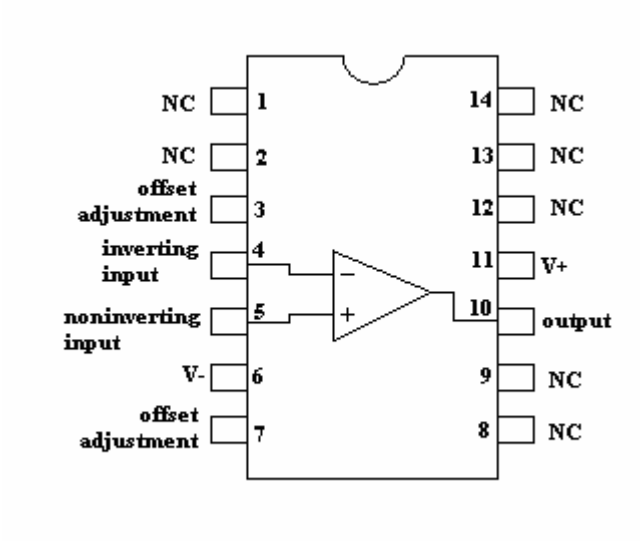

Figure 4: Connection diagram for 14-pin DIP; as seen from top.

5. Power supply requirements.

Op amps generally need dual supply. Values from +/- 12 V to +/- 18 V could be used. Sensitivity to supply variations is, in general, very minimal. Op amps with supply voltages as low as 2.5 V are now available.

As seen in the previous section, the terminals on to which the positive and negative supplies are to be connected are clearly identified. Most of the op amps are protected damage due to power supply reversal. As an additional precaution, some designers prefer to employ diodes in series with the supplies, as shown in figure 5, so that supply reversal will not lead to any damage to the op amp.

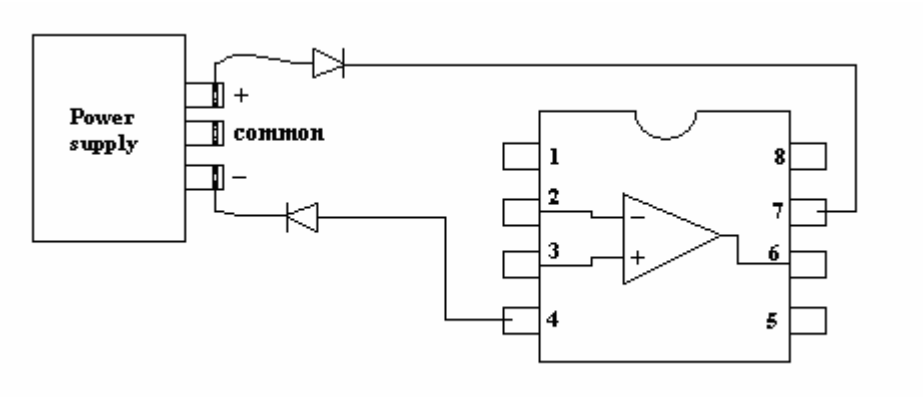

Figure 5: Safe connection of power supplies.

6. Block Diagram

Here we will attempt only a very brief discussion on the internal scheme of an op amp. We will see more about it later.

The general purpose bipolar op amp contains three basic circuit blocks. They are (i) the input differential amplifier, (ii) a common emitter amplifier, and (iii) the output stage which is an emitter follower. Figure 6 shows the scheme. [Remember that it is not the circuit; it is only the block scheme.

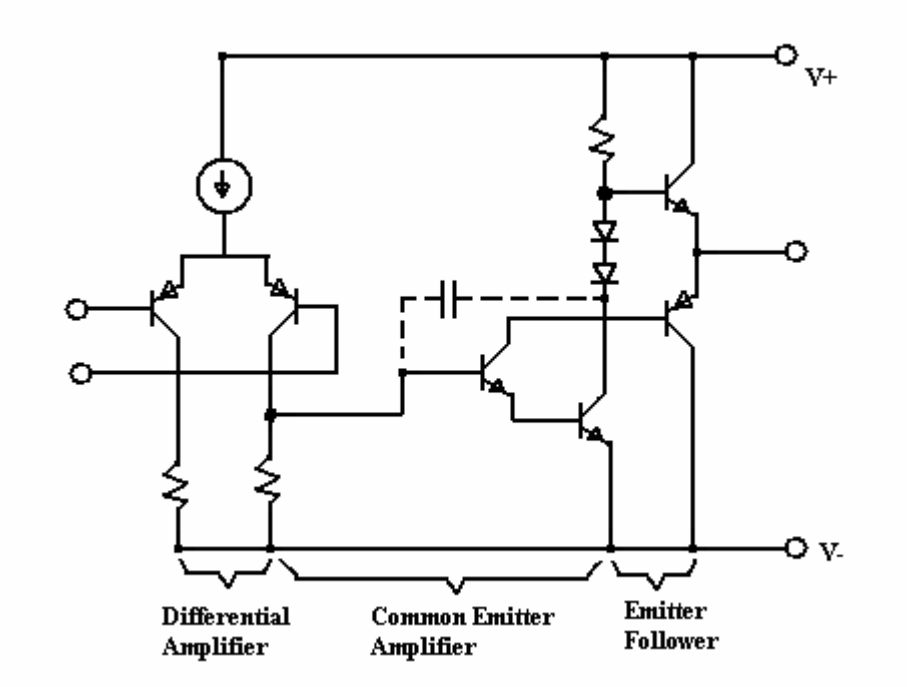

Figure 6: Simplified scheme of op amp

The first two stages provide the high gain of around $2x10^5$. First stage provides high input resistance, and high common mode rejection. The output emitter follower stage provides very low output impedance. The capacitor shown, connected by broken lines, is for frequency compensation.

7. Op Amp Parameters

Recollect what we discussed in section 1. It must be possible for you to identify the important performance parameters of an op amp.

We can group the performance parameters generally into two classes, namely the dc parameters and the ac parameters. These are not to be taken as two exclusive sets of specifications. It is not to be taken that one set is only applicable to dc functions, and the other set only to ac functions. The dc parameters are all required to be considered for ac applications as well. The ac parameters will not be strictly applicable for normal dc and low frequency applications. But, be sure that the ac parameters need due attention not

only for ac functions, but are necessary to be considered for all pulse applications including dc.

From sections 7.1 to 7.14 we consider the dc parameters, and from 7.15 to 7.19, we present the important ac parameters. Then in one section, 7.20, we will briefly cover what are called the absolute maximum ratings.

7.1. Open loop gain (A_{OL})

An op amp is essentially a voltage amplifier with very high gain. The gain is so high that for most applications we use it with reduced gains, achieved through negative feedback. We will learn more about feedback later. Now consider what will happen if we connect an op amp as shown in figure 7. The op amp has no elements connected between the output and any of the input terminals, or in other words, there is no feedback. Such a

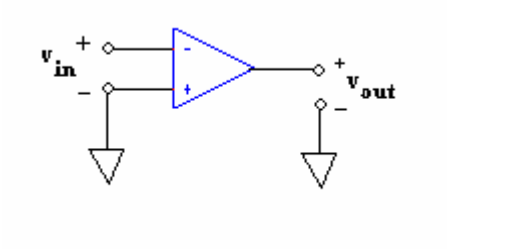

Figure 7: Open loop circuit

circuit is called an open loop circuit. You may say that the op amp is operating in the open loop mode. The gain you get now is termed the open loop gain. Open loop gain is one of the most important performance parameters of any op amp. It must be as high as possible. Ideally it must be infinite. In practice, with dc input, the open loop gain may range in magnitude from 10^5 to 10^9. Open loop gain has dependence on frequency, which we will learn in detail, later.

The extremely high gain of the op amp helps to design circuits with performance controllable very well with external components. In fact, it is this high open loop gain which makes the op amp really ‘operational’.

Typical value for 741: 2×10^5

7.2. Input impedance (Z_i)

A second important parameter is input impedance. We will be concerned mostly with comparatively low frequency applications. So we will neglect the input capacitance, and talk about input resistance only. What do you mean by input resistance? Do you mean that if you measure the resistance between the two input terminals using a multimeter, the value shown by the meter is the input resistance? No. Input resistance is effectively an active component. You cannot do a straight measurement of it.

Input resistance tells you about the current which can be expected to be drawn from a source connected to the input. You have already a current passing between the two input terminals inside the device. This current is very very small, normally taken to be zero. There could be a change in this current when you connect an input. You may conceive input resistance as the ratio of the change in input voltage to the change in this current. An op amp is expected to have very high input resistance.

Typical value: 0.2 M Ω to 2 MΩ.

7.3. Output resistance (R_O)

This is the resistance seen between the output terminal and the signal reference/power supply common. When the op amp is to feed signal (a voltage) to the stage coming next, we can treat the op amp as a source, in which case we can see the output resistance as the source resistance. It implies the current driving capability of the op amp output. Lower the output resistance, higher the current which can be drawn from the op amp. Of course, maximum current which can be got from the output will depend on the output voltage level and the output power rating of the op amp. An op amp is expected to provide as low output impedance as possible.

Typical value: 5 Ω to500 Ω.

7.4. Input offset voltage (V_{os} or V_{io})

Ideally, the output of an op amp must be zero if there is no input. But this is never the practical case. There is always a nonzero output. We can make it zero by giving a suitable voltage at the input. The dc voltage which must be given between the input terminals to make the output equal zero is called the input offset voltage. In many op amps a pair of terminals is provided for implementing a simple circuit to force the output to be zero.

A typical circuit used for offset adjustment is shown in figure 8.

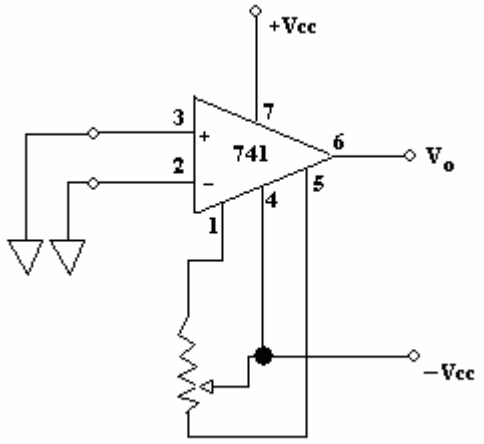

Figure 8: Typical circuit for input offset adjustment.

What does the offset potential, the pd between the input terminals, represent? You know that the input stage is a differential amplifier, and you want the two input transistor stages to be perfectly balanced. But it can never be so. The input offset voltage can be related to the mismatch in the transistor parameters and the mismatch in the loading of the two halves of the differential amplifier circuit.

Typical input offset voltage: 0.5 mV to 10 mV.

It is important to note that the input offset voltage is temperature dependant. It can vary by a few $\mu V/^{o}C$. This temperature dependence originates from the temperature dependence of base-to-emitter voltage of the input stage transistors. Remember that initial nulling of the offset voltage will not eliminate the issue of the effect due to temperature variation. Sometimes, your compensating circuit may worsen the situation, the circuit itself contributing to the variation.

7.5. Input bias current (I_B)

The functioning of an op amp needs biasing of all the internal active components. Consider the input differential amplifier stage of the op amp. The two input terminals are connected to the base of the two transistors of the differential stage. For the differential amplifier to function, base currents must pass. This happens when you connect external circuit to the two input terminals. [You may look at it another way. You must provide external paths at the two inputs for the bias currents to flow, so that the amplifier can function.] This current which passes into, or out from, the input terminals is called the input bias current. Ideally the currents into, or out from, the two input terminals must be equal. [Remember that we are talking of a balanced input stage.] But in practice the two currents are never exactly equal. We give the mean value of the two currents as the input bias current. The currents are represented in figure 9. Note that external resistors are shown to provide paths for the bias currents. [The figure does not represent any practical circuit.]

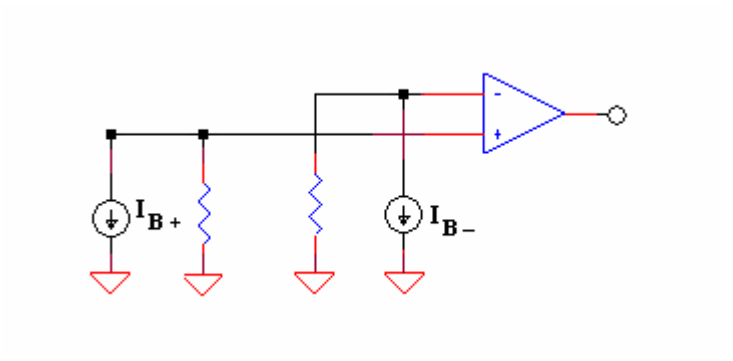

Figure 9: Input bias currents

$$I_B = \frac{I_{B+} + I_{B-}}{2}$$

I_{B+} is the current entering/leaving the noninverting input terminal, and

I_{B-} is the current entering/leaving the inverting input terminal.

How do we know whether the current is entering or leaving? [Try to recollect your lessons on npn and pnp transistors. Remember how you mark the arrow on the emitter. Extend this arrow to the base.]

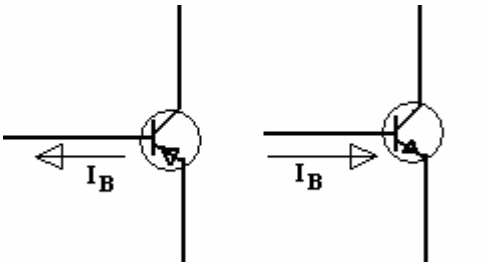

Figure 10: Base currents in npn and pnp transistors.

For monolithic op amps with npn transistors in the differential stage, the direction of the currents is *into* the transistor through the base (*into* the op amp), and for pnp transistors the direction of the currents is *out from* the transistor through the base (*out from* the op amp).

Input bias current is also temperature dependant.

Typical value of input bias current for 741 is 80 nA at 25 ^oC.

IC designs use super beta transistors and Darlington or complimentary pairs to reduce the value of the bias current. Bias current of op amps which make use of JFET in the difference amplifier stage, is one or two orders less than that of those which use BJTs.

7.6 Input offset current (Ii_O)

We have already seen that the two input bias currents are never equal. With the output set to zero, there is always a difference between the two input currents. This difference is called the input offset current.

$$I_{io} = \left| I_{B+} - I_{B-} \right|$$

Think it over: Which is more, input bias current or the input offset current?

Typical value of offset current for 741 is 20 nA at 25 ^{o}C.

7.7 Input voltage range (V_i)

It is the maximum input voltage that can be applied to any of the input terminals with respect to ground. If this limit is exceeded the amplifier performance becomes nonlinear. It is about 12V for 741.

7.8 Maximum peak to peak output voltage swing (V_{opp})

This represents the maximum output voltage swing without clipping the output wave form for the condition where the quiescent output is zero. More strictly it could be seen as the maximum swing at the output with linear performance of the amplifier. Its value is primarily established by the dc supply voltages and the output current. The manufacturer guarantees this parameter using a graph of output voltage versus supply voltage for some value of load resistance (typically 2kΩ and 10kΩ). Typical value for 741 is 27 V.

7.9 Common mode rejection ratio (CMRR)

An op amp is expected to work as a differential amplifier. That means that the amplifier should not pass the same signals applied at both the inputs together, to the output. Signal appearing at both inputs together is called common mode signal. Ideally amplifier gain for common mode signal must be zero, or in other words, common mode signals must be rejected totally by the op amp. In practice, common mode signals also get low priority pass to the output; they do not get completely rejected. Then how can we say how good an amplifier is with respect to the capability of rejecting common mode signals? We introduce a figure of merit called common mode rejection ratio. We compare the capability of the amplifier to amplify the difference signal with its capability to reject the common mode signal. It is a very important term in instrumentation. Let us see in some more detail.

Let us first get more clarity on common mode signal itself. We said that it is the same signal appearing at both inputs together. You must realize that the difference signal (which is in fact the actual signal) is also simultaneously present. How do you distinguish between the two? Let us see an example. Suppose that the two input levels are +100 mV and +200 mV. The total difference signal now is 200 – 100 = 100 mV. We can see it as +50 mV at one input and -50 mV at the other input. Taking both common mode and difference signals together we can give the inputs as: (150 + 50) mV [=200 mV] at one input and (150 – 50) mV [=100 mV] at the other input. So, at both inputs we have 150 mV as common. Is it not clear that 150 mV is the common mode signal?

In general, we can express input levels at the two inputs as $v_c + v_d/2$ and $v_c - v_d/2$.

Obviously both common mode and difference signals are present together at the inputs. The above discussion should help us to get these two separately.

Let v_1 and v_2 be the levels at the two input terminals. Then

$v_1 = v_c + v_d/2$ and

$v_2 = v_c - v_d/2$

We get

$v_c = (v_1 + v_2)/2$ and $v_d = (v_1 - v_2)/2$

[Take the example discussed above, for example. $v_c = (200 + 100)/2 = 150$ mV, and

$v_d = (200 - 100)/2 = 50$ mV.]

Figure 10 shows how a common mode voltage is modeled.

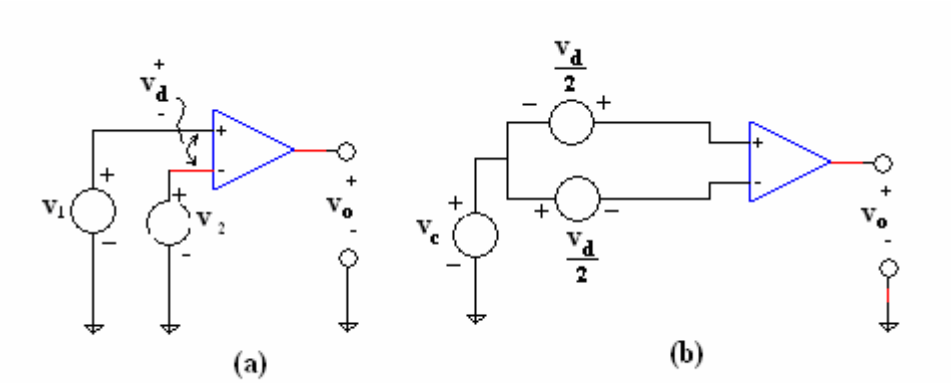

Figure 11: Modeling a common mode voltage.

Based on the model given in figure 11, we can do the following analysis for common mode error.

Let us assume that the dc offset at the output is first adjusted to zero. Now apply a common signal at both the inputs. Ideally we must get zero at the output. But as we have already discussed, it is never so; instead there is always a common mode output. This is called the common mode error. This is due to the difference in voltage gains available to the signals at the two input terminals. Let us designate the individual voltage gains by A^+ and A^-; A^+, for input at the noninverting input terminal, and A^-, for the input at the input at the inverting input terminal. ($A^+ > 0$, and $A^- < 0$).

Expression for output is then,

$$v_o = v_c(A^- + A^+) + \frac{1}{2} v_d (A^- - A^+)$$

or

$$v_o = v_c A_c + v_d A_d$$

where A_d is the differential gain, and A_c is the common mode gain.

$$A_c = A^+ + A^-$$

and

$$A_d = \frac{1}{2}(A^+ - A^-) .$$

Now we take the ratio A_d / A_c as the figure of merit for common mode rejection. This is defined as the common mode rejection ratio (CMRR). This is generally expressed in dB using the expression

$$CMRR = 20 \log(A_d / A_c) , \text{ dB.}$$

We can give expression for output in terms of common mode input signal (v_c) , differential input signal (v_d) , common mode rejection ratio(CMRR), and the differential gain (A_d) as

$$v_o = A_d (v_d + v_c / CMRR)$$

Look at the above expression. It is obvious that the incomplete common mode rejection (having CMRR less than infininity) can be represented by an equivalent input offset voltage equal to v_c/CMRR. In other words, you may define CMRR also as follows:

Common mode rejection ratio is the ratio of a change in common mode signal to the resulting change in input offset voltage.

CMRR is of great significance when we are dealing with low level differential signals, especially in environments where noise pick ups could be expected. There are contexts where part of an excitation voltage itself appears as common mode signal. This could be ac or dc. The common Wheatstone bridge application is an excellent example, where half the excitation voltage appears as common mode signal. This is illustrated in figure 12.

Exercise: In the circuit shown in figure 12, suppose we are using an ac excitation voltage of 10 Vpp. Suppose the minimum signal expected from the bridge is 1mVpp. This is to be amplified to a level of 1 Vpp. Find the minimum value of CMRR required so that the error due to the excitation voltage appearing at the input of the amplifier is less than 1%. [Answer: 114 dB]

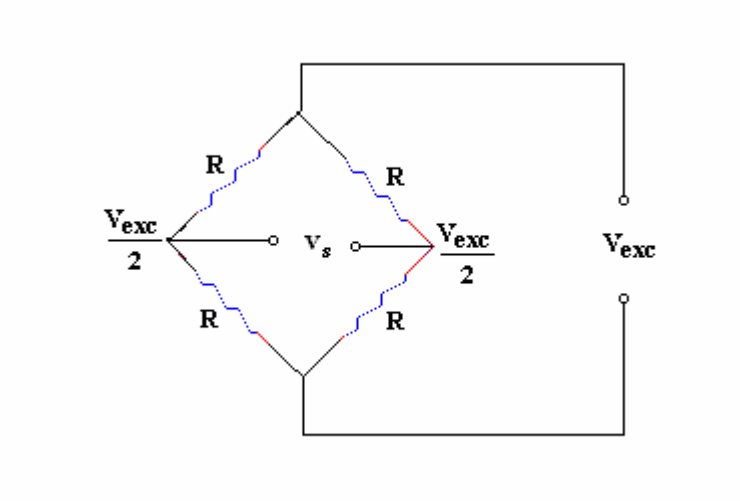

Figure 12: Common mode signal from Wheatstone bridge.

7.10. Supply voltage sensitivity ($\Delta v_{io} / \Delta v_{cc}$)

Ideally, performance of an op amp should not be sensitive to power supply variations. This is not achieved cent per cent in practice. Changes in supply voltage do affect the performance. One should know how much this is, so that appropriate supply can be used, to get desired performance. Supply voltage sensitivity is an index of the impact of power supply variations on the performance.

Supply voltage sensitivity is assessed in terms of the change in input offset voltage caused by the change in supply voltage. It is defined as the ratio of change in input offset voltage to the change in the supply voltage which caused it, ie., $\Delta v_{os} / \Delta v_{cc}$.

Supply voltage sensitivity is sometimes given as voltage supply rejection ratio (VSRR), supply voltage rejection (SVR) or sometimes as power supply rejection ratio (PSRR). You need not be much worried about the actual terminology, more important is the concept.

PSSR = $\Delta v_{io} / \Delta v_{cc}$

Data sheets normally give it in dB.

PSSR, dB = 20 log ($\Delta v_{io} / \Delta v_{cc}$)

Normally we get 80 dB to 100 dB of PSSR.

Exercise: Specification sheet for 741 gives its PSSR as 94 dB. Calculate the change in input offset voltage for supply voltage change of 15V to 16 V.

7.11. Large Signal Differential Voltage gain (A_{VD})

This is the ratio of the output voltage swing to the change in input voltage required to produce this output swing. It is not generally given as a number, but as mV/V.

Typical value for 741 is 200V/mV for an output swing of $\pm 10V$.

7.12. Short circuit output current (Io_{SH})

It is not advisable to short the output, especially with an input on, or with an expected output. But accidental shorting for very short durations cannot be totally ruled out. Op amps generally provide short circuit protection, in the forem of an output current limiter. Maximum output current available from the op amp with the output terminal connected to ground or to either of the supplies is called the short circuit output current.

Typical value for 741 is 25 mA.

7.13. Total power dissipation (P_D)

The op amp has a number of stages. Each stage needs a minimum level of operating current. The current is drawn from the power supplies. Current is drawn from both the positive and negative supplies. The power thus dissipated by the op amp without any load connected to it is called the total power dissipation. Some manufacturers specify power dissipation for small signal condition. The two cases differ only marginally. Total power dissipation may be given as

$PD = V_{CC+}.I_{CC+} + V_{CC-}.I_{CC-}$

where V_{CC+} and V_{CC-} are the positive and negative supplies respectively, I_{CC+} is the current drawn from the positive supply, and I_{CC-} is the current drawn from the negative supply. It is a temperature dependent parameter, and in general it increases with temperature.

Typical value for 741 is 50 mW at 25^oC.

7.14. Offset voltage adjustment range, Δv_{io}.

We have seen the meaning of input offset voltage. We have also seen that input offset voltage could vary from around 0.5 mV to about 10 mV, typically. Try to assess its

impact when you design an amplifier using the op amp. The input offset voltage also will get amplified. This may not at all be desirable except for very low gain applications.

We will attempt a more detailed discussion of the impact of offset voltage at a later stage. Now let us be clear that we cannot permit, in many cases of application, the presence of an offset voltage. That is why manufacturers of op amps give provision for offset adjustment. Data sheet gives the range of values of offset which could be adjusted to zero. This is given as offset voltage adjustment range.

Typical value of offset voltage adjustment range for 741: $\pm 15mV$. This is much more than the offset specification itself. This means that small values of offset voltages generated on interfacing of signal sources also can be adjusted. One should not attempt to supply high levels externally at the input to balance off the offset voltage, if it happens to be very much more than the specification; the op amp could be defective.

A typical circuit used for offset adjustment is shown in figure 13.

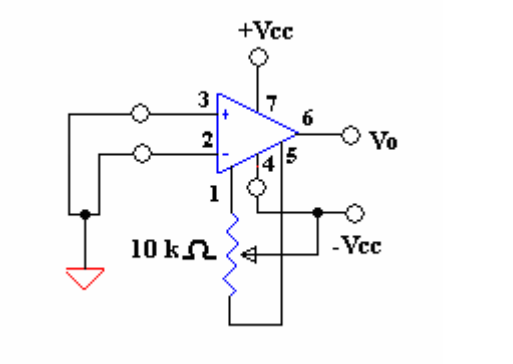

Figure 13: Circuit for nulling offset voltage.

7.15. Gain-Bandwidth product

We have discussed about the open loop gain. We said that seldom we use circuits with open loop gain. We make use of negative feedback to attain stable performance with desired gain, which is much lower than the open loop gain. We will discuss about feed back and how we design circuits with required gain, later. Now we discuss another important aspect about the performance of amplifiers, which will definitely be applicable for oscillators as well.

Does the gain of an amplifier vary with frequency? You must be aware of this. You have learned about frequency response of transistor amplifiers. Gain is a frequency dependent parameter. For all normal dc amplifiers, gain decreases with frequency beyond a certain frequency. The rate of reduction depends on the number of poles in the transfer function, which is the ratio of the output phasor to the input phasor. Most of the op amps make use of single pole transfer function. Linearised (neglecting minor gradual variation in the pass band, and eliminating the corner curving) model of the transfer function is as shown in figure 14. The cut off frequency is very low, generally less than 10 Hz. Then the gain falls

by 6 dB/octave (20 dB/decade), which means that for every scaling up of frequency by 10, the gain falls by 20 dB. Examples of three closed loop gains are shown by coloured lines.

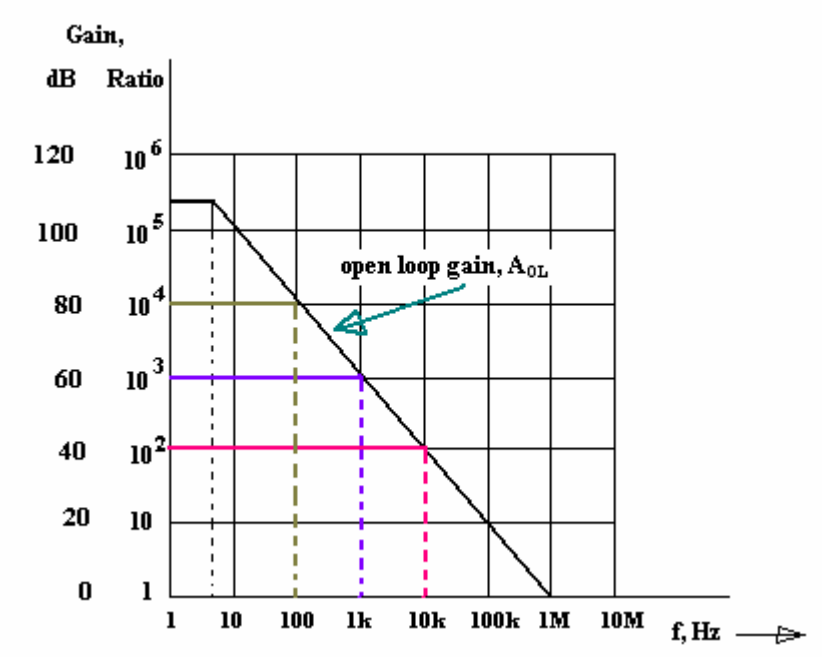

Figure 14: Variation of gain with frequency

For a gain of 10^4, bandwidth is 100 Hz;

product of gain and bandwidth = 10^4 x 100 =10^6.

For a gain of 10^3, bandwidth is 1 kHz = 1000 Hz;

product of gain and bandwidth = 10^3 x 1000 =10^6.

For a gain of 10^2, bandwidth is 10 kHz = 10000 Hz;

product of gain and bandwidth = 10^2 x 10000 =10^6.

And, for bandwidth of 1 MHz (10^6 Hz), gain available is unity.

You can see that the product of the closed loop gain and the bandwidth is a constant. This is given as a specification of the device, named the gain-bandwidth product. You may define the gain-bandwidth product as the unity gain bandwidth.

Note: Do not be under the impression that you can use the given op amp for a gain equal to the ratio of gain bandwidth product and the band width required. The op amp may not

approve your design. The voltage swing of the signal is also to be taken into account. We will see this aspect in detail later.

Exercise:
1.Assuming that all other specifications of the given op amp are ok, estimate (i) the gain possible for a signal of maximum frequency of 12.5 kHz; (ii) the bandwidth for a gain of 80.

2. Can you get gain of more than the magnitude of the gain-bandwidth product, for frequencies less than 1 Hz? Justify your answer.

7.16. Slew rate (SR)

Any ac signal has a rate of change of level associated with it. Can the op amp respond to any value of this rate of change? Is it controlled only by the frequency response specification?

How do you answer the above question?

Let us see a simple example. Let us represent a signal by

$$v = v_o \sin \omega t = v_o \sin 2\pi ft \quad \ldots \quad (7.16.1)$$

In the above relation, v represents the time varying signal with a maximum value of v_o; f is the frequency of the variation. The above relation represents the variation with time, ok. But do you get an idea of how fast it varies? For that, we have to see the derivative:

$$\frac{dv}{dt} = 2\pi f v_o \cos 2\pi ft \quad \ldots \quad (7.16.2)$$

What does it mean? The rate of variation of the signal level at any instant is proportional to the frequency and the amplitude of the signal. The maximum value of the rate of variation is $2\pi f v_o$. So frequency response alone cannot decide the response; the op amp must see the total rate, which means that both amplitude and frequency of the signal are to be considered. Let us try to illustrate it further through examples with numerical values.

Let us consider an amplifier using an op amp of gain bandwidth product 1 MHz. Let us take the dc gain as 100. We can normally expect that the frequency response will be 10 kHz (1 MHz/100). Let us check how far this expectation could be satisfied.
Consider two input signals at 10 kHz: one with amplitude of 20mV and the second, with amplitude of 100 mV. We expect to get 2V peak at the output for the former signal, and

10 V peak for the latter. Based on relation (7.16.2), we can calculate the maximum demanded rate of change of voltage at the output of the op amp as follows.

For 20 mV input:

$$\frac{dv}{dt} = 2\pi f v_o \cos 2\pi ft \quad = 2\text{x}3.14\text{x}10000\text{x}2 \text{ V/s} = 125.6 \text{ V/ms} = 0.1256 \text{ V/}\mu\text{s}.$$

Obviously, for 100 mV input, the required maximum rate of change of output is five times the above value, that is equal to 0.628 V/μs. This rate cannot be just guaranteed based on frequency response alone. The manufacturers test to see what is the maximum value of the rate of change of voltage variation which can be got at the output of an op amp, and this value is given as a separate specification called slew rate.

Slew rate is the maximum rate of change of output which an op amp can give at its output. [Caution: Do not leave out the word maximum; it is not just the rate of change of output voltage.]

Again, based on relation 7.16.2, we can give a relation between the maximum output (V_m) that can be obtained at the output of an op amp without distortion, the frequency(f) of the signal and the slew rate (SR) of the op amp as

$$SR = 2\pi f V_m$$

Know any two of the three parameters SR, f and V_m, you can estimate the third one.

Exercise: You want to design an amplifier using an op amp of known slew rate. Maximum output required is 4V peak. How can you find the maximum usable frequency?

It is a very important relation for design of op amp circuits. Note that slew rate does not take much importance while dealing with small amplitude signals; it is important for large amplitude signals. It is a large signal parameter.

Let us see a direct effect of slew rate:

Take the case of an amplifier made using 741. Its slew rate is given as 0.4 V/μs. Let us give a square pulse at the input, such that for the given gain of the amplifier, we expect amplitude of the pulse at the output to be 10 V. Assume that impact of frequency response is negligible. What do we get at at the output?

For the ideal pulse, rise time is zero; so also is the fall time. Out put can rise only by

0.4 V in every μs, because of the limited slew rate. So it needs 25 μs for the output to reach a level of 10 V. Similar is the case with fall of the output level from high to low level also. Impact on different pulse durations is illustrated in figure 15.

7.17. Rise time (t_r)

Rise time is another important ac parameter. In fact it describes the transient response of the op amp. It is applicable for any electronic device or network. Apply a step input to the device. You do not get the output as a step. Instead the output takes a finite time to rise to the expected maximum value. It has no relation with the amplitude of the signal. It is not related to the slew rate.

Rise time, in a general sense, is illustrated in figure 15. The output shown in the figure is on a noramlised scale, in the sense that maximum output is equated to unity. Rise time is the time taken by the output pulse to reach 90% of its full output from the time it has reached 10 % of its full output, for a step input. An op amp also behaves like a normal lag net work and introduces slight delay. Thus rise time is an important specification for op amps.

Typical value for 741 is 300 ns.

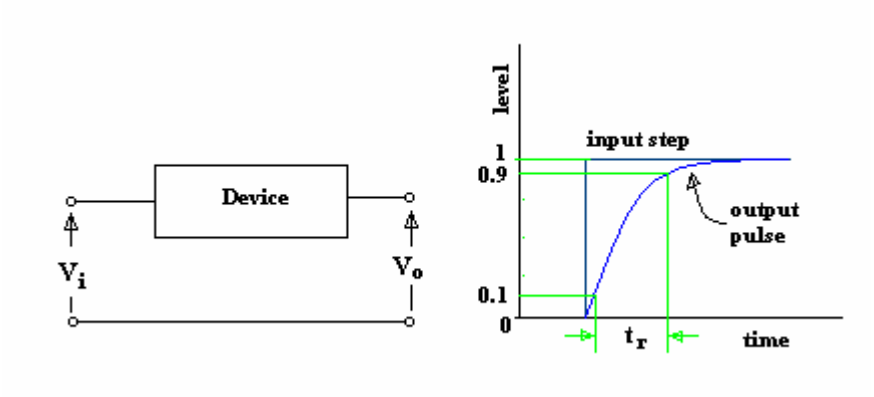

Figure 15: Rise time

Exercise: Model the op amp as a simple R-C network, with respect to rise time. Show that the rise time is independent of the signal level. Find an expression for the rise time in terms of R and C.

7.18. Overshoot

In section 7.17, we discussed the rise time. While illustrating the concept of rise time, we have shown the output curve to rise smoothly to the final level. Does it happen always like that? Just see the response illustrated in figure 16 a. Are you not familiar with such responses? It is typically the response of a two pole system. The simplest representation of a two pole system is an L-C-R circuit, shown in figure 16 b. An op amp is designed not to be a two pole system; it is expected to be a single pole device. But, it is not possible to completely avoid inductance equivalents. Every op amp has, to a small extent, two pole behaviour also; most often it could be neglected. Give an input pulse; output rises first to a level slightly above the final stable output. This is the overshoot. [We will see details on how the number of poles in an op amp response is reduced to one later.]

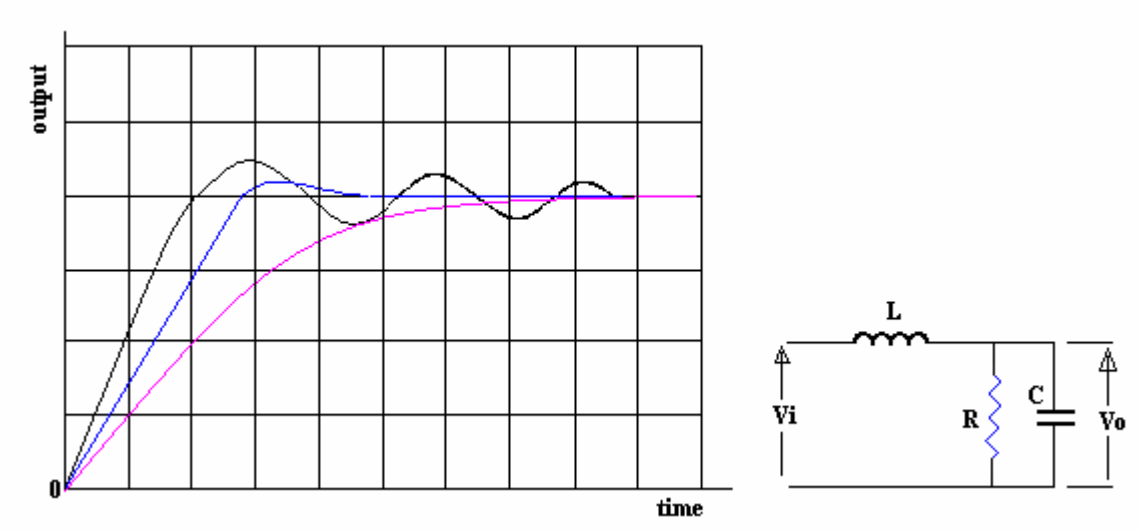

Figure 16a: Two pole responses

Figure 16b: Simple two-pole circuit

Op amp data sheets specify overshoot. Obviously, it is another ac parameter. It helps to assess how much the output can swing more than the expected steady state output. To understand the overshoot specification, you must understand clearly the technical definition of it.

Overshoot is defined as the ratio of the largest deviation of the output signal value from its steady state value after a step change in the input signal to the difference between the output signal values in the steady state before and after the step change in the input. This ratio multiplied by 100 gives the overshoot in percentage.

Let the output steady state without any input be V_1.

Let the output rise to a level V_{21} first, after being given a step input, and then let it get stabilized at V_{22} corresponding to the steady level of the step.

Then, overshoot = $\{(V_{21} - V_{22})/(V_{22} - V_1)\}$x100%

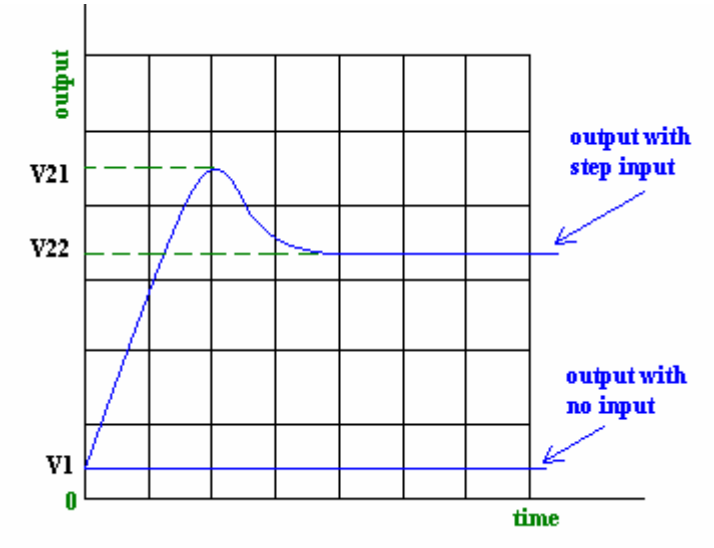

Figure 17: overshoot

Typical value for 741 is 5%.

7.19. Settling time

It is another very important ac parameter which describes the transient response. We can permit overshoot to a small extent. But it is important that the output settles down fast.

Settling time is the time necessary for the output to slew through a defined voltage change and settle down to within a defined error of the final output voltage.

When do we encounter errors due to poor settling time? Naturally, it is applicable for fast changing signals. It is one of the most important considerations for a high speed amplifier. Poor settling time spoils the advantages of having high slew rate and band width.

Which is the fastest change of voltage we can talk of? It is the step voltage. So settling time is defined with reference to the context of the response of the op amp to a step input. On application of the step input let the output overshoot a little, and then make a few oscillations about the steady state output, with fast reducing amplitude (ringing). We define settling time as the total time required for the output to come within a specified percentage deviation from the final steady value. How do you decide whether this level should be within 0.1%, 0.5%, 1%, 2% or 5% of the final steady value? The answer is obvious. It depends on the error we can permit. Figure 18 illustrates settling time for 2% error.

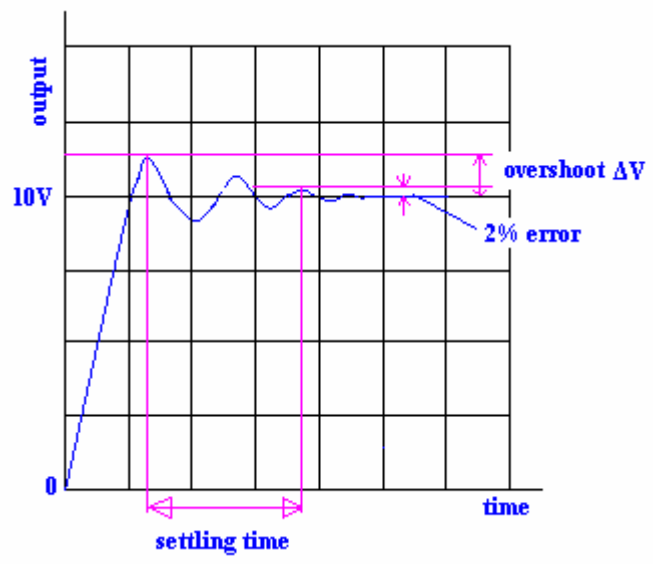

Figure 18: Settling time

Is the time required for the output to settle down to a given level independent of the output level itself, like the rise time? No. It depends on the level. Usually it is taken for 10V step.

Though we discuss settling time along with the performance parameters of the op amp, we must remember that it depends to a large extent on external circuit conditions, closed loop gain, etc.

Exercise: Discuss what happens if settling time is more. Take an example and try to discuss, with different inputs like triangle and pulse. Take settling time equal to 10%, and 20% of the input's period/pulse duration.

7.20. Absolute maximum ratings

There are a set of specifications termed absolute maximum ratings for any op amp. By no chance we are supposed to cross these limits. Absolute maximum ratings for μA741C and μA741 are given in the following table.

Table1: Absolute maximum ratings of 741

SYMBOL	PARAMETER	RATING	UNIT
VS	Supply voltage	μA741C ±18	V
		μA741 ±22	V
PD	Internal power dissipation	D package 780	mW
		N package 1170	mW
		F package 800	mW
VIN	Differential input voltage	±30	V

VIN	Input voltage[1]	±15	V
ISC	Output short-circuit duration	Continuous	
TA	Operating temperature range	µA741C 0 to +70	°C
		µA741 -55 to +125	°C
TSTG	Storage temperature range	-65 to +150	°C
TSOLD	Lead soldering temperature (10s max)	300	°C

NOTE:

1. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

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8. **Data sheet.**

[See Fiore to modify introduction to this section]

We have seen the important performance parameters of op amps. To get the values of any of these parameters for a given op amp, we have to see the data sheet provided by the manufacturers. It is very important that we understand how to interpret data sheets.

Data sheets give package details, pin details, general specifications, absolute maximum ratings, typical performance curves, etc. [See the data sheet of 741 given along with this note in the same folder.]

9. Ideal op amp.

An ideal op amp is a simple model of the op amp. It is characterized by 100% linearity, and has the following specifications/features:

Open loop gain: ∞

Input impedance: ∞

Input bias current: 0

Output impedance: 0

Bandwidth: ∞

Output will be zero with zero difference of potential across its input terminals.

Power supply sensitivity of performance: 0

Influence of environmental parameters on performance: 0

An ideal op amp is represented in figure 19.

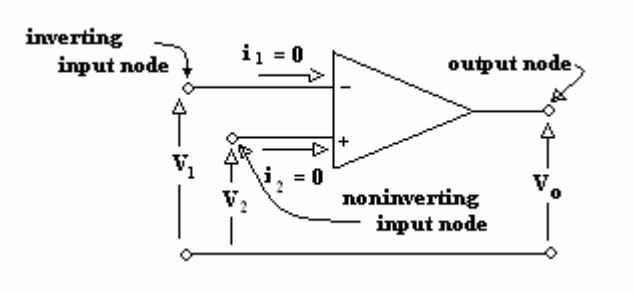
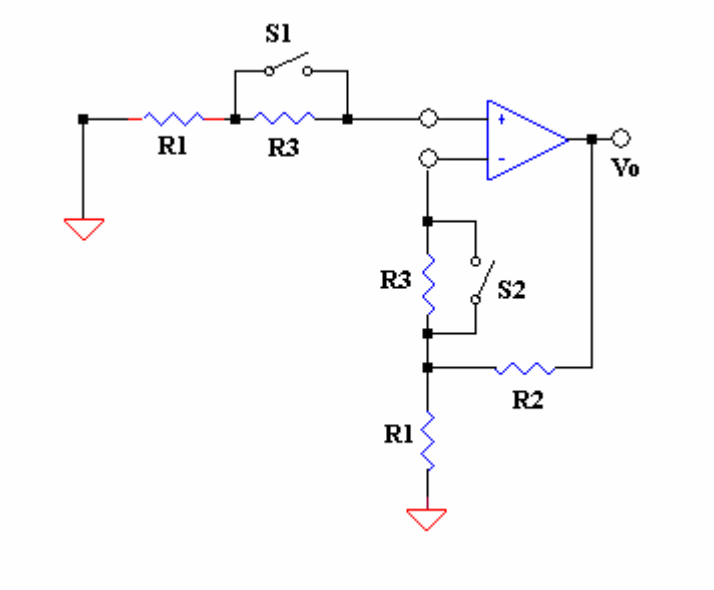


Figure 19: Ideal op amp

Experimental Determination of Op Amp Parameters

1. **Vos, I_B, Ios**

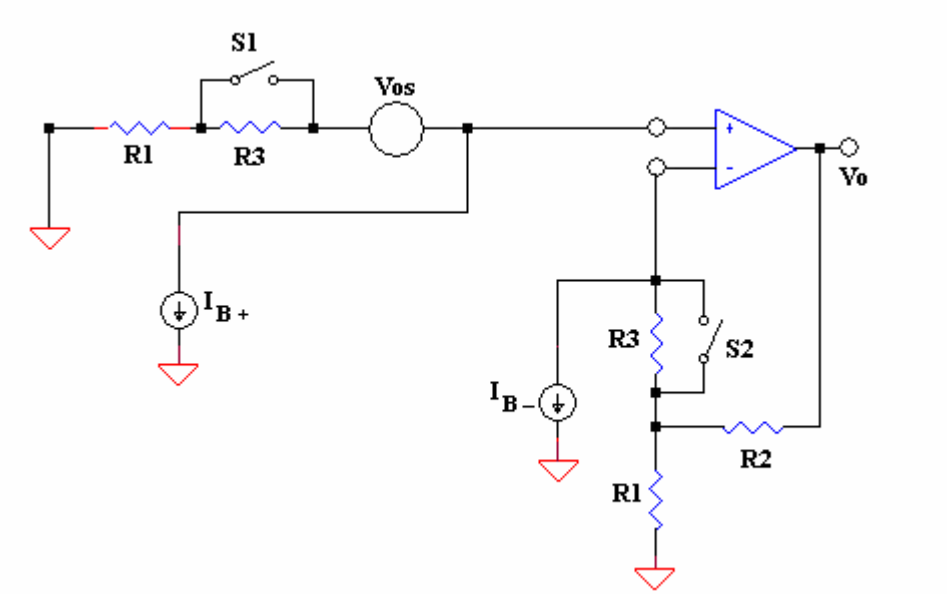
   Many circuits could be configured to find these offset parameters. These are basically dc error causing terms. A simple circuit is shown in figure .



We can consider 4 cases: (i) With both S1 and S2 kept closed; (ii) With S1 open and S2 closed; (iii) With S1 closed and S2 open; and (iv) With both S1 and S2 kept open. Let the outputs be V_{o1}, V_{o2}, V_{o3} and V_{o4} respectively. We can get expressions for these outputs as

follows. Figure shows a model of the circuit with the bias currents and offset voltages included. I_{B+} and I_{B-} are individual bias currents as already explained, and $I_B = (I_{B+} + I_{B-}$.

Let us consider the case where the offset voltages and currents contribute to the output, that is, when both switches S1 and S2 are kept open.



$$V_{o3} = [1 + R_2 / R_1]V_{os} - R_1 I_{B-}(R_2 / R_1)$$
$$V_o = [1 + R_2 / R_1]V_{os} + (R_1 + R_3)I_{B+}[1 + R_2 / R_1] - (R_1 + R_3)I_{B-}(R_2 / R_1) \quad \ldots \quad (A)$$

We will keep $R_1 << R_3$, which will serve two purposes. On the one hand it will help to make pd due to the bias current across R_1 to be negligible. Secondly, it will help to achieve high gain without going for very large values of R_2.

Now let us write expressions for outputs for the four cases.

(i) With both S1 and S2 kept closed:

Make $R_3 = 0$.

$$V_o = [1 + R_2 / R_1]V_{os} + R_1 I_{B+}[1 + R_2 / R_1] - R_1 I_{B-}(R_2 / R_1) \quad \ldots \quad (B)$$

Also let us see typical values of the offset voltage, and bias currents. For 741, the typical values are 0.8 mV and 30 nA. Also, the difference between the bias currents is typically 10% of the bias current itself.

Suppose we select R_1 not greater than 500 Ω. Also let us keep R_2/R_1 100 to 500. See the following comparison now.

30 nA x 500 Ω = 15 μV

So $V_{os} + I_{B+}R_1 = 0.8$ mV + 15 μV = 815 μV, typically.

Now take I_{B-} to be 10% different from I_{B+}. Calculate $I_{B-}R_1$. It will be typically 13.5 μV or 16.5 μV. With a gain of 200 to 500, you may now work out the error that could be present if we neglect the I_B terms. You will see that the error is very small. So we can modify relation (B) as

$$V_{o1} = [1 + R_2 / R_1]V_{os} \quad \ldots \text{ (C)}$$

Thus we can first determine V_{os}. It is better to repeat the experiment a few times for different values of R_1 and R_2 and find the mean value.

(ii) With S1 open and S2 kept closed:

Now, following the arguments presented earlier we can neglect the contribution of I_{B-}. Then we get

$$V_{o2} = [1 + R_2 / R_1]V_{os} + (R_1 + R_3)I_{B+}[1 + R_2 / R_1] \quad \ldots \quad \text{(D)}$$

V_{os} is already found out. So you can find I_{B+} from V_{o2} .

(iii) With S1 closed and S2 kept open:

Following the same reasoning as above, we get

$$V_{o3} = [1 + R_2 / R_1]V_{os} - R_1 I_{B-}(R_2 / R_1) \quad \ldots \quad \text{(E)}$$

(iv) With both S1 and S2 kept open:

This case could be used for finding the input offset current; but is not required, since the offset current can be calculated as the difference between the two bias currents.

Notes:

- Forget not to give the value of bias current as the mean value of the two input bias currents.
- Direction of bias current could be the opposite of what is shown in the figure. In such a case V_{o2} could be less than V_{o1}, and V_{o3} could be more than V_{o1}.

Some practical tips:

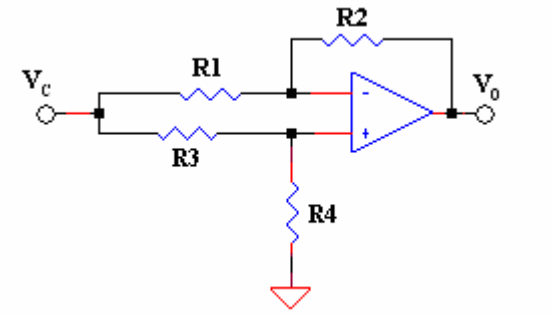
Select R3 about 100kΩ to 330 kΩ. For a bias current of about 30 nA you get a pd of 3mV to 10 mV. With a gain of 100, you can get outputs of 300 mV to 1 V.

Use R1 = 100Ω; R2 = 100kΩ , 220kΩ

R1 = 220Ω; R2 = 100kΩ , 220kΩ

2. Measurement of CMRR

Measurement of CMRR of an op amp is a tedious task. Any external circuit spoils the CMRR. A simple circuit used in labs to determine CMRR is given below.



It looks quite simple. We keep R3 = R1, and R4 = R2. Assume an ideal op amp; try to estimate the output. You get it as zero. But in practice you do not get the output to be zero. There are two reasons for it. First reason is that the CMRR of the op amp has a finite value; it is not infinite. If you assume that this is the only reason, you will expect an output given by

$$Vo = (1 + R2/R1)(Vc/CMRR) = (1 + R2/R1)V_{OSC}$$

The above expression tells you that the effect of finite value of CMRR is generation of an input offset voltage, $V_{OSC,}$ proportional to the input common mode voltage.

You may think that by giving a proper common mode voltage and measuring the output it must be possible to estimate CMRR. But, suppose you use a 741, and try to do the experiment. It has a typical CMRR specification of 90 dB. When you experimentally determine the CMRR using the above circuit, you may end up with a result of 50 dB to 60 dB only. This means that the output is not caused by the finite value of CMRR alone.

Second reason is that the mismatch of the external circuit components spoils the CMRR.You can only wish that the resistors R1 and R3, connecting the common mode signal to the two input terminals, are equal. You cannot make them equal. There will always be some finite difference. Similar is the case with the resistors R2 and R4.

This mismatch leads to the generation of a differential signal from the common mode signal, which we can see as an added input offset voltage.

Let us try to analyse a practical situation. Let us select resistors with a tolerance of x%. Let us check the following scenario:

R1 = (1+x) times the proposed value.

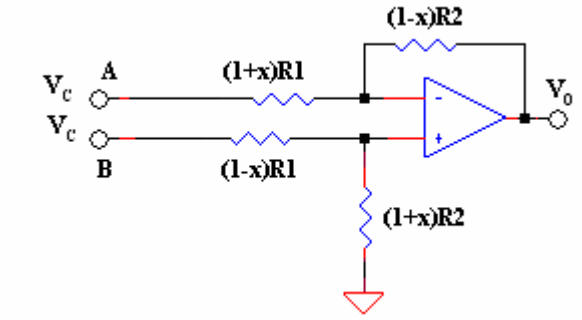
R2 = (1-x) times the proposed value.

R3 = (1-x) times the proposed value.
R4 = (1+x) times the proposed value.

Or, we will give the values as

R1 = (1+x)R1
R2 = (1-x)R2
R3 = (1-x)R1
R4 = (1+x)R2

So, the circuit can be given, for analysis purpose, as follows.



Common mode input is shown separately at the two input terminals (shown as A and B) to facilitate application of superposition. First connect point B to the common first. Find the output due to input at A:

$$V_{COA} = -[(1-x)/(1+x)]\{R_2/R_1\}V_C = -[(1-2x)R_2/R_1]Vc$$

where we have neglected higher degrees of x, considering that we will go for resistance tolerances better than or equal to 1%.

Now connect point A to common, and find the output due to input at B.

$$\frac{V_{CO}}{(1+R_2/R_1)} = 4x\frac{R_2}{R_1(1+R_2/R_1)}V_C$$

We can simplify the above relation and get

$$V_{COB} = (1+2x)\frac{R_2}{R_1}V_C$$

Now we can add the two outputs and get the common mode output as

$$V_{CO} = 4x\frac{R_2}{R_1}V_C$$

This is equivalent to having an input offset voltage of

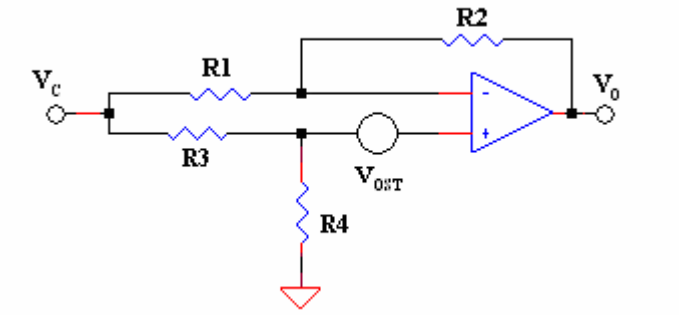
$$\frac{V_{CO}}{(1+R_2/R_1)} = 4x\frac{R_2}{R_1(1+R_2/R_1)}V_C$$

Now we have three input offset voltages:

(i) The input offset voltage of the op amp itself, V_{os}.
(ii) The equivalent input offset voltage of the common mode input voltage, V_{OSC} due to the finite value of CMRR.
(iii) The equivalent input offset voltage of the common mode input voltage, V_{OSCR} due to the mismatch of the resistors.

We can represent all the three input offset voltages together, as shown in the following figure, by V_{OST} given by

$$V_{OST} = V_{os} + V_{OSC} + V_{OSCR}$$



Of the three offset terms, V_{os} is a constant for a given op amp, and it is a dc level; by using ac of frequency of at least a few tens of hertz, you can eliminate it. V_{OSC} depends on the CMRR and the input common mode voltage only; V_{OSCR} depends on the mismatch of the resistor values. By accurately measuring the values of all the resistors, you can estimate V_{OSCR}. So if you can measure the output accurately for a given input common mode voltage, it must be possible to solve for V_{OSC}, and hence to find CMRR.

The above experiment demands very high accuracy for measurements. Let us see typical values and try to assess the accuracy requirement.

We have seen that, for 741, typical values of input offset voltage are 0.5 mV to 10 mV. Typical value for CMRR is 90 dB. For a common mode input of 10 V, we can calculate the equivalent input offset voltage, V_{OSC} to be -90 dB referred to 10 V, which is 10 V/31623, which is equal to 0.316 mV.

Let us assume that we will use high precision resistors with 0.1% tolerance. We will take a specific case and estimate the offset due to mismatch of resistors. We have seen a case with x% tolerance, where we got the input offset voltage as

$$\frac{V_{CO}}{(1+R_2/R_1)} = 4x\frac{R_2}{R_1(1+R_2/R_1)}V_C$$

With common mode voltage of 10 V, R2/R1 = 500, and x = 0.1%, we get VOSCR as 40 mV.

From these typical values we can make the following important inferences:

(i) Even 0.1% mismatch in the values of the resistors can lead to spoiling the CMRR by a factor of 40/0.316 = 126, which is equal to 40 dB; in other words, you may get a value of 50 dB in place of 90 dB.

(ii) To achieve an accuracy of at least 10% in the value of CMRR, you have to achieve an accuracy of [0.316/(10x40)]x100%, ie, 0.08%. This implies that, you must measure 20Vpp with an accuracy of 15 mV. You cannot achieve this directly using an oscilloscope. To improve the accuracy of measurement, you can make use of a subtractor stage to subtract off the common mode voltage from the output, so that you do the measurement at a much lower voltage.

The following scheme is suggested. You may analyse the circuit and see how CMRR can be calculated from Vo.