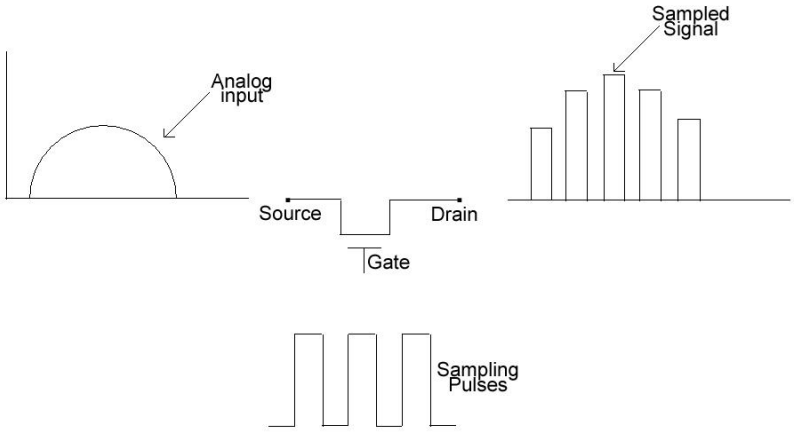
INTEGRATED CIRCUITS – MODULE III

Introduction

- Most of the signals in current use are generated in analogous form.
- For such signals, their amplitudes vary continuously with respect to time.
- Analog signals are easily affected by noise because noise is generated mainly in the form of amplitude variations.
- Hence if we want to restrict and reduce noise, amplitude has to be limited.
- But, when amplitude is limited, signal also will be clipped, and this will lead to distortion of signals.
- To limit noise and avoid distortions, the modern technique is to use digital signals.
- Digital signals are fixed width pulses, which occupy only one of two levels of amplitude 0 or 1, at any instant of time.
- Digital signals can be obtained from analog signals by what is known as analog to digital (A/D) conversion.
- To convert a given analog who corresponding digital signal, we first sample it.
- Sampling is done based on the Nyquist Sampling Theorem.

Nyquist Sampling Theorem

- Sampling theorem states that a signal can be recovered from its samples if sampling is done with a sampling frequency fs
  - such that $f_s > 2 f_m$
  - where f_m is the maximum frequency of the analog signal.
- For example, if f_m = 4 kHz, then f_s has to be greater than 8 kHz.
- Sampling can be done by applying the analog signal to the input of MOS switch, and applying sampling pulses to its gate.



- The sampled signal exists only in places where the sampling pulses exist.
- Thus, the 'continuous' analog signal becomes a discrete analog signal.
- These signal amplitudes can now be converted into digital signals by using an analog to digital converter (ADC).

Digital to Analog Converters (DACs)

Specifications

1. Accuracy

- Accuracy is defined the nearness of a measured value to the true value.
- For example, if the value of voltage level is 12V, and its value measured using an instrument is 11.9V, we say that there is an error of 0.1 V is the measurement.
- This error is usually expressed as a percentage with reference to the full – scale reading of the instrument.

If in the above case, the full scale reading is 15V, we have

$$\text{Accuracy} = \frac{0.1}{15} \times 100 = 0.67\%$$

- In the case of a DAC, accuracy depends on the number of bits of the converter and will be limited to half the value of the least – significant bit.

For example, consider the case of a 12 bit digital to analog converter.

$$\text{The L. S. B of this DAC can read} = \frac{1}{2^{12}} = 0.244 \times 10^{-3}$$

Now for this 12-bit DAC,
Accuracy = ½ x 100/4096 = 0.0122%

- An accuracy of ± 1% means that 100 volts could be in the range 99-101 volts.

2. Resolution

- Is defined as the smallest quantity that an instrument can measure without ambiguity.
- Percentage resolution is calculated as =1/(Total no: of steps) * 100
- For as n- bit digital input, the total number of steps $2^n - 1$
- Then % resolution $= \frac{1}{2^n - 1} * 100$
- This means that it is only be number of bits which determines the percentage resolution
- For example, the LSB of a 10-bit converter has a weight of 1/1024
  - Thus the smallest increment change in the output of this converter is 1/1024 of the full scale voltage.
  - If this converter has a +10V full scale voltage, the resolution is approximately 10 x 1/1024 ≈10mV.
  - This converter is then capable of representing voltages to within 10mV.

- Voltage resolution =Full Scale Voltage / ($2^n - 1$) where n is the number of bits.

3. Offset voltage

- Ideally the output DAC will be zero volts when the binary inputs are all 0s.
- But in practice, there will be a very small output voltage called the offset voltage or offset error.

4. Settling time

- The time required for the output of the DAC to settle to within ± (1/2) LSB of the final value for a given digital input is known as settling time.
- In all practical cases, the DAC will take a finite time to settle to its final value.
- The DAC will settle only after the output load parasitic capacitance has been fully charged.

5. Linearity

- A DAC is said to be linear if, for equal increments in the binary digits, the DAC produces equal amounts of output voltages.

Variable – Resistor Networks

- The basic problem in converting a digital signal into an equivalent analog signal is to change the 'n' digital voltage levels into one equivalent analog voltage.
- This can be most easily accomplished by designing a resistive network that will change each digital level into an equivalent binary weighted voltage.

Binary Equivalent Weight

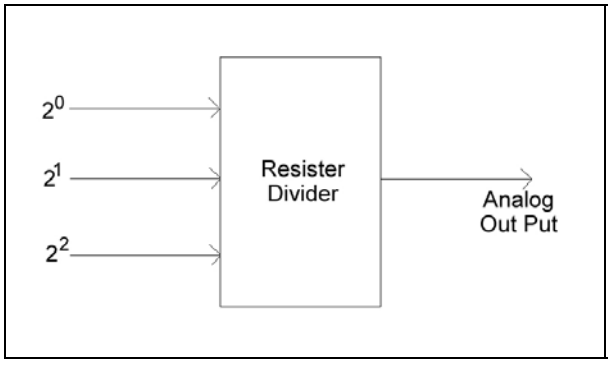
Consider the truth table a 3-bit binary signal shown below:

Bit	Weight	Bit	Weight
2^0	1/7	2^0	1/15
2^1	2/7	2^1	2/15
2^2	4/7	2^2	4/15
Sum =	7/7	2^3	8/15
		Sum =	15/15

- Our task is to change the eight possible digital signals into equivalent analog voltages.
- Smallest number = 000 = 0V
- Largest number = 111 = 7V
- Between 000 and 111, there are seven discrete levels to be defined.
- Therefore, it will be convenient to divide the analog signal into seven levels.
- The smallest incremental change in the digital signals is represented by the least significant bit (LSB) 2^0
- Thus, a change in this bit will cause a change in the analog output that is equal to one-seventh of the full scale analog output voltage.
- Like wise a 1 in the 2^1 bit position must case a change in the analog output voltage that is twice the size of the LSB.
- The resistive divider will then be designed such that a '1' in the 2^0 position will cause 7x 1/7 = +1V the output.
- A '1' in the '2^1' bit position will cause a change of 7x 2/7 = 2V in the analog output voltage.
- The process can be continued, and it will be seen that each successive bit must have a value twice that of the preceding bit.
- In general, the binary equivalent weight assigned to the LSB is $\frac{1}{2^n - 1}$ where n is the number of bits.
    - i.e. LSB weight = $\frac{1}{2^n - 1}$

1. Binary Weighted Resistive Divider Digital to Analog Converter

- We need to design a resistance divider that has three digital inputs and one analog output as shown below:



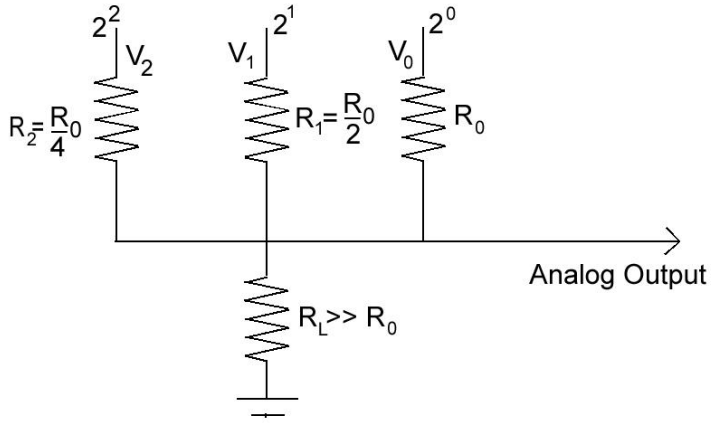
Digital Input	Analog Output
000	0 V
001	1 V
010	2 V
011	3 V
100	4 V
101	5 V
110	6 V
111	7 V

- From the table, it is evident that for an input of 001, the output will be +1 Volts.
- For 011, the output has to be +3 V.
- But 011= 001+010
- If the +1V from the 2^0 bit is added to the +2V from the 2^1 bit, the desired +3V out put for 011 input is achieved.
- The other voltage levels are additive combination of voltages.

Thus the resistive divider must do two things in order to change the digital input to an equivalent analog out put voltage.

1. The 2^0 bit must be changed to +1V and 2^1 bit must be changed to +2 V and 2^2 bit must be charged to +4V.
2. These three voltages representing the digital bits must be summed together to form the analog output voltage.

A resistive divider that performs these functions is shown below:



- Resistors R0, R1, and R2 from the divider network.
- Resistances, R^1 represents the load to which the divider is connected.

- The analog output voltage

$$V_A = \frac{\frac{V_0}{R_0} + \frac{V_1}{R_1} + \frac{V_2}{R_2}}{\frac{1}{R_0} + \frac{1}{R_1} + \frac{1}{R_2}}$$

$$V_A = \frac{\frac{V_0}{R_0} + \frac{V_1}{\frac{R_0}{2}} + \frac{V_2}{\frac{R_0}{4}}}{\frac{1}{R_0} + \frac{1}{\frac{R_0}{2}} + \frac{1}{\frac{R_0}{4}}}$$

- If digital input = 001 i.e. $V_0 = 7V$, $V_1 = 0$, $V_2 = 0$

$$V_A = \frac{7}{7} = +1V$$

To summarize, a resistive divider can be built to change a digital voltage into an equivalent analog voltage. The following criteria can be applied to this divider:

1. There must be one input resistor for each digital bit.
2. Beginning with the LSB, each following resistor value is one – half the size of the previous resistor.
3. The full scale out put voltage is equal to the positive voltage of the digital input signal.
4. The LSB has a weight of $1/ (2^n-1)$ where is the number of input bits.
5. The change in output voltage due to a change in the LSB is equal to $V/(2^n-1)$, where V is the digital input voltage level.
6. The output voltage V_A can be found for any digital input signal by using the following:

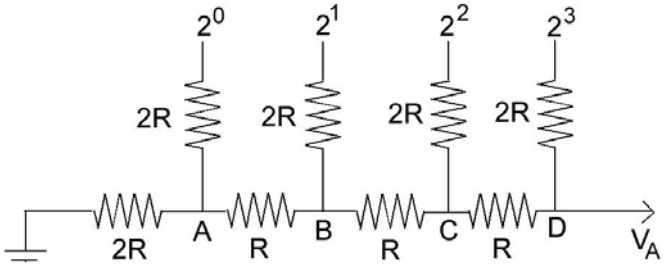
$$V_A = \frac{V_0 2^0 + V_1 2^1 + V_2 2^2 + V_3 2^3 + ...V_{n-1} 2^{n-1}}{2^n - 1}$$

Drawbacks

1. Since each resistor (these are precision resistors), in the network has a different value, there is an added expense.
2. The resistor used for the MSB is required to handle a much greater current than that used for the LSB resistor.

2. Binary R- 2R Ladder type DAC

- The binary ladder is a resistive network whose output voltage is a properly weighted combination (sum) of the digital inputs.
- A ladder designed for 4 bits is shown below:



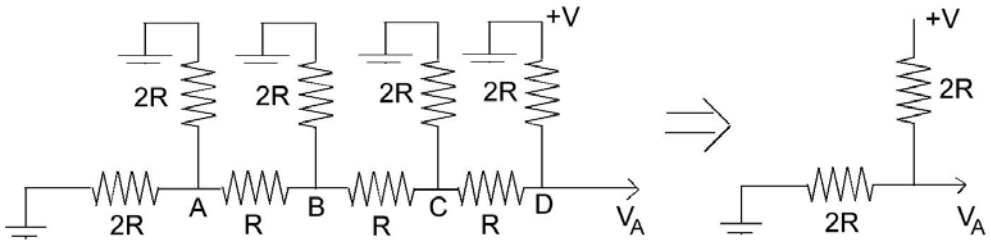
- It is constructed of resistors that have only two values and thus overcomes one of the drawbacks of the resistive divider.
- The left and the ladder in the terminated in a resistance of 2R.

Resistive properties of the Network

- Let us assume initially that all the digital inputs are at ground.
- At node A, the total resistances looking out towards the terminating resistor is 2R.
- The total resistances looking out towards the 2^0 input is also 2 R.
- These two resistors can be combined to form access equivalent resister of value R.
- At other nodes also, the total resistances looking towards terminating resistor and in the opposite direction is 2R.
- This is true regardless of whether the digital inputs are at sound or +V (Since the internal impendence of an ideal voltage source is 0 ohm)

Working

- Assume that the digital input signal is 1000 (i.e. the MSB is 1).
- The binary ladder is redrawn as shown below:



- Since there are no voltage sources to the left of node D, the entire network to the left of this node can be replaced by a resistance of 2R to form an equivalent circuit shown above.
- From this circuit, $V_A = V * \frac{2R}{2R+2R} = \frac{+V}{2}$
- Like wise, the second MSB provides $= \frac{+V}{4}$
- Like wise, the third MSB provides $= \frac{+V}{8}$
- Like wise, the fourth MSB provides $= \frac{+V}{16}$
- Since this ladder is composed of linear resistors it is a linear network and the principle of superposition can be used.

$$V_A = \frac{V}{2} + \frac{V}{4} + \frac{V}{8} + ... \frac{V}{2^n}$$

n - total number of bits at the input

or in another form $V_A = \frac{V_0 2^0 + V_1 2^1 + V_2 2^2 + V_3 2^3 + ...V_{n-1} 2^{n-1}}{2^n}$

where V_0, V_1, V_2….are the digital input voltage levels

Analog to Digital Converters (ADC's)

- ADCs are used for the conversion of analog signals into digital signals.
- All digital instruments and systems must have ADCs as part of their structure, if their inputs one of analog nature.

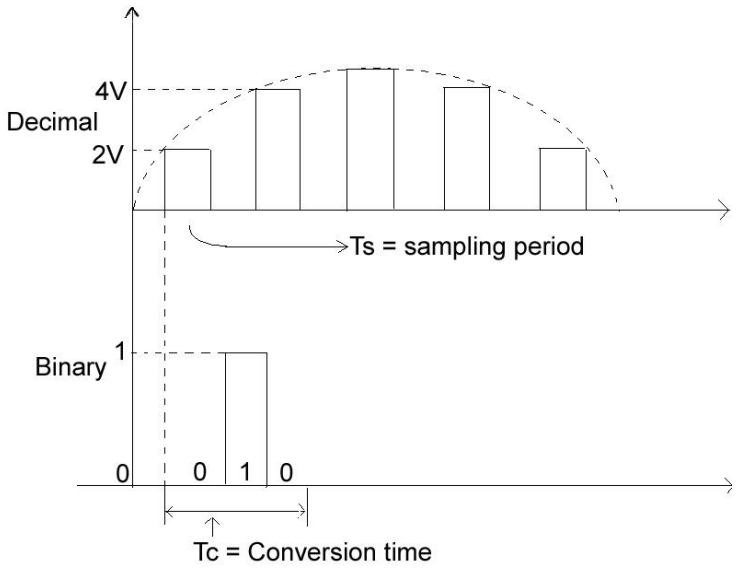
Specifications of A/D Converter

Sampling and Holding

- An ADC requires finite time for analog to digital conversion.
- The amplitude of the analog input must be kept constant during this period.
- For this, we Sample and then Hold the analog signal by using sample and hold (S/H) circuits.

Conversion time

- The time taken by an ADC for converting one sample level of analog signal, expressed in decimal value into corresponding binary equivalent value.
- For example, consider the figure below, which shows an analog sample and the binary equivalent value:



- From the figure, we notice that the first analog sample has an amplitude of 2 volts, expressed in decimal form.
- The binary equivalent of 2 is 010.
- The time equivalent taken for converting decimal 2 into binary 010 is the conversions time.
- Also the sampling period $T_S > T_C$ for smooth conversion.

Resolution

- It is the smallest voltage that can be measured with an ADC.

$$\text{Voltage resolution} = \frac{V_{FullScale}}{2^n - 1}$$

where n is the no. of bits

- If n = 8bits and $V_{Full\ Scale}$=15V,

$$\text{Voltage resolution} = \frac{15}{2^8 - 1} * 100$$

$$\text{Percentage resolution} = 1/2^n \text{x} 100$$

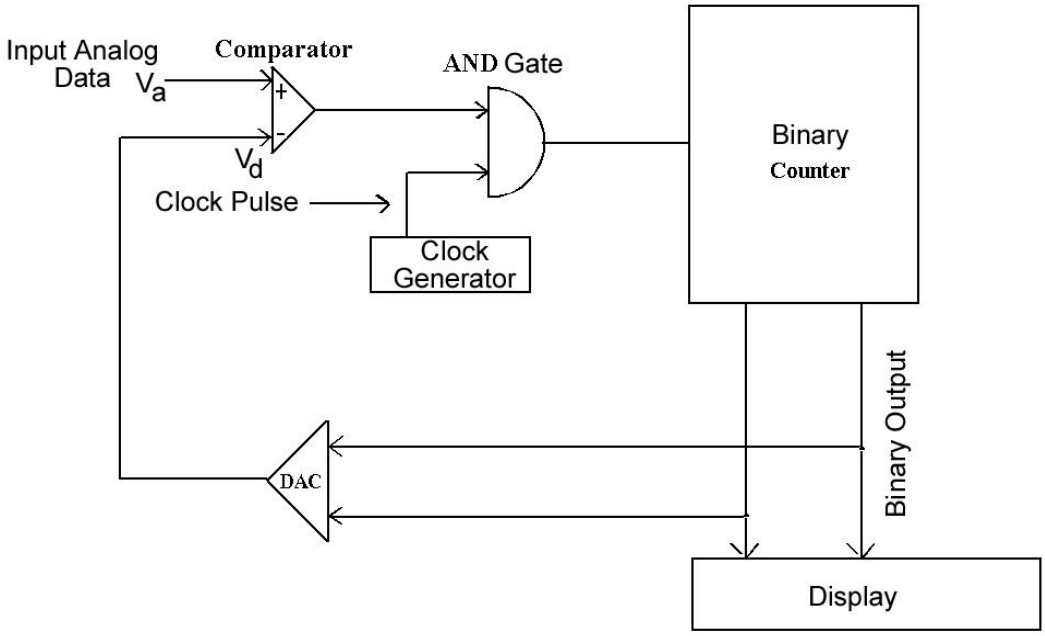
- Percent resolution of an 8 bit ADC= $1/2^8$x100 = 0.3902

Differential Linearity

- Defined as a measure of the variation is voltage step size that causes the converter to change from one state to another.
- It is normally expressed as a percentage of average step size.

1. Counter Ramp Type A/D converter

- As shown in the figure below, the ADC consists of a comparator, an AND gate, a counter and associated display, and a DAC.

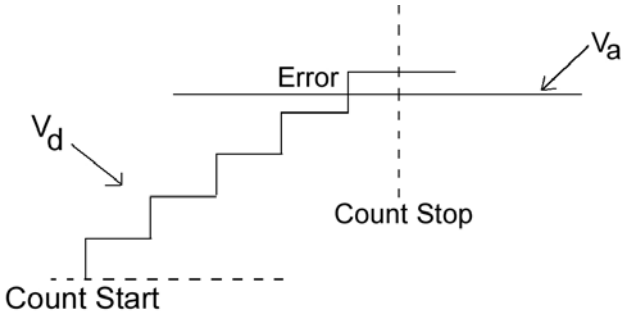


- Initially, Va will always be greater than Vd so that the comparator always outputs a +1.
- This enables the counter to register the number of pulses it counts on in its 7 segment display.
- This binary out put is fed to a DAC that converts these digital bits into corresponding analog data Vd for comparison with the input Va.

Example- Analog input of 3V to corresponding binary data

- When this voltage Va is applied to the comparator, since V_d=0 initially, the comparator outputs a +1, which enables the AND gate.
- A single pulse sets transmitted from the clock generator to the counter, which now reads 0001.
- This is then converted by the DAC to an analog equivalent voltage V_d=1V
- Since Va> Vd at this instant, the and gate is still enabled and one more clock pulse goes to the counter, which now reads 0010.
- This is converted back to Va=2V by the DAC and since Va>Vd, the clock sends one more pulse to the counter
- The counter now records 0011.
- The DAC converts this back to a value of 3V.
- Now Va=Vd and here the comparator outputs a zero to disable the counter and the AND gate.
- The display now reads 3V.

The waveform below shows that Vd is a *staircase waveform*.



- When Vd>Va, the counter stops.

Advantages

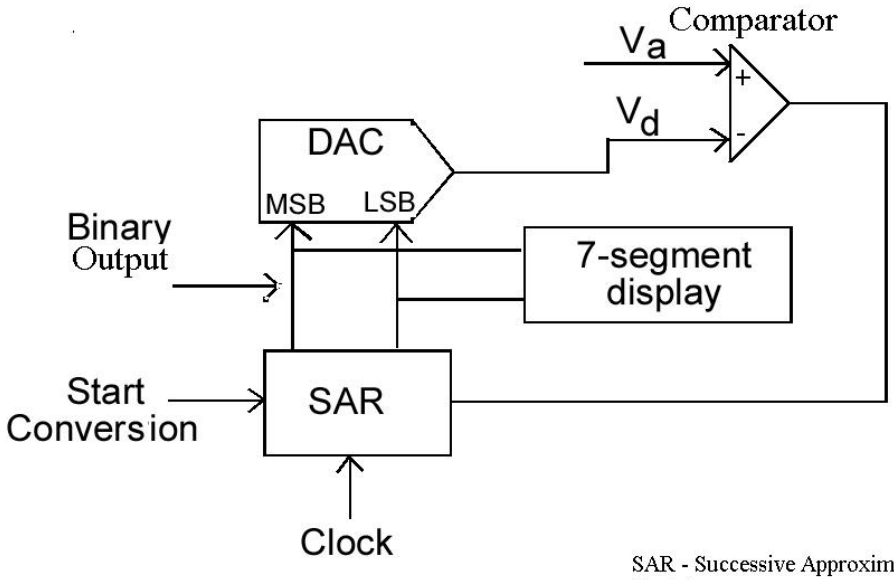
1. The principle is simple and straight forward.
2. It is very easy to construct.

Disadvantages

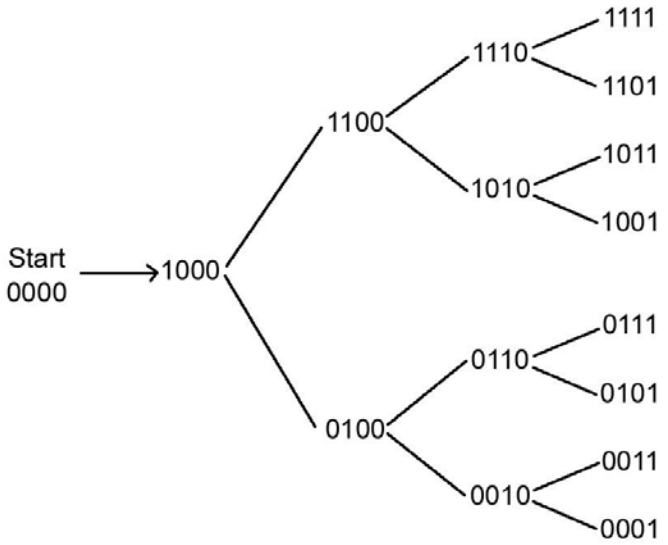
1. Only increasing voltages can be measured.
2. The system is very slow.
3. Practically, the system comes to rest only when Vd>Va.

2. Successive – Approximation A/D Converter

The block schematic of the SA-ADC is shown below:



SAR - Successive Approximation Register



- The analog voltage to be converted is applied to the comparator.
- The fed back voltage Vd is compared with the analog voltage Va and the output is applied to the SAR.
- The voltage Vd is initially reset to all zeros.
- The comparator then searches for whether the input voltage Va is more (or less) than Vd.
    - If Va>Vd, the SAR registers a 1 as its MSB.
    - If Va<Vd than the MSB registered is a 0.
- The SAR than puts a 1 in the next lower – significant bit position automatically by itself, and the DAC converts this to an analog equivalent voltage Vd corresponding to the new value of the binary in the counter.
- If Va is still greater, a 1 is registered at the next lower significant bit; otherwise a 0 is registered.
- This process is continued till the input is fully converted to binary.

Example

- Assume, full scale voltage = 15 V
- Let a voltage of 10V be applied to the input of the comparator (Va)
- Initially, MSB = 1, all the lower significant bits being 0's.
- Assuming, a 4 bit counter, the reading of the SAR would them, be 1000.
- This corresponds to the decimal 8. i.e. Vd = 8 V
- Since Va (10V) > Vd (8V), the MSB retains its 1, and the next significant bit is made 1 by the SAR.
- Now SAR, reading = 1100, which corresponds to Vd = 12 V
- Since Va (10V) < Vd (12V), the second significant bit is made o by the SAR, instead of 1.
- The binary counter now becomes 1000 again.
- But the SAR on the third clock pulse register a 1 for the third bit and the display reads 1010, which corresponds to Va = 10V.
- Now, since Va = Vd, the conversion stops.

- Conversion time of SA - ADC = N x 1/f
  where N – number of bits, f – clock frequency

Advantages

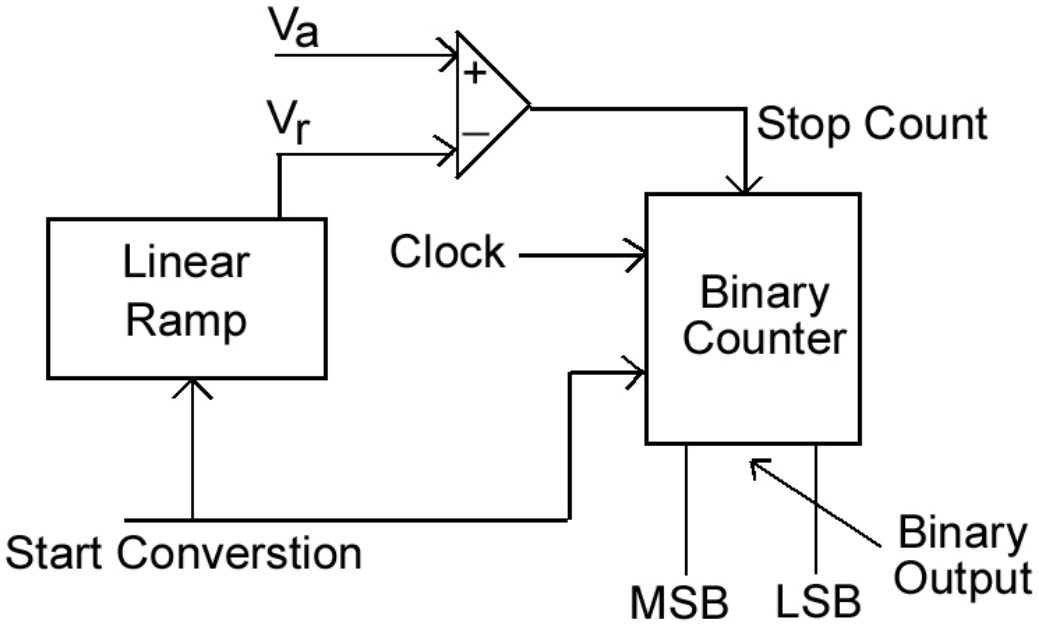
1. More accurate than the staircase ADC.
2. Higher resolution.
3. Much faster.
4. Conversion time is much less.

Disadvantages

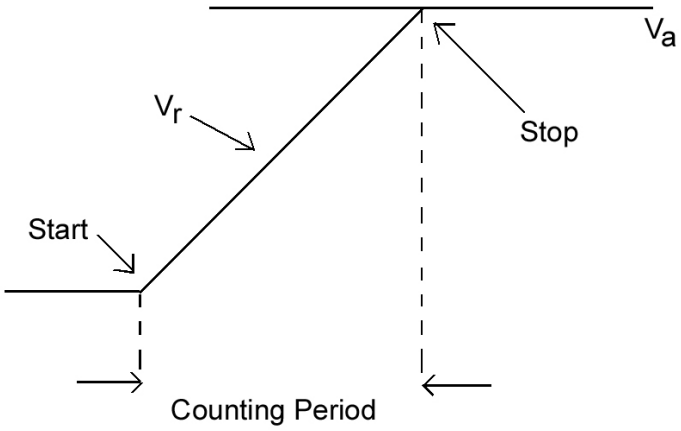
1. Requires a complex register called the SAR.
2. Costly, as it contains more components.

3. Linear Ramp A/D converter (Single – Slope Type)

- If a very short conversion time is not a requirement, there are other methods of A/D conversion that are simpler to implement and much more economical.
- Basically, these techniques involve comparison of the unknown input voltage with reference voltage that begins at zero and increases linearly with time.
- The time required for the reference voltage to increase to the value of the unknown voltage is directly proportional to the magnitude of the unknown voltage, and this time period is measured with a digital counter.



- The ramp generator is a circuit that produces an output voltage ramp.
- It is important that this voltage be straight line that is, it must have a constant slope.
- We assume that the clock is running continuously and that the input voltage that we wish to digitize is positive.
- Since Va is positive, and the ramp Vr begins at zero, the output of the comparator when Vs>Vr is used to stop the count of the digital binary counter.
- The counter begins counting upward and the ramp continues upward until the ramp voltage is greater than the input voltage Va.
- At this point, the output of the comparator goes low, thus disabling the counter.



Advantages

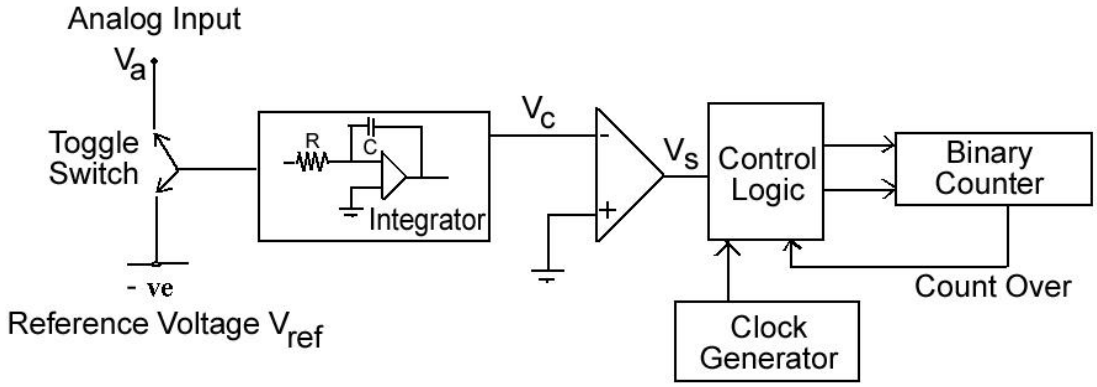
1. Very simple circuitry.
2. Quite fast, no need for D to A conversion.
3. Lower cost.

Disadvantages

1. Dependent on extremely accurate ramp voltage. This in turn is strongly dependent on the value of R and C and variations of these values with time and temperature.
2. Poor conversion accuracy.
3. Poor resolution.

4. Dual slope A/D converter

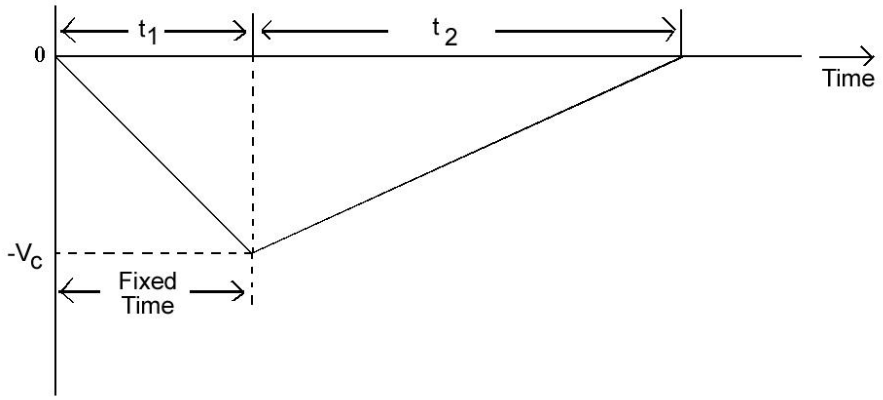
The logic diagram for a basic dual-slope A/D converter is given below:



- We begin with the assumption that the clock is running, and the input voltage Va is positive.
- Since Va is positive, the integrator output will be a negative ramp (i.e. Vc).
- The comparator output Vg is thus positive and the counter is counting (running).
- We allow the ramp to proceed for fixed time period t1.
- The actual voltage Vc at the end of the fixed time period t1 will depend on the unknown analog input Va.

$$Vc = - (Va / Rc) \times t1$$

- Since the integrator capacitor will charge to a voltage level depending on the value of the input analog voltage.



- When the counter reaches the fixed count at time t1 the control logic switches the integrator input to the negative reference voltage $V_{ref.}$

- The integrator will now begin to generate a ramp beginning at – Vc and increasing steadily upward till it reaches 0V.
- All this time, the counter is counting, and the conversion cycle ends when V_C=0V since the comparator output Vg becomes negative.
- The equation for the positive ramp is $Vc = (Vref / RC) \times t_2$
- In this case, the slope of the ramp is constant but the time period t2 is variable.

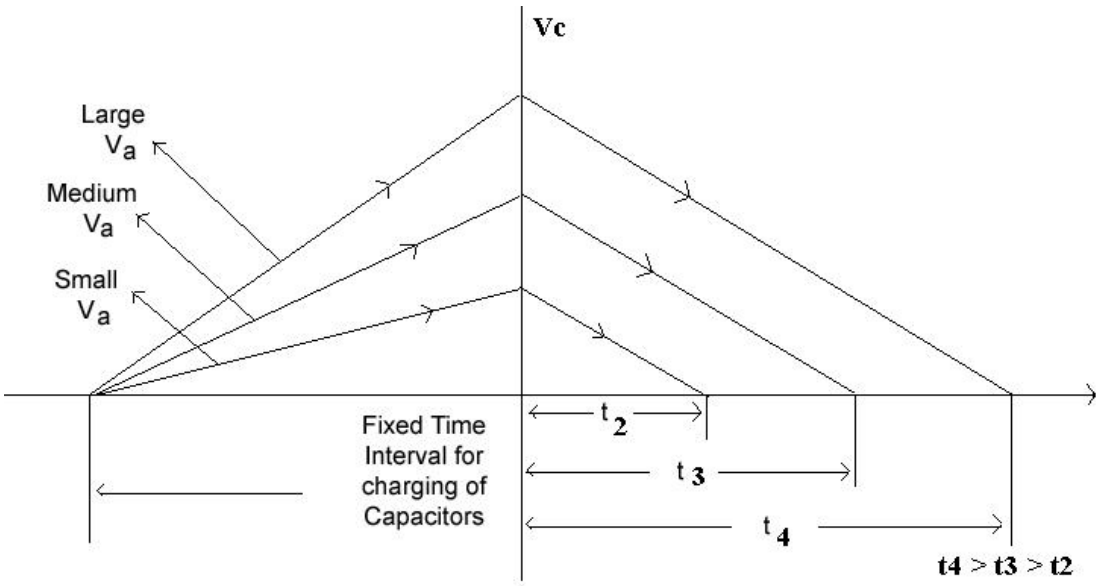
i.e. $\frac{V_a}{RC} * t_1 = \frac{V_{ref}}{RC} * t_2$

The value RC will cancel from both sides, leaving

$$V_a = V_{ref} * \frac{t_2}{t_1}$$

Vref – is a known reference voltage
t1 – is a predetermined time.

- Clearly the unknown analog input voltage is directly proportional to the variable time period t_2.
- This time period is exactly the contents of the counter at the end of a conversion cycle.



Charge Discharge Intervals of Integrator

- Depending on the level to which the capacitor had been initially charged, the discharge time varies and hence the binary counters counting time varies.
- This then reads the input voltage in terms of the count duration.
- The larger the duration, the more the count.

Advantages

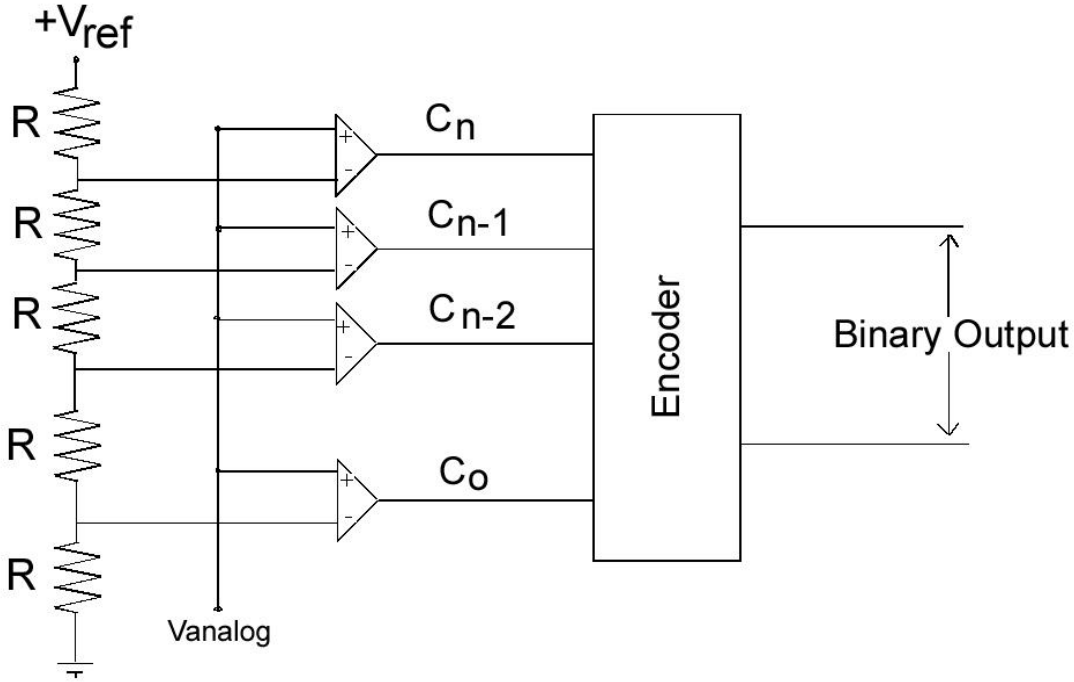
1. This technique is free from the absolute value of either R or C since the RC terms cancel from both sides of the equation.
2. Increased accuracy
3. Low conversion time

Disadvantages

1. Complicated circuitry
2. Higher cost

5. The Parallel (Flash) A/D Converter

- The flash converter is the fastest ADC.
- It works on direct conversion of analog data into digital data, and it does not make use of a DAC.



- The flash converter consists of several comparators driving an encoder circuit.
- The voltage Vref is divided equally among the resistors, and the voltage drop at the top of each resistor is used to drive the – (negative) input terminal of the corresponding comparator.
- The analog input voltage Va is applied to the + (positive) terminal of all the comparators.
- The comparator outputs a 1 when its positive terminal gets a higher voltage than its negative terminal.

For example, when Vref = 20 V

- If there are 20 resisters and 20 comparators, the voltage at the input of the first comparator Co = 20/20 = 1V
- Voltage at the second comparator = 2 V and so on.

If Va = 6 V

- Then up to comparator C5, we find that a 1 is output to the encoder.
- The seventh comparator C6 and above it will remain idle.
- The encoder logic immediately converts (in a flash) into corresponding binary data.

Advantages

1. Fast conversion (governed only by propagation delay of the gates)
2. High accuracy.
3. High resolution possible by increasing the number of comparators.

Disadvantages

1. Complicated circuitry
2. Cost is proportional to the number of comparators, which in turn depends on the resolution required.