INTEGRATED CIRCUITS – MODULE I

LOGIC FAMILIES

Introduction

- Logic circuits make use of logic gates such as NAND and NOR for performing logic operations governed by Boolean Algebra.
- Logic gates are manufactured in a variety of configuration, structures and technologies.
- All of these gates are now available as integrated circuits.

Depending on the number of devices integrated on a substrate, we have the following classification for digital logic gates:

1. Small scale integration (SSI) - this consists of a maximum of 100 discrete devices, or 12 logic gates on a single substrate.
2. Medium scale integration (MSI) - in each MSI IC, we have 100 to 1000 components or 12 to 100 gates on a chip.
3. Large scale integration (LSI) - these chips contain 1000 to 10,000 components or 100 to 10000 gates on a single chip. Example: ROM, RAM.
4. Very large scale integration (VLSI) - These chips contain 10,000 to 1, 00,000 or 1000 to 10,000 gates per IC chip. Example 8085, 80356 (Micro processor chips)

For manufacturing digital IC's, there exist several technologies and structures. Depending these structures and technologies, we have three major logic families currently in existence. They are

1. Transistor – transistor logic (TTL) family
2. Complementary metal oxide semiconductor (CMOS) logic families
3. Emitter coupled logic (ECL) family

Use

1. TTL: in digital circuit belonging to the SSI, MSI and LSI categories.
2. CMOS: used in all modern low-power digital circuits and high density computer chips.
3. ECL: in super high speed computers.

Some families have become obsolete. They are

a. Diode-logic (DL)
b. Resistor – transistor logic (RTL)
c. Diodes – transistor logic (DTL)
d. Integrated – injection logic (I^2L)
e. N-type MOS logic (NMOS)

Gates

- Logic systems consist of logic elements called gates and flip-flops.
- Gates are electronic circuits whose terminal characteristics correspond to the various Boolean operations.
- Flip-Flops are memory devices that are capable of storing the logic constants.
- The interconnection of gates and flip-flops result in logic networks.

Gate properties

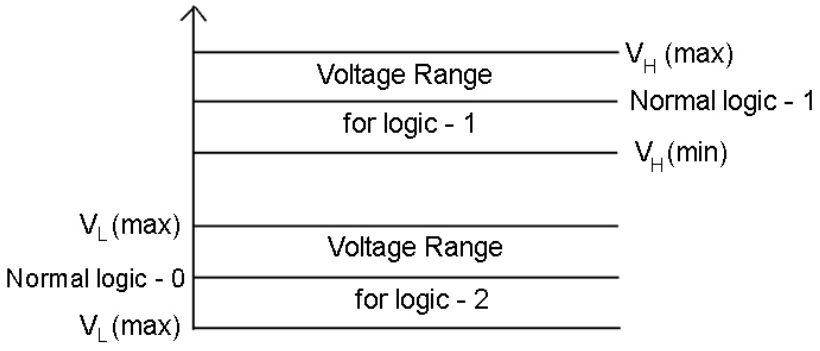
There are several properties associated with logic gates that determine the environment in which a digital system can operate as well as introduce constraints on its topological structure.
These include

- Noise margins
- Fan-out
- Propagation delays
- Power dissipation

Voltage ranges (for Positive Logic)

- The two signal values associated with logic –0 and logic -1 are not really single values but, rather, ranges of values.
- If a signal value is in some low level voltage range between $V_{L(\min)}$ and $V_{L(\max)}$ then it is assigned to logic -0.
- Similarly when a signal value is in some high-level voltage range between $V_{H(\min)}$ and $V_{H(\max)}$ it is assigned to logic-1.

This is illustrated below.

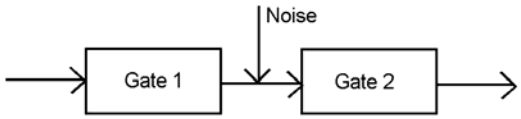


- As long as the signal values stay within their assigned ranges, except during transit between ranges, the logic gates behave as intended.
- It is because a pre specified range of signal values, is regarded as the same logic value, that digital systems are highly reliable under such conditions as induced noise, temperature variations, component fabrication variations and power supply variations.

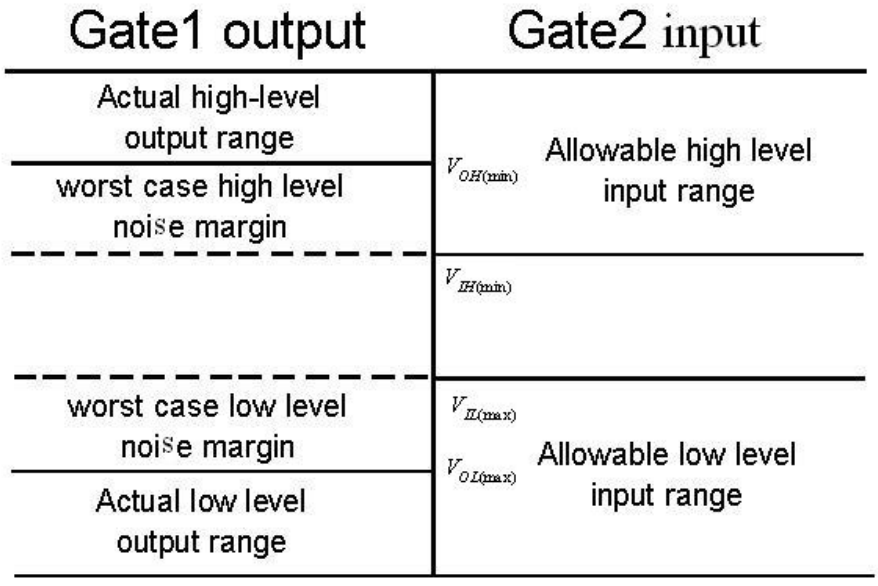
Noise Margins

- For performance purposes, gate circuits are designed so that $V_{H(\min)}$ is different at the input and output terminals of a gate.
- That is the minimal signal value that is acceptable as logic -1 at the input of gate is different from the minimal logic -1 signal value that a gate produces at its output.
- A similar situation also occurs for $V_{L(\max)}$.
- Thus, manufacturers normally state a $V_{IL(\max)}$, $V_{IH(\min)}$, $V_{OL(\max)}$ and $V_{OH(\min)}$ in the gate specifications.
- That is the manufacturer guarantees that any input voltage less than $V_{IL(\max)}$ is recognized by the gate as corresponding to a low range (logic 0) voltage input.
- On the other hand, any input voltage greater than $V_{IH(\min)}$ is recognized by the gate as corresponding to a high range (logic 1) voltage input.
- Further more, the manufacturer guarantees that the low range output voltage of the gate does not exceed $V_{0L(\max)}$ and that the high range (logic-1) voltage output of the gate does exceed $V_{0H(\min)}$.

Consider the effect of connecting the output of a gate to another gate as shown below.



Noise is induced between the gates



- Any additive noise induced between the gates less than $V_{1L(\max)} - V_{0L(\max)}$ does not affect the logic behavior of the two gates in cascade.
- This is called the worst-case low level noise margin.
- In a similar manner, any subtractive noise induced between the gates less than $V_{0H(\min)} - V_{1H(\min)}$ does not affect the logic behavior of the two gates in cascade.
- This is called the worst case high level noise margin.
- Noise margins are a measure of digital circuit's immunity to the presence of induced electrical noise.

Actual low level noise margin

$NM_L = V_{1L(\max)} - V_{0L1}$

V_{0L1} – actual low level output voltage of gate 1 and $V_{0L1} \leq V_{0L(\max)}$

Actual high level noise margin

$NM_H = V_{0H1} - V_{1H(\min)}$

V_{0H1} – actual high level output voltage of gate 1 and $V_{0H1} \geq V_{0H(\min)}$

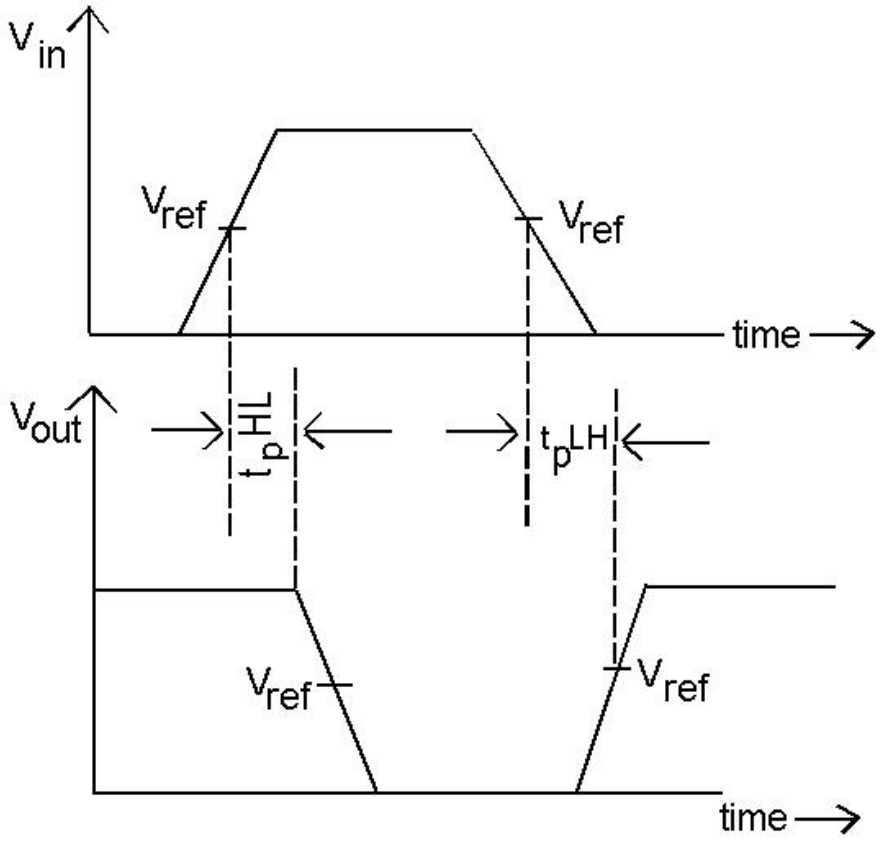
Fan Out

- When loads are connected to the output of a digital circuit, the output signal levels are affected.
- This is a consequence of the fact that there is a current flow between gates and hence a power consumption.
- For reliable operation the amount of this current is limited.
- The number of circuits (measured in terms of similar gates in the same logic series) connected to the output of a digital gate as loads is called the fan-out of the gate.
- The maximum number of such loads that can exist without impairing the normal operation of a gate is referred to as the gates fan-out capability.

Propagation Delays (Speed of operation)

- Digital signals do not change nor do circuits respond instantaneously..
- For this reason, there is a limitation to the overall speed of operation associated with a gate.
- Signals do not go between their logic –0 and logic -1 values in zero time.
- In addition, the effect of a change at the input terminal does not appear immediately as a change at the output terminal.
- Rather, owing to the physical behavior of the electronic components in the gate, there is a time delay before the output changes.

The waveforms at the input and output terminals of a NOT gate are shown below.



- Using a specified reference point, say 50 percent point, on the rise and fall of the signals, V_{ref} , two delays are indicated in the waveforms above.
- These are referred to as propagation delays.

t_pHL – Time required for the output signal to change from its High level to Low level as a consequence of an input signal change.
t_pLH - time required for the output signal to change from its Low level to High level as a consequence of and input signal change.

- These two delay times are in general, not equal.

As a general measure of the response speed of a gate, one frequently uses an average propagation delay time t_{pd} , which is defined as

$$t_{pd} = \frac{t_pHL + t_pLH}{2}$$

Power dissipation

- In the course of operation, a digital circuit consumes power as a result of the flow of current.

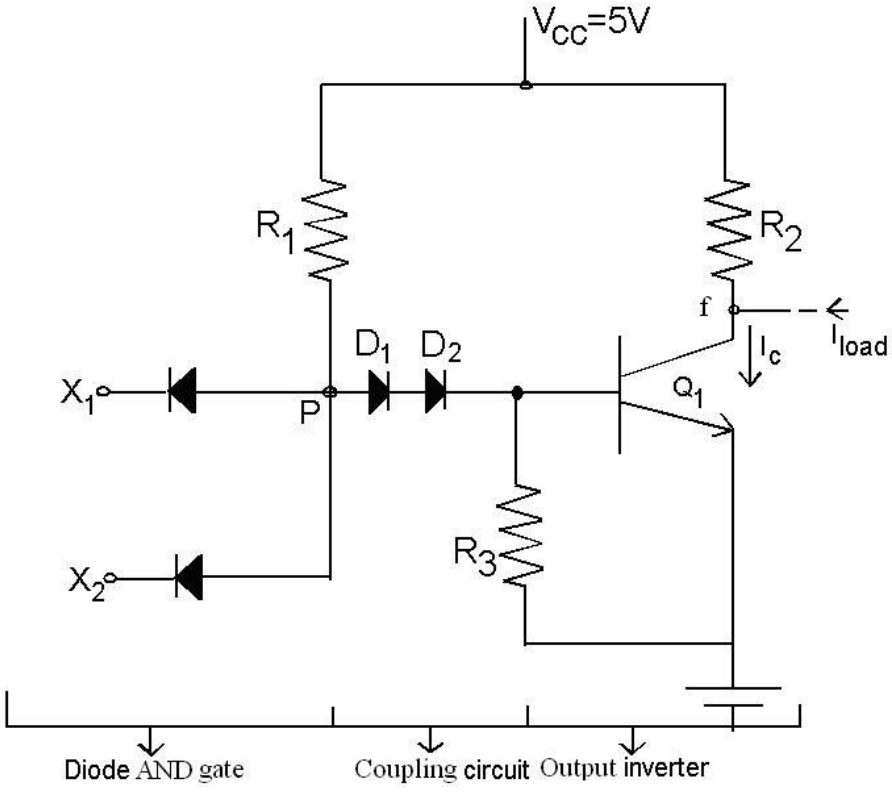
There are two components to this power dissipation

1. Static power dissipation – occurs as a consequence of the flow of currents while the circuit is in its steady state.
2. Dynamic power dissipation – occurs as the result current flow due to changes of the input signals to the circuit.

- In both cases, the necessary currents must be provided by the power supply of the digital system.
- It is desirable in a digital system to have gates with low power dissipation and high speed of operation (ie low propagation delay times)
- Unfortunately, the faster a circuit operates, the greater it power requirements.
- For this reason, a figure of merit of a circuit is its delay-power product, which is the product of the propagation delay time and the power dissipation of the gate.

Diode – Transistor Logic (DTL)

- Diode – Transistor logic (DTL) was the forerunner to the popular transistor – transistor logic (TTL).
- Although DTL is no longer in use, an understanding of DTL aids in the understanding of TTL.



V_{x1}	V_{x2}	V_f
L	L	H
L	H	H
H	L	H
H	H	L

L = 0.2 V
H = 5 V

A two input DTL NAND Gate

The basic DTL rand gate consists of 3 sections

- An input diode AND gate
- A coupling circuit
- An output inverter

- To understand the general operations of the gate, first assure that at least one input x_1, or x_2 is low (at 0.2 V) and any inputs that are high are at 5 V.
- Also assume that no loads are connected to the output of the DTL gate.
- Each low input diode is forward biased due to the power supply Vcc.
- Therefore, the voltage at point P is Vin + V_D (On) = 0.2 + 0.7 = 0.9 V
- Current flows from Vcc, through R, and through each forward biased input diode.
- Since the voltage at point P is only 0.9 V, it is not enough to forward bias D1 and D2.
- A voltage of at least 1.4 V is required to turn on D1 and D2.
- No current flows through D1 and D2 and correspondingly no current flows into the base of Q1.
- The net result is that transistor Q1 is in cutoff, no current flows through R2 and the voltage at point 'f' is Vcc = 5 V.
- This situation corresponds to the first three rows of the voltage table.

Now consider the case when both the input voltages are high at 5 V.

- The two input diodes are reverse biased and off.
- When the voltage at point P gets to 1.4 V, diodes D1 and D2 start to conduct current through R3 to ground.
- When the voltage at P is sufficiently high to overcome the base-emitter junction voltage of transistor Q1, the base current flows and the transistor starts to conduct.
- The circuit is designed so that the transistor Q1 operates in saturation.
- Voltage at point P = $V_{DI(on)}$ + $V_{D2(on)}$ + $V_{BE(sat)}$ = 0.7 + 0.7 + 0.7 = 2.1 V
- Although some current flows through R3, most of the current flows into the base of transistor Q1 to guarantee saturation.
- With transistor Q1 saturated, the voltage at the output the gate, ie point 'f' $V_{CE(sat)}$ = 0.2 V.
- This corresponds to the last line in the voltage table.
- Resistor R3 is used to improve the speed of performance of the gate.
- When transistor Q1 is in saturation, it is necessary to remove the minority charge carriers from the base region of the transistor before it can go into cutoff.
- As a result of removing these charge carriers, current flows away from the base terminal.
- Resistor R3 provides a path to ground for this current.
- If resistor R3 were not present, then it would be necessary to remove the charge carriers by a flow of current though diodes D1 and D2 in the reverse direction.
- Since current does not flow readily in that direction, the switching time of transistor Q1 would be relatively high.
- Thus the smaller the value of R3, the faster the output transistor can switch.
- There is a limit, however, to how small the value of R3 can be made.
- When transistor Q1 is in saturation, current is diverted from base to resistor R3.
- But the fan-out capability of the gate is dependent on the base current.
- Hence by decreasing R3, the fan out capabilities of the gate is also decreased.

Loading effects

- For DTL gates, the fan-out of a fact is limited by the amount of current the output transistor stage is capable of sinking, since it must accept current from the input diodes of the load gates.
- Assume that the DTL gate has N identical DTL gates connected to it output as loads.
- First consider the case when the output of the driving point f , is high at 5 V
- This occurs when the transistor Q1 is in cutoff.
- Therefore, the input diodes of the loads connected to point 'f' are reverse biased and have the currents I1 …….I_N are zero and no current flows between the driving and load gates.
- Thus there is no significant loading effect upon the driving gate.

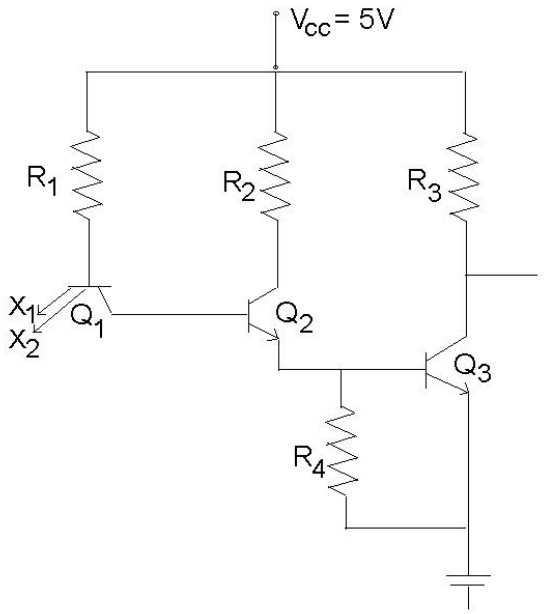
Now consider the situation when the output of the driving gate, point f, is low.

- In this case the transistor Q1, for proper operation is in saturation and the voltage at point f is $V_{CE(sat)}$ = 0.2V.
- The load diodes connected to point 'f' are forward based and a net current of

$I_{load} = I_1 + \ldots\ldots\ldots I_N$ flows from the load network toward the driving gate.

- This current along with the current component I_{R2}, flows into the collector of transistor Q1.
- Transistor Q1 stages in saturation as long as $\beta_F I_B > I_c$ where $I_c = I_{R_2} + I_{load}$
- Thus for a given β_F and I_B there is a limit in the number of permissible loads that allows transistor Q1 to remain in saturation.

Transistor - Transistor Logic (TTL)



Basic two input TTL NAND Gate

- The TTL NAND-gate is a modification of the DTL NAND gate.
- The first difference is the use of a multi-emitter npn transistor as the input stage in place of the diode AND gate.
- The multi-emitter junction can be regarded as a collection of pn junction diodes whose anodes are connected together.
- From a steady state point of view, this configuration with resistor R1 essentially forms a diode AND gate.
- The two coupling diodes D1 and D2 of DTL NAND gate are replaced by the Base Collector junction of transistor Q1 and the Base emitter junction of transistor Q2.
- The final stage, consisting of a transistor inverter is same for both.

First assume that both inputs are high at 5V.

- This causes the base emitter junction to be reverse biased. (for Q1)
- Like wise, the Base – Collector of Q1 and Base emitter of Q2 and Q3 forward biased.
- The circuit is designed so that transistors Q2 and Q3 saturate.
- This causes the out put of the gate to become VCE3 (sat) =0.2V which corresponds to the low level logic value.

  Voltage at base $Q_3 = V_{BE3(sat)}$ =0.7V

  Voltage at base $Q_2 = V_{BE3(sat)} + V_{BE2(sat)}$ =0.7+0.7=1.4V

  Voltage at base $Q_1 = V_{BE3(sat)} + V_{BE2(sat)} + V_{BC1(ON)}$ =0.7+0.7+0.5=1.9V
- As a consequence of the Base emitter junction of Q1 being reverse biased and its base collector function being forward biased the transistor Q1 is operating in its inverted active mode.

Next consider the situation when at least one input is low at 0.2V.

- The corresponding base emitter junction of transistor Q1 is forward biased.
- Voltage at base of Q1= V_{in}+ $V_{BE(sat)}$ =0.2+0.7 =0.9V
- This voltage is insufficient to support the base collector junction drop of Q1+ base emitter junction drops of Q2 +Q3.
- Therefore Q2 and Q3 are in cut off and the out put voltage is 5V.
- The transistor Q1 is in saturation.

<u>Why TTL is faster than DTL?</u>

- When both inputs are high, transistor Q1 is not saturated. (inverted active mode)
- Therefore it is capable of switching quite rapidly.
- The transistors Q2 and Q3 cannot come out of saturation until the stored charges are removed from their bases.
- Then when at least one input goes low to 0.2V the base of transistor Q1 quickly goes to 0.9V while the collector remains at 1.4V.
- Therefore, at the time of switching, the base collector junction of Q1 is reverse biased and the base emitter junction is forward biased.

- This causes the transistor Q1 to enter its normal active mode, which permits a large collector current to flow.
- This collector current corresponds to the removal of the stored charges of transistor Q2 and Q3.
- It is not until these stored charges are removed that transistor Q1 enters saturation.
- The net effect is the quick removal of the stored charges and correspondingly, rapid switching of transistors Q2 and Q3 from saturation to cutoff.
- Propagation delay times are one tenth of that in DTL.

TTL Gates

Advantages

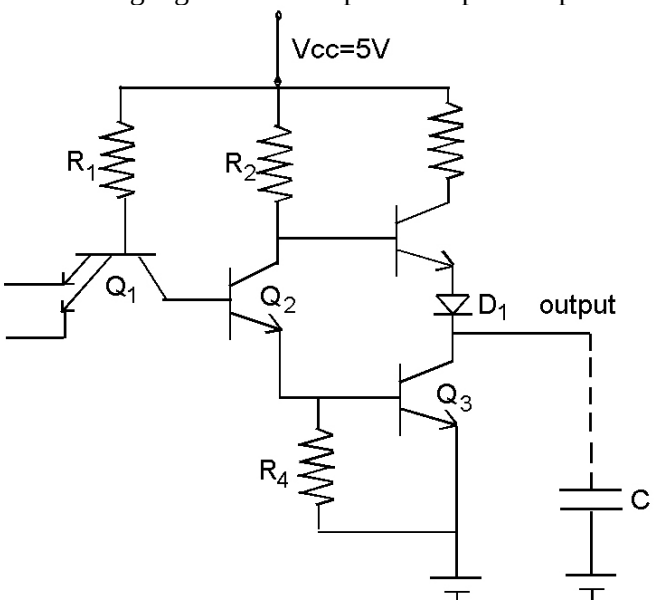
1. It is the fastest saturating logic family. The propagation delay time of a standard TTL gate is approximately 10 ns.
2. It has good noise immunity. Typical noise margin is about 0.4V
3. Compatible with other logic families.
4. Good fan out, can drive up to10 gates.
5. Almost all functions are available in TTL family of gates.
6. Low out put impedance for high/ low states.

Disadvantages

1. VLSI circuits are not possible because of isolation problems.
2. Power dissipations is much higher than MOS gates.
3. Cost is higher than NMOS/CMOS, when MSI and LSI gates are considered.
4. It generates transient voltages at switching instants.

TTL with Totem – Pole Output

The speed of operation of a logic gate is also dependent upon the parasitic output capacitance.



A two input TTL NAND gate with Totem pole output

- This capacitance appears as the dotted capacitor C in the figure above and is associated with the wiring capacitance, input diode capacitance of the load gate and the collector emitter capacitance of transistor Q3.
- The rate at which this parasitic capacitor is charged and discharged affects the switching time of the driving gate.
- The discharging of capacitor C occurs when the output of the gates goes from its high value to its low value. i.e. Q3 goes cutoff to saturation.
- The discharge path is through Q3 with a time constant $R_{Q3\ (on)}$ C, where $R_{Q3(on)}$ is the small conducting resistance of transistor Q3.
- On the other hand, the capacitor C must be charged when the output of the gate goes from its low value to high value.
- In this case, the charging path is through resistor R3 and time constant is R3C.
- By reducing the value of R3, output low to high switching time of the gate is decreased.
- However, a low value of R3 increases the power consumption of the circuit when the output is low. $\frac{\left[V_{CC} - V_{CE3(sat)}\right]^2}{R_3}$
- It is desirable to have R3 as small as possible while the output is switching from its low to high value in order to have a small RC time constant.
- And have R3 as large as possible when the gate is in its steady state with a low output in order to have low power dissipation.
- One way this is achieved is by the use of an active pull-up circuit known as a totem pole output.

The output is high when Q4 is ON.

- The collective resistance of resistor R3, the saturation collector emitter resistance of transistor Q4 and the ON resistance of diode D1 along with the parasitic capacitance determine the charging rate of the parasitic capacitance.
- This time constant is low.
- The output quickly changes from its low value to its high value.

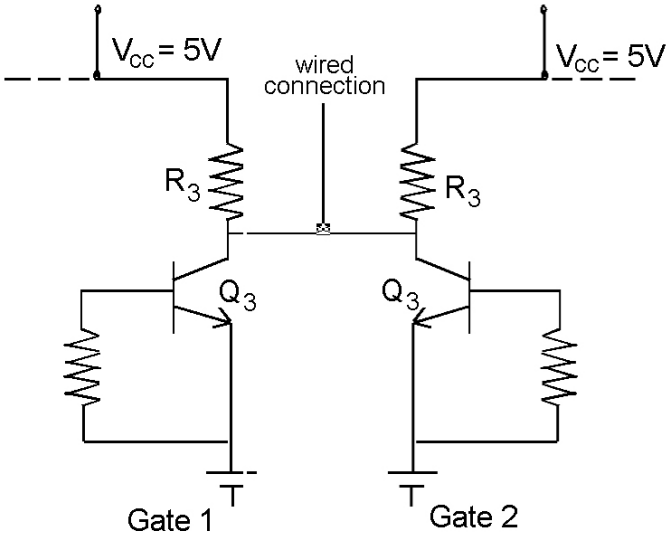
The output is low when Q3 is ON – Q4 and Diode D1 are OFF.

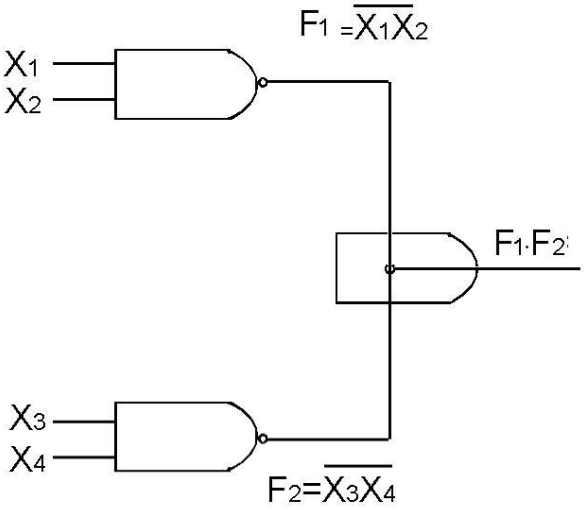
- With transistor Q4 in cutoff, no current flows through the low valued resistor R3.
- As a result, the objective of having no power dissipation in this section of the circuit has how been achieved when the output of the gate is low.

The circuit is designed in such a way that both Q3 and Q4 can never be on at the same time. When Q3 or Q4 conducts, the output impedance is low.

Wired Logic

- With some logic gate it is possible to connect their outputs together so as to achieve logic behavior at the connection.
- This is known as wired logic.
- Consider two TTL NAND-gates. If the outputs are connected together as shown below, then the wired output appears at the collectors of the parallel connection of the two output transistors.



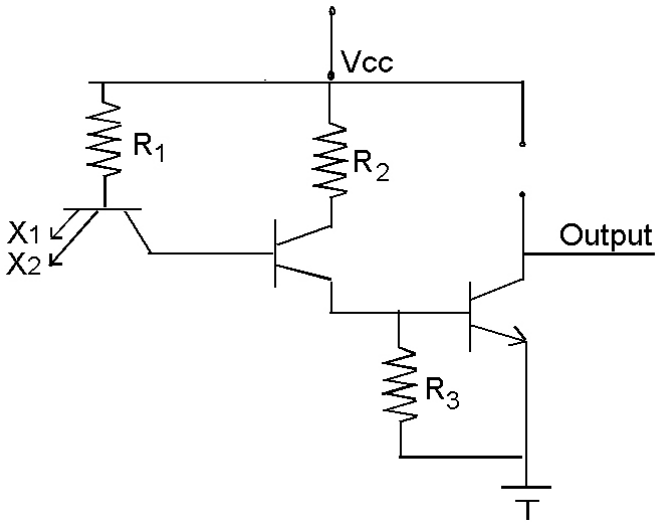


$$f_1 . f_2 = \overline{(x_1 x_2)} . \overline{(x_3 x_4)} = \overline{x_1 x_2 + x_3 x_4}$$

- The wired output is high if both output transistors are in cutoff.
- If at least one output transistor is in saturation, then the wired output is at relatively low voltage (VCE3(sat) = 0.2V)
- Thus the voltage at the wired connection is high if and only if the outputs of both of the individual gate are high.
- Therefore, an AND operation is achieved at the wired connection.

Open - Collector output

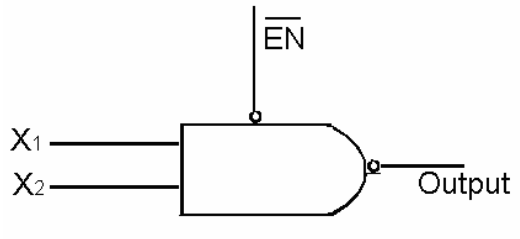
- The resistors R3 from the two gates in the above figure are placed in parallel when the gate outputs are connected.
- This results in an effective resistance of R3/2 and therefore increases the power dissipation of the gate whose output transistor Q3 is in saturation.
- For this reason, TTL gates without resistor R3 are available commercially specifically for applications in which the wired AND capability is desirable.
- This is known as Open-Collector TTL.



- Of course, after the outputs of open-collector TTL gate are connected together in a network, a single collector resistor, referred to as a passive pull-up resistor must be added externally.

Tri-state output

- Wired logic is not permissible with the TTL NAND gate having the totem pole output.
- How ever for a special situation in which several TTL gate outputs one tied together to a common bus, there is a special form of TTL gate that is used, which retains the advantages of the totem pole output.
- This is shown below the (the logic symbol) and is called TTL with three-state output.



Logic symbol for TTL NAND gate with three state output

Truth Table

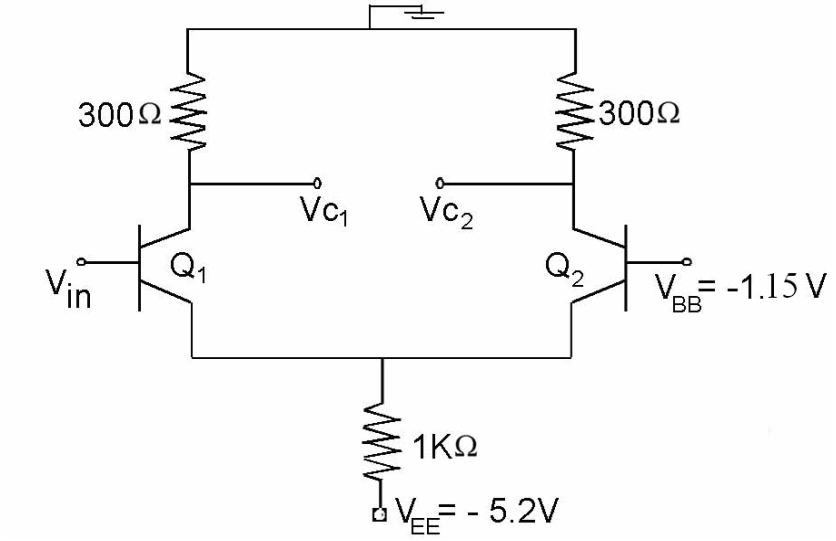
X1	X2	En'	Output1
0	0	0	1
0	1	0	1
1	0	0	1
1	1	0	0
X	X	1	Open-circuit

- When the control input EN'is at logic 1, both the output transistors Q3 and Q4 of the totem pole are forced into cutoff, with the net effect that the output of the gate appears as an open circuit or equivalently, high impedance.
- This high impedance condition is regarded as the third state of this TTL gate.
- When the control input is at logic 0, the output is at logic 0, if the inputs x1 and x_2 are both at logic – 1.
- Transistor Q3 is in saturation and transistor Q4 is cutoff.
- Also when the control input is at logic-0, the output is at logic-1 if at least one input x1 or x_2 is at logic 0.
- Here transistor Q3 is in cutoff and Q4 is in saturation.
- The outputs of several three state TTL gate can be wired together if at most only one of the control inputs is allowed to be at logic – 0 at any time.
- In such a case, the corresponding gate controls the logic output of the wired connection, while all the remaining gates are in their high impedance state.

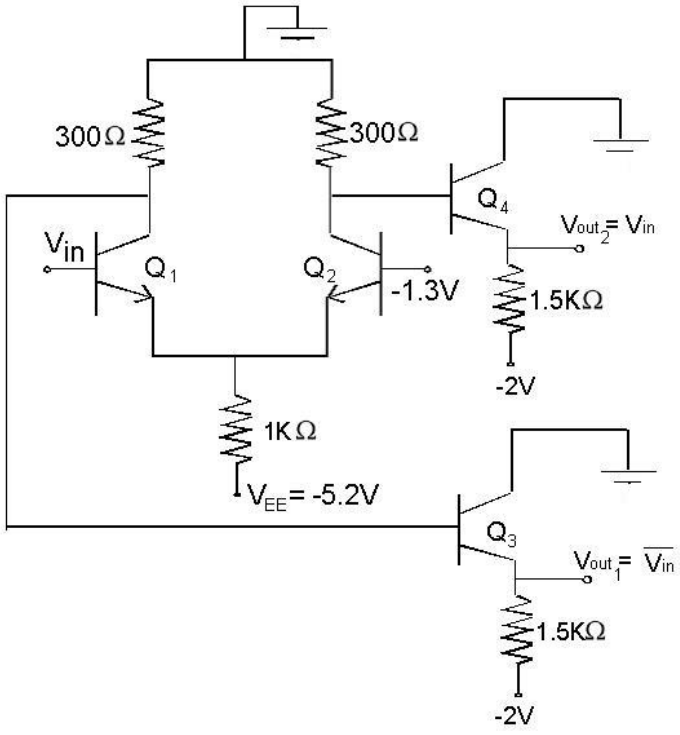
Emitter-Coupled logic (ECL)

- Emitter Coupled Logic (ECL) is a Current Mode Logic (CML) or non saturating digital logic family which eliminates the turn off delay of saturated transistors by operating in the active mode.
- At present, the ECL family has the fastest switching speed among the commercially available digital IC's.

The basic circuit ECL is a differential amplifier as shown below. (*Current Switch*)



- The VEE supply (of – 5.2V) produces a fixed current I_E, which remains around 3mA during operation.
- This current is allowed to flow through Q1 or Q2 depending on the voltage level at Vin.
- In other words the current switches between the collectors of Q1 and Q2 as Vin switches between its two logic levels of -1.6V (logical 0 for ECL) and -0.7V (logical 1 for ECL).
- The transistors operate in either their normal active mode or in cut off.
- The output voltage at the collector of Q2 is in phase with Vin, while the output voltage at the collector of Q1 is out of phase with Vin.
- Vc1 and Vc2 are the complements of each other and the output voltages are not the same as the input logic levels. Logic level 0 = 0V, Logic level 1 = -0.9V at the collectors of Q1 and Q2.
- Therefore these output signals from the current switch cannot serve as input signals to another current switch.
- The output voltage levels are made equal to the input logic level by connecting Vc1 and Vc2 to emitter follower stages Q3 and Q4 as shown below.



The emitter followers perform two functions

- They subtract approximately 0.7V (base emitter voltage drop of the emitter follower transistor) from Vc1 and Vc2 to shift the output to the correct ECL logic levels.
- They provide a very low output impedance (typically 7 Ohms), which provides for large fan out and fast charging of the load capacitance.

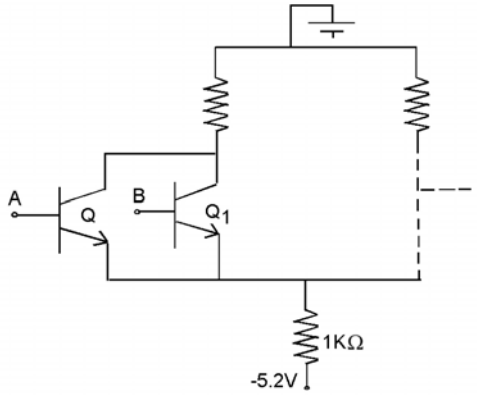
This circuit provides low complementary outputs

$$V_{out1} = \overline{V_{in}}$$

$$V_{out2} = V_{in}$$

ECL OR/NOR Gate

- The basic ECL circuit can be used as an inverter if the out put is taken at $V_{out1.}$
- The basic out put circuit can be expanded to more than one input by making transistor Q1 parallel to other transistors for other inputs.
- By connecting one more transistor Q in parallel with Q1 as shown below, the circuit becomes a two input ECL OR/NOR gate with inputs A and B.



- If both the inputs A and B are low, then both transistors Q and Q1 are in the OFF state while transistor Q2 is in the active region and its collector is in a low state.
- i.e. V_{out2} = Logical 0 and when A= Low and B= Low
- If either A or B is High, then accordingly either transistor Q or Q1 conducts and the transistor Q2 is in OFF state, resulting in high state at its collector.
- i.e. V_{out2} = Logical 1 (High) when either A or B = High
- Thus $V_{out2} = A + B(OR), V_{out1} = \overline{A + B}(NOR)$

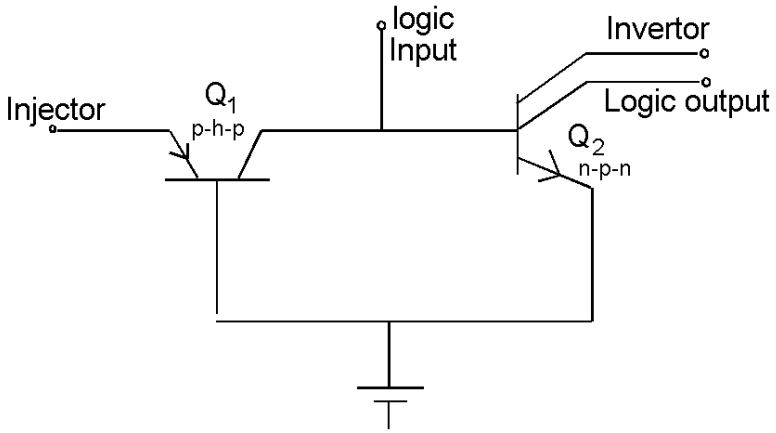
ECL Characteristics

1. The logical which are -0.7 V (logical 1) and -1.6V (logic 0) i.e. negative supply voltage and logic levels.
2. The transistors never saturate i.e. storage delay in ECL circuit is eliminated, and hence switching speed is very high. Typically propagations delay time is 1ns.
3. Because of low noise margin (250mv) ECL circuits are not reliable in heavy industrial environments.
4. An ECL logical block usually produces an output and its complement. This eliminates the need for inverters.
5. Fan outs are typically around 25, owing to the low impedance emitter follower out puts. Such a small fan out is a limitation compared with other logic families.
6. Power dissipation for a basic ECL gate is 40 mW, some what on the high side. This is because all the transistors are in the active mode.
7. The total current flow in an ECL circuit remains relatively contact regardless of its logic state. This helps maintain an unvarying current drain on the circuit power supply even during switching transitions.
   Thus no noise spikes will be internally generated like those produced by TTL totem pole circuits.

Use - Not as widely used as the TTL and MOS families except in very high frequency applications, where speed is superior.

Integrated Injection Logic (I^2L)

I^2L is a new LSI technique also called Merged Transistor logic (MTL) that uses both up n-p-n and p-n-p bipolar junction transistors to form a large number of IC gates as a chip.
The basic I^2L inverter circuit is shown below:



- Due to the absence of resistors, the I^2L inverter occupies much smaller area than a TTL inverter.
- The base of Q1 and emitter of Q2 are internally merged.
- The collector of Q1 and the base of Q2 are merged.
- Hence only four separate regions are required to form the two transistors.
- Thus, the entire I^2L gate takes only the space of a single TTL multiple emitter transistor.
- The p-n-p transistor Q1 as a current source.
- The multiple collector n-p-n transistor Q2 operation as an inverter.
- Most of the current leaving from the emitter of Q1 is injected directed into the base of Q2, and hence the emitter of Q1 is known as the Injector.

Advantages

1. Since I^2L gates are made up of BJTs, they have high speed of operation.
2. Since only transistors are used for construction, I^2L gates have high packing density, and are hence suitable for construction of VLSI circuits.
3. Very low power supply requirement.
4. Process steps required are less. Hence cost per gate in low.

Disadvantages

1. Very low voltage swing. Only from 0.8V to 0.2V
2. Lower noise margin.
3. External resistance required for proper functioning.
4. Lower packing density than NMOS.

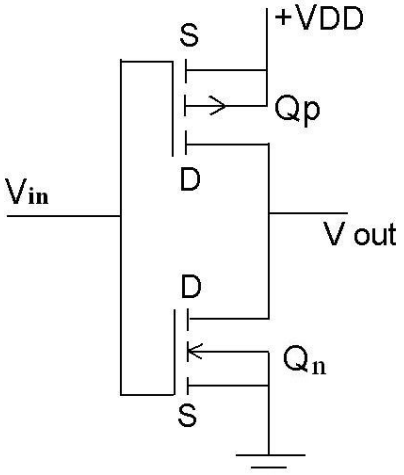
CMOS Logic

CMOS - Complementary MOS

- This logic family utilize both n- channel and p- channel enhancement type MOSFETs within the same circuit.
- CMOS digital circuits are available as standard small scale and medium scale integrated packages for use in logic design.
- In addition CMOS circuits are also used for very large scale integrated digital circuits as memories and in microprocessors.

The CMOS Inverter (NOT- gate)

The basic CMOS inverter is shown below:



- It consists of a p- channel enhancement type MOSFET Qp in series which an n –channel enhancement type MOSFET, Qs.
- Their drain terminals are connected together as well as their gate terminals.
- The input to the circuit is the common gate terminal and the out put is the common drain terminal.

To under stand the operation of the invertors, assume Vin is ground i.e. logic 0.

- In this case the gate to source potential of transistor Qn is zero, which is insufficient to create the n- channel needed for conduction.
- Therefore the transistor Qn is cut off.
- On the other hand, the gate to source potential of transistor Qp is – Vdd.
- Such a large negative potential on the gate terminal off transistor Qp relative to its source terminal causes the p-channel to be formed, which in turn results in transistor Qp being turned On.
- Since transistors Qn and Qp are in series, the same drain source current, which is very small must flow through both of them.

- Hence with transistor Qn appearing as a very high resistance and transistor Qp as a relatively low resistance, the voltage drop across transistor Qp is very small and the out put is approximately +Vdd or logic-1.

Now consider the case when the input to the CMOS invertors is +Vdd. i.e. logic-1.

- The gate to source potential of transistor Qp is zero.
- This results in no channel being formed in transistor Qp, while a channel is formed in transistor Qn.
- Thus Qp is on and appears as a relatively low resistance.
- Therefore the out put becomes approximately ground potential i.e. logic – 0.

CMOS Characteristics

1. Low Down dissipation
   - From the earlier circuit, we find that only one of the switches remains closed at any instant of consideration, while the other will remain open at that instant.
   - This means that no current will flow through the circuit at any instant of time, and hence no power loss will occur in the circuit.
   - In actual practice, a very small amount of leakage current may flow through the device, especially when the transistors are switched on or off.
   - This is due to the fact, during a transition between states, both MOSFETS, conduct for a small period of time.
2. Noise margin - typically about 45% of the supply voltage VDD.
3. Propagation delay time - ranges from 25 to 150 ms, with the exact value depending on the power supply voltage and other factors.
4. Voltage levels - can be operated over a supply voltage range of 3 to 15V.

Advantages

1. Lowest power dissipation of all gates (nano watts)
2. Very high noise immunity and noise margin (typically VDD/2)
3. Lower propagation delay than NMOS.
4. Large logic swing (= VDD)
5. Large fan- out capability (>50)
6. Directly compatibles with TTL gates.

Disadvantages

1. MOS chips must be protected from acquiring static charges by keeping the leads shorted. Static charges acquired in leads will destroy the chip.
2. Increased cost due to additional processing steps.