ECSE 534 Analog Microelectronics – Course Project (Final Phase)

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***Abstract*—A first order, single bit,** ∆Σ **A/D converter was designed. As an initial stage, system level analysis was done using Simulink MATLAB model and then the schematic level implementation in cadence is provided. In Simulink, the system level model was simulated and the results were provided. The obtained OSR is 95.2 and the system level was designed such that the SNR is 62dB.To meet this specification the input frequency is 7.5KHz and the sampling frequency was set to 5.13MHz with input amplitude of 0.2V. At Schematic level the circuit is designed and simulated using cadence in 65nm technology and the results are compared with system level.**

***Keywords*:** ∆Σ **A/D Converter, Simulink, MATLAB, SNR, OSR, 65nm technology.**

1. INTRODUCTION

This report follows the design, simulation, and analysis of a first order, single bit, low pass ∆Σ A/D converter using a 65nm process from IBM. We used MATLAB and Simulink to perform system level simulations and Cadence and Analog Environment to perform circuit level simulations. The circuit was designed to meet the following specifications:

* Output: 1 bit
* Power Supply: 1.0 V
* Technology: TSMC CMOS 65 nm
* Bandwidth: (1+ α) x 10 kHz, where α = (last 3 digits of student ID) / 1000.
* SNDR (peak): 50 dB (> 8 bits)
* Input Voltage Range: ± 0.20 V relative to AGND
* Power Dissipation: Minimum

To make sure that the circuit implementation will have the required specification we are first designing at system level using Simulink in MATLAB. Once the system level meets our specs then will move to the next step of designing at the schematic level trying to match with the system level results.

1. SYSTEM LEVEL SIMULATION

Firstly, the bandwidth is calculated from the student ID and it turns out to be *f*Bw= 18.80KHz. To keep some buffer for the design at schematic level, the circuit is designed for 55dB. As a result, the oversampling ratio (OSR) calculated to be 59.97.

*OSR* = 10(*SNRpeak−*2*.*61)*/*30 =59.97

The minimum sampling frequency will therefore be

*fs* = 2 *OSR f*3*dB* = 2.25 MHz

To allow for some buffer the sampling frequency is taken to be 5.13MHz and to match the coherent condition the input frequency used is 7.5KHz. Then, the Simulink model is arranged as shown in Fig.1. with input as sine wave with 0.2V amplitude and with stop time 0.7978msec along with the relay of 0.5/0.5 V to see a proper output.

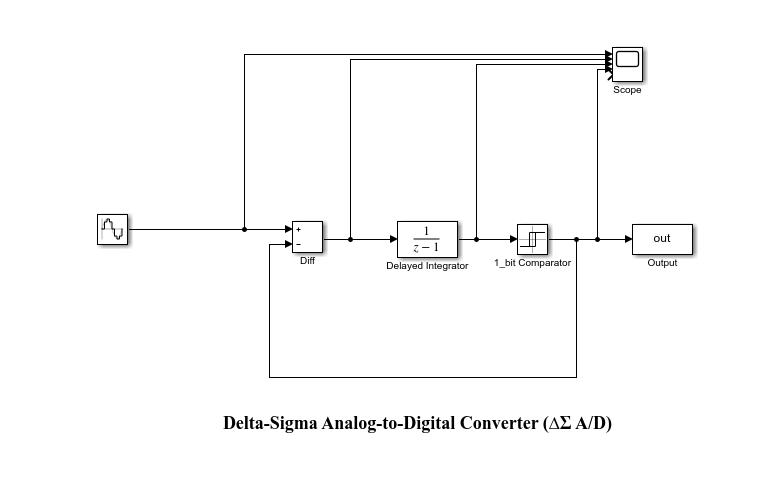


Figure 1. System level block diagram of the ∆Σ A/D converter from Simulink

Initially the PSD curve was obtained from the data collected and then using the PSD curve the SNR is calculated using the MATLAB code.

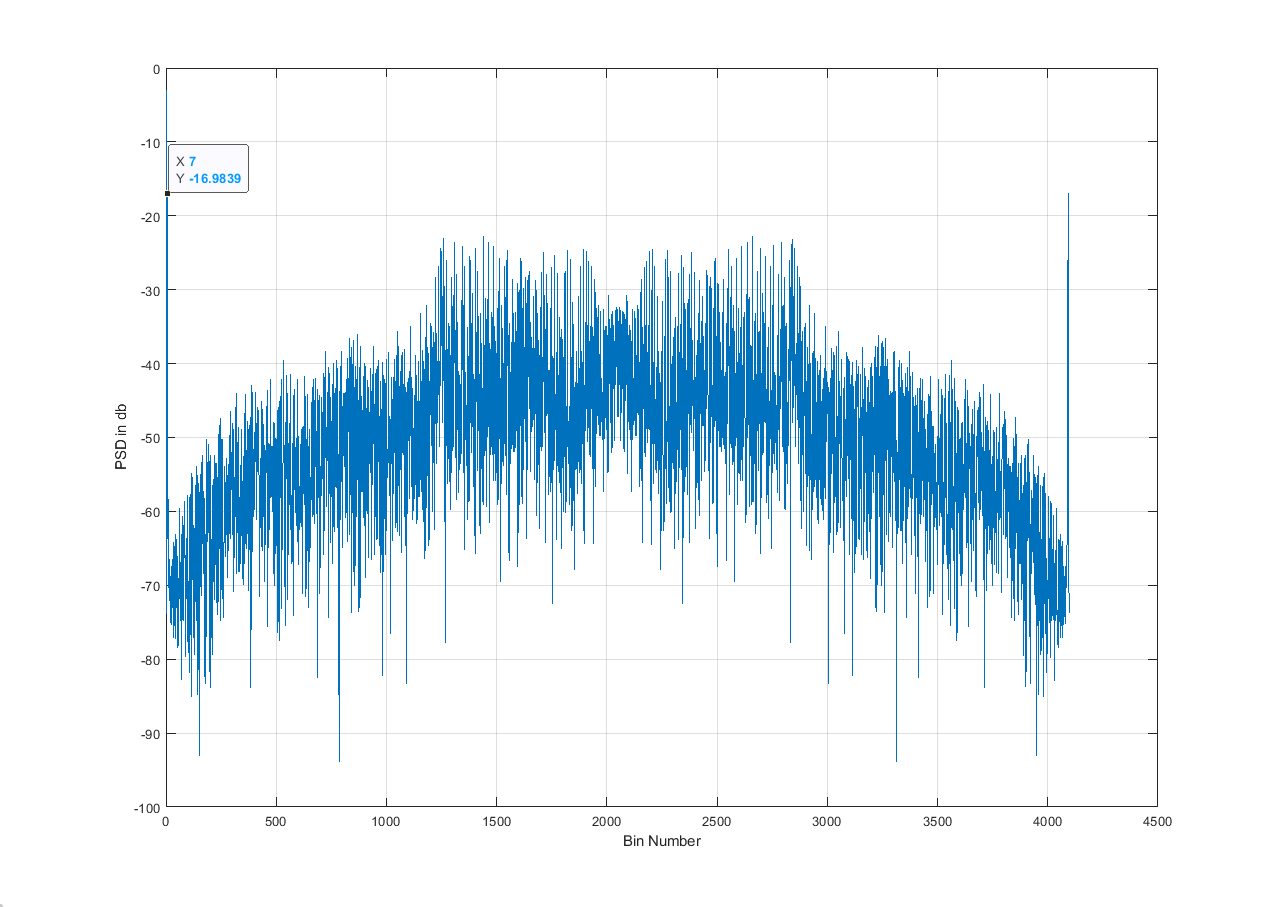


Figure 2: PSD plot from Simulink model of 1-bit DSM A/D

As seen from the fig.2 the marker shows the input signal frequency i.e. at 7th bin number and depending on the bandwidth, the bin number is 15 and from this we can calculate the SNR is calculate as the Power at 7th bin divided by the sum of the powers till 15th bin except the 7th bin power, and therefore

SNR =

The SNR is calculated to be around 57dB and this matches with our specification. SNR is calculated at different amplitudes and the result is plotted as shown in Fig.3.One can see that as the amplitude increases the SNR is decreasing and then after 0.7 V the SNR drops drastically. The Nth order SDM with NTF is highly unstable as a result loop filters with less aggressive noise shaping are used. But, even this less shaping SDM becomes unstable with large input values[X].

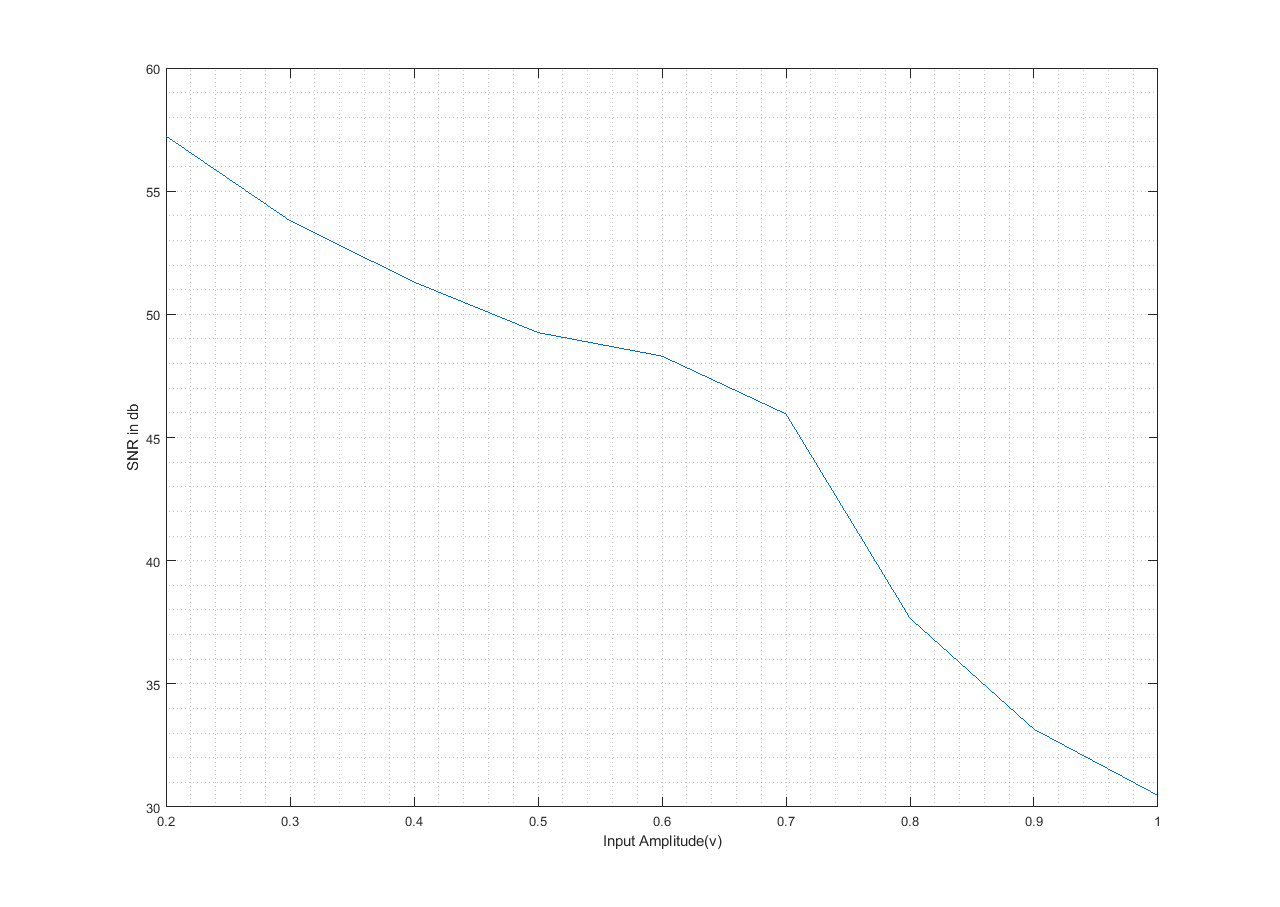


Figure 3: SNR vs. diff. input amplitude

The process of conversion of the input sine wave to the digital values is clearly shown in Fig.4. Fig.5 illustrate the input signal with the quantized output signal, as its seen that as the sine wave reached maximum or minimum the output is less dense compared to the output at other time interval. AS in this transient interval from moving from 1 to 0, it is very dense, this is because of pulse-density modulation, the principle behind SDM. To keep all the results and easy for comparison in the further stages, results are tabulated in table Ⅰ.

Table Ⅰ: Simulink Model Results

|  |  |
| --- | --- |
| Input voltage range | 0.2-1.0V |
| Bandwidth | 18.80KHz |
| Input, Oversampling Freq. | 7.5kHz, 5.13MHz |
| Minimum OSR | 59.97 |
| Simulated SNR | 57dB |
| UTP | 0.7978msec |

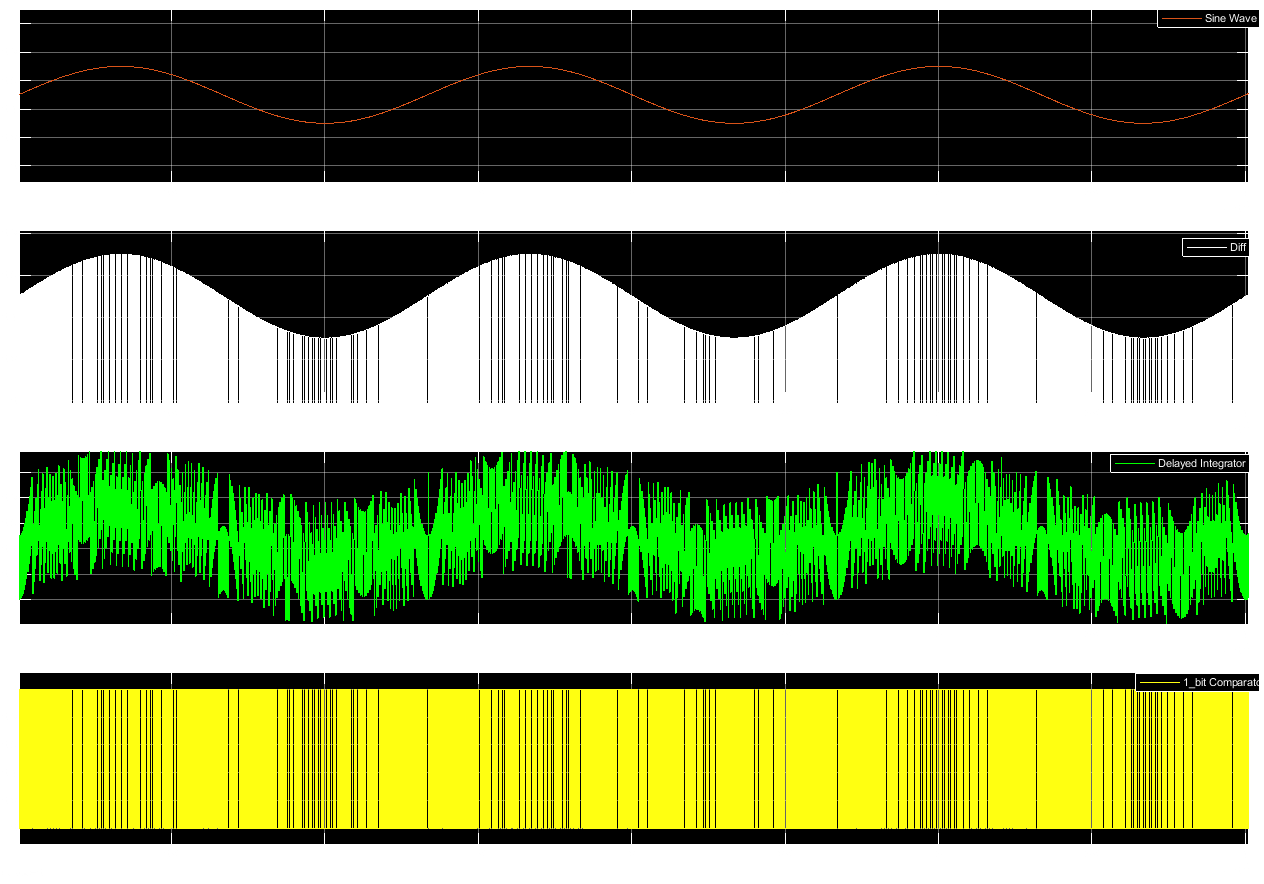


Figure 4: From top to bottom: input, subtraction integration, and output

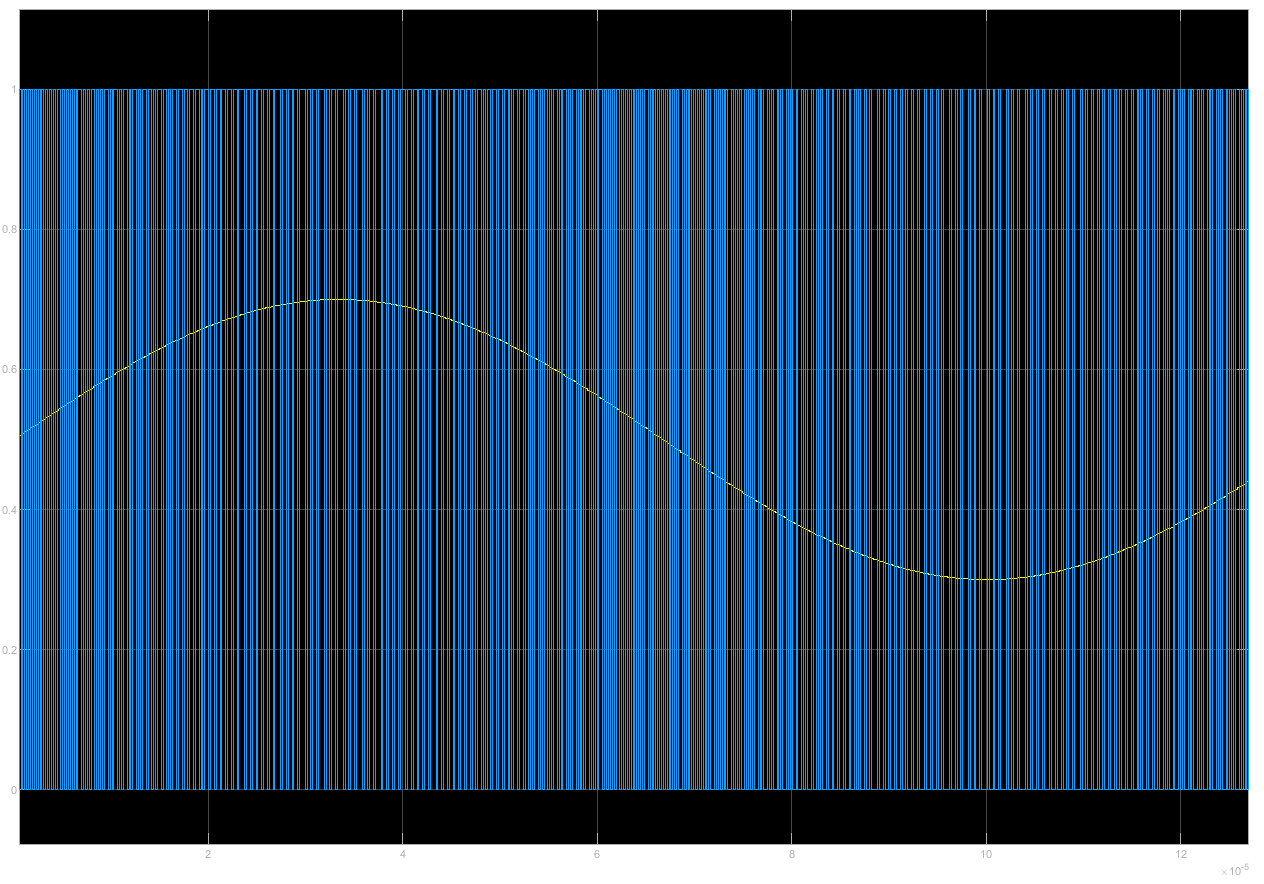


Figure 5: Input Sin Wave(yellow) vs. output (blue)

1. CIRCUIT LEVEL SIMULATION

Now, as we have the system level simulation results, its time to move on to the next stage for circuit level simulations in the cadence and all the simulations are done in analog environment.

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