Operational Amplifier Design Layout and Verification Assignment # 3

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Abstract—Three stage OTA is simulated and the results match with the required specification. In this paper, the layout and post simulations are considered and the results are compared with the previous assignment results which was without any parasitic values. Here the schematic has to go through some process before its being fabricated and made commercially ready. This paper explains the steps for layout and any difference observed between the post and pre layout.

Keywords—Three stage, OTA, layout, fabrication.

I. INTRODUCTION

Operational Amplifier Design: Layout and Verification. Integrated circuit layout, also known IC layout, IC mask layout, or mask design, is the representation of an integrated circuit in terms of planar geometric shapes which correspond to the patterns of metal, oxide, or semiconductor layers that make up the components of the integrated circuit. Originally the overall process was called tape out as historically early ICs used graphical black crepe tape on mylar media for photo imaging (erroneously believed to reference magnetic data--the photo process greatly predated magnetic media). When using a standard process—where the interaction of the many chemical, thermal, and photographic variables is known and carefully controlled—the behavior of the final integrated circuit depends largely on the positions and interconnections of the geometric shapes. Using a computer-aided layout tool, the layout engineer—or layout technician—places and connects all of the components that make up the chip such that they meet certain criteria—typically: performance, size, density, and manufacturability. This practice is often subdivided between two primary layout disciplines: Analog and digital.[1].
The generated layout must pass a series of checks in a process known as physical verification. The most common checks in this verification process are:

- design rule checking (DRC),
- layout versus schematic (LVS),
- parasitic extraction,
- Post-layout simulation,
- Comparison between post and pre layout results.

When all verification is complete, the data is translated into an industry-standard format, typically GDSII, and sent to a semiconductor foundry. The milestone completion of the layout process of sending this data to the foundry is now colloquially called "tape out". The foundry converts the data into another format and uses it to generate the photomasks used in a photolithographic process of semiconductor device fabrication. The layout view of CMOS op-amp is shown in Fig.1.[1].

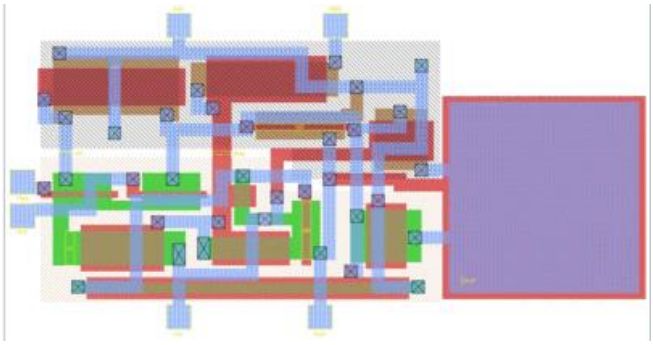

Figure 1: Layout view of a simple CMOS operational amplifier

These steps are explained one by one for three stage OTA which was designed in the second assignment as shown in Fig.2.

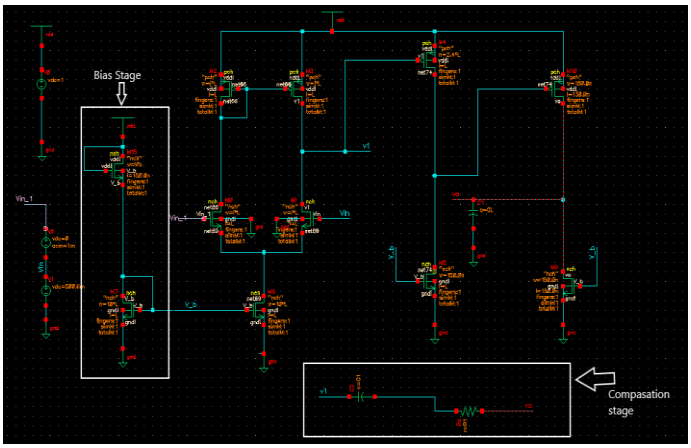

Figure 2: schematic diagram of given CMOS amplifier in cadence

Firstly, DRC analysis is presented in section II. LVS analysis and the QRC analysis are presented in sections III and IV, respectively, and in section V post simulation and comparison, while section VI concludes the work presented in this paper.

Table 1: W/L of all components

Stage	Device	Ratio	W in nm	L in nm
Diff Pair	M0, M1	5	750	150
	M2, M3	7	1050	150
Third stage	M4	2.4	360	150
	M5	1	150	150
Second stage	M9, M10	1	150	150
Bias Stage	M15	1.41	212	150
	M7	10	1500	150
	M6	10	1500	150

II. Design Rule Checking (DRC)

A design rule is a geometric constraint imposed on circuit board, semiconductor device, and integrated circuit (IC) designers to ensure their designs function properly, reliably, and can be produced with acceptable yield. Design rules for production are developed by process engineers based on the capability of their processes to realize design intent. Electronic design automation is used extensively to ensure that designers do not violate design rules; a process called design rule checking (DRC).[3]

There is a certain process to make sure that your layout passes DRC and is explained one by one. Firstly, before generating the layout from the source make sure that your spacings are set to 0.0005um otherwise it will show errors. The area of closed loop in the layout should be greater than 1um(square). The guard error can be cleared by creating the MPP and appropriate VSS and VDD metal layout around the circuit. It's always good to exactly match the metal layers in dimensions while overlapping two layers. A good practice is to always use "path" drawing rather then going by rectangle or square unless it's necessary. The rules if any occurs can be resolved by looking into the error message carefully and going through the document provided by tsmc in their server. Table 1 shows the dimension of the transistors. Once, the DRC is run from caliber then if the circuit doesn't have any error then it will show the Fig.3. The designed OTA after layout went through the DRC and after all the errors are resolved the window looks like the one shown in Fig.3.

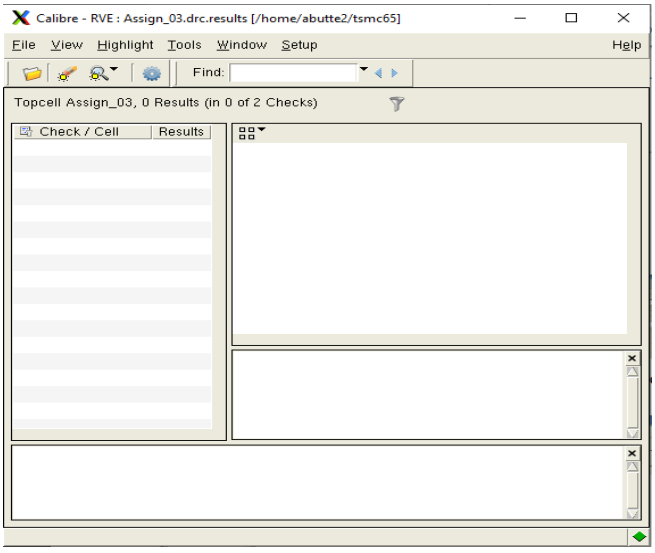

Figure 3: DRC with no errors

III. Layout Vs Schematic (LVS)

LVS checking software recognizes the drawn shapes of the layout that represent the electrical components of the circuit, as well as the connections between them. This netlist is compared by the "LVS" software against a similar schematic or circuit diagram's netlist. Design inputs needed for running LVS are as follows:

- Graphical database system (GDS) layout database of the design
- Schematic netlist of the design
- Cell definition file including Intellectual property files and standard cells
- Pad reference file

Referring the document set up the LVS and once you run LVS from the ASSURA tab the LVS if runs without any error should pop up a window as shown in Fig.4. One can see that it shows the folder and the summary shows that it matches exactly with the schematic.[4] If any errors don't jump to the next step as if we ignore this step our simulation results will differ too much from the pre layout results as there is no correct connections between the instances.

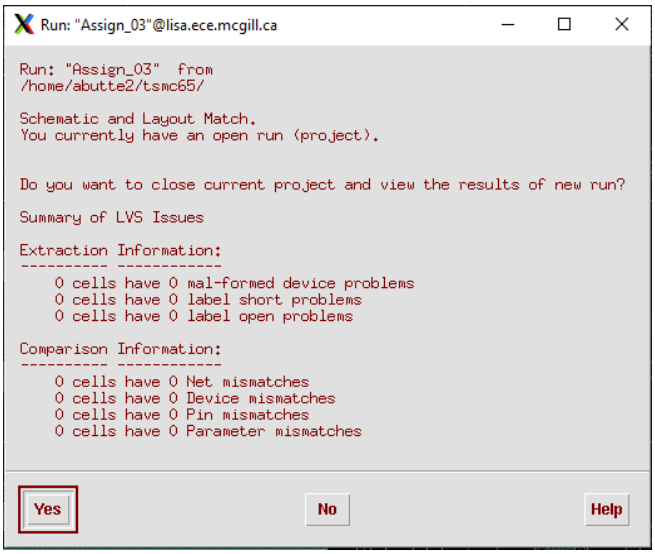

Figure 4: LVS with no errors

IV. QRC

Parasitic are 'devices' which are not intended but intrinsic to any physical representation of a circuit. For instance: interconnect traces have Resistance, Capacitance to their surrounding and Inductivity. The circuit schematic does (in first order) not include any physical layout information. Only after the layout exact parasitic can be extracted. Simulation with annotated parasitic models the circuit behavior most accurately. Parasitic become more relevant (can even become dominant) as feature sizes shrink. Here the tool used is ASSURA QRC. select: QRC à Run Assura –Ok. In the next window, in the setup tab change the output to extracted view, now go to extraction and do the necessary changes mainly change the extraction type to RC. Once the QRC runs successfully one can see a window similar to Fig.5. If we look at the log file it shown the summary of QRC as shown in Fig.6.Finally the layout is ready for post simulation and the layout of the schematic is shown in Fig.7.

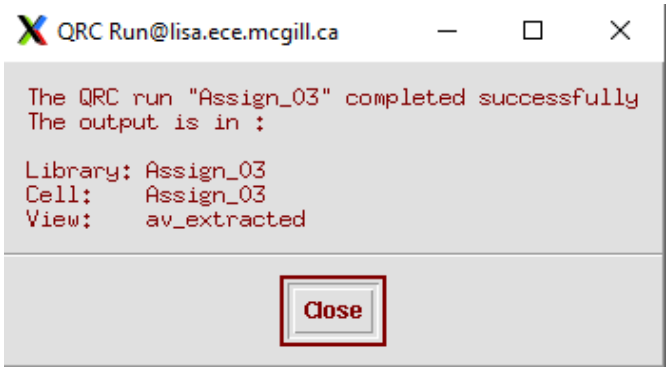

Figure 5: QRC successful result

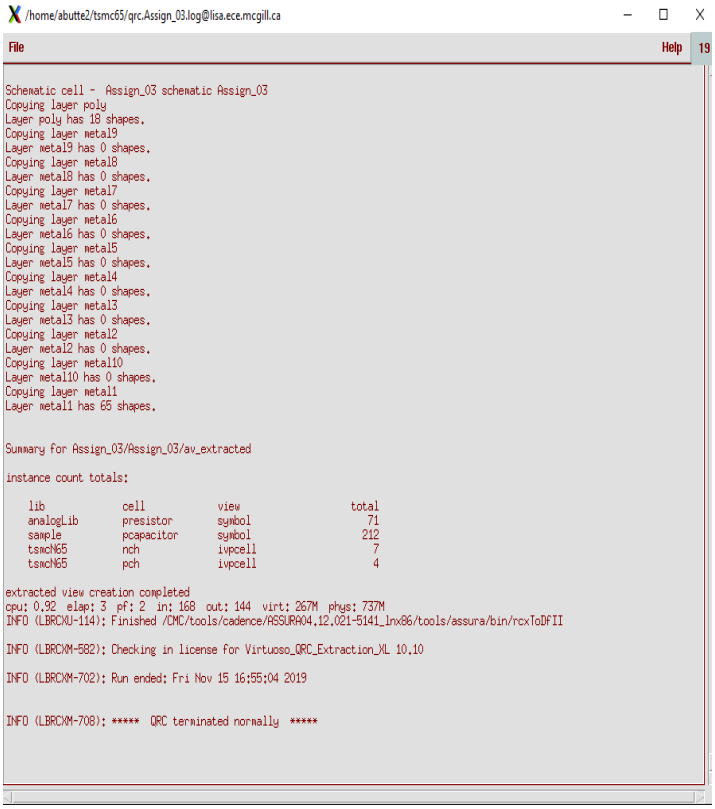

Figure 6: QRC log File

V. Post-Layout Simulation and Comparison

Once the layout is lay down then the simulation is carried on with the layout which includes the parasitic. The results are then compared in the table 2. The results match good with the pre layout and are within the specifications. The gain,3_db, PM and UGBW are shown in Fig.8. The input-output range is shown in Fig.9. The input referred noise is shown in Fig.10.The poles and zeros are shown in Fig.11.Finally the power consumption is shown in Fig.12 and is 22 µA. All the values in the figures are tabulated in table 2. Once the layout is done the load capacitor as its too large 10pf when we connect it looks like Fig.13.[2]

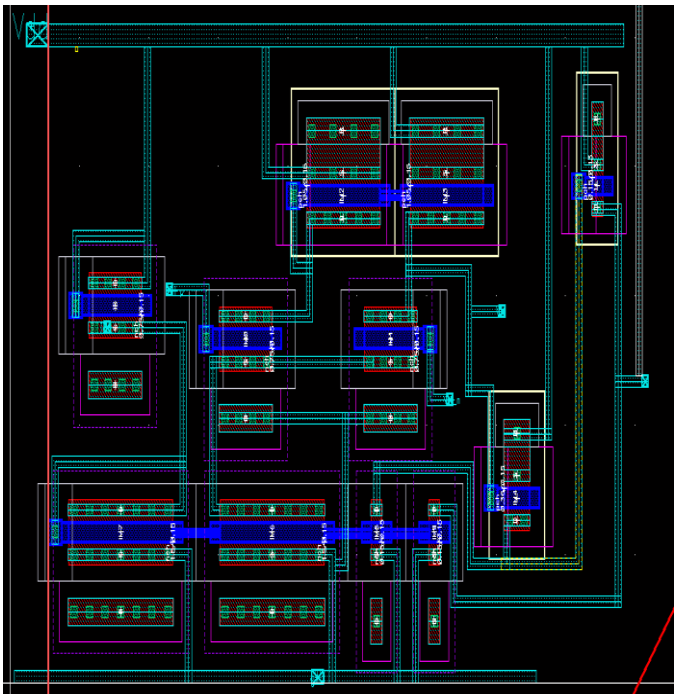

Figure 7: Final layout of 3 stage OTA

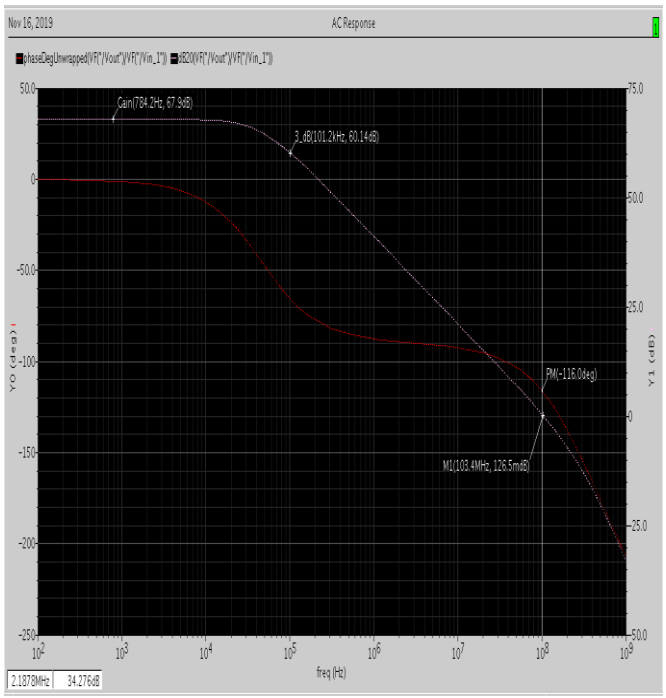

Figure 8: DC gain, UGBW and PM

In Fig.13, the capacitor is shown where its too large to fit into the CMOS design so I decided to put them offchip but just to show that we can design that I have used this view.

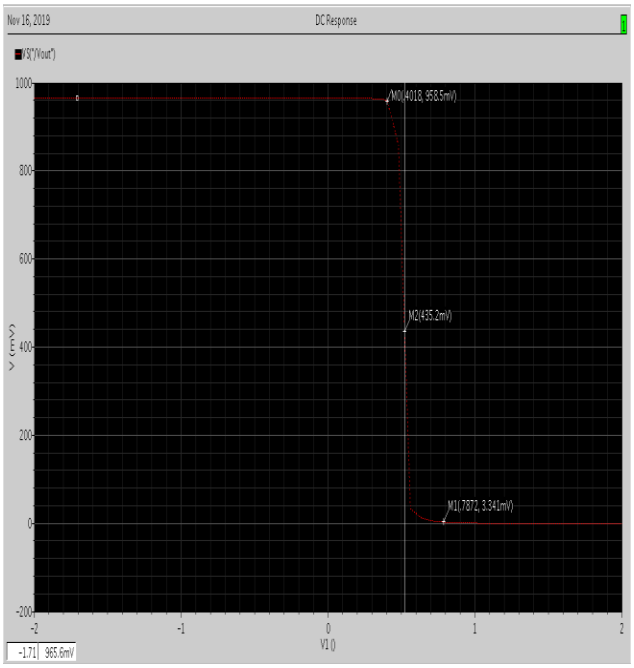

Figure 9: Voltage range

Results Display Window@lisa.ece.mcgill.ca

Window Expressions Info Help 29

Device	Param	Noise Contribution	% Of Total
/M1	fn	3.57922e-12	26.12
/M0	fn	3.49892e-12	25.53
/M3	fn	1.25374e-12	9.15

Spot Noise Summary (in V^2/Hz) at 1M Hz Sorted By Noise Contributors
Total Summarized Noise = 1.37044e-11
Total Input Referred Noise = 1.07133e-15
The above noise summary info is for noise data

Figure 10: total Input referred Noise

Results Display Window@lisa.ece.mcgill.ca

Active 30

Window Expressions Info Help

Poles(Hz)

	Real	Imaginary	Qfactor
Pole_1	-4.557e+04	0.000e+00	5.000e-01
Pole_2	-2.643e+08	0.000e+00	5.000e-01
Pole_3	-1.082e+09	0.000e+00	5.000e-01
Pole_4	-3.189e+09	0.000e+00	5.000e-01
Pole_5	-3.945e+09	0.000e+00	5.000e-01

Zeros(Hz)

	Real	Imaginary	Qfactor
Zero_1	-2.069e+09	0.000e+00	5.000e-01
Zero_2	-5.538e+09	0.000e+00	5.000e-01
Zero_3	-1.036e+10	0.000e+00	5.000e-01
Zero_4	-2.294e+10	1.572e+10	6.061e-01
Zero_5	-2.294e+10	-1.572e+10	6.061e-01

Network function gain(magnitude)= 4.436e-06

Figure 11: List of the pols-zero positions

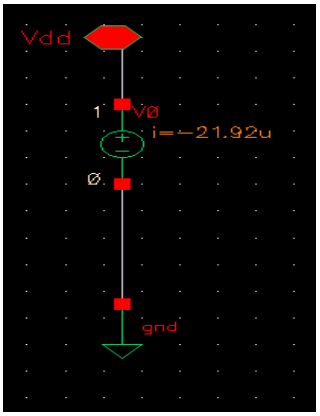

Figure 12: Power consumption calculation

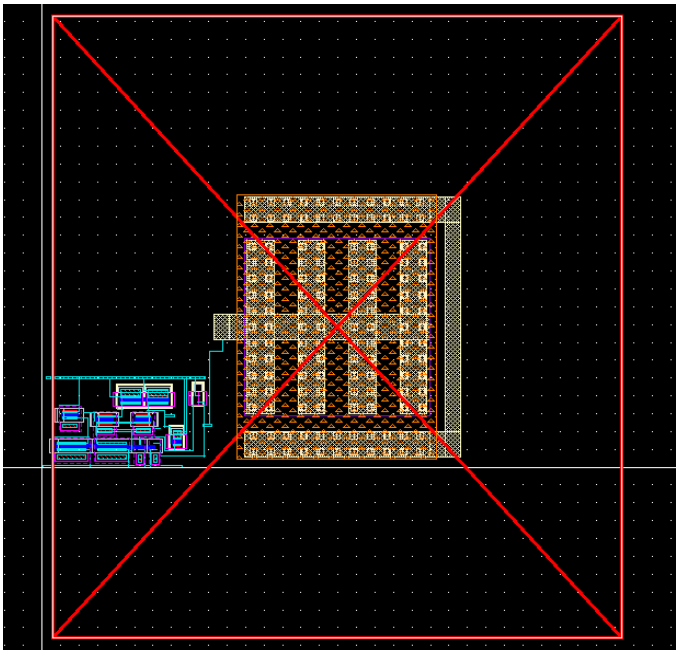

Figure 13: layout with capacitor

As seen from the fig.9 the offset voltage is 3.3mv and the Input referred noise is 1.07e-15 v^2/HZ. The layout showing the extracted parasitic is shown in Fig.14.

Table 2. Comparison

Parameter	Post_layout	Pre_layout
DC gain	67.90 dB.	67.93dB
Amplifier poles	-45.5 KHz and -264.3 MHz	-45.4 KHz and -264.4 MHz
Static power dissipation	22 µA	41.92 µA
PM	63.8 degrees	64
UGBW	103.4MHz	101MHz
3_dB	101.2kHz	85.08kHz

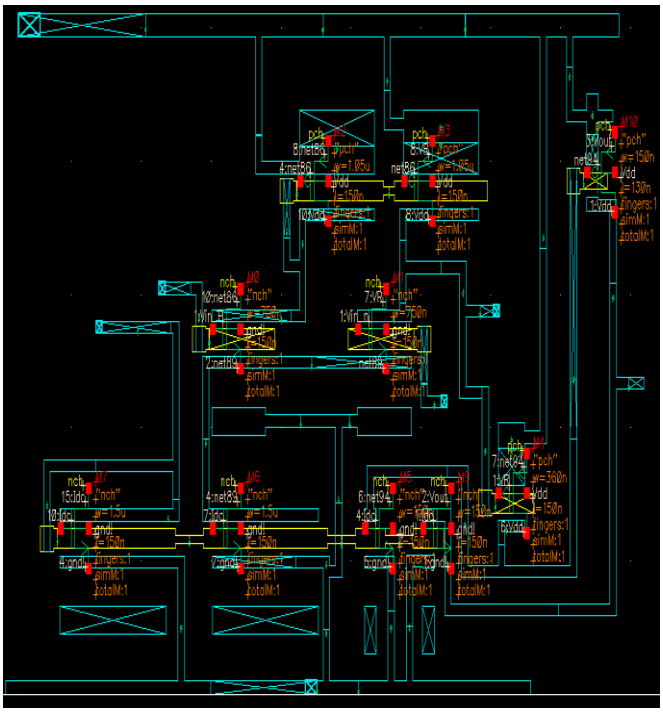

Figure 14: extracted Layout

VI. CONCLUSION

This paper presents the post simulation results of the 65nm technology of three stage OTA using the cadence tool in the analog environment. All the different process has been implemented step by step to get the appropriate results.

REFERENCES

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[2] K. H. Mak and K. N. Leung, "A signal- and transient-current boosting amplifier for large capacitive load applications," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 61, no. 10, pp. 2777–2785, Oct. 2014.

[3] A. D. Grasso, G. Palumbo, S. Pennisi, and W. Sansen, "The noise performance of CMOS Miller operational transconductance amplifiers with embedded current-buffer frequency compensation," Int. J. Circuit Theory Appl., vol. 45, no. 4, pp. 457–465, Apr. 2017.

[4] B. K. Thandri and J. Silva-Martinez, "A robust feedforward compensation scheme for multistage operational transconductance amplifiers with no Miller capacitors," IEEE J. Solid-State Circuits, vol. 38, no. 2, pp. 237–243, Feb. 2003.

Appendix:

Extracted Layout:

/home/abutte2/tsmc65/Assign_03/Assign_03/av_extracted

Layout:

/home/abutte2/tsmc65/Assign_03/Assign_03/layout_gen

Schematic:

/home/abutte2/tsmc65/Assign_03/Assign_03/schematic