ECSE 534 Analog Microelectronics – Course Project (Final Phase)

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***Abstract*—A first order, single bit, ΔΣ A/D converter was designed. As an initial stage, system level analysis was done using Simulink MATLAB model and then the schematic level implementation in cadence is provided. In Simulink, the system level model was simulated and the results were provided. The obtained OSR is 59.97 and the system level was designed such that the SNR is 57dB.To meet this specification the input frequency is 7.5 KHz and the sampling frequency was set to 5.13MHz with input amplitude of 0.2V. At Schematic level the circuit is designed and simulated using cadence in 65nm technology and the results are compared with system level.**

***Keywords*: ΔΣ A/D Converter, Simulink, MATLAB, SNR, OSR, 65nm technology.**

I. Introduction

This report follows the design, simulation, and analysis of a first order, single bit, low pass ΔΣ A/D converter using a 65nm process from IBM. We used MATLAB and Simulink to perform system level simulations and Cadence and Analog Environment to perform circuit level simulations. The circuit was designed to meet the following specifications:

- Output: 1 bit
- Power Supply: 1.0 V
- Technology: TSMC CMOS 65 nm
- Bandwidth: (1+ α) x 10 kHz, where α = (last 3 digits of student ID) / 1000.
- SNDR (peak): 50 dB (> 8 bits)
- Input Voltage Range: ± 0.20 V relative to AGND
- Power Dissipation: Minimum

To make sure that the circuit implementation will have the required specification we are first designing at system level using Simulink in MATLAB. Once the system level meets our specs then will move to the next step of designing at the schematic level trying to match with the system level results.

II. System Level Simulation

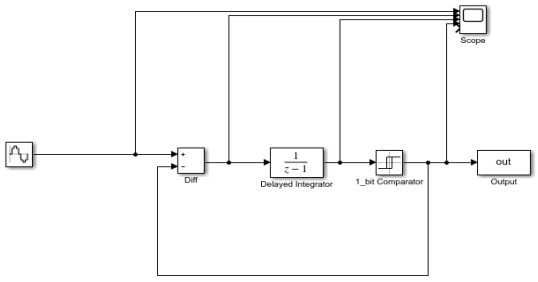
Firstly, the bandwidth is calculated from the student ID and it turns out to be f_{Bw} = 18.80 KHz. To keep some buffer for the design at schematic level, the circuit is designed for 55dB. As a result, the oversampling ratio (OSR) calculated to be 59.97.

$$OSR = 10^{(SNR_{peak}-2.61)/30} = 114.46$$

The minimum sampling frequency will therefore be

$$f_s = 2\ OSR\ f_{3dB} = 4.38\ \text{MHz}$$

To allow for some buffer the sampling frequency is taken to be 8.19MHz and to match the coherent condition the input frequency used is 16KHz. Then, the Simulink model is arranged as shown in Fig.1. with input as sine wave with 0.2V amplitude and with stop time 0.125msec along with the relay of 0.5/0.5 V to see a proper output.



Delta-Sigma Analog-to-Digital Converter (ΔΣ A/D)

Figure 1. System level block diagram of the ΔΣ A/D converter from Simulink

Initially the PSD curve was obtained from the data collected and then using the PSD curve the SNR is calculated using the MATLAB code.

As seen from the fig.2 the marker shows the input signal frequency i.e. at 3rd bin number and depending on the bandwidth, the bin number is 5 and from this we can calculate the SNR is calculate as the Power at 7th bin divided by the sum of the powers till 15th bin except the 7th bin power, and therefore

$$\text{SNR} = \frac{(Power)_{i=3}}{\sum_{i=2}^{5}(Power)_i}$$

The SNR is calculated to be around 61dB and this matches with our specification.

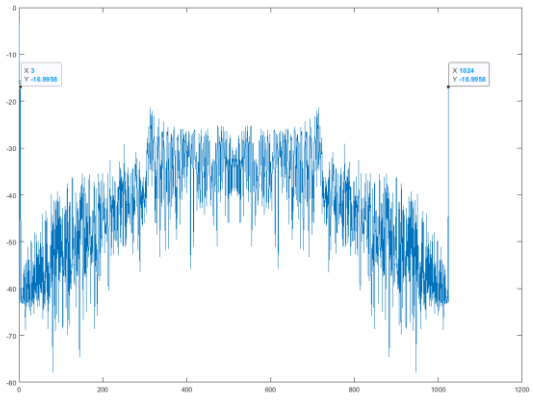


Figure 2: PSD plot from Simulink model of 1-bit DSM A/D

SNR is calculated at different amplitudes and the result is plotted as shown in Fig.3.One can see that as the amplitude increases the SNR is decreasing and then after 0.7 V the SNR drops drastically. The Nth order SDM with NTF$(1-z^{-1})^N$ is highly unstable as a result loop filters with less aggressive noise shaping are used. But, even this less shaping SDM becomes unstable with large input values [1].

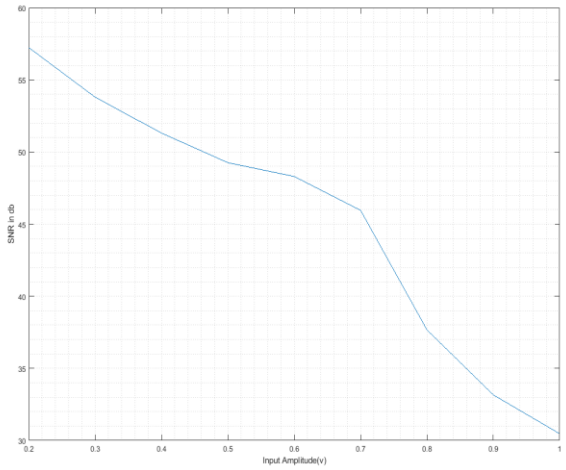


Figure 3: SNR vs. diff. input amplitude

The process of conversion of the input sine wave to the digital values is clearly shown in Fig.4. Fig.5 illustrate the input signal with the quantized output signal, as its seen that as the sine wave reached maximum or minimum the output is less dense compared to the output at other time interval. AS in this transient interval from moving from 1 to 0, it is very dense, this is because of pulse-density modulation, the principle behind SDM. To keep all the results and easy for comparison in the further stages, results are tabulated in table I.

Table I: Simulink Model Results

Bandwidth	18.80KHz
Input, Oversampling Freq.	16kHz, 8.12MHz
Minimum OSR	59.97
Simulated SNR	61.71dB
UTP	0.1250msec

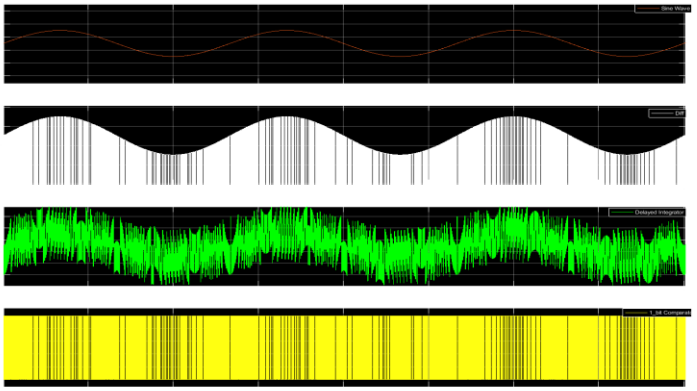


Figure 4: From top to bottom: input, subtraction integration, and output

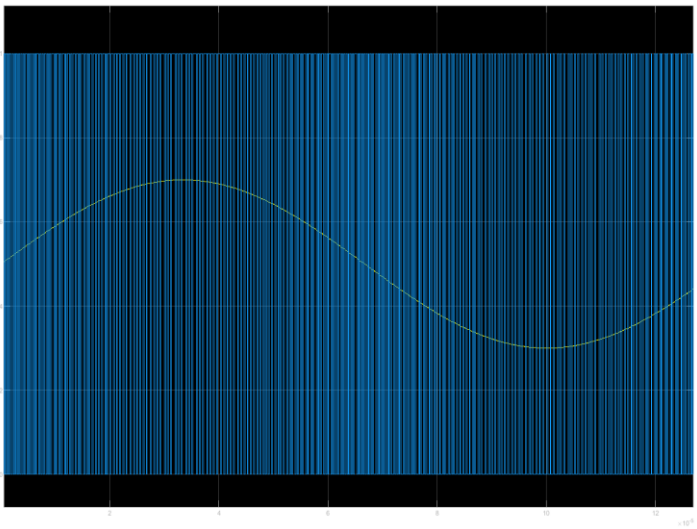


Figure 5: Input Sin Wave (yellow) vs. output (blue)

III. CIRCUIT LEVEL SIMULATION

Now, as we have the system level simulation results, it's time to move on to the next stage for circuit level simulations in the cadence and all the simulations are done in analog environment.

Here it's important to build all the components and then add

them finally to make the complete sigma delta [2]. So, for that I have to design the following components which are explained one by one in the below section.

A. Four Phase Clock

This is designed to generate all the clock signal which will be used in the circuit. To design this, two NOR gates and couple of invertor's are used and the schematic is shown in Fig.6.It's a four phase clock but in the main design I have just used it as two phase clock because that itself it giving me required output. The basic logic gates used are also designed and then their symbols are created and used in this schematic. In the schematic all the VSS are already connected to ground terminal as a result not seen in the schematic. The output is as shown in Fig.7.

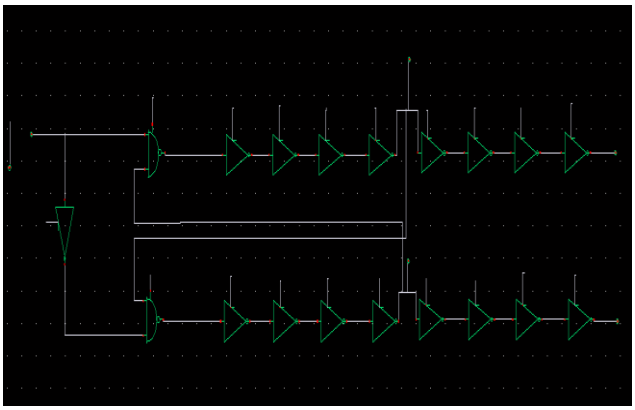


Figure.6: Schematic of 4-phase clock

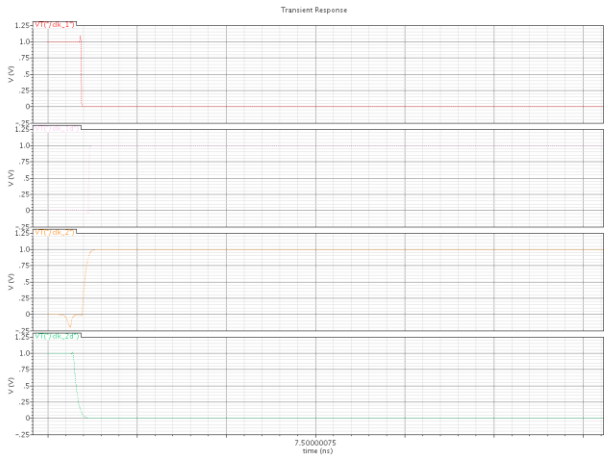


Figure.7: Output of 4-phase clock

B. D Latch

D latch is used to sample the comparator output and sending its output as a feedback to the D/A. Implementation of D latch was done using four NAND gates as shown in Fig.8. There are two outputs "Q" and "Bar_Q" and two inputs i.e. clock and "D".NAND gate is implemented using two NMOS and two PMOS and their W/L is kept such that one get the expected result. The "D" is the output terminal of the whole sigma delta circuit.

C. Transmission Gate

It is sometimes referred to as the analog switch and is an electronic element that will select or pass a signal depending upon the reference values which we provide. It is designed using an inverter, a single PMOS and NMOS as shown in Fig.9.To build Switched capacitor and D/A circuit these transmission gates are used and the schematic is shown in Fig.10 and 11 respectively. As seen in Fig.10, four transmission gate are combined to function as a switched capacitor circuit the capacitor is given a value of 100f F. Similarly to form D/A, two transmission gates are used with reference voltages as input as shown in Fig.11.

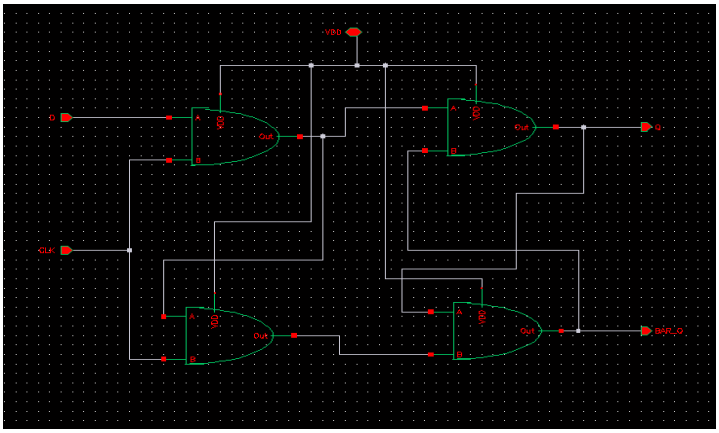


Figure.8: schematic of D Latch

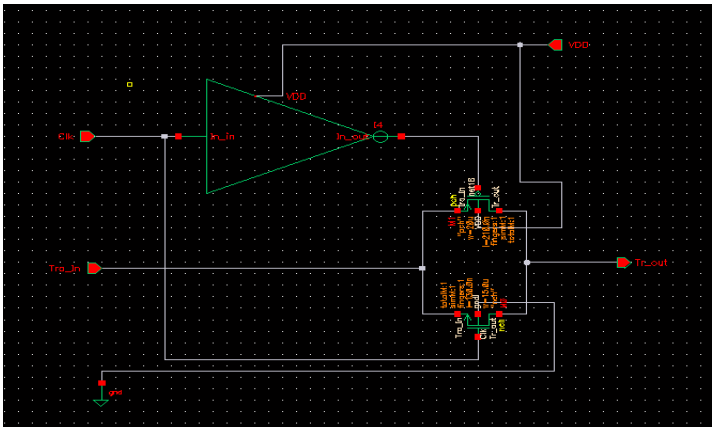


Figure.9: schematic of Transmission gate

D. Integrator and Comparator

These are the main components of sigma delta and as a result it is required to see that their circuit works as expected. We have already designed and even tabulated all the results of these components in our 2nd assignment. The OTA, if we use it with a feedback capacitor then it works as a comparator, and if there is no feedback then it functions as a comparator and both the schematics are shown in Fig.12. The function of the integrator is to integrate the signals coming from the SC circuit as its name suggest with a miller capacitance of 100f F. Comparator receives the input from the integrator and then it works as analog to digital convertor circuit where the analog ground is set to 0.5V.

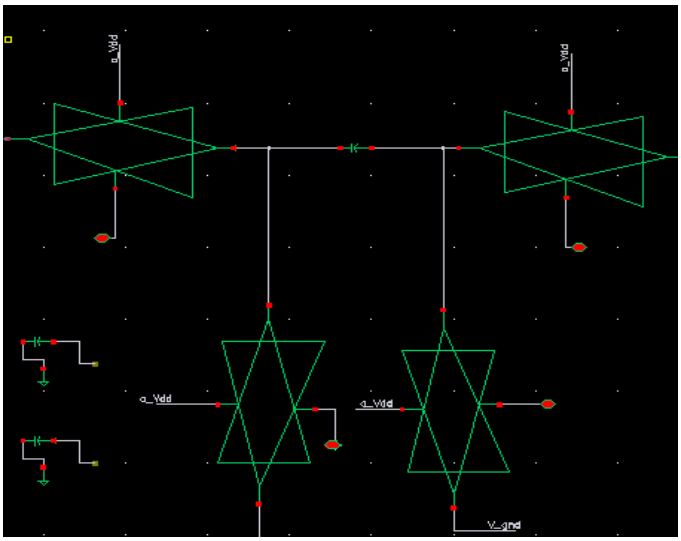


Figure.10: schematic of SC block

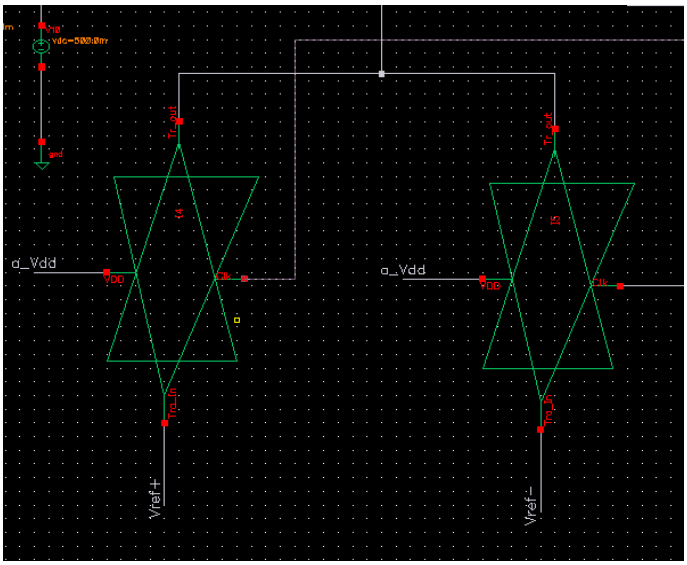


Figure.11: schematic of D/A block

E. A first order, single bit, ΔΣ A/D converter

After all the components are created and simulated and once we are sure that all the single components works as expected then we can combine them in a single circuit to create our sigma delta convertor and is as shown in Fig.13.All the components are labeled and the connections are shown clearly in Fig.13.

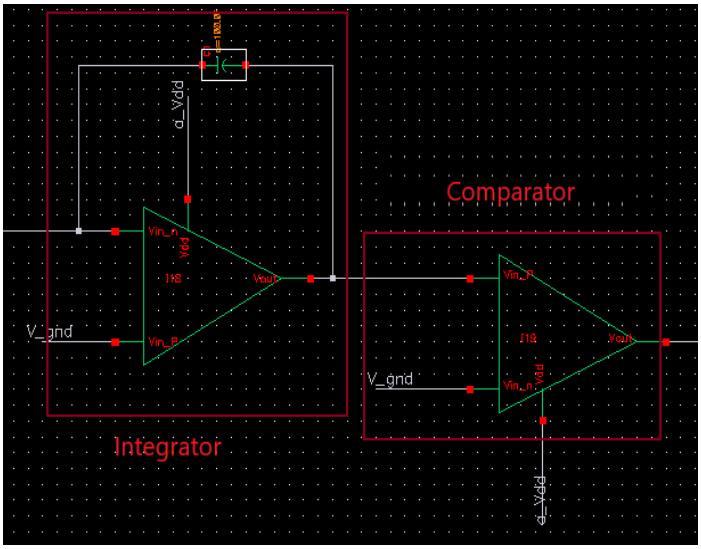


Figure.12: schematic of Integrator and Comparator block

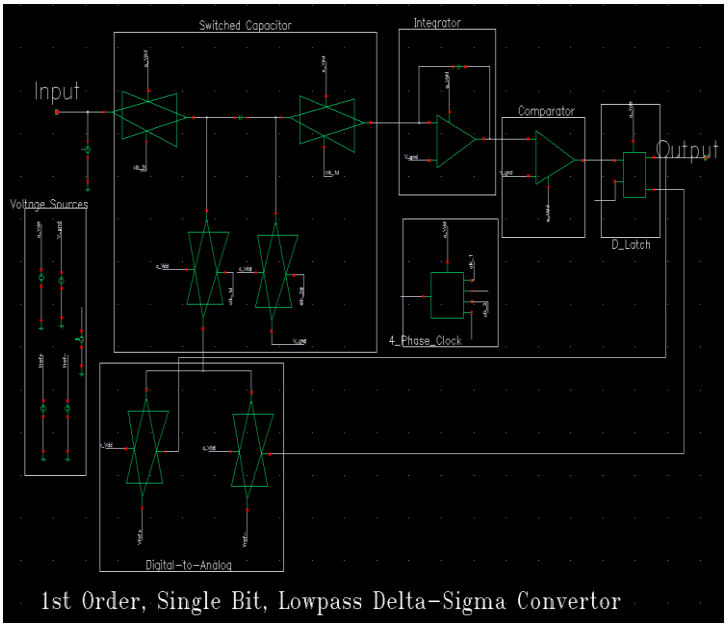


Figure.13: schematic of Sigma-Delta Convertor

The output and input wave forms are clearly shown in Fig.14

And it can be seen that the analog signal (red) is converted to digital signal (yellow) as expected out of the circuit.

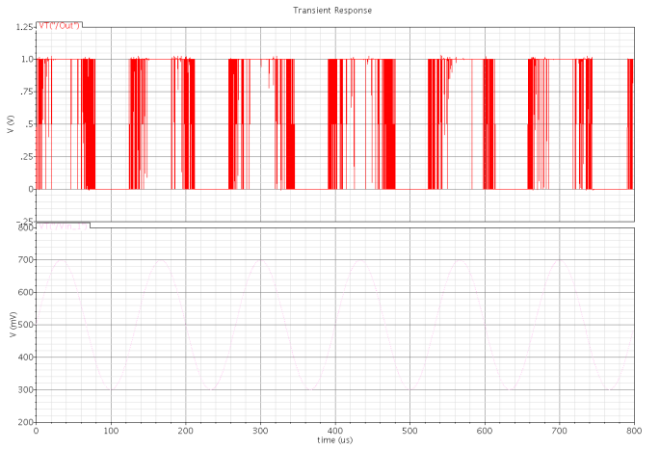


Figure.13: Output (top) and input (bottom) of Sigma-Delta Convertor

The SNR is calculated using cadence data in matlab and it observed to meet the specification of the design i.e. 55dB approximately. The PSD plot is shown in fig 14. Then we moved to the next step where we did the layout and simulated the extracted parasitic layout.

IV. CHANGES IN FINAL PHASE

Some important changes were made and are updated in this report from the initial phase for better results. Cadence analog environment takes too much of time to simulate for 4096 points so we reduced that to 1024 in the final project and as a result we also increased the sampling frequency to make sure that SNR is above the specification. We found out that input frequency is very crucial for a good SNR and if it's close to the bandwidth we have a better result. The reason for this is that the more close the fundamental frequency the less number of spikes in the bandwidth and most of their harmonics are not within the bandwidth.

V. LAYOUT OF SIGMA DELTA ADC

The next part is to simulate the circuit by extracting the parasitic. It's very important that we layout our design in a way that it takes less space and we have to follow the procedure we followed during the third assignment [3]. It's crucial that the layout passes the DRC checks and LVS. As seen in Fig.15 the layout we designed has passed DRC and then we moved to the next step for LVS and one can see the result as shown in Fig.16. Both DRC and LVS are passed successfully and then we moved for parasitic extraction using QRC and the results are highlighted in Fig.17. Then to get the extracted view for simulation we run the QRC and the Result is shown in Fig.17 and it's successful. The layout is as shown in Fig.22. As the capacitors are big we are not able to highlight clearly all the components. The designed is optimized and tried to reduce the size and compactness. The green highlighted area is switched capacitor and similarly all the other components are labeled and highlighted with same color. All the pins are labeled at that spot. The designed is optimized and tried to reduce the size and compactness. The green highlighted area is switched capacitor and similarly all the other components are labeled and highlighted with same color. All the pins are labeled at that spot. Then the circuit is simulated using the process as in assignment 3 and then the results are calculated as before and it matches with the specification.

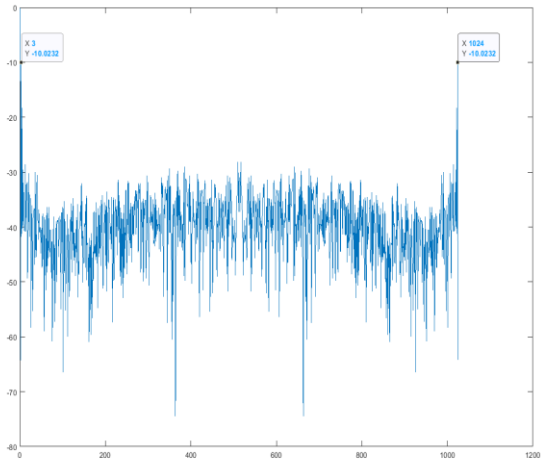


Figure.14: PSD of circuit level simulation

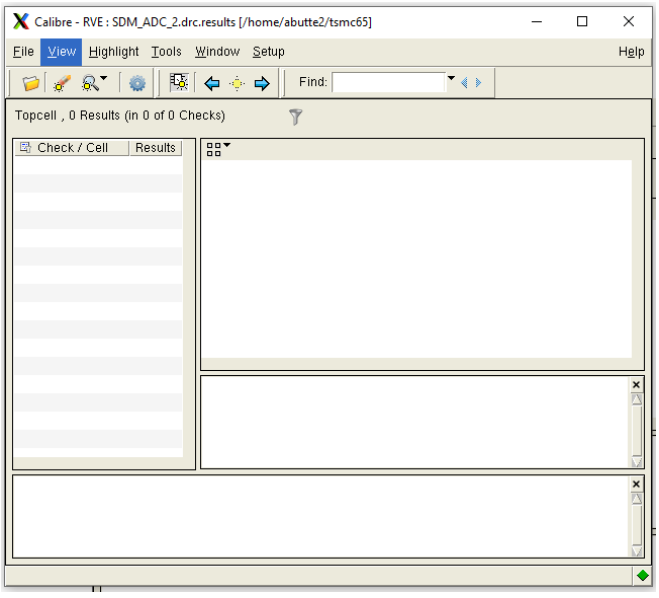


Figure.15: DRC with no errors

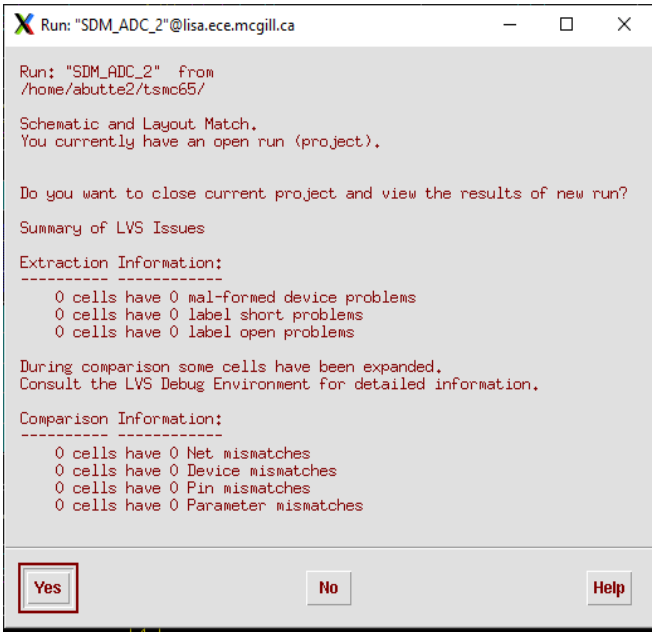


Figure.16: LVS result

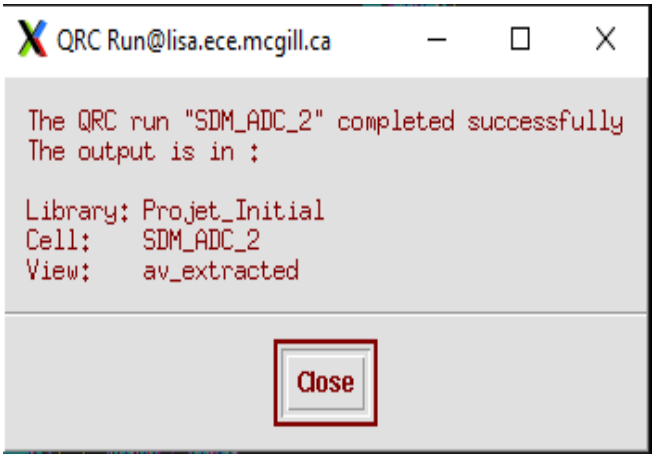


Figure.17: QRC result

To give a clear picture of the layout, each component layout is specified in the figures below. In Fig 18, the transmission gate to construct the switched capacitor is shown. As seen the PMOS has the larger W/L ratio to get the optimum result. Then in Fig.19, the comparator is shown which is similar to what we have designed in the previous assignments. 4-phased clock generator is shown in Fig.20, even though we have used only two clock in the circuit but we have tried with four clocks initially. The D-latch shown in Fig.21. All these components passes LVS and DRC checks and we have tried to optimize the size as much as possible so that our complete layout takes less space.

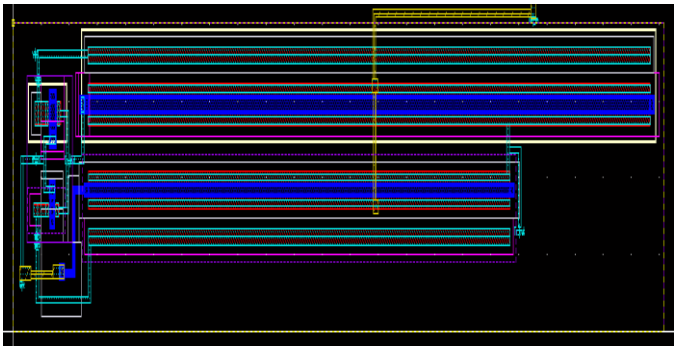


Figure.18: Transmission gate layout

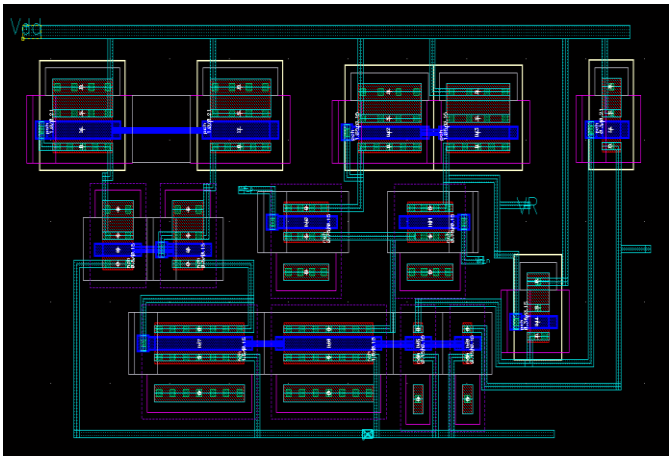


Figure.19: Comparator layout

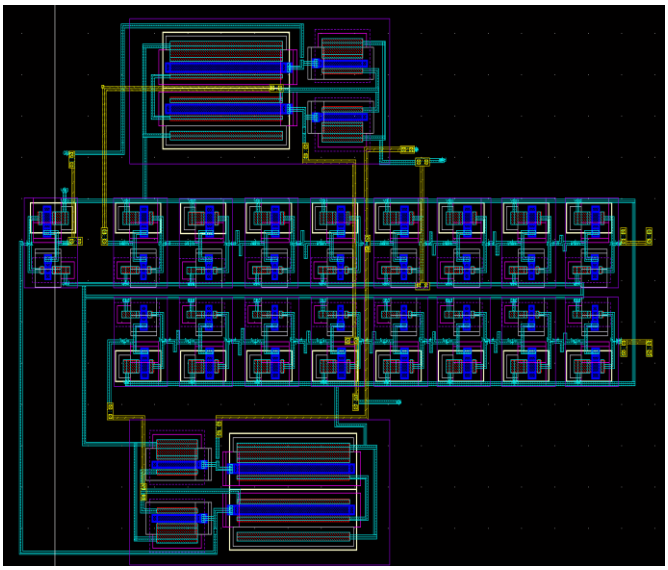


Figure.20: Layout of 4_phase_clock

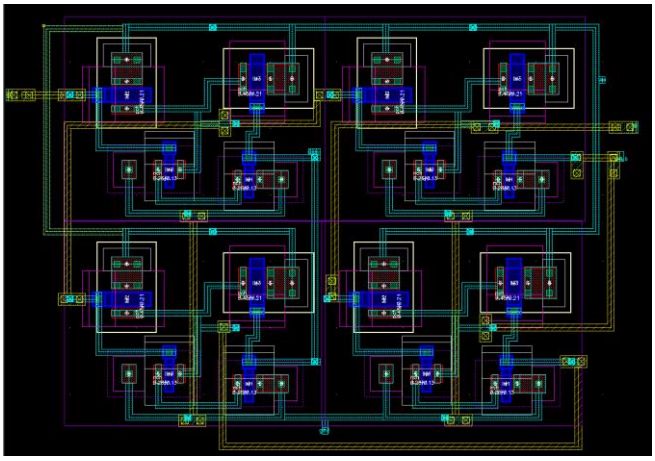


Figure.21: Layout of D_latch

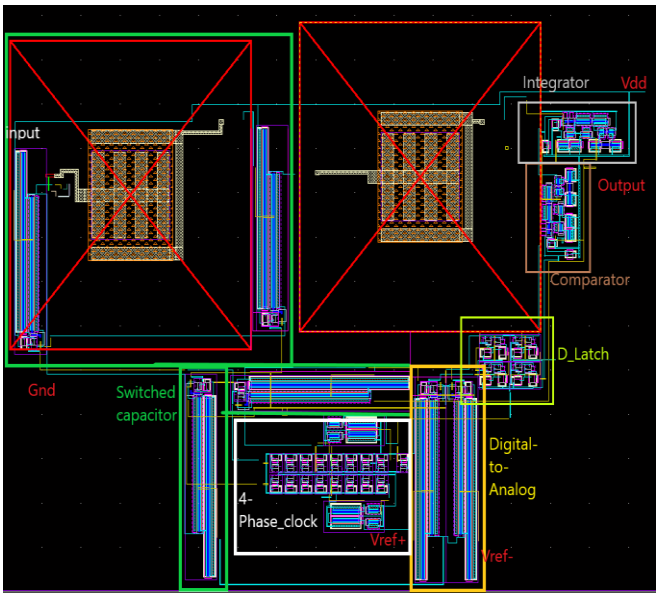


Figure.22: Layout of Sigma delta ADC

VI. PLS SIMULATION

As the layout passes all the checks we moved to extract the parasitic and then simulate the extracted components and we obtained a good and a matching result which is good enough to match the specification. The PSD plot is shown in Fig.19 and the obtained SNR is 54dB approximately. I think the main reason for the decrease of SNR is because of the mimcap we used in the layout. I think we can match the circuit simulation result if we can construct our own capacitors using different layers but the time constraint made us to use the mimcaps.

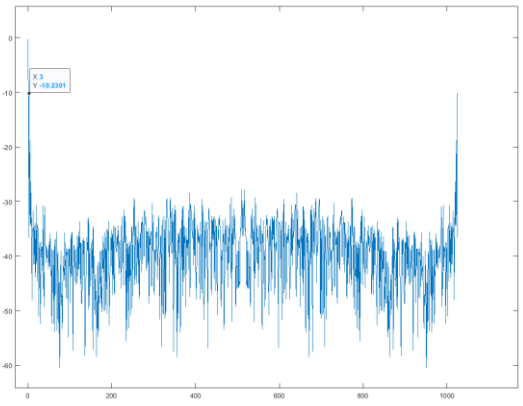


Figure.23: Layout of D_latch

Table II: Results of sigma-delta ADC

Specifications	Matlab	Circuit level	Cadence PLS	Requirement
Power supply (V)	1	1	1	1
bandwidth	18.80 KHz	18.80KHz	18.80KHz	-
SNR	61.71 dB	55dB	53dB	50dB
Power consumption (W)	-	-	≈300µ	-

VII. CONCLUSIONS

To conclude, we have designed a first order, single bit, sigma delta A/D converter using MATLAB and Cadence. The Circuit meets the specification at every level. The output is shown in Fig.20.The power consumption was calculated to be nearly 300 µW. To summarize all the results and as shown in table II, our circuit meets the specification. The paper takes over, initially to the system simulation in section II and we designed algorithm to test the PSD and calculate the SNR, then we moved for circuit level simulation in section III where we came to know that it's better to use 2 phase clock and its very crucial to check your comparator separately [4] and finally we did the layout and PLS simulation in section VI.

In the Fig.24 the library of the cadence which shows the file name and the cell names.

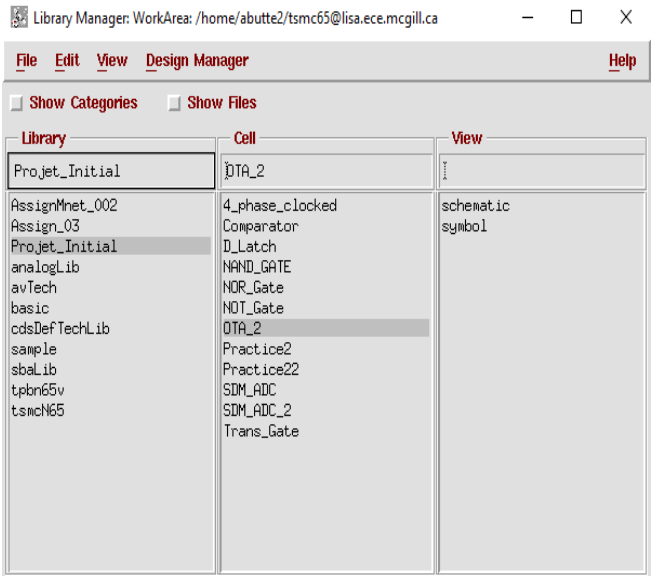


Figure.24: Location of files (/home/abutte2/tsmc65/*)

Some redundant files which I have used for practice are to be ignored like OTA_2 practice2, practice22, SDM_ADC. The complete ADC is SDM_ADC_2 and other files represent the components.

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[1] J. D. Reiss, "Understanding Sigma-Delta modulation: The solved and unsolved issues," J. Audio Eng. Soc., vol. 56, no. 1+2, pp. 49–64, Feb. 2008.

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[3] G. W. Roberts, "An Introduction to Cadence Virtuoso Layout Tool and the Analog Simulation Environment," ECSE 534 CMOS Analog Microelectronics, Tutorial notes, 2016.

[4] G. W. Roberts, "Comparators," ECSE 534 CMOS Analog Microelectronics, lecture 9, 2016.