# ECSE 534 Analog Microelectronics Assignment # 1

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**Abstract—First assignment solution is presented in this paper for analog microelectronics. A CMOS amplifier is designed in 0.65nm CMOS process from TSMC. The design is implemented using the cadence tool and the simulation tools are used to plot the results. Firstly, the topic of amplifier is introduced and the it's implemented in the tool. After that the test bench simulation is explained with the graphs and the schematics.**

***Keywords—IBM 65nm, CMOS amplifier.***

## 1.INTRODUCTION

Amplifiers are essential building blocks of both analog and digital systems. An amplifier is an electronic device that increases the voltage, current, or power of a signal. The amount of amplification provided by an amplifier is measured by its gain: the ratio of output to input [1]. Amplifiers are needed for variety of reasons including: To amplify a weak analog signal for further processing, and to reduce the effect of noise of next stage. The schematic diagram of a CMOS inverting amplifier is shown in Fig.1.

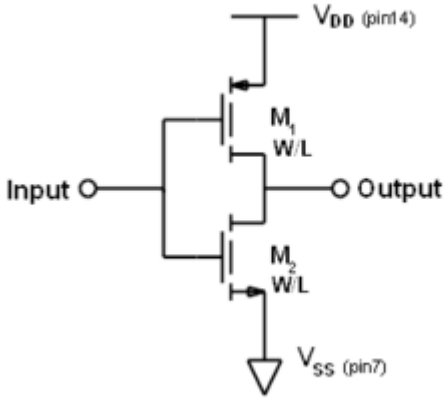


Figure 1: schematic diagram of a CMOS inverting amplifier

## 2. Schematics from cadence

The circuit schematic given in the assignment is fully traced with the given specifications in the cadence schematic tool. To do so, we have to click on Add→ instances, this will pop up the component window where we have to browse the required components to add to the schematic, in this case I have added "nfet" and "pfet" from the "cmrf8sf" library. To modify the parameters of the components we must select the component and then go edit→properties→objects. After adding all the components given in the assignment the schematic will look like, as it's shown in Fig.2.

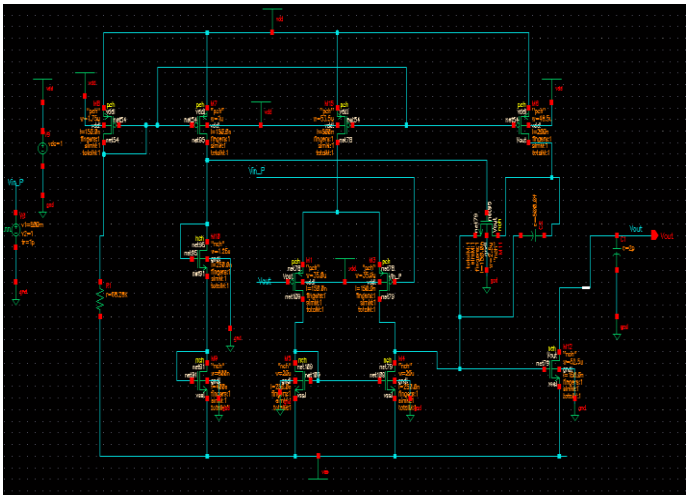

Figure 2: schematic diagram of given CMOS amplifier in cadence

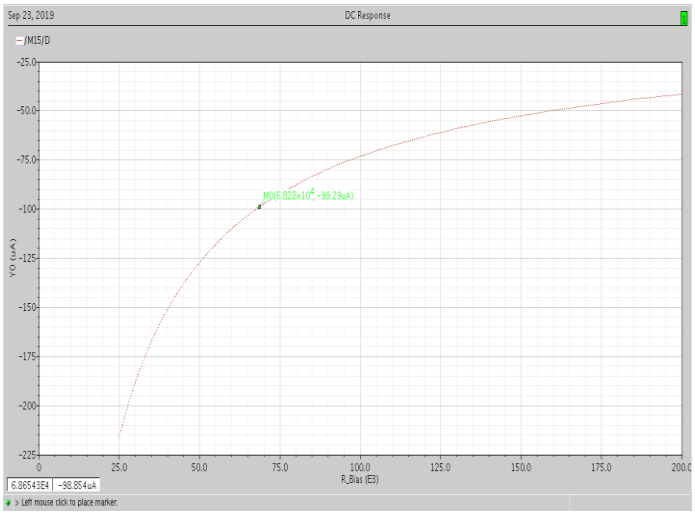


Figure 3: Drain Current Vs R_Bias sweep

To calculate the R_Bias, I sweep the R_Bias and observed the drain current of M5. From Fig.4. the value of R_Bias is 68.28K ohm when the drain current was 99.2uA and that satisfies the condition stated in the assignment.

## 3. DC ANALYSIS

I used cadence tool with analog environment to simulate the circuit and the graphs are plotted. In this section, I have presented all the DC analysis.

### *A. Large Signal, Common Mode (CM) and Differential Mode (DM) Transfer Characteristics*

For Common Mode transfer characteristics, input voltage is swept from -2V to 2V and the change in the output terminal is observed by plotting the simulation which is shown in Fig.4.As seen from the Fig.4.the operating point is calculated to be the middle of the linear region is about 0.62V,wherein the output voltage is about 0.9V and its highlighted in with the green marker.

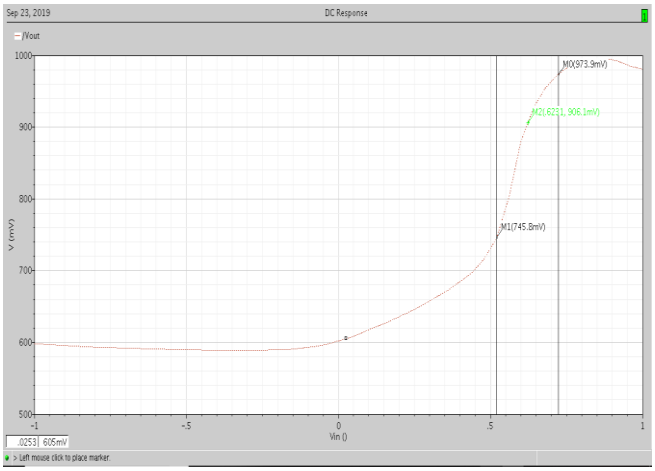


Figure 4: CM transfer characteristics

For a DM the input and output offset are shown in Fig.5. wherein M1 represents the input offset voltage which is 31.5mV whereas M0 is output offset voltage which has the value of 0.91V. The offset voltage is nothing but the difference between the input and output voltages from the ground level.

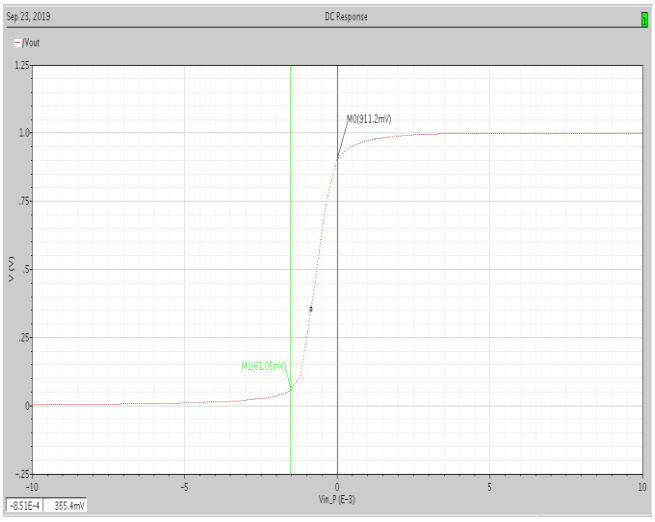


Figure 5: DM transfer characteristics

### *B. voltage ranges:*

To calculate the input and output voltage range I have used the DM simulation results which is shown in Fig.6. and as seen from the figure the input range is from -1.3mV to nearly 0.1mV and the output voltage ranges from 61mV to 911mv.

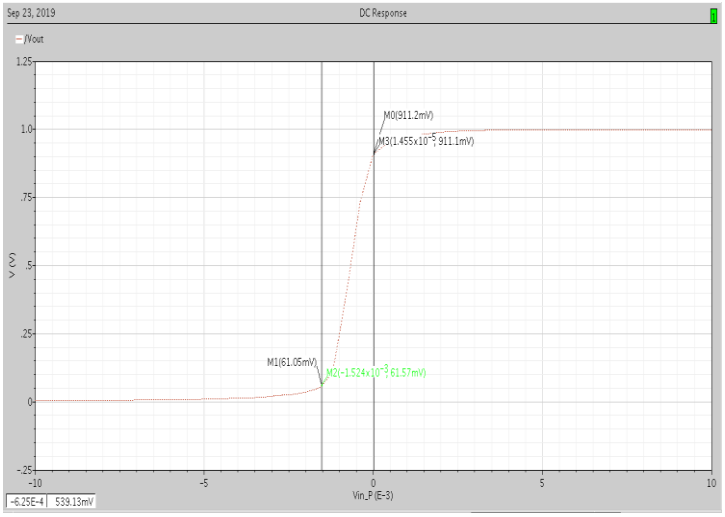


Figure 6: Voltage range

## 4. AC ANALYSIS

### *A.CM and DM Low Frequency Gain*

Fig.6 shows the DM characteristics and the marker shows the values of the parameters. LF gain is about 36.8dB and 3-dB bandwidth is 462.8kHz

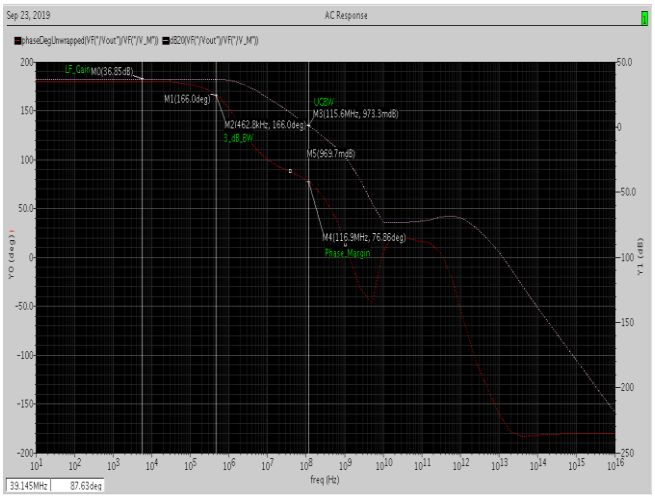


Figure 6: DM LF gain, UGBW and phase margin.

Similarly, for CM configuration the graph is shown in the Fig. 7. And the LF gain is 74.47dB with 1.12kHz of 3_dB bandwidth.

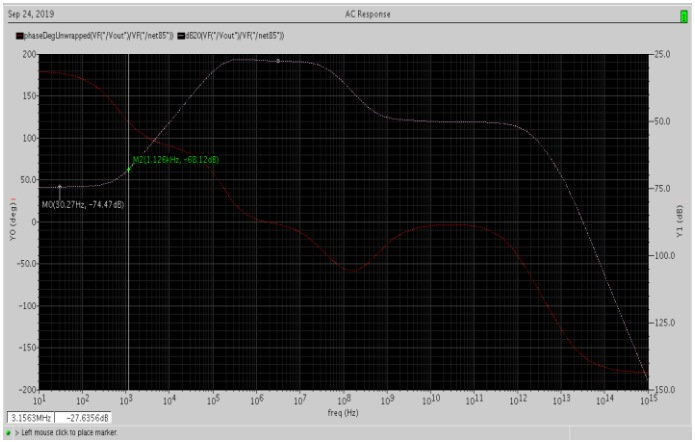


Figure 7: DM LF gain, UGBW and phase margin.

*B.unity-gain bandwidth (UGBW) and phase margin*

As seen from the Fig.6 and Fig. 7 we can see that the unity gain bandwidth for DM is 115.6Mhz and the phase margin is -103.14 degree.

*C.pole-zero*

Cadence provides a summary of poles and zeros of the circuit within a certain frequency range. We just have to d0 pz analysis for a certain range of frequency to see the results in the print option of the result. Fig.8 shows these poles and zeros [2].

Poles(Hz)

| | Real | Imaginary | Qfactor |
|---|---|---|---|
| Pole_1 | -1.697e+03 | 0.000e+00 | 5.000e-01 |
| Pole_2 | -4.499e+04 | 0.000e+00 | 5.000e-01 |
| Pole_3 | -5.402e+04 | 0.000e+00 | 5.000e-01 |
| Pole_4 | -1.005e+05 | 0.000e+00 | 5.000e-01 |
| Pole_5 | -6.845e+05 | 0.000e+00 | 5.000e-01 |
| Pole_6 | -6.047e+07 | 0.000e+00 | 5.000e-01 |
| Pole_7 | -3.790e+08 | 0.000e+00 | 5.000e-01 |
| Pole_8 | -8.035e+08 | 0.000e+00 | 5.000e-01 |
| Pole_9 | -9.758e+11 | 0.000e+00 | 5.000e-01 |

Zeros(Hz)

| | Real | Imaginary | Qfactor |
|---|---|---|---|
| Zero_1 | -7.756e+01 | 0.000e+00 | 5.000e-01 |
| Zero_2 | -3.086e+04 | 0.000e+00 | 5.000e-01 |
| Zero_3 | -9.827e+04 | 0.000e+00 | 5.000e-01 |
| Zero_4 | -1.891e+05 | 0.000e+00 | 5.000e-01 |
| Zero_5 | -6.788e+05 | 0.000e+00 | 5.000e-01 |
| Zero_6 | -6.484e+07 | 0.000e+00 | 5.000e-01 |
| Zero_7 | -2.635e+08 | 0.000e+00 | 5.000e-01 |
| Zero_8 | -8.188e+08 | 0.000e+00 | 5.000e-01 |
| Zero_9 | -8.039e+11 | 0.000e+00 | 5.000e-01 |

Network function gain(magnitude)= 1.528e-03

Figure 8: Pole-Zero analysis result

*A. spectral noise spectral and RMS thermal noise level.*

As we can see from the Fig.9 and Fig.10 the input and output spectral noise is inversely proportional to the frequency. The thermal noise can also be calculated using the calculator tool in the graph window. But here I have used a simpler result window that displays the thermal noise.

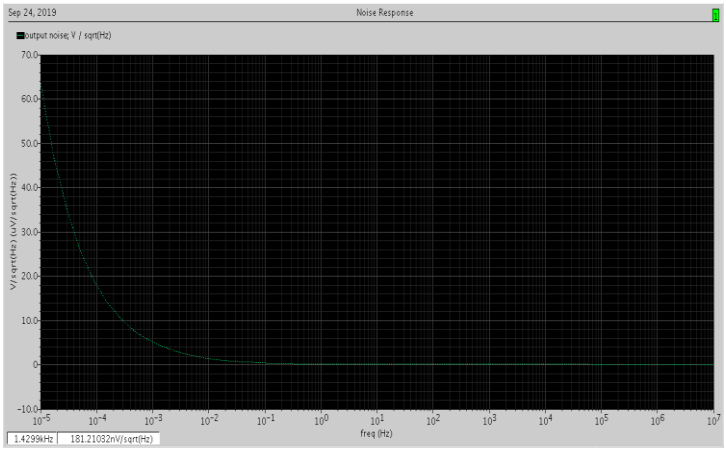


Figure 9: Curve of output spectral noise

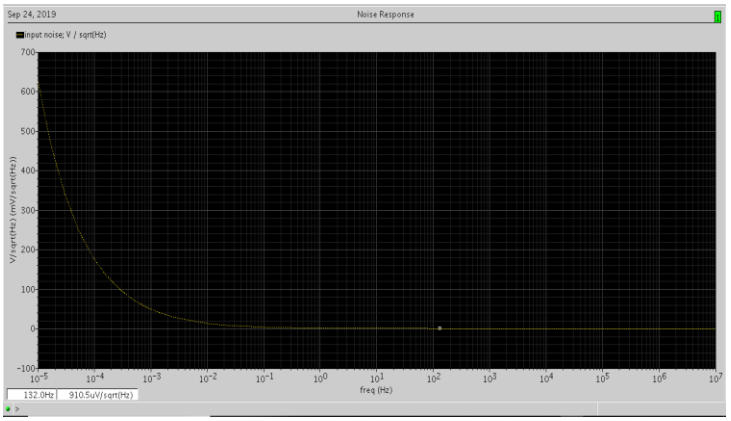


Figure 10: Curve of input spectral noise

Window Expressions Info Help 47

| Device | Param | Noise Contribution | % Of Total |
|---|---|---|---|
| /M6 | id | 3.22321e-14 | 98.04 |
| /M12 | igd | 2.11587e-16 | 0.64 |
| /M8 | id | 1.33363e-16 | 0.41 |

Spot Noise Summary (in V^2/Hz) at 1K Hz Sorted By Noise Contributors
Total Summarized Noise = 3.28773e-14
Total Input Referred Noise = 2.82669e-08
The above noise summary info is for noise data

Figure 11: Total RMS value of spectral noise

## 4. Transient Analysis

The transient simulation is the calculation of a network's response on arbitrary excitations. The results are network quantities (branch currents and node voltages) as a function of time. This analysis is time window analysis and one of the main analysis to understand and verify any circuit whether the circuit is giving the expected output or not. The transient analysis

attempts to find an approximation to the analytical solution at discrete time points using numeric integration

*A.Slew rate,*

slew rate is defined as the change of voltage or current, or any other electrical quantity, per unit of time. the slew rate specification guarantees that the speed of the output signal transition will be at least the given minimum, or at most the given maximum. When applied to the input of a circuit, it instead indicates that the external driving circuitry needs to meet those limits in order to guarantee the correct operation of the receiving device. If these limits are violated, some error might occur and correct operation is no longer guaranteed. Its calculated by the slope of the output wave when a pulse wave is applied at the input terminal. If you calculate the slope of this curve, then the slew rate is about 70.2 $v|\mu s$.

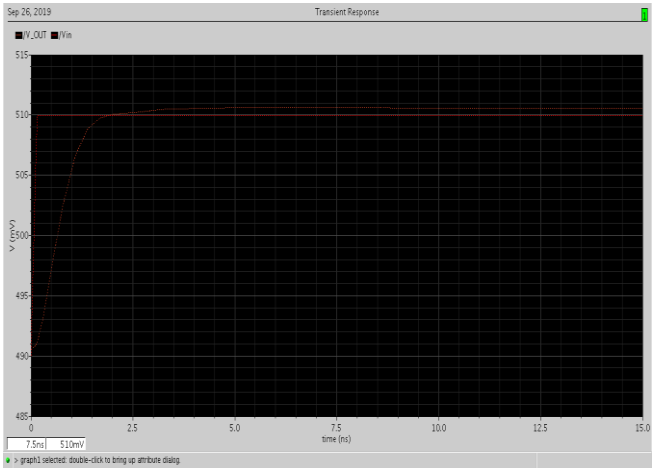


Figure 12: Slew Rate

*B.Rise/settling time, and maximum input/output swing*

The settling time of an amplifier is defined as the time it takes the output to respond to a step change of input and come into, and remain within a defined error band, as measured relative to the 50% point of the input pulse. rise time is the time taken by a signal to change from a specified low value to a specified high value. As seen from the Fig.13the output takes about 1.42ms to reach the steady state level. The Maximum swing is obtained by sweeping the input in the DC analysis and observing the output with respect to input voltage.

*C.Distortion behavior to sinusoidal CM and DM signals*

Amplitude distortion occurs when the peak values of the frequency waveform are attenuated causing distortion due to a shift in the Q-point and amplification may not take place over the whole signal cycle. The distortion behavior of the system can be presented by the Thermal Harmonic Distortion (THD). Cadence provides tools to calculate the THD.

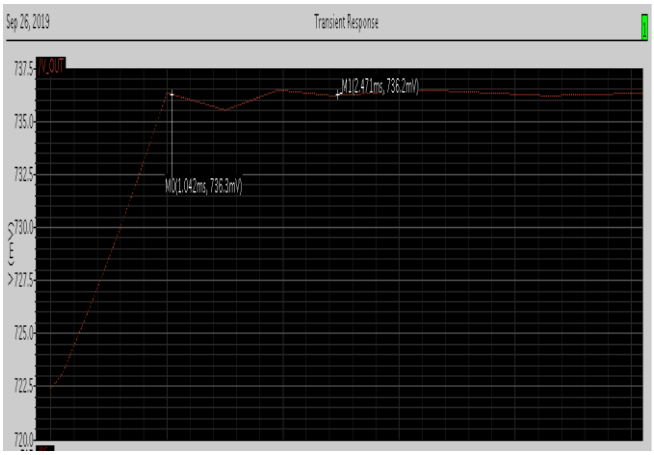


Figure 13: Rise/Setting time

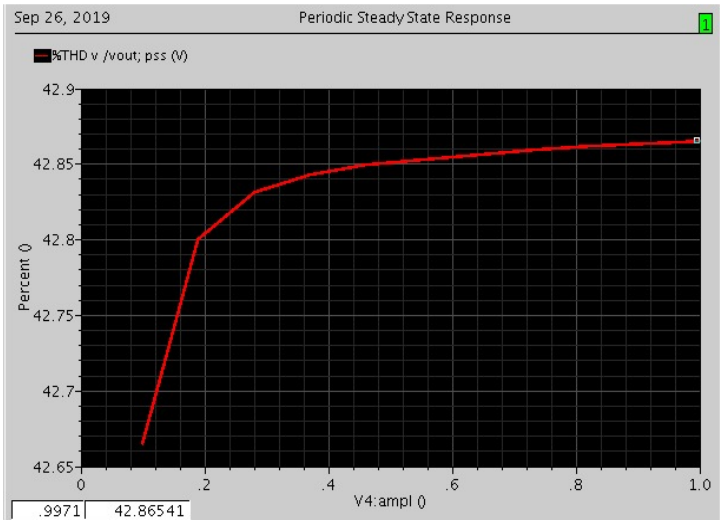


Figure 14: DM THD result

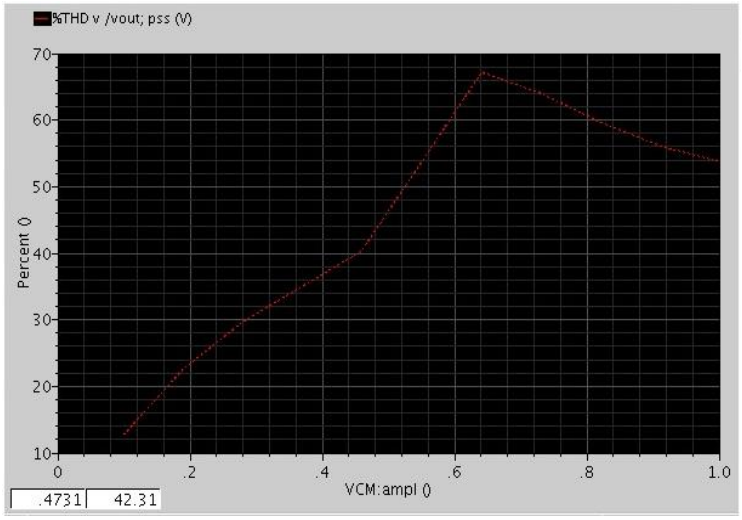


Figure 15: CM THD result

## 5. CONCLUSION

This paper presents the simulation results of the 65nm technology using the cadence tool in the analog environment. All the different analysis has been implemented i.e., AC, DC, and Transient and the important characteristics have been plotted. Table 1 below summaries the results.

Table 1: Summery of the results.

| Analysis | Parameters | Value | unit |
|---|---|---|---|
| DC | R_bias | 68.28 | K ohm |
| | Input Offset Voltage | 31.5 | mV |
| | Output Offset Voltage | 0.91 | V |
| | Range of Vin | -1.3 to 0.13 | mV |
| | Range of VO | 61 to 911 | mV |
| AC | CM LF gain | 74.47 | dB |
| | CM 3-dB frequency | 1.12 | kHz |
| | DM LF gain | 36.8 | dB |
| | DM 3-dB frequency | 462.8 | kHz |
| | UGBW | 115.6 | MHz |
| | Phase margin | -103.14 | Degrees |
| | Total RMS Thermal noise | 3.28x10-10 | V2/Hz |
| Transient | Slew rate | 70.2 | V/µs |
| | Rising/settling time | 1.42 | ms |

## REFERENCES


[1] Behzad Razavi: 'Design of Analog CMOS Integrated Circuits', (McGraw-Hill Publisher, New York, 2001), p.p. 291.

[2] G. W. Roberts, ECSE 534 Analog Microelectronics Course Notes, McGill University.