THREE-STAGE CMOS OPERATIONAL TRANSCONDUCTANCE AMPLIFIER Assignment # 2

Arun Arun 260881882
M.Eng. Student, McGill University
Arun.butte@mail.mcgill.ca

Abstract—Three stage OTA is presented in this paper where the first stage is a differential input stage and to increase the gain, two additional common source stages are added. This is implemented in 65nm technology in cadence. This OTA has a supply of 1v and all the transistors in the circuit as biased such that they are in saturation to achieve a gain of approximately 67dB with static power consumption of 41µA.

Keywords—Three stage, OTA, gain, power consumption.

I. INTRODUCTION

Amplifiers are essential building blocks of both analog and digital systems. An amplifier is an electronic device that increases the voltage, current, or power of a signal. The amount of amplification provided by an amplifier is measured by its gain: the ratio of output to input [1]. The operational transconductance amplifier (OTA) is an amplifier whose differential input voltage produces an output current. Thus, it is a voltage controlled current source (VCCS). There is usually an additional input for a current to control the amplifier's transconductance. The OTA is like a standard operational amplifier in that it has a high impedance differential input stage and that it may be used with negative feedback. The schematic diagram is shown in Fig.1.

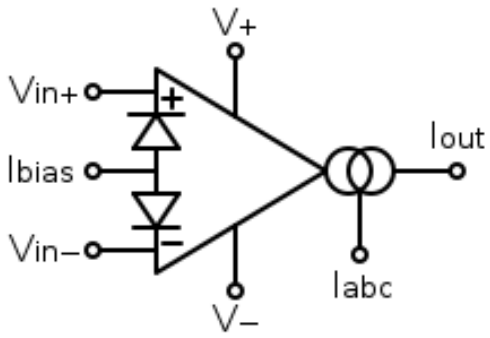

Figure 1: schematic diagram of OTA

True that single stage OTAs provide potential replacement of multistage architecture and indeed the dominant pole of C_L will help for the frequency compensation. Single stage OTAs provide limited DC gain and which cannot be increased by vertically stacking transistors on one another. So, in this case we have to adopt two stage or three stage OTAs depending on the gain requirement[2]. Increase the stages will cost us on handling the complex poles and zeros, circuit complexity, area consumption and noise will eventually increase[3].

The schematic will look like, as it's shown in Fig.2.As its seen, it has a differential pair as the first stage which will give most of the circuits gain. The other two stages added after that will boost the gain of the circuit to meet the requirement. The pole and zeros are placed as per the requirement using a capacitor and a resistor[4]. The circuit is biased in such a way that all the transistors are in saturation (region 2). The circuit is biased such that a current source of 15µA is injected into the diff pair using two transistors as shown. The other transistors are biased with the same voltage as the diff pair is biased. The other two stages are biased by using width as the only degree of freedom. To place the poles and zeros, a capacitor and a resistor connected between output of diff pair to the output of the third stage. The Diff pair has the current mirror which will help the circuit to supply with the same current.

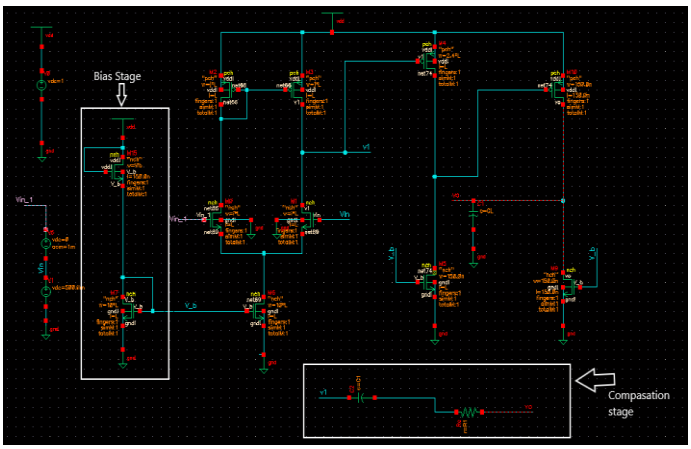

Figure 2: schematic diagram of given CMOS amplifier in cadence

In this paper, the achieved DC gain is 67dB with phase margin of 64deg, input referred noise is 32nV/sqrt(Hz) and static power consumption of 41µA with input of 0.5V and supply voltage of 1v.The simulation are carried out in 65nm technology using cadence. Table I gives the transistor W/L ratio and the value of all the components used. Here the value of length is taken around 150nm for all the transistors.
The DC analysis is presented in section II. AC analysis and the Transient analysis are presented in sections III and IV,

respectively, while section V concludes the work presented in this report.

Table 1: W/L of all components

Stage	Device	Ratio	W in nm	L in nm
Diff Pair	M0, M1	5	750	150
	M2, M3	7	1050	150
Third stage	M4	2.4	360	150
	M5	1	150	150
Second stage	M9, M10	1	150	150
Bias Stage	M15	1.41	212	150
	M7	10	1500	150
	M6	10	1500	150

II. DC ANALYSIS

A. voltage offset

The input offset voltage is defined as the voltage that must be applied between the two input terminals of the op amp to obtain zero volts at the output. Ideally the output of the op amp should be at zero volts when the inputs are grounded. In reality, the input terminals are at slightly different dc potentials. This can be calculated by sweeping the input voltage and observing the change in the output. As it is seen from Fig.5 the offset voltage if 17mv and the input and output voltage ranges are marked in the Fig.5 as well.

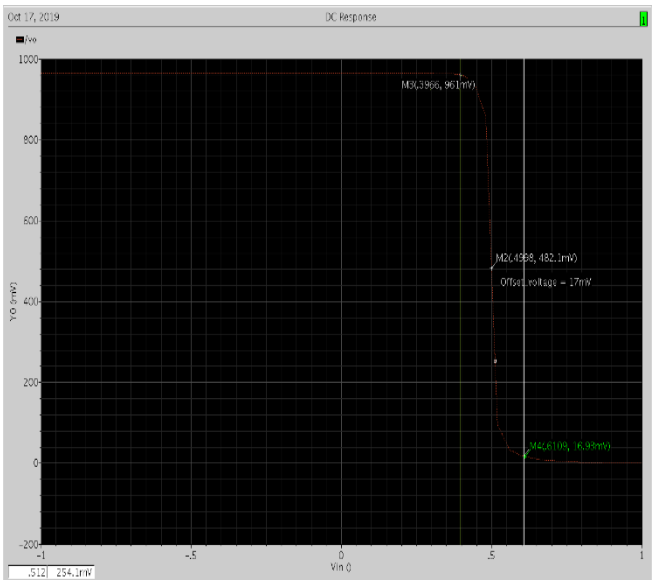

Figure 3: Voltage range

B. large-signal transfer characteristics

For Common Mode transfer characteristics, input voltage is swept from -2V to 2V and the change in the output terminal is observed by plotting the simulation which is shown in Fig.4 which is like Fig.3.

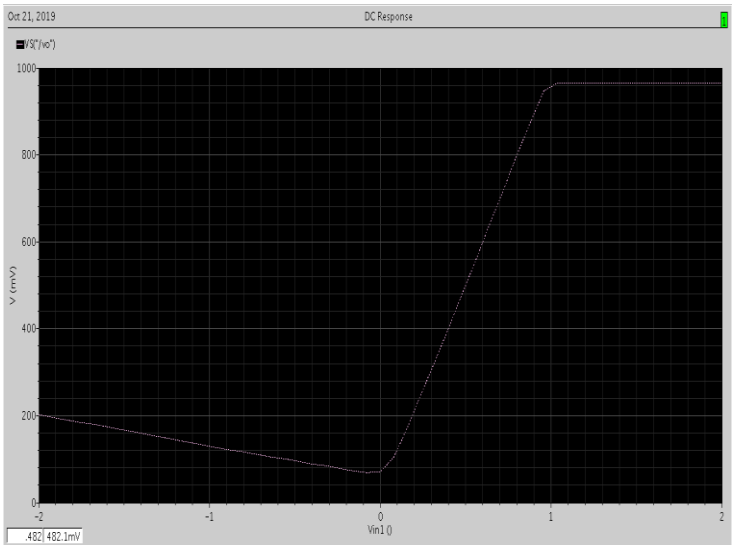

Figure 4: transfer characteristics

III. AC ANALYSIS

A. DC gain, unity-gain frequency

The AC parameters, which are the DC gain, UGBW and the phase margin, can be seen in Fig.5 which are 67dB of DC gain with 64degress of PM and 101MHz. AC analysis is simulated and then the curve is plotted using Ac gain and phase option in the result window.

B. 3-db bandwidth

The 3_dB plot is also plotted using the same way and the results are shown in Fig.6.

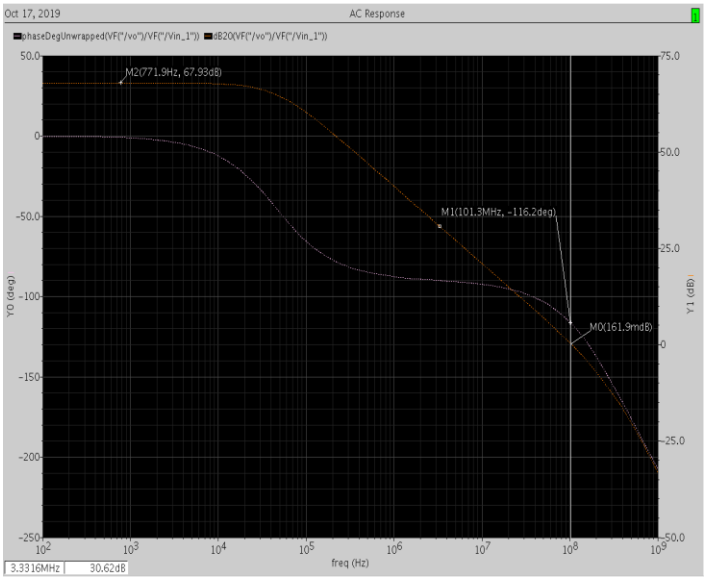

Figure 5: DC gain, UGBW and PM

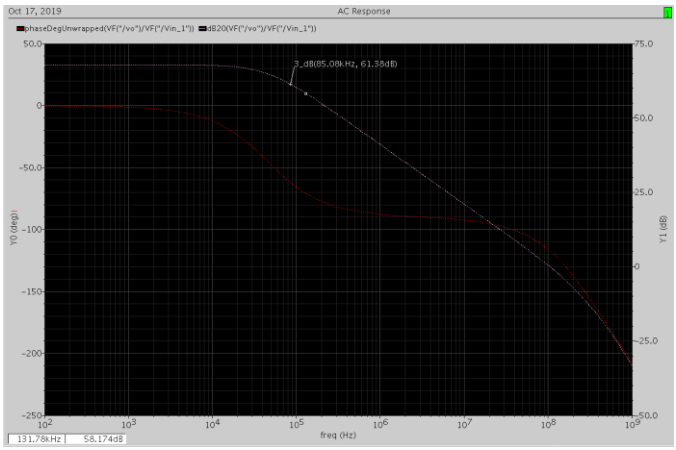

Figure 6: 3-dB bandwidth

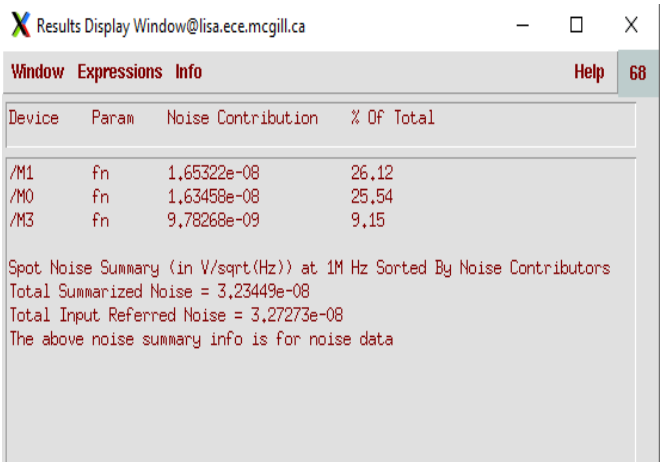

Figure 8: total Input referred Noise

C. Input-referred PSD Noise Voltage

Input referred noise is used to determine the noise contribution of the circuit when it is used in a system. It gives a useful frame of reference. A circuit with a lower input referred noise will contribute less noise to overall system than one with a higher input referred noise. Its calculated by the option of noise in the result option where one can plot it as shown in Fig.7. As shown in Fig.8 it can been seen that the input referred noise is 32nV/sqrt(Hz).

D. The pole-zero locations

Placed of poles and zeros becomes where much complicated as you increase the number of stages in the circuit and even it can have complex values. To place them in the appropriate negative plane to make the circuit more stable, I used a capacitor and the resistor. Finally, I was able to place them at the negative plane by appropriately selecting the values of load and compensation capacitor. The first pole is at -45KHz and the second one is at -264MHz and these approximately meets the requirements as can be seen from Fig.9.

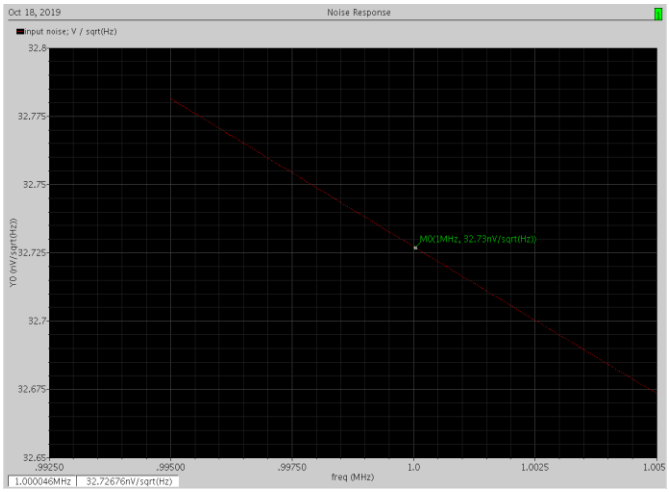

Figure 7: Input referred Noise

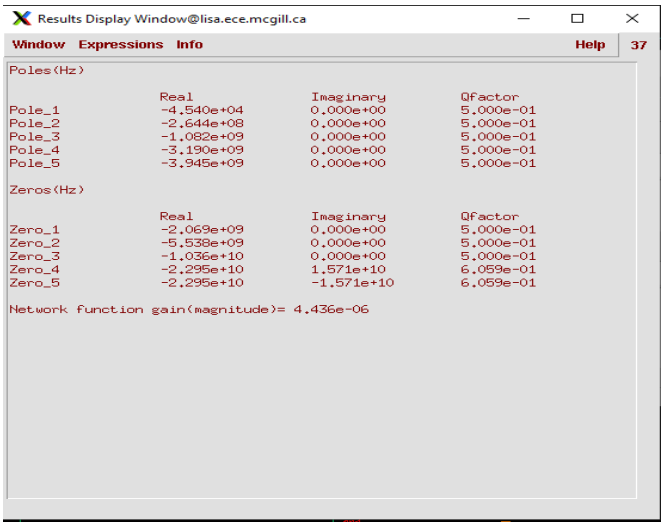

Figure 9: List of the pols-zero positions

IV. TRANSIENT ANALYSIS

The transient simulation is the calculation of a network's response on arbitrary excitations. The results are network quantities (branch currents and node voltages) as a function of time. This analysis is time window analysis and one of the main analysis to understand and verify any circuit whether the circuit is giving the expected output or not. The transient analysis attempts to find an approximation to the analytical solution at discrete time points using numeric integration

A. Rise and Settling Times

The settling time of an amplifier is defined as the time it takes the output to respond to a step change of input and come into, and remain within a defined error band, as measured relative to the 50% point of the input pulse. rise time is the time taken by a signal to change from a specified low value to a specified high value. As seen from Fig.10 the rise and setting time is calculated by calculator tool as is shown in Fig.11 and Fig.12 respectively.

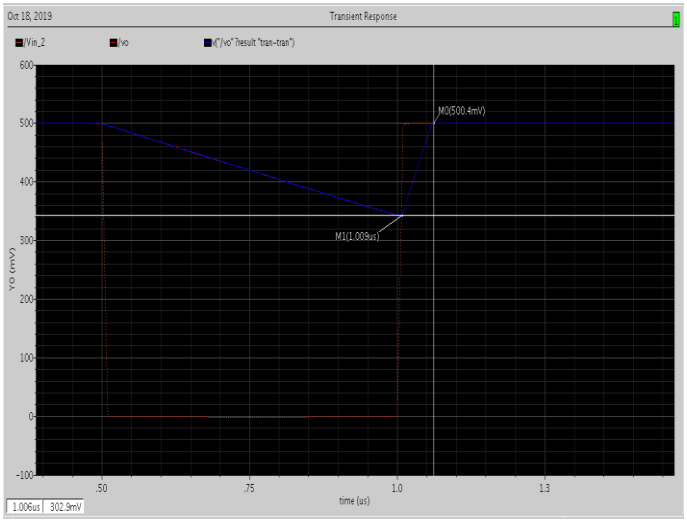

Figure 10: Rise/Setting time

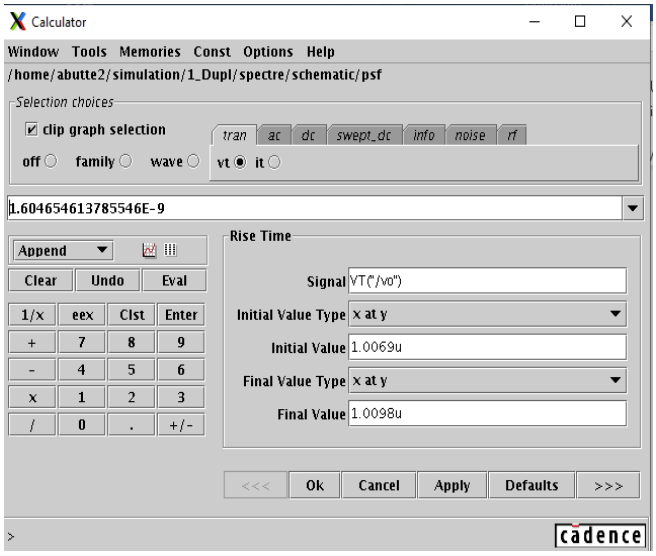

Figure 11: Rise time calculation

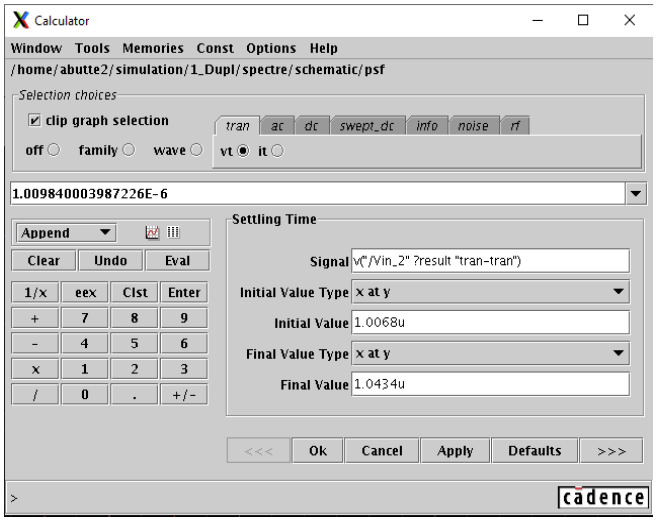

Figure 12: Settling time calculation

As seen, rise time is 1.6ns and the setline time is 1μs.

B. Maximum Swing

The Maximum swing is obtained by sweeping the input in the DC analysis and observing the output with respect to input voltage and is shown in Fig.13 and it can be seen that the output voltage swings from 74mv to 960mv.

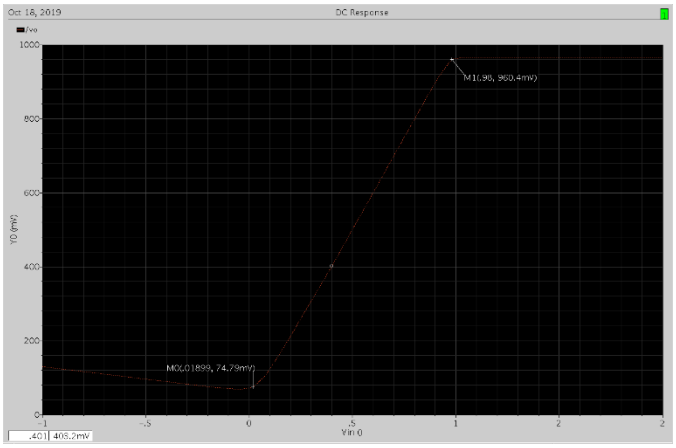

Figure 13: Maximum Swing

C. Distortion

Amplitude distortion occurs when the peak values of the frequency waveform are attenuated causing distortion due to a shift in the Q-point and amplification may not take place over the whole signal cycle. The distortion behavior of the system can be presented by the Thermal Harmonic Distortion (THD). The distortion is calculated and is shown in Fig.14 and Fig.15 explains the calculations which gives the distortion of 0.13 (V/V) which meets our specification. In Fig.16 THD curve is plotted with respect to different input values.

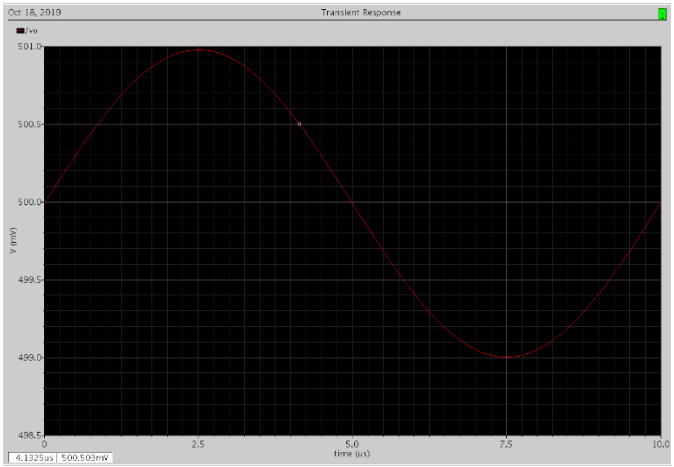

Figure 14: THD calculation curve

D. Static power dissipation

The small amount of static power consumption due to reverse-bias leakage between diffused regions and the substrate. Static

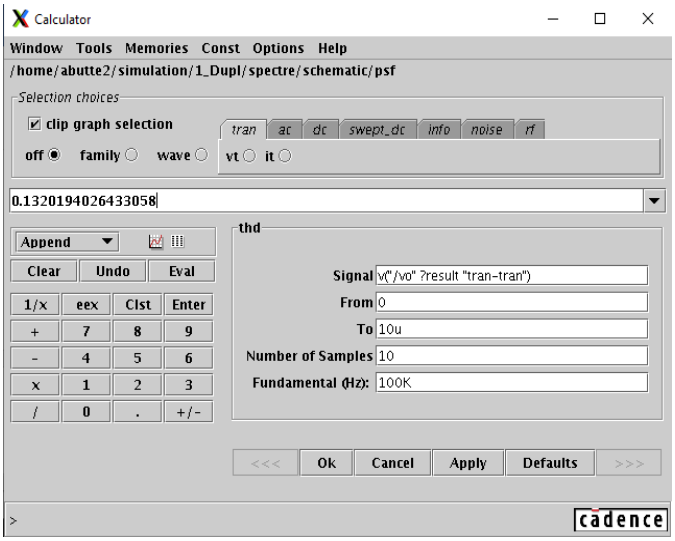

Figure 15: THD calculation

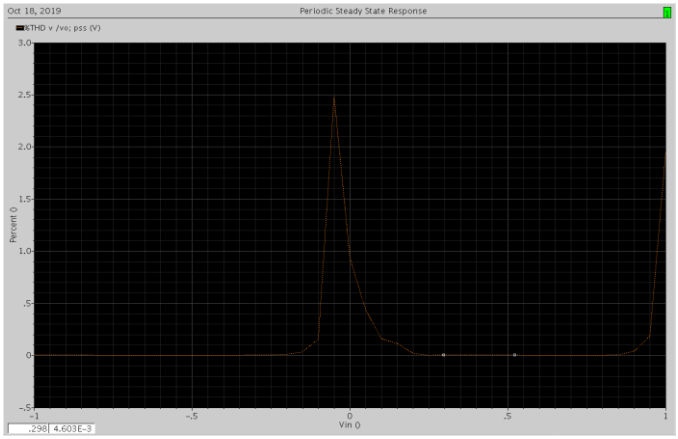

Figure 16: THD percentage curve

power consumption is the product of the device leakage current and the supply voltage. Total static power consumption, PS, can be obtained as shown in equation 1.

PS = (Current through VDD) × (supply voltage) (1)

As the supply voltage in the design is 1v so the power consumption is 41.92 µA as it's shown in the Fig.17 that the current flowing in the VDD is 41.92 µA and the power consumption is calculated using the formula in equation (1).

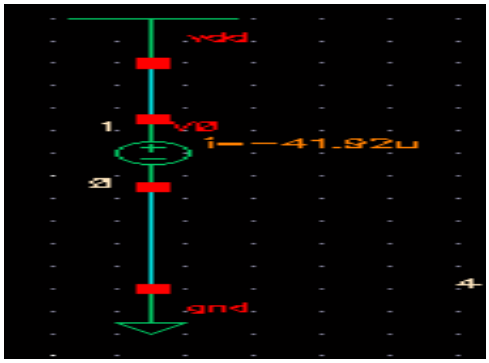

Figure 17: Power consumption calculation

V. Monte-Carlo simulations

The small random variations (Device Mismatch) in the characteristics of identically designed devices, occur during the manufacturing of ICs. These mismatches result in behavior change of ICs. It is difficult to predict the behavior of a circuit due to the combination of the mismatch errors of individual devices. The impact of these random parameter variations on circuit behavior can be studied with Monte Carlo simulation by analyzing a large set of circuit instantiations with randomly varied devices. The result of this simulation is plotted for count Vs gain as shown in Fig.18.

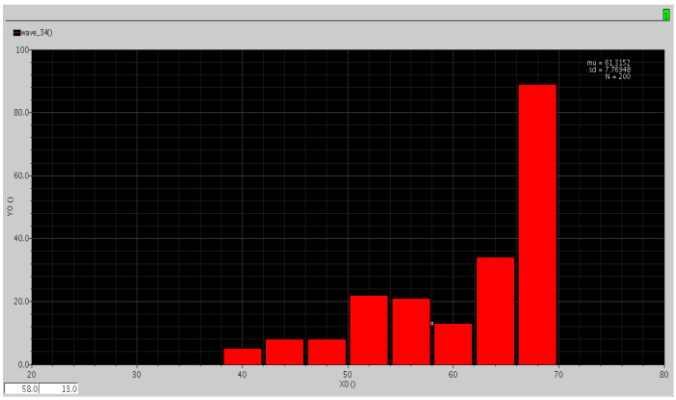

Figure 18: count Vs gain

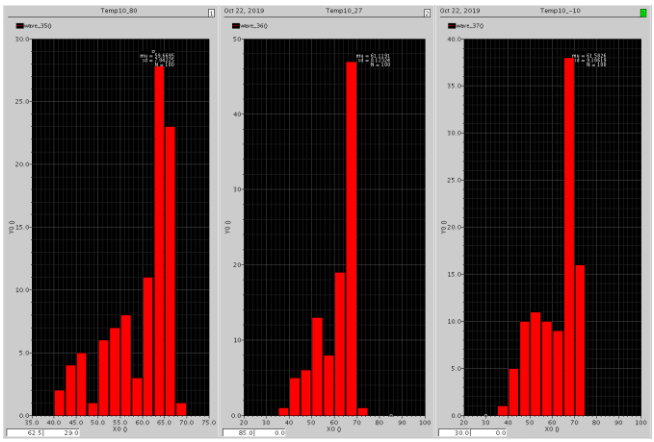

Figure 19: Histogram of three Temperature

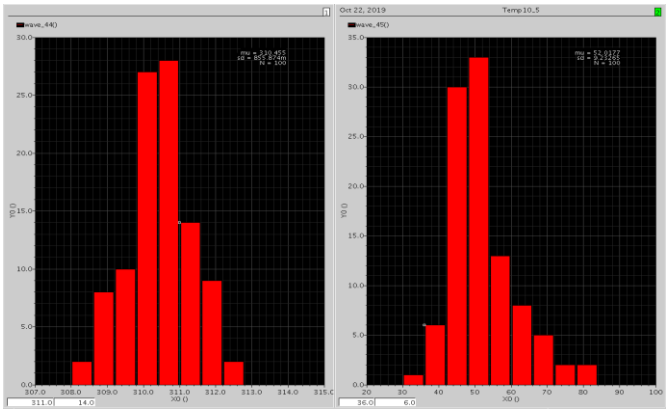

Figure 20: Histogram of supply voltages

As depicted in Fig.19. its monte carlo simulation for three different temperatures i.e. 10°C, 27°C and 80°C and Fig.20 shows the simulation of different supply variations of 5%.

VI. CONCLUSION

This paper presents the simulation results of the 65nm technology of three stage OTA using the cadence tool in the analog environment. All the different analysis has been implemented i.e., AC, DC, and Transient and the important characteristics have been plotted. Table 2 below summaries the results.

Table 2: Summery of the results.

Parameter	Specification	This work
DC gain	≥ 60 dB.	67dB
Amplifier poles	approx. 10 kHz and 100 MHz	-45KHz and -264MHz
Distortion	0.20%	0.13
Input-referred PSD Noise Voltage	< 100 nV/sqrt(Hz)	32nV/sqrt(Hz)
Static power dissipation	< 200 µW	41.92 µA

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