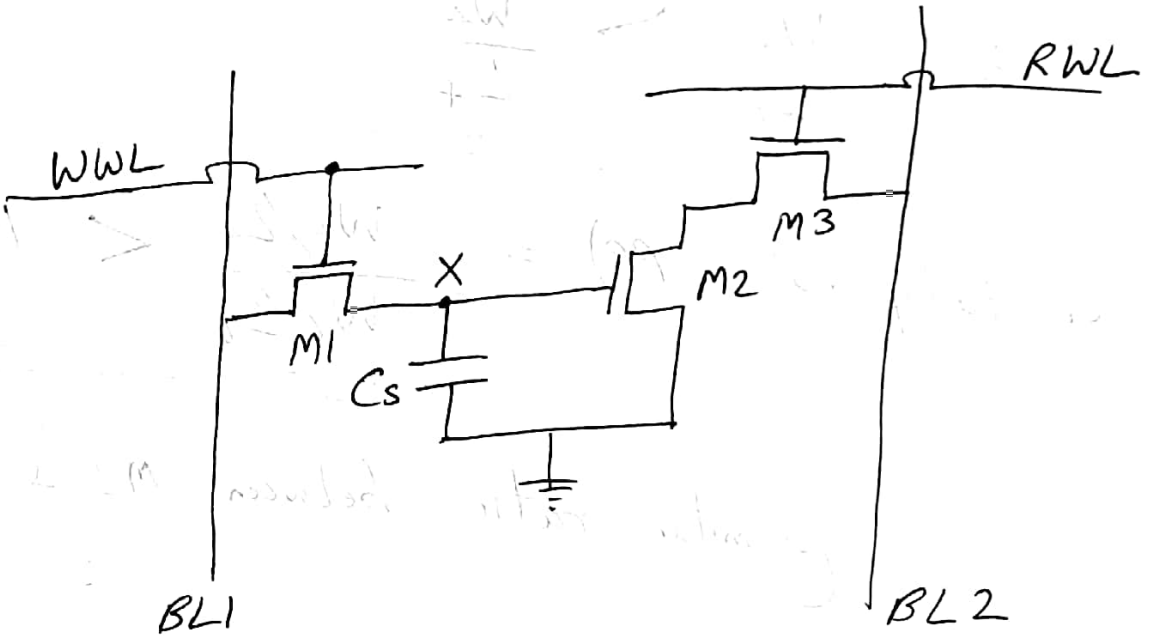
DRAM (Dynamic RAM)

→ Data is stored in the form of charge stored in a capacitor. Since, this charge can decrease over time due to leakage, it is called dynamic RAM.

→ Periodic refreshing is required to maintain data inside DRAM.

3-Transistor DRAM cell



→ Logic 1 ⇒ Cs is charged
Logic 0 ⇒ Cs is discharged.

WWL → Write Word Line

RWL → Read Word Line

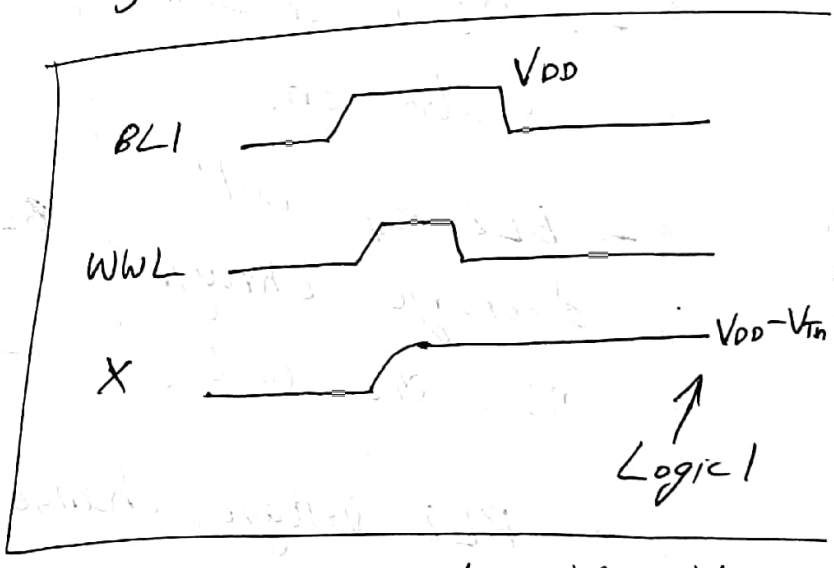
→ BL1 is used to write data into cell & BL2 is used to read data from cell.

Write operation

→ Assume that 0 is stored in cell. So voltage at X = 0 V.

→ We want to write 1 into the cell.

→ BL1 is made high (VDD) & then WWL is enabled. (RWL = 0).



→ M1 turns on & Cs charges towards VDD.

→ Max voltage that can be stored = $V_{DD} - V_{Tn}$ (Threshold of M1)

→ At this time, even though gate voltage of M2 is high current will not flow because M3 is off & hence there is no connection.

→ Similarly, to write 0 to the cell, BL1 is made 0 & WWL is enabled, thus turning on M1. So Cs will discharge to 0.

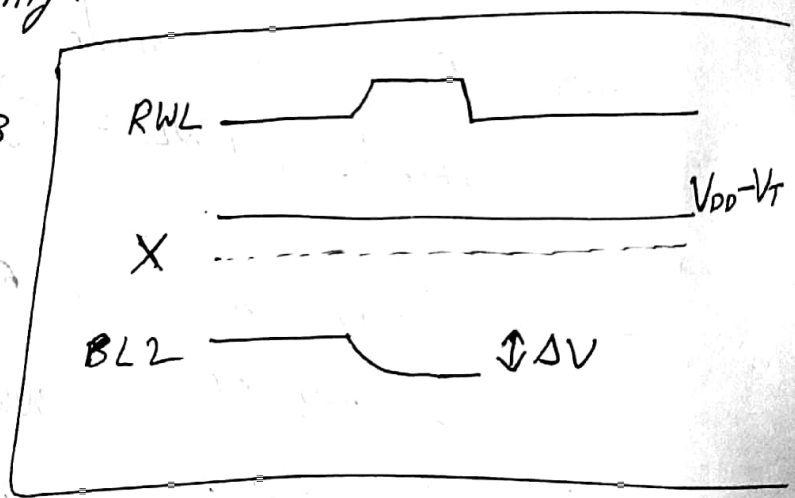
Read operation

→ Assume that a 1 is stored in cell.

→ BL2 is precharged to V_{DD} & RWL is ~~enable~~ made high.

→ M2 is on & M3 is also on.

→ BL2 ~~cap~~ will discharge through M3 & M2 to 0.



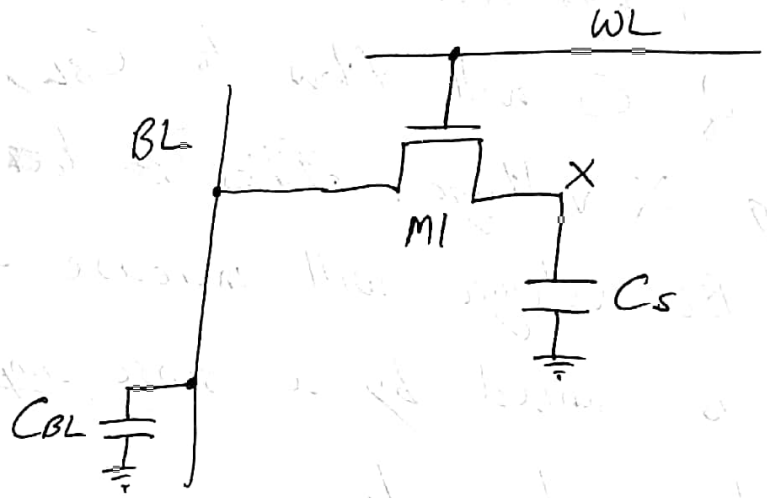
→ BL2 voltage change is sensed. If BL2 decreases, it is recognized as logic 1.

→ Instead, if 0 was stored in cell, then M2 will be off. So BL2 cannot discharge. So it will be read as logic 0.

Refresh operation

→ Data is read from the cell & it is again written back to the cell through write operation. This must take place at a certain frequency such that data do not get corrupted.

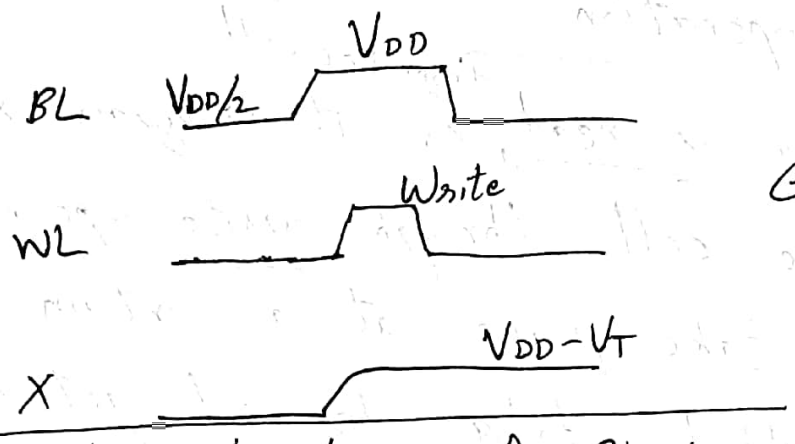
One-Transistor DRAM cell



→ Write operation

→ Assume that 0 is stored in cell. So capacitor is not charged.

→ To write a 1 into the cell, BL is made high(V_{DD}) & M1 is turned on using WL. So Cs charged through M1, thus storing 1.



← Write operation

→ Similarly, to store a 0, BL is made 0 & M1 is turned on.

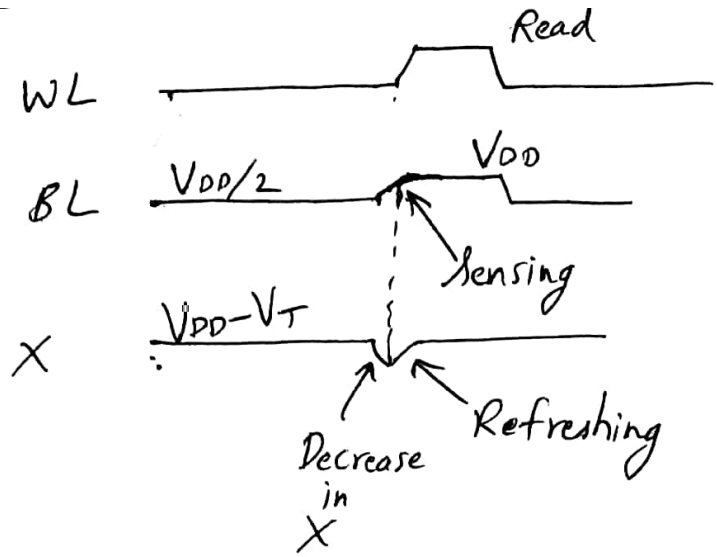
Read operation

→ BL is precharged to $V_{DD}/2$ & WL is enabled.

→ Assume that 1 was stored in cell. Then some charge of C_S will flow to C_{BL}, thus reducing X voltage. ~~This decrease in X~~ So BL voltage will increase & this increase is sensed by a sense amplifier. It is recognized as logic 1.

Since there is a decrease in X voltage associated with read (destructive readout), a refresh operation should be done along with read.

→ ~~Instead~~



Read operation of logic 1

→ Instead, if logic 0 was stored in cell, the BL will decrease upon read & this will be sensed as logic 0.