Ext. No. 1

Date: 23 / 5 / 22

CLIPPING AND CLAMPING CIRCUITS

AIM:

To design and setup clipping and clamping circuits and to plot their waveforms and transfer characteristics

COMPONENTS REQUIRED:

Resistor of 10kΩ, Diode (IN4007), Capacitor, Voltage sources, signal generator, breadboard

THEORY:

The property of a diode as a switching device is utilised in clipping circuits. Clipping circuits are linear wave shaping circuits. They are useful to clip off the positive or negative portions of an input waveform. It can also be used to slice off an input waveform between two voltage levels. The diode clippers can be classified as series and shunt clippers. If the diode is connected in series with input in a clipper, such a clipper is called series clipper. If the diodes are connected in parallel with the input, that clipper is called a shunt clipper. Shunt clippers are discussed in the following session

A resistance is used to limit the current in the diode. The value of series resistance used in the clipping circuits are given by the expression $R = \sqrt{R_f \times R_r}$

where R_f = forward resistance of the diode

R_r = reverse resistance of the diode.

1. Positive clipper at clipping level at 0V :

This circuit passes only negative going half waves of the input to the output till the positive half cycles are bypassed through the diode since the diode gets forward biased when the input voltage becomes positive Due to the voltage drop across the diode the clipping occurs exactly at 0.6 V.

2. Negative clipper at 0V :

This circuit passes only positive going half waves of the input to output till the negative half cycles are bypassed through the diode since diode get forward biased when the input voltage becomes negative. Clipping occurs at -0.6V due to the voltage drop across the diode.

3. Positive clipping at +3V :

Till the input become greater than +3 V, diode is reverse biased and input will appear at the output. When input exceeds +3 V, diode becomes forward biased and cell voltage appear at the output. ~~When input~~ Since the diode is in series with the cell, actual clipping level is at +3.6 V

4. Negative clipping at -3V :

Till the input become less than -3V diode is reverse biased and the input will appear at the output. When input is less than -3 V, diode becomes forward biased and the cell voltage appear at the output ~~when input~~ Since the diode is in series with the cell, the clipping level is at -3.6 V

5 Combinational clipper :

The circuit is the merging of positive and negative clippers. During the positive half cycle of the input, one branch will be effective and the other remains open. Vice versa during the negative half cycle. Actual clipping levels are +3.6 V and -3.6 V due to diode drops.

6. Slicer :

This circuit allows the signal pass to the output only between +3 V and +6 V. During the negative half cycle of the input, diode D_1 conducts and diode D_2 gets reverse biased. Thus the output remains at +3 V. During the positive half cycle of the input when input exceeds +3 V D_1 is reverse biased and input appears at the output. If the input exceeds +6 V. D_2 conducts and the output remains at +6 V. When the diode drop is considered actual clipping occurs at +2.4 V and +6.6 V.

Clamping circuits :

THEORY:

In some situations it is necessary to add or substract a dc voltage to a given waveform without changing the shape of the waveform. Circuits used for this purpose is called clamping circuits. A capacitor which is charged to a voltage and subsequently prevented from discharging can serve as a suitable replacement for a dc source. This principle is used in clamping circuits. The clamping level can be made at any voltage level by biasing the diode. Such a clamper circuit is called biased clamper.

1. Positive clamping at 0 V :

Input voltage is represented by expression $V_m \sin \omega t$. During one negative half cycle of the input sine wave, the diode conducts and capacitor

charges to Vm with positive polarity at right side of the capacitor. During the positive half cycle of the input sine wave, the capacitor cannot discharge since the diode does not conduct. Thus capacitor act as a dc source of Vm volts connected in series with input signal source. The output voltage then can be expressed as $V_o = V_m + V_m \sin \omega t$

2. Negative clamping at 0V:

During one positive half cycle of the input sine wave, the diode conducts and capacitor charges to Vm with negatively polarity at right side of the capacitor. During negative half cycle of the input wave the capacitor cannot discharge since the diode does not conduct. Thus capacitor act as a dc source of Vm volts connected in series with input signal source. The output voltage can be then expressed as $V_o = -V_m + V_m \sin \omega t$

3. Positive clamping at +3V:

During one half cycle of the input sine wave, capacitor charges through the dc source and diode till (Vm+3)V with positive polarity of the capacitor at its right side in negative cycle. The charging of the capacitor is extended upto (Vm+3) V due to the presence of the dc source. The output is then expressed as $V_o = (V_m + 3) + V_m \sin \omega t$

4. Negative clamping at -3V:

During one positive half cycle of the input wave capacitor charges through the dc source and diode till (Vm+3) V with negative polarity of the capacitor at its right side. The charging of the capacitor is extended upto (Vm+3) volts due to the presence of the dc source. The output is then expressed as $V_o = -(V_m + 3) + V_m \sin \omega t$.

5. Negative clamper at +3V :

During one positive half cycle of the input sine wave capacitor charges through the dc source and diode till (Vm-3) V with negative polarity of the capacitor at its right side the charging of the capacitor is limited to (Vm-3) volts due to the presence of the dc source. The output is then expressed as $V_o = -(Vm-3) + Vm \sin\omega t$

6. Positive clamper at -3V

During one negative half cycle of the input sine wave, capacitor charges through the dc source and diode till (Vm-3) volts with positive polarity of the capacitor at its right side. The charging of the capacitor is limited to (Vm-3) V due to the presence of the dc source. The output is then expressed as $V_o = (Vm-3) + Vm \sin\omega t$.

PROCEDURE :

Clipping circuits :

1. Set up the circuit after testing the diode. Set the signal generator in sine wave mode and fix the amplitude at 20V peak to peak connecting directly with one channel of CRO.
2. Using another probe connect the signal generator output to the input of the circuit.
3. Observe the clipped waveform on CRO screen by connecting the output of the circuit to the other channel of CRO so that the input and output of the circuit can be seen simultaneously.
4. To observe the transfer characteristics on CRO screen, feed Vin to A-channel and Vo at B channel and keep the time / div knob of CRO in X y/a A mode (Transfer characteristic mode)
5. While drawing the output waveforms, mark exact values considering

the diode voltage drop also

For clamping circuits :

1. Set up circuit after testing the components
2. Set the amplitude of input sine wave at 20V peak to peak. If the input sine wave has any dc level, nullify it by turning the offsets knob of the signal generator.
3. Observe the input and output on CRO screen simultaneously keeping AC-DC switch of the CRO in DC position.

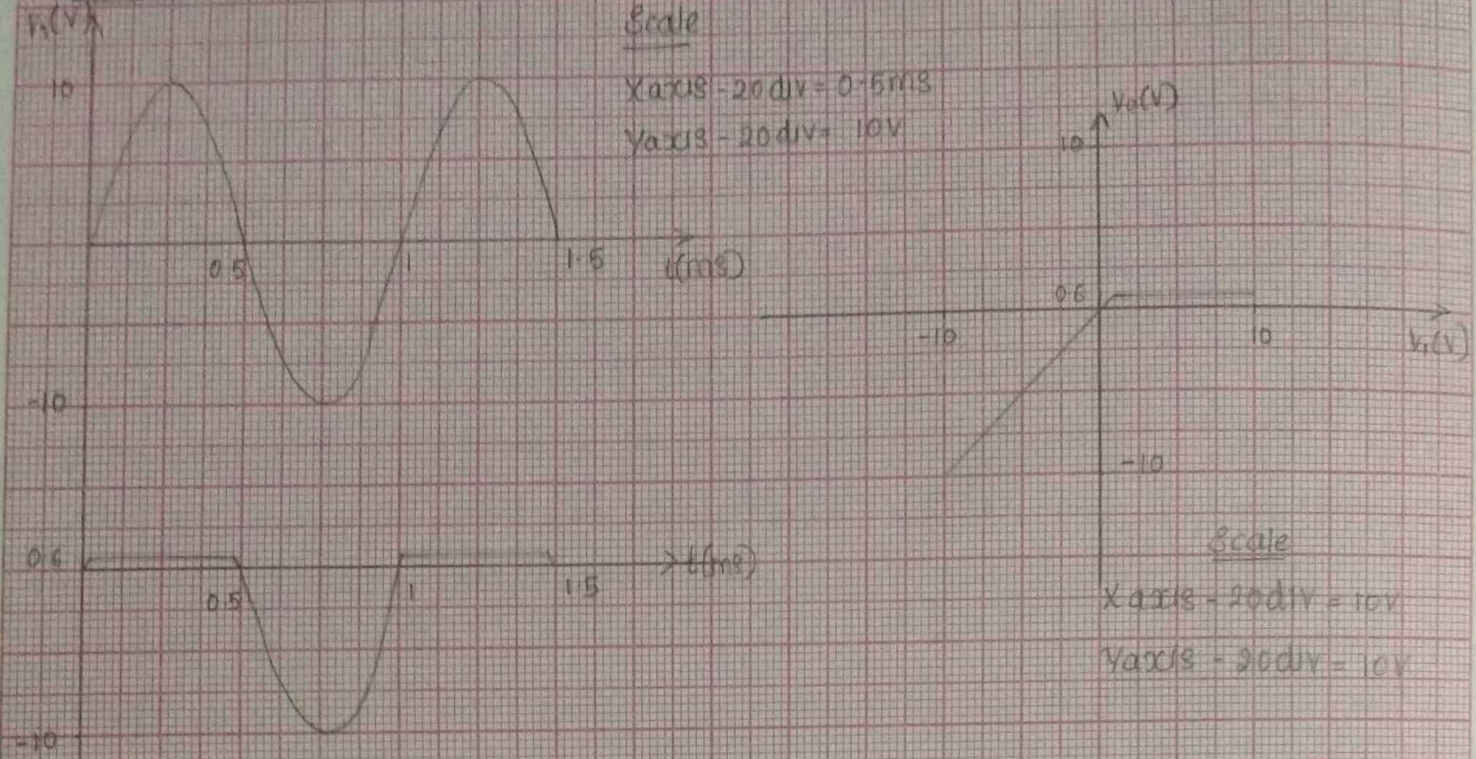
RESULT :

A

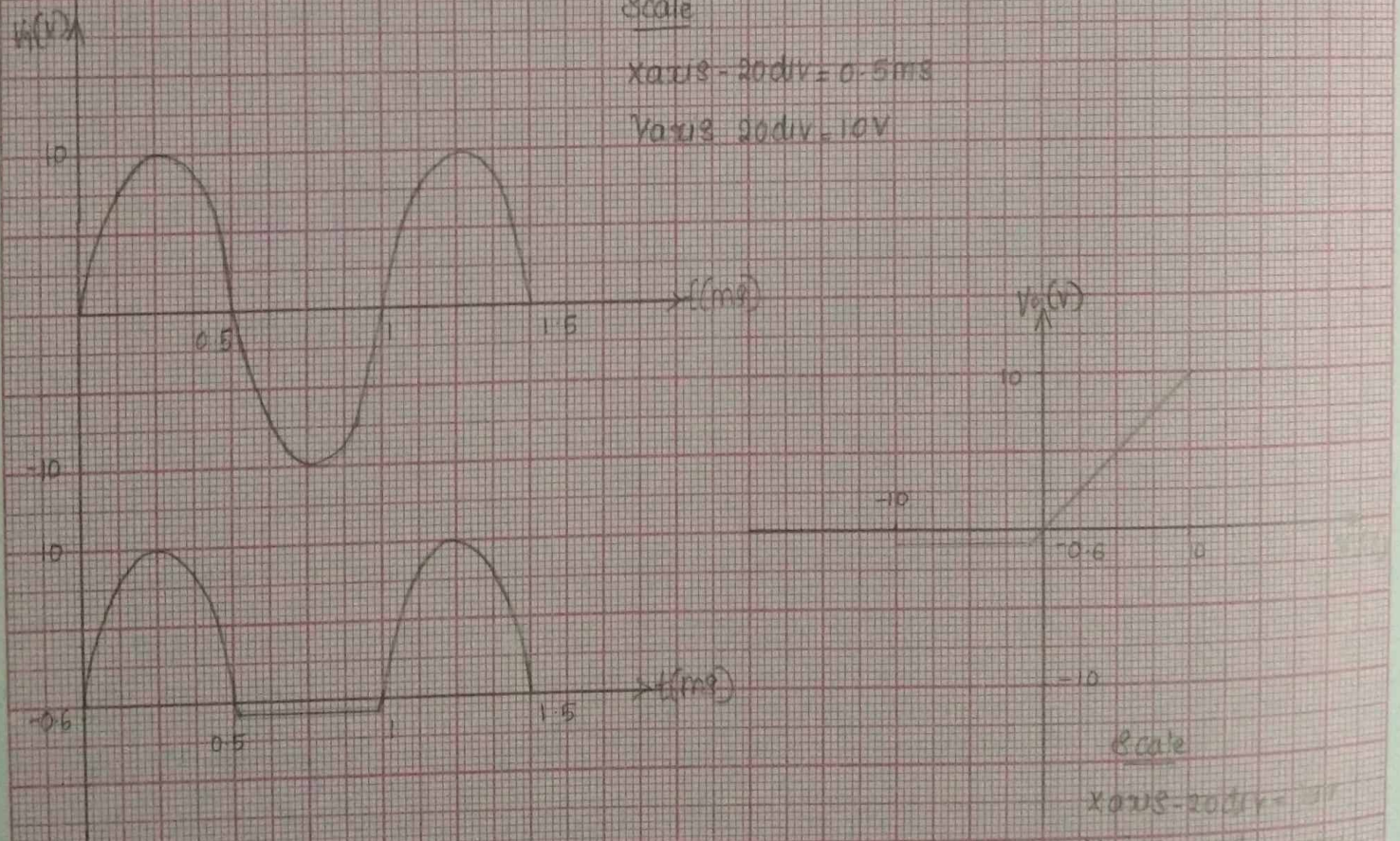
Designed clipping and clamping circuits and plotted their waveforms and transfer characteristics.

13/6/22

POSITIVE CLIPPER AT 0V

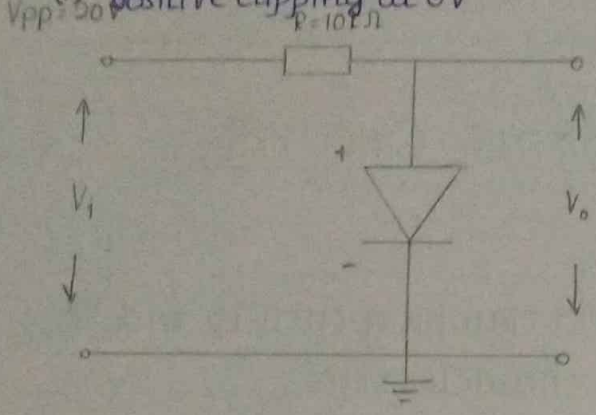


NEGATIVE CLIPPER AT 0V

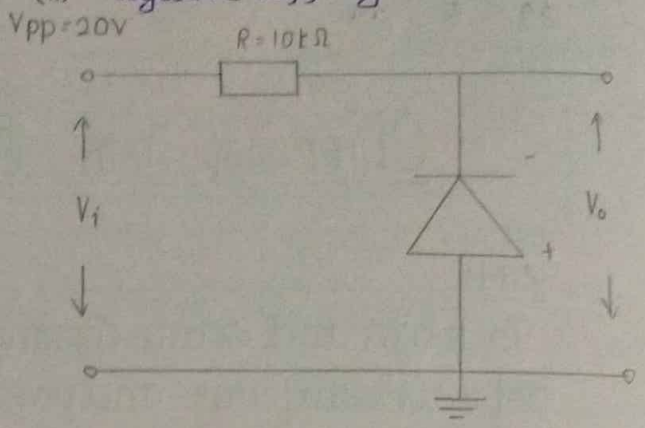


CLIPPING CIRCUITS :

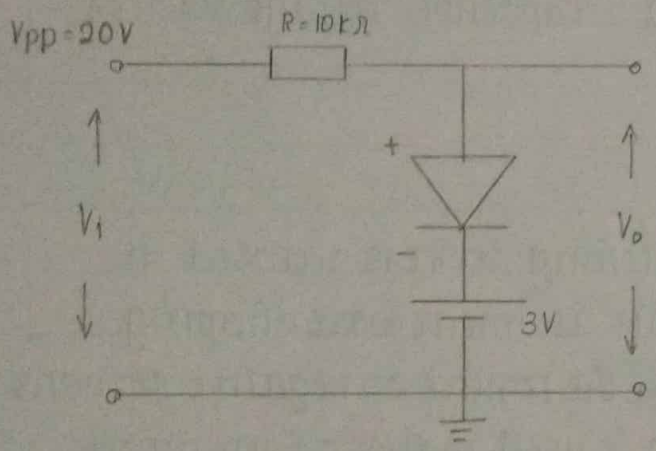
(i) Positive clipping at 0V



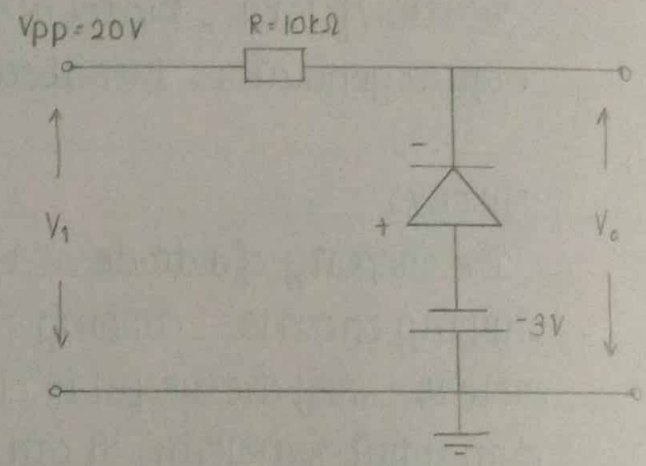
(ii) Negative clipping at 0V



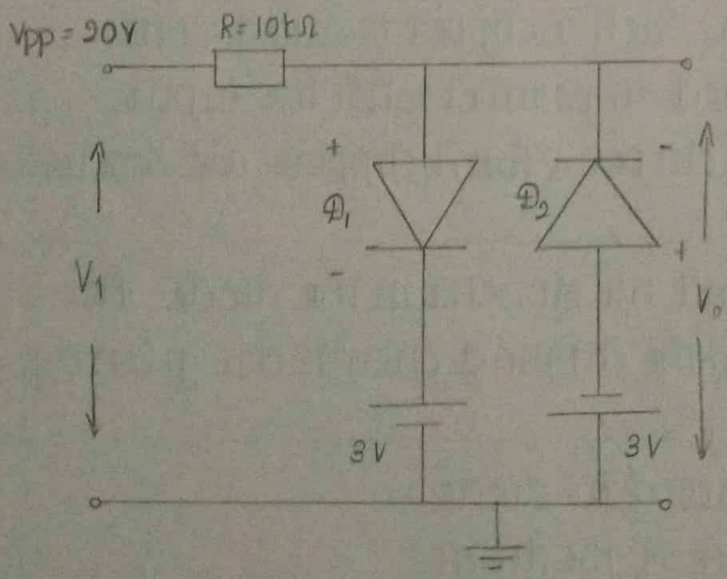
(iii) Positive clipping at 3V



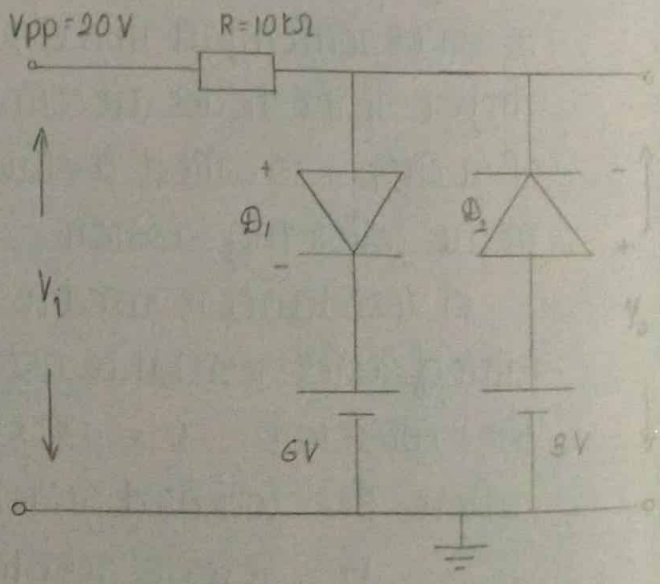
(iv) Negative clipping at -3V



(v) Combinational clipper

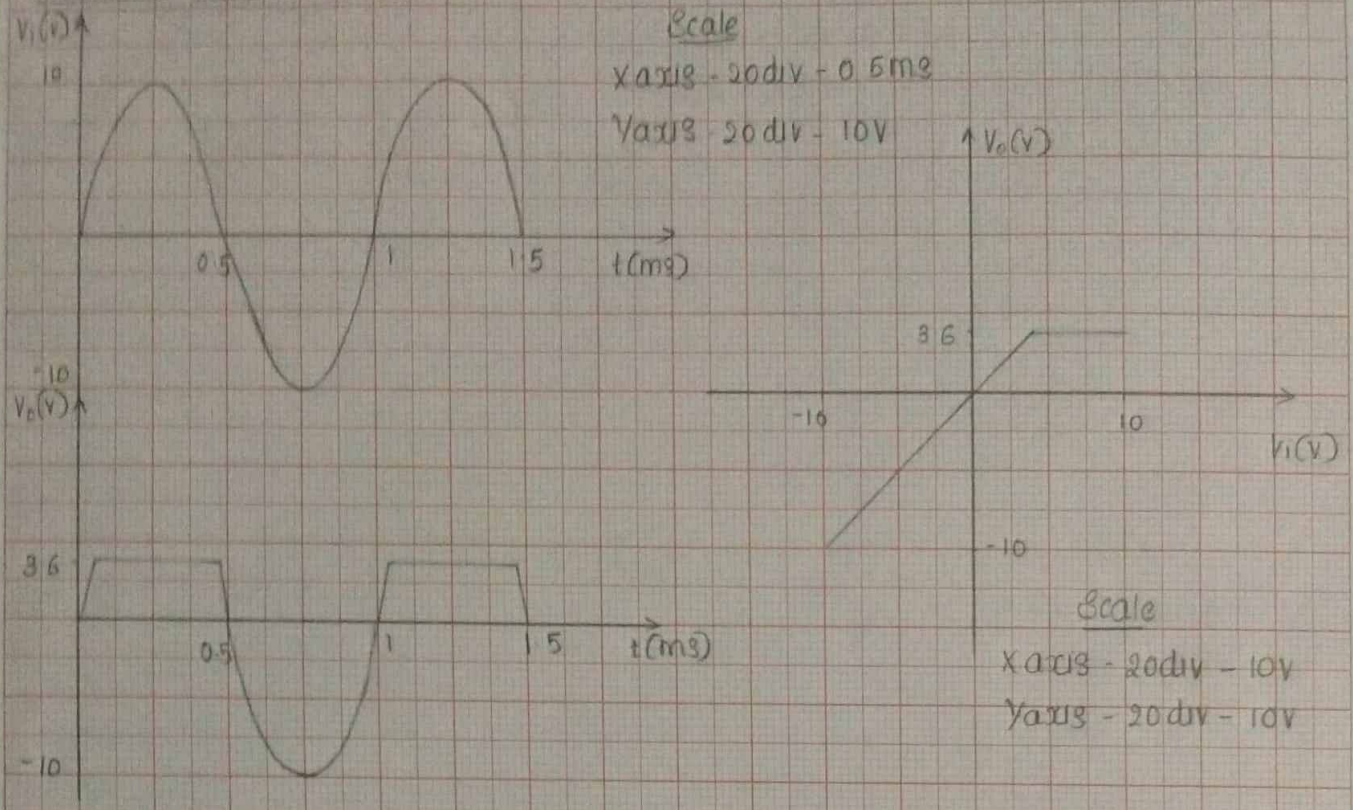


(vi) Slicer

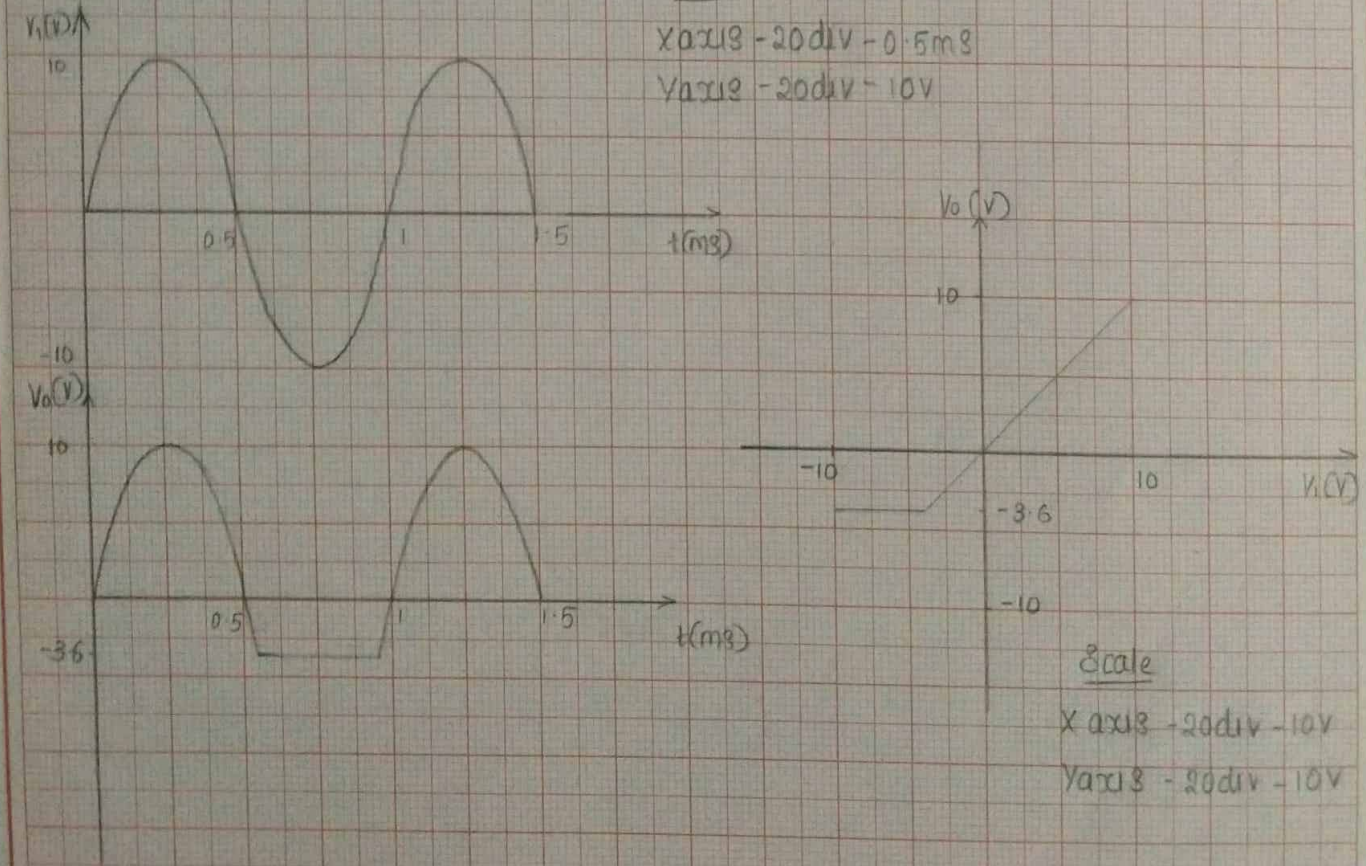


Batch No: ..... Date : ☐☐☐☐☐☐☐☐

POSITIVE CLIPPER AT 3V



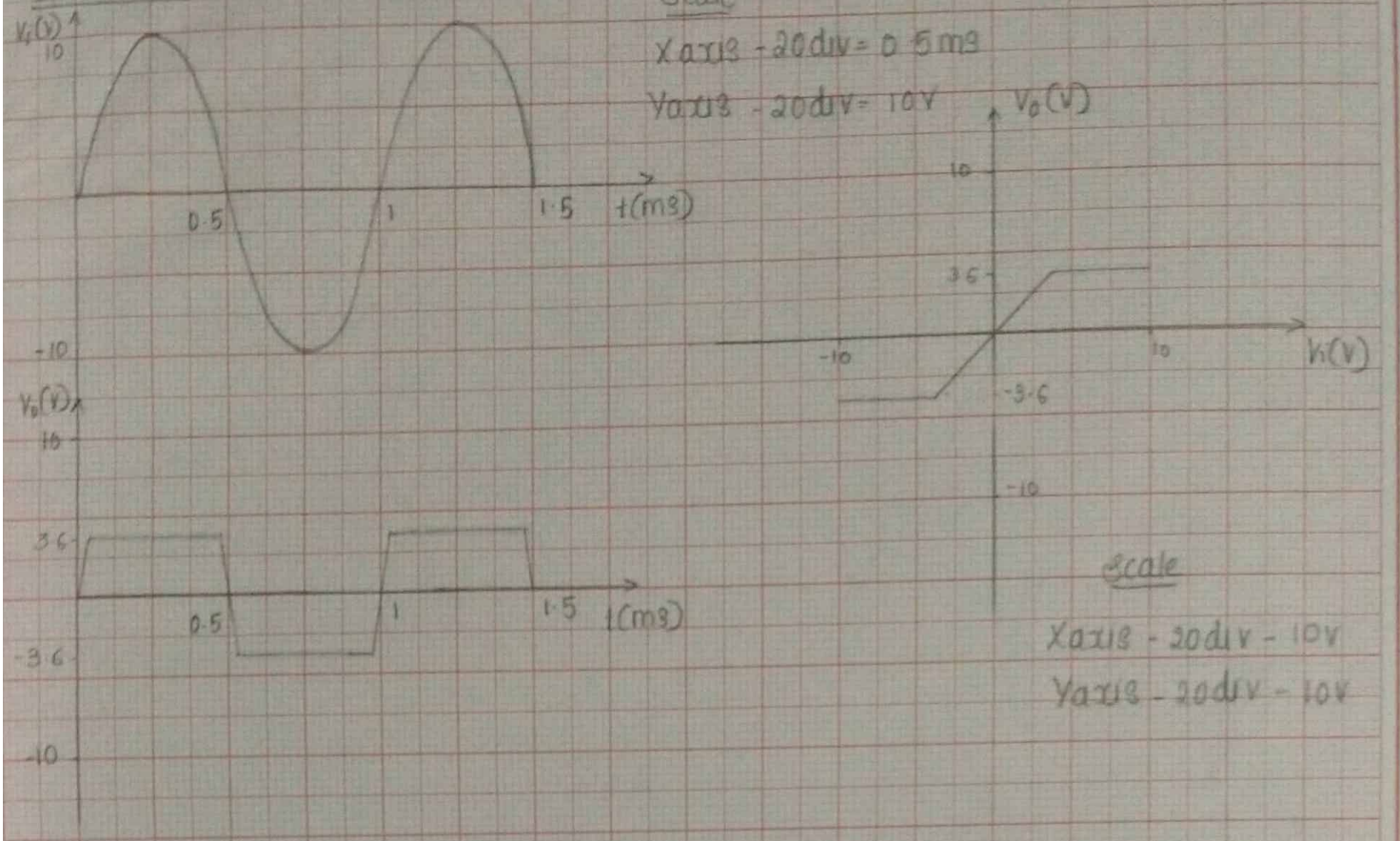
NEGATIVE CLIPPER AT -3V



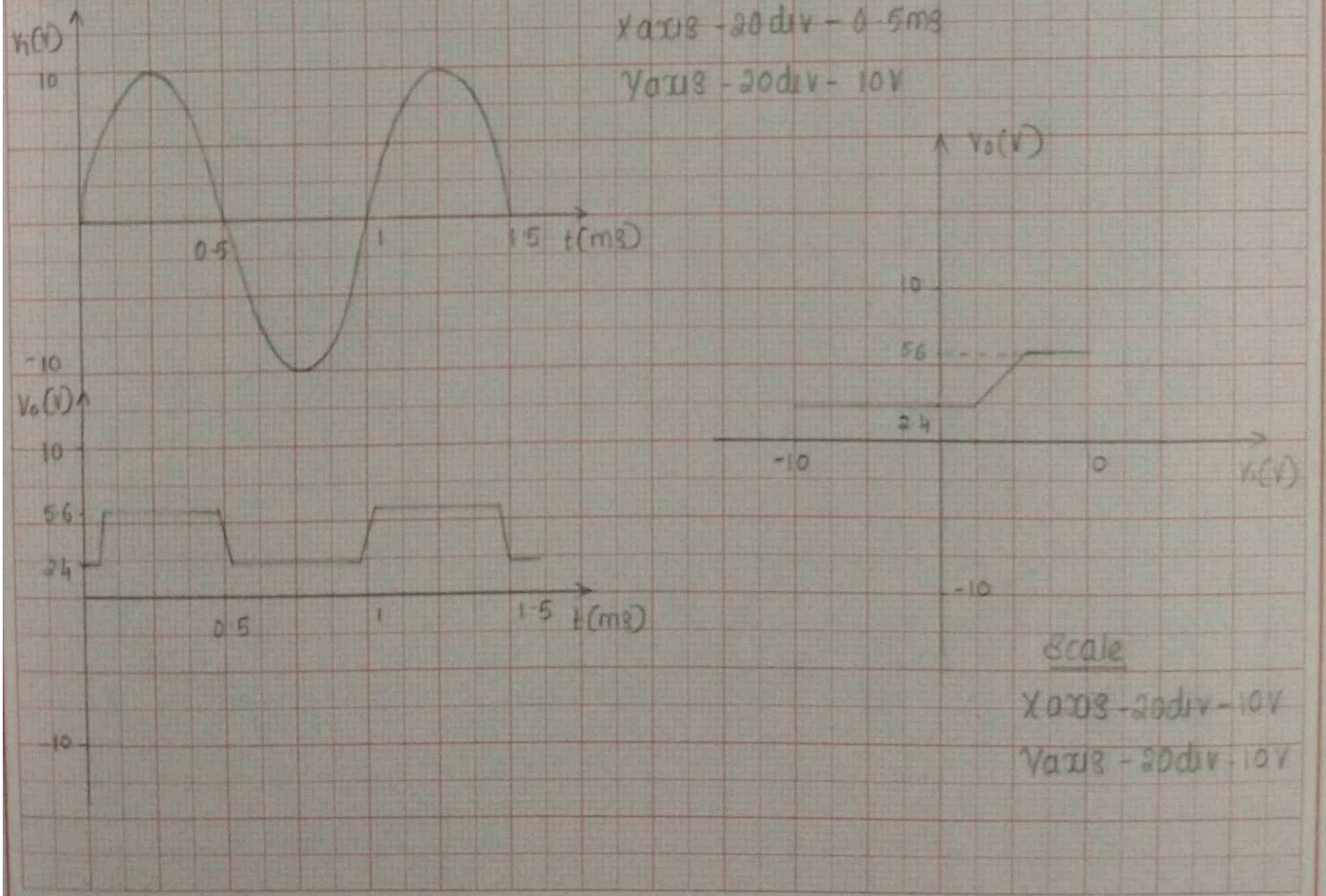
Batch No: .....

Date :

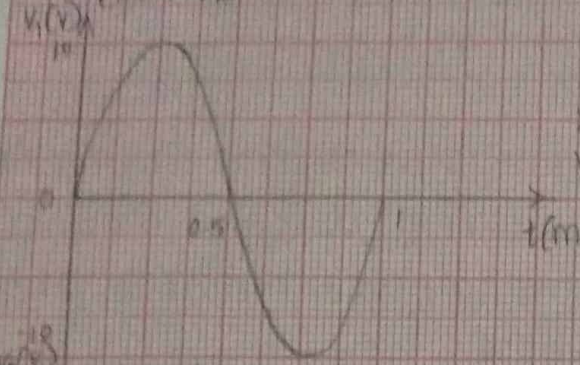
COMBINATIONAL CLIPPER



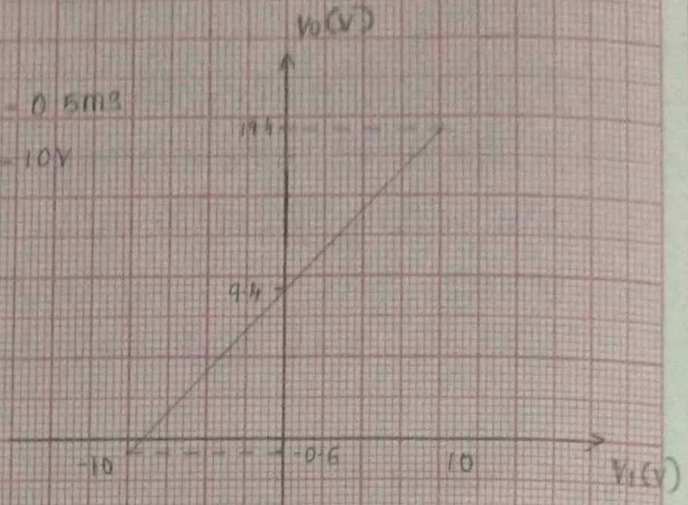
SLICER



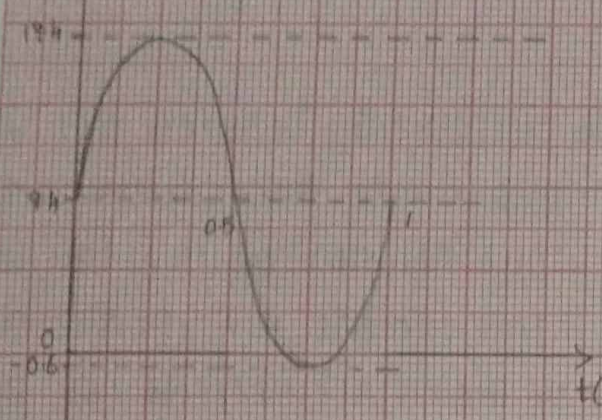
POSITIVE CLAMPER AT 0V



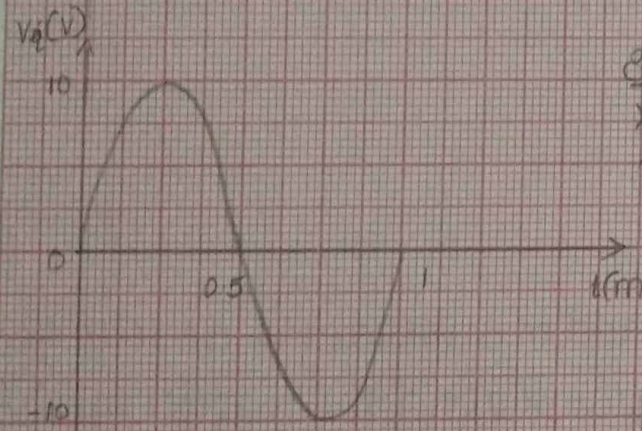
Scale
X axis 20div - 0.5ms
Y axis 20div - 10V



Scale
Xaxis 20div - 10V
Yaxis 20div - 10V

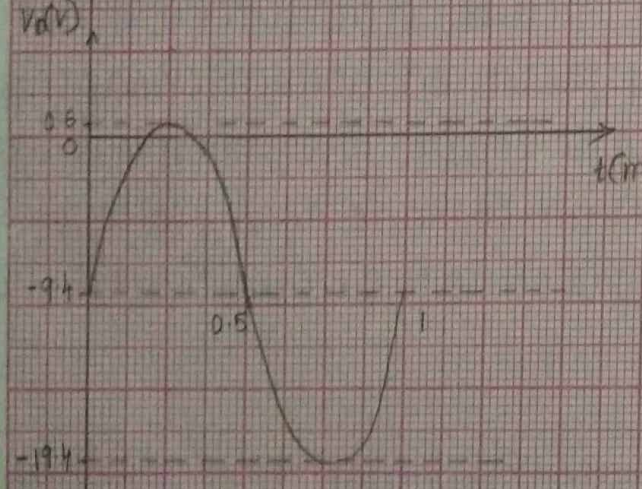


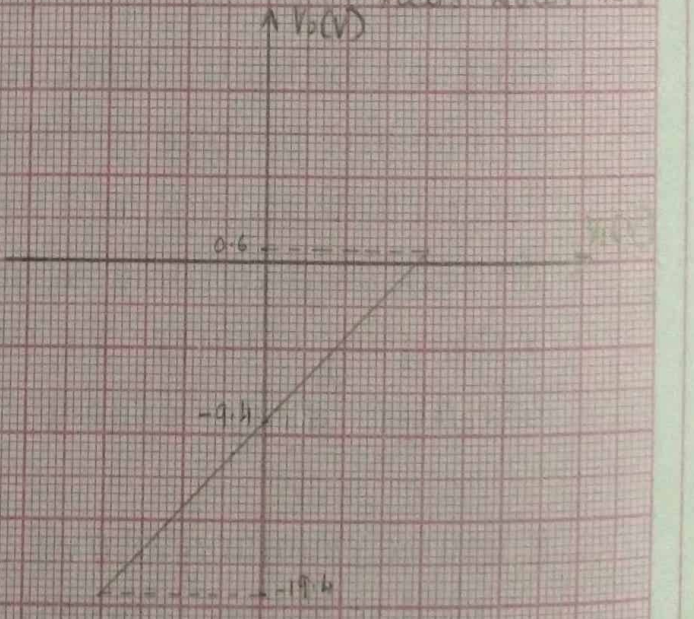
NEGATIVE CLAMPER AT 0V



Scale
X axis 20div - 0.5ms
Yaxis 20div - 10V

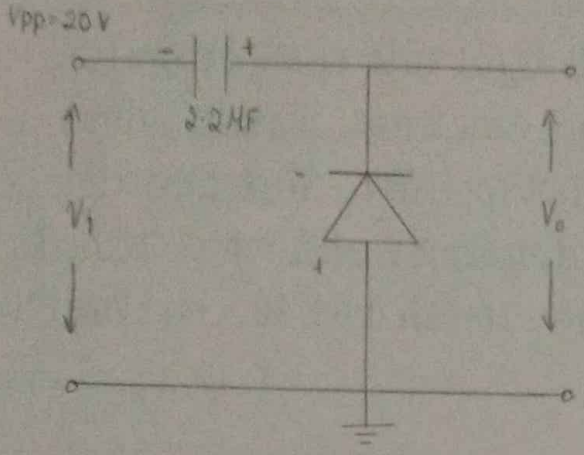
Scale
Xaxis - 20div - 10V
Yaxis - 20div - 10V



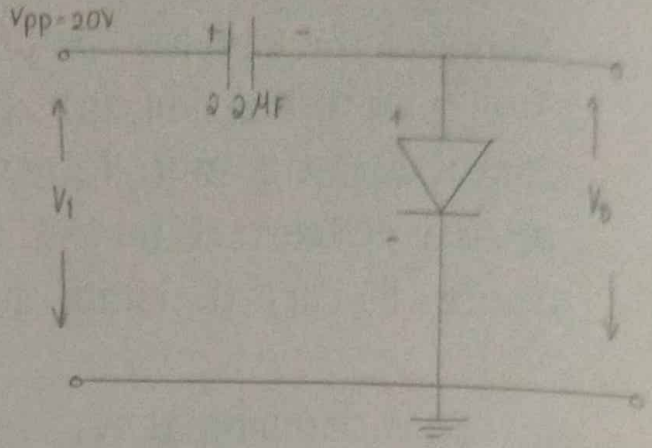


CLAMPER CIRCUITS

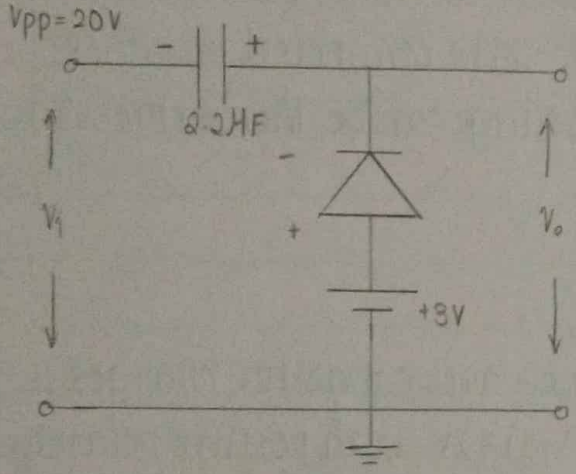
(i) Positive clamper at 0V



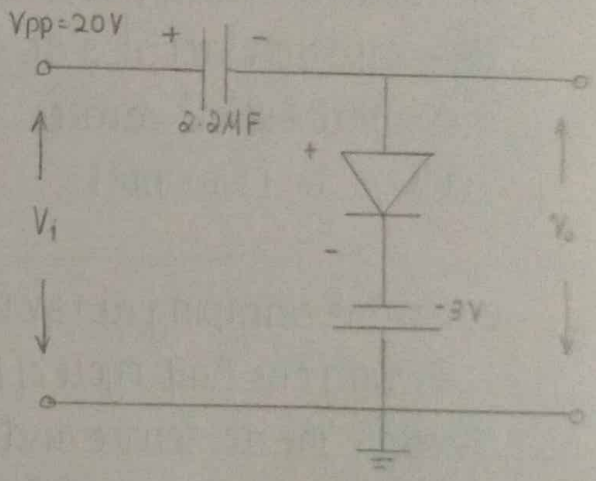
(ii) Negative clamper at 0V



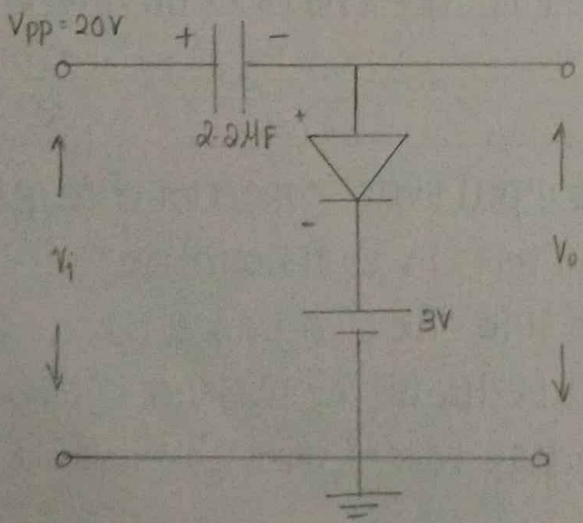
(iii) Positive clamping at +3V



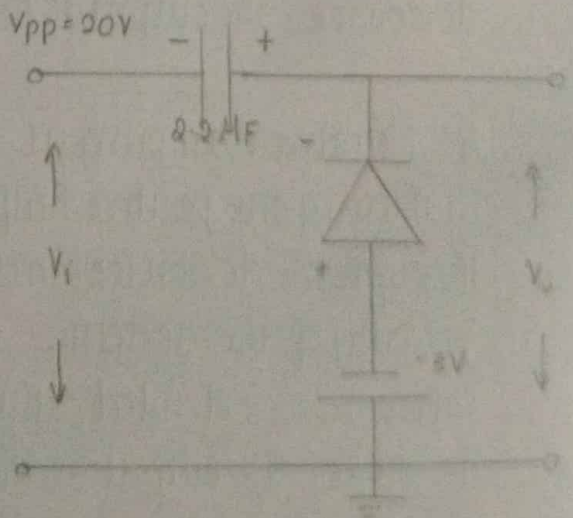
(iv) Negative clamping at -3V



(v) Negative clamping at +3V



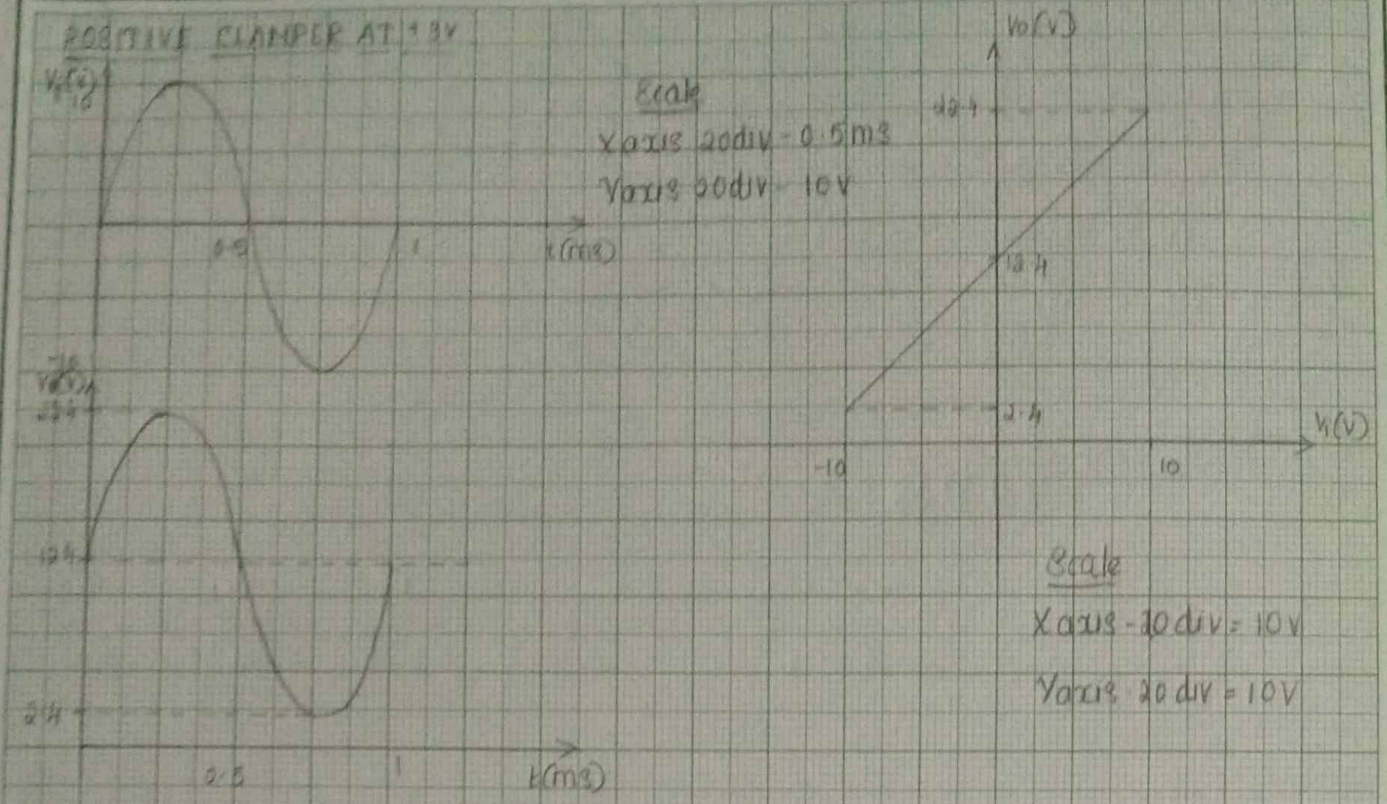
(vi) Positive clamping at -3V



Batch No: .....

Date : [ ][ ][ ][ ][ ][ ]

POSITIVE CLAMPER AT +8V



Scale

X axis 20div - 0.5ms

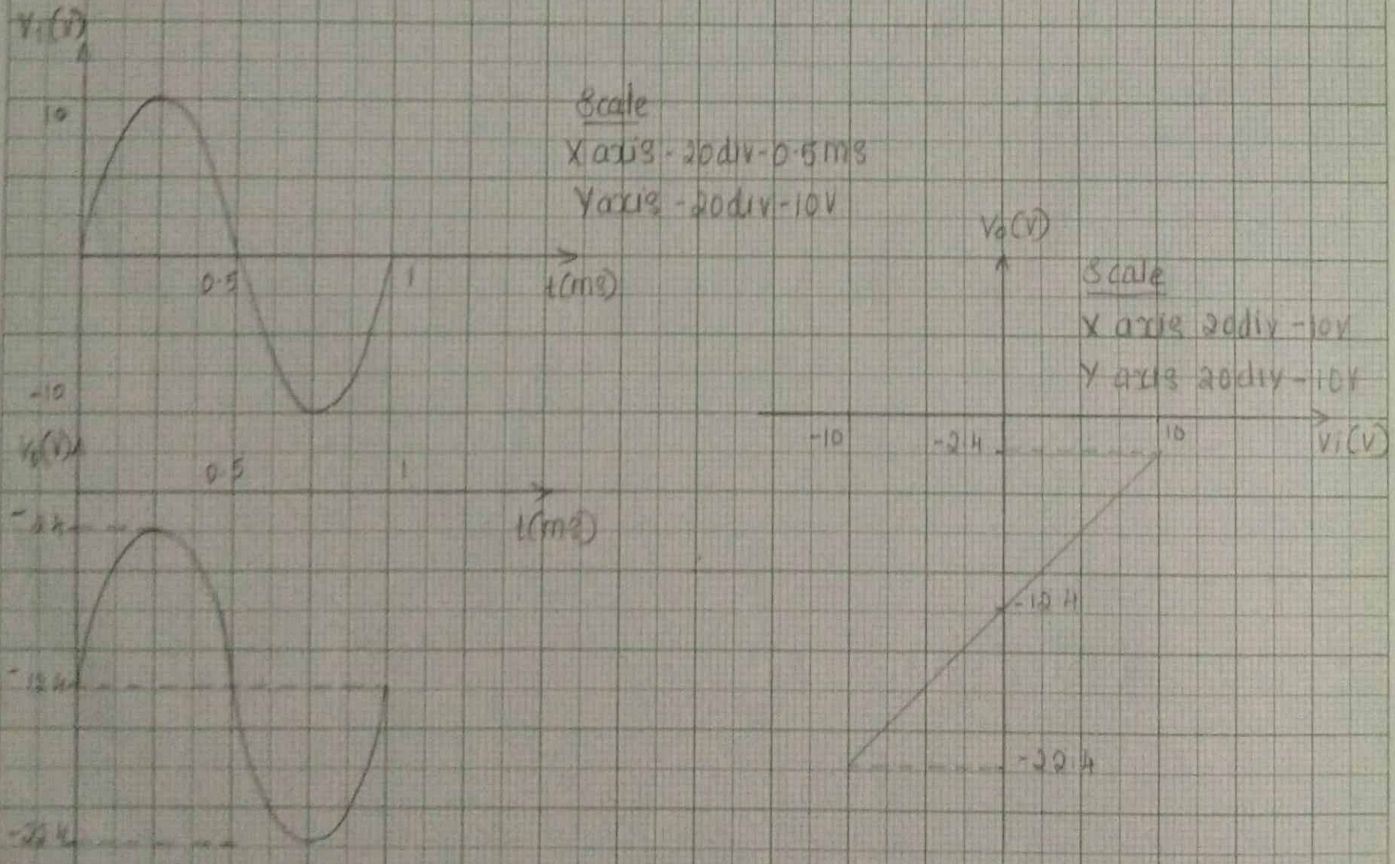
Y axis 20div - 10V

Scale

X axis - 20 div = 10 V

Y axis 20 div = 10 V

NEGATIVE CLAMPER AT -8V



Scale

X axis - 20div - 0.5 ms

Y axis - 20div - 10V

Scale

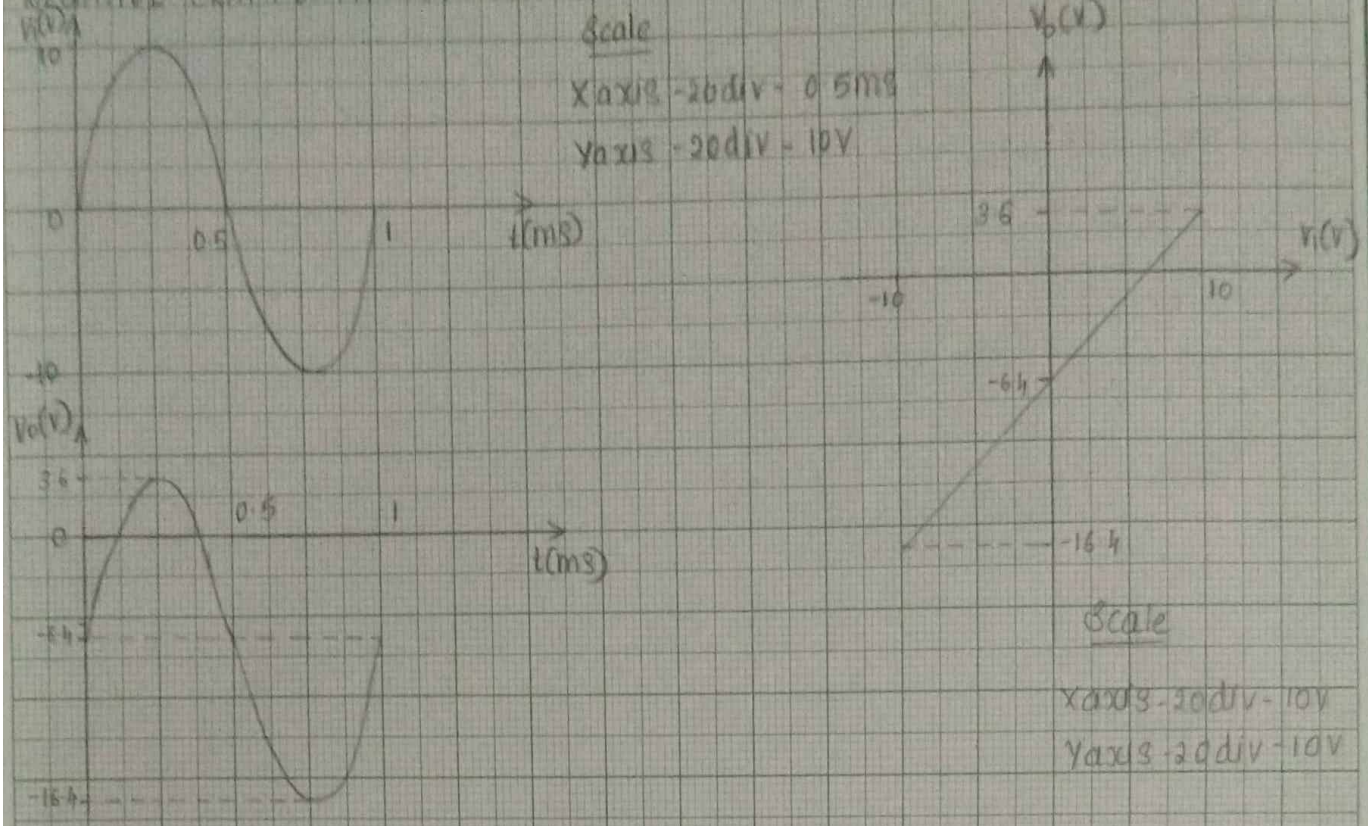
X axis 20div - 10V

Y axis 20div - 10V

Batch No: .....

Date :

NEGATIVE CLAMPER AT +3V



Scale

Xaxis - 20div - 0.5ms

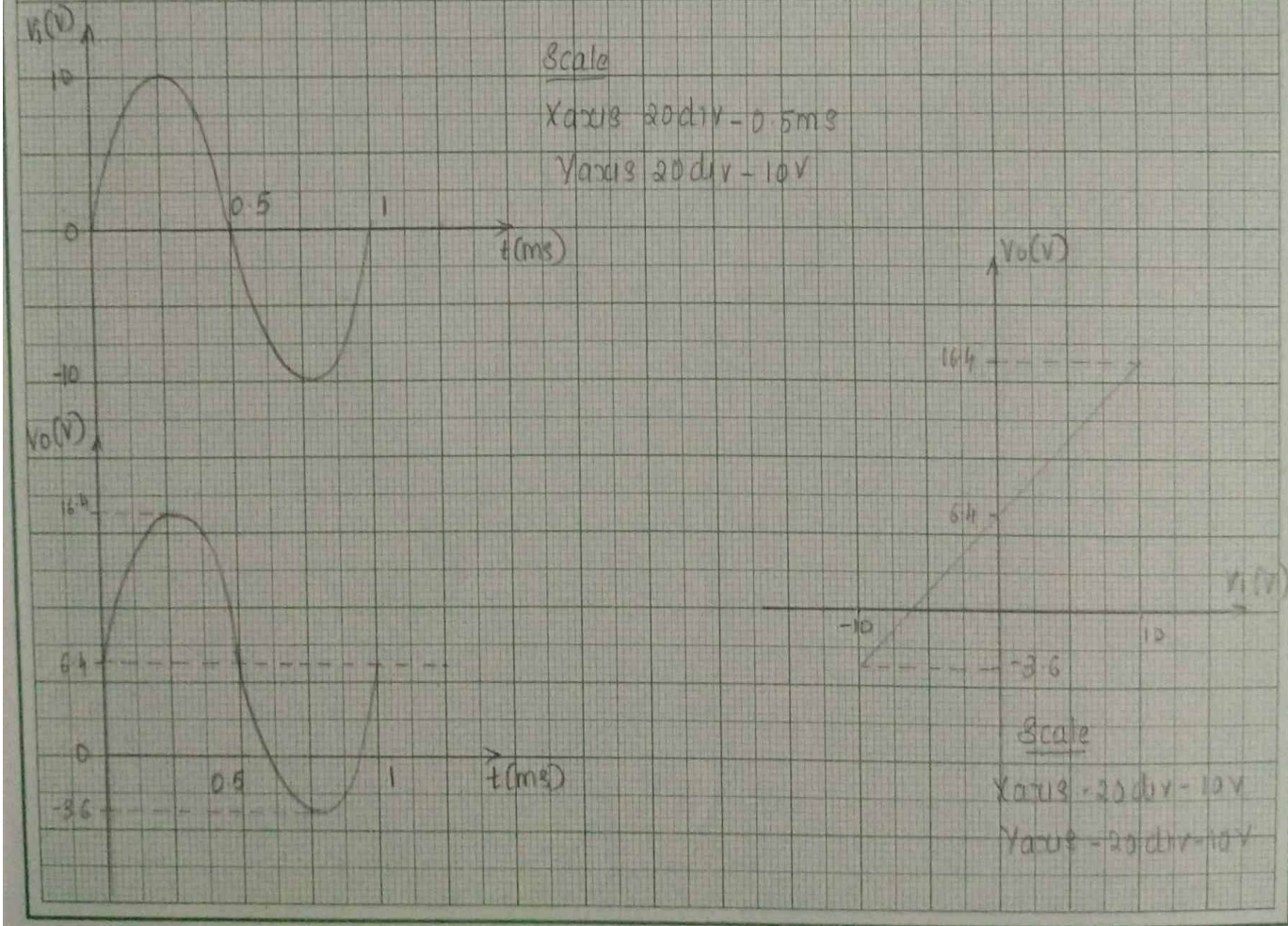
Yaxis - 20div - 10V

Scale

Xaxis - 20div - 10V

Yaxis - 20div - 10V

POSITIVE CLAMPER AT -3V



Scale

Xaxis - 20div - 0.5ms

Yaxis 20div - 10V

Scale

Xaxis - 20 div - 10V

Yaxis - 20 div - 10V