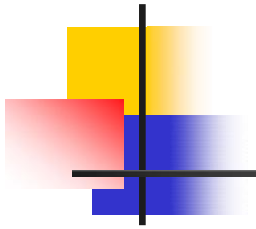
Digital Signal Processors

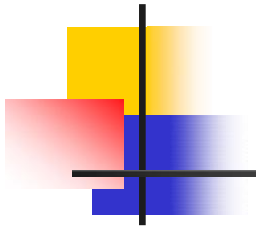
- Specially designed for efficient implementation of digital signal processing systems
- Texas Instruments has released TMS320C series of DSPs.
- TMS320C67xx series are VLIW(Very Long Instruction Word) architecture processors.
- VLIW architecture has an enhanced parallelism in the instruction execution. In this processor, many instructions are fetched at the same time and issued to multiple execution units to be executed in parallel.

Features of TMS320C67xx



- Advanced VLIW CPU with eight functional units
  - Two multipliers & Six arithmetic units
  - Executes up to eight 32-bit instructions per cycle
  - Develop highly effective RISC-like code
- CPU consists of 32 general purpose registers (32-bit)

Features of TMS320C67xx



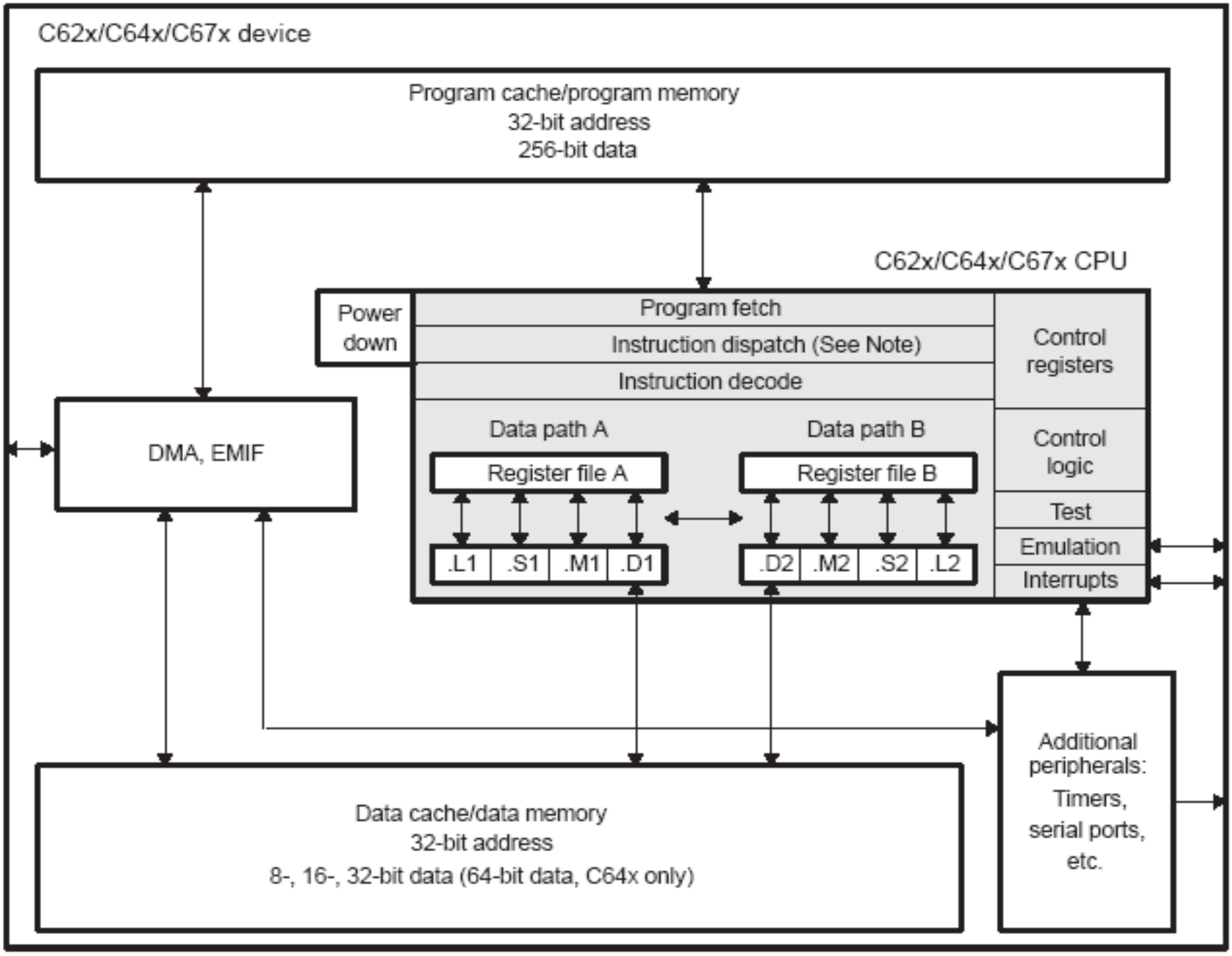
- Variable-width instructions: flexibility of data types
  - 8/16/32-bit data support, providing efficient memory support
- Efficient code execution on independent functional units
  - Industry's most efficient C compiler on DSP benchmark suite
  - Industry's first assembly optimizer for fast development and improved Parallelization

Features of TMS320C67xx

- Hardware support for
  - Single-precision (32-bit).
  - Double-precision (64-bit) IEEE floating-point operations.
- 32 x 32-bit integer multiply with 32- or 64-bit result

TMS320C67xx Architecture

- TMS320C6000 devices come with
  - Program memory
  - Varying sizes of data memory
  - Peripherals
  - Direct memory access (DMA) controller
  - Power-down logic
  - External memory interface (EMIF)
  - Serial ports
  - Host ports


C62x/C64x/C67x device
Program cache/program memory
32-bit address
256-bit data
C62x/C64x/C67x CPU
Power down
Program fetch
Instruction dispatch (See Note)
Instruction decode
Control registers
Data path A
Data path B
Control logic
Register file A
Register file B
Test
Emulation
Interrupts
.L1
.S1
.M1
.D1
.D2
.M2
.S2
.L2
DMA, EMIF
Additional peripherals:
Timers,
serial ports,
etc.
Data cache/data memory
32-bit address
8-, 16-, 32-bit data (64-bit data, C64x only)

TMS320C67xx Architecture

- **Central Processing Unit (CPU)**
  - Program fetch unit(Instruction is fetched from Program Memory)
    - Program address is generated in the CPU.
    - Program Address is sent to the memory.
    - Program Memory access (read /write)is carried out.
    - Fetch packet is received at CPU.
  - Instruction dispatch unit
    - Instructions are assigned to appropriate functional units
  - Instruction decode unit
    - Source registers, destination registers, associated data paths are decoded for the execution of instructions in the functional units.

TMS320C67xx Architecture

- **Central Processing Unit (CPU)**
  - Two data paths, each with four functional units(.L1, .S1, .M1,.D1) and (.L2, .S2, .M2,.D2)
  - Processing of instructions occur in each of the two data paths(A and B)
  - Thirty two 32-bit registers(Register file A contains 16 registers(32 bit size) + Register file B contains 16 registers (32 bit size))
  - Control registers (to configure and control various processor operations)
  - Control logic
  - Test, emulation, and interrupt logic

TMS320C67xx Architecture

Internal Memory

- 32-bit, byte-addressable address space.
- Internal (on-chip) memory is organized in separate Data and Program spaces.
- Off-chip memory - Unified memory space
- Two 32-bit internal ports to access internal data.
- Single internal port to access internal Program memory with an instruction fetch width of 256 bits

TMS320C67xx Architecture

Memory and Peripheral Options

- Large on–chip RAM, up to 7M bits
- Program cache
- 2–level caches
- 32–bit EMIF supports SDRAM, SBSRAM, SRAM & other asynchronous memories.
- DMA Controller transfers data between address ranges in the memory map without intervention by CPU.
- The DMA controller has four programmable channels and a fifth auxiliary channel

TMS320C67xx Architecture

- EDMA Controller(has same functions as DMA Controller)
  - 16 programmable channels
  - RAM space to hold multiple configurations for future transfers.
- HPI(Host Port Interface) is a parallel port through which a host processor can directly access the CPU's memory space.

TMS320C67xx Architecture

- Timers are two 32–bit general–purpose timers
  - Time events
  - Count events
  - Generate pulses
  - Interrupt the CPU
  - Send synchronization events to the DMA/EDMA controller
- Power–down logic allows reduced clocking to reduce power consumption

Functional Units

- The eight functional units are divided into two groups of four.
- 2 Multipliers and 6 ALUs

General-Purpose Register Files

- There are two general-purpose register files (A and B) in the data paths. Each of these files contains 16 32-bit registers (A0–A15 for file A and B0–B15 for file B).
- The general-purpose registers can be used for data, data address pointers, or condition registers.
- The C67xx general-purpose register files support data ranging in size from packed 16-bit data through 40-bit fixed-point and 64-bit floating point data.
- Values larger than 32 bits, such as 40-bit long and 64-bit float quantities, are stored in register pairs. In these the 32 LSBs of data are placed in an even-numbered register and the remaining 8 or 32 MSBs in the next upper register (which is always an odd-numbered register).