

EXPERIMENT .NO.8  
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## ASTABLE AND MONOSTABLE MULTIVIBRATORS USING IC 555

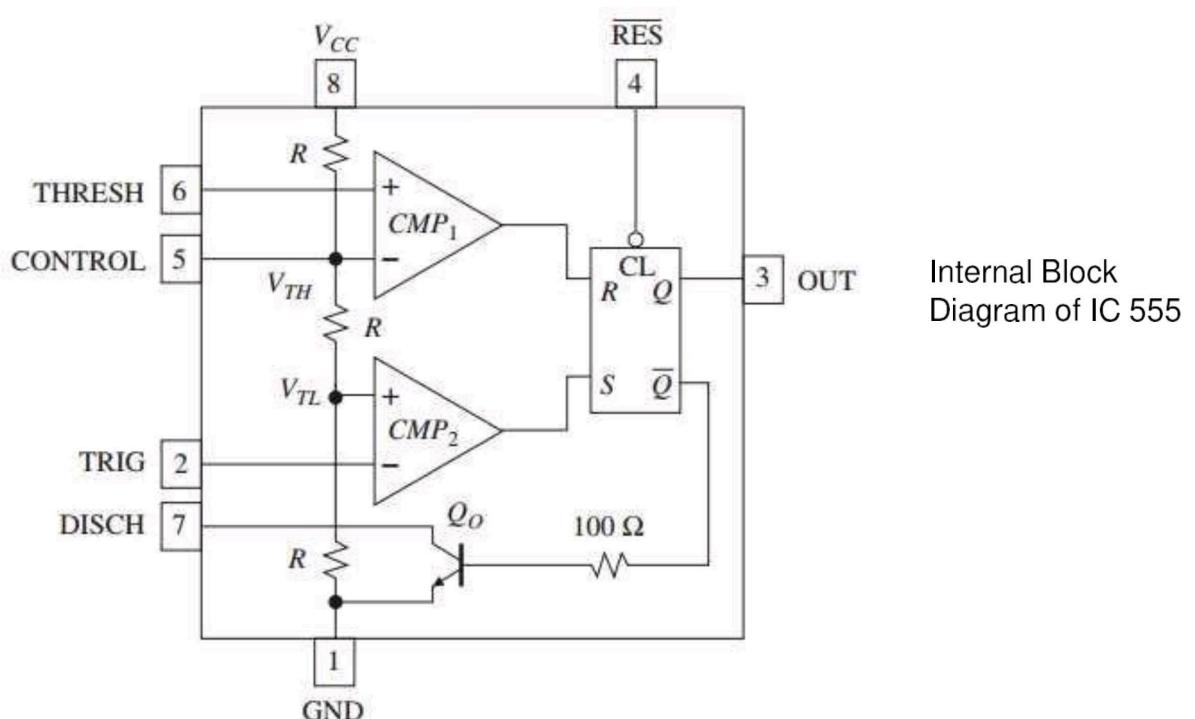
### AIM

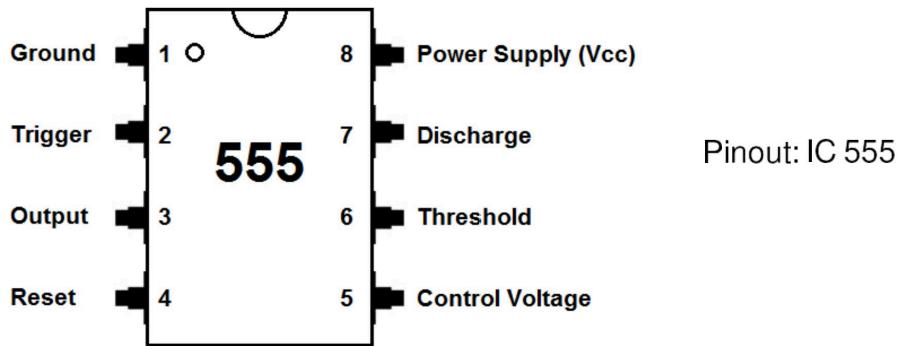
To design and setup,

- 1 An astable multivibrator using IC 555 for a duty cycle of 75% and a total time period of  $2ms$
2. A Monostable multivibrator using IC 555 to produce a pulse of  $10ms$  width

### THEORY

IC 555 is a popular monolithic timer IC which can be used for timing applications.





The Basic blocks of the 555 timer are:

- A trio of identical resistors
- A pair of voltage comparators
- An RS flip-flop and
- A BJT switch  $Q_o$

The resistances set the comparator thresholds at  $V_{TH} = \frac{2}{3}V_{CC}$  and  $V_{TL} = \frac{1}{3}V_{CC}$

The upper threshold node is also externally accessible via pin 5(control) so that the user can modulate the value of  $V_{TH}$ .

The non-inverting input of CMP1 is connected to the threshold pin(pin 6) and the inverting i/p of CMP2 is connected to trigger pin(pin 2)

The outputs of the comparators goes to an RS Flip-flop whose o/p is connected to the output pin(pin 3)

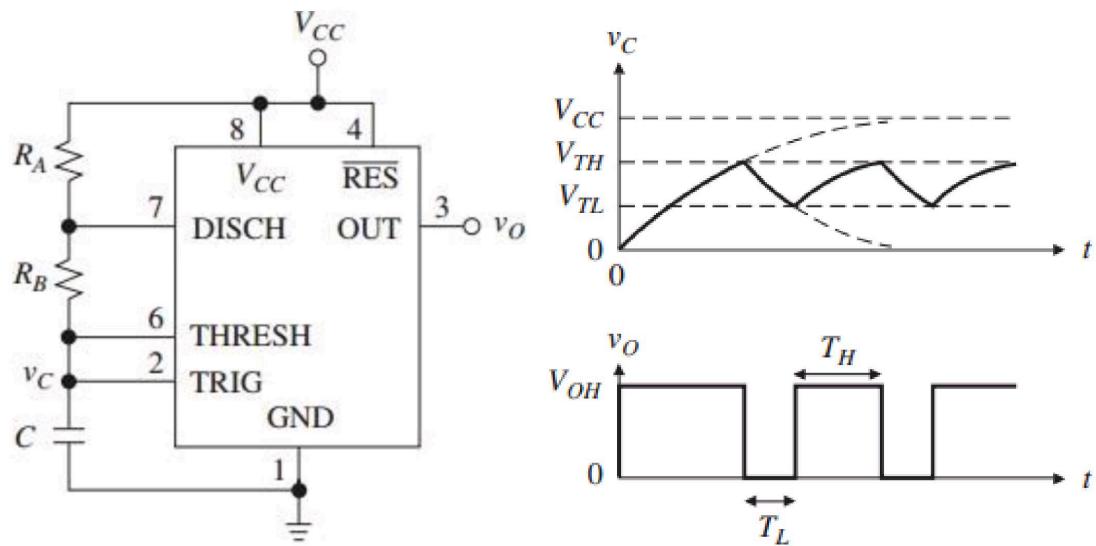
The state of the flip-flop is controlled by the comparators:

- Whenever the voltage at the trigger input drops below  $V_{TL}$ , CMP2 fires and sets the flip-flop, forcing Q high and  $\bar{Q}$  low; with a low voltage at its base,  $Q_o$  is in cutoff.

- Whenever the voltage at the threshold input rises above  $V_{TH}$ , CMP1 fires and clears the flip-flop, forcing Q low and  $\bar{Q}$  high. With a high voltage applied to its base via the  $100\Omega$  resistance,  $Q_O$  is now ON

The 555 IC is available in both bipolar and CMOS versions.

### ASTABLE MULTIVIBRATOR USING 555



At power-on, when the capacitor is still discharged, the voltage at the TRIG input is less than  $V_{TL}$ . This forces Q to be High and keeps the BJT in cutoff, thus allowing C to charge toward  $V_{CC}$  via the series combination of resistors  $R_A + R_B$ .

As soon as  $v_C$  reaches  $V_{TH}$ , CMP1 fires and forces Q low. This turns on  $Q_O$ , which then pulls the DISCH pin to  $V_{CE(sat)} \cong 0V$

Consequently, C now discharges toward ground via  $R_B$ . As soon as  $v_C$  reaches  $V_{TL}$ , CMP2 fires, forcing Q high and turning off  $Q_O$

This cycle will repeat itself providing an astable operation

To find the time intervals  $T_L$  and  $T_H$ :

During  $T_L$  the time constant is  $R_B C$ ,

$$\Rightarrow T_L = R_B C \ln\left(\frac{0-V_{TH}}{0-V_{TL}}\right) = R_B C \ln(2)$$

During  $T_H$  the time constant is  $(R_A + R_B)C$ ,

$$\Rightarrow T_H = (R_A + R_B)C \ln\left(\frac{V_{CC} - V_{TL}}{V_{CC} - V_{TH}}\right) = (R_A + R_B)C \ln\left(\frac{\frac{2}{3}V_{CC}}{\frac{1}{3}V_{CC}}\right) = (R_A + R_B)C \ln(2)$$

Where we have used  $V_{TH} = \left(\frac{2}{3}\right)V_{CC}$

$$\Rightarrow T = T_L + T_H = (R_A + 2R_B)C \cdot \ln(2)$$

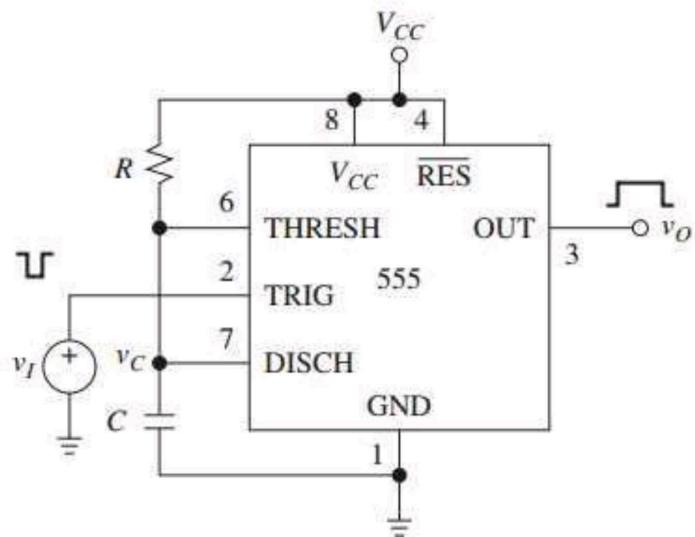
Thus, the time period of oscillations,  $T \cong 0.69(R_A + 2R_B)C$

$f_0 = 1/T = \frac{1.44}{(R_A + 2R_B)C}$  is the frequency of oscillations and,

$D(\%) = \frac{100T_H}{T_L + T_H} = 100 \times \frac{R_A + R_B}{R_A + 2R_B}$  is the duty cycle.

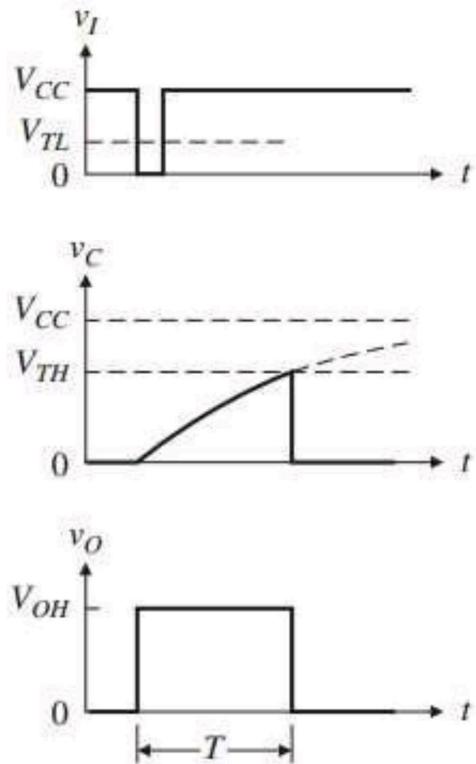
Since  $T_H > T_L$ , the circuit always gives  $D(\%) > 50\%$

## MONOSTABLE MULTIVIBRATOR USING 555



Under normal conditions, the TRIG input is held high, and the circuit is in the stable state with  $Q$  low and the BJT switch  $Q_O$  is closed, keeping  $C$  discharged, or  $v_C \cong 0$

The circuit is triggered by lowering the TRIG input below  $V_{TL}$ . This will cause CMP2 to set the flip-flop, forcing  $Q$  high and turning off  $Q_O$ . This, in turn, causes  $C$  to charge toward  $V_{CC}$  via  $R$ . As soon as  $v_C$  reaches  $V_{TH}$ , the upper comparator clears the flip-flop, forcing  $Q$  low and turning  $Q_O$  on. The capacitor is rapidly discharged, and the circuit returns to the stable state.



The pulse width  $T$  is found as,

$$T = R C \ln \left( \frac{V_{CC}}{V_{CC} - V_{TH}} \right) = R C \ln(3) \cong 1.10 R C$$

The pulse width is thus independent of  $V_{CC}$

## **DESIGN**

### **ASTABLE MULTIVIBRATOR USING 555**

Required time period  $T = 2ms$

Required Duty Cycle = 75%

$$T_H = 0.75 \times T = 1.5ms$$

$$T_L = T - T_H = 0.5ms$$

We have  $T_H \cong 0.69(R_A + R_B)C$  and  $T_L = 0.69R_B C$

Choose  $C = 0.1\mu F$

$$\Rightarrow R_B = \frac{T_L}{0.69C} = \frac{0.5m}{0.69 \times 0.1\mu} = 8.33k; \text{ Use } 8.2k \text{ Std}$$

$$\text{Also, } T_H = 1.5ms = 0.69(R_A + R_B)C = 0.69(R_A + 8.2k)0.1\mu F$$

$$R_A = 13.54k \text{ Use } 10k \text{ in series with } 3.3k$$

### **MONOSTABLE MULTIVIBRATOR USING 555**

Desired pulse width  $T = 10ms$

We have, the pulse width  $T \cong 1.10RC$

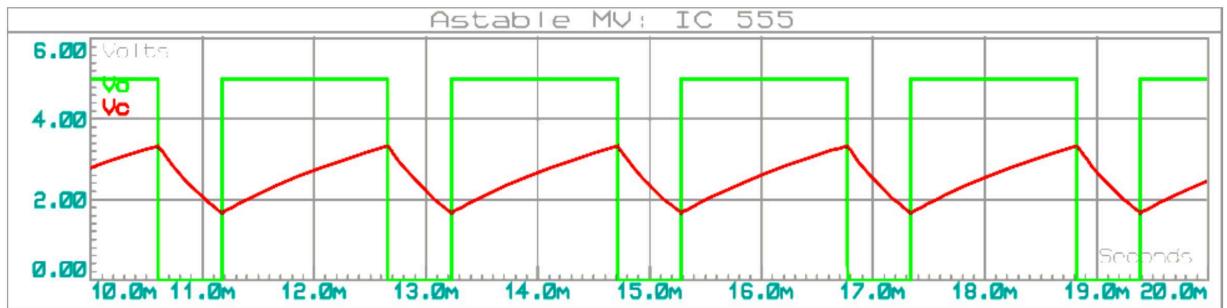
$$\text{Choose } C = 0.1\mu F \Rightarrow R = \frac{10m}{1.1 \times 0.1\mu F} = 90.9k \text{ Use } 100k \text{ std.}$$

## **PROCEDURE**

### **ASTABLE MULTIVIBRATOR USING 555**

- Set up the circuit and give  $+5V$  supply as  $V_{CC}$
- Observe the output waveform  $v_O$  and the capacitor waveform  $v_C$  simultaneously on the CRO
- Note the on and off times and compute the duty cycle of the output waveform

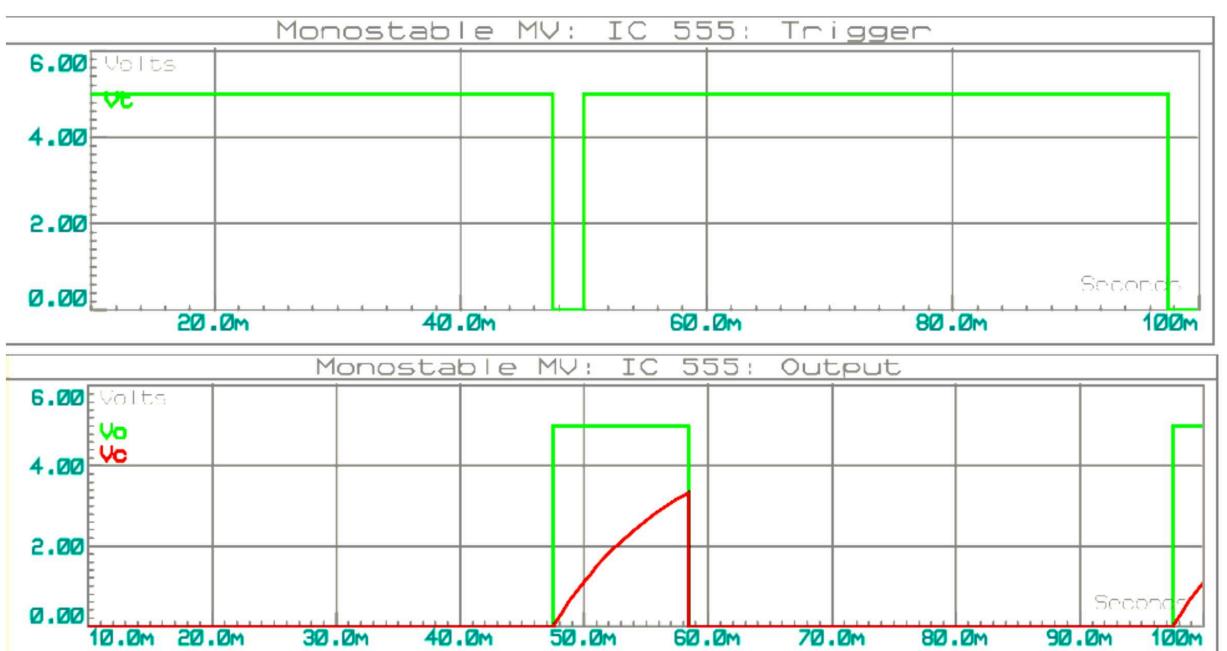
### Expected Waveforms: Astable Multivibrator using IC 555



### **MONOSTABLE MULTIVIBRATOR USING 555**

- Set up the circuit and give  $+5V$  supply as  $V_{CC}$
- At the trigger input give a square wave with 20Hz frequency and 95% duty cycle with  $5V$  amplitude ( $V_{max} = 5V$  and  $V_{min} = 0V$ )
- Observe the trigger waveform  $V_t$ , the output waveform  $V_o$  and the capacitor waveform  $V_c$  simultaneously on the CRO
- Measure the time period  $T$  of the output pulse

### Expected Waveforms: Monostable Multivibrator using IC 555



## **OBSERVATIONS**

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## **RESULTS**

The following circuits were designed and setup using timer IC 555.

- 1 An astable multivibrator for a duty cycle of 75% and a total time period of 2ms
  - Observed Duty Cycle =\_\_\_\_\_
  - Observed Total time period =\_\_\_\_\_
2. A Monostable multivibrator using IC 555 to produce a pulse of 10ms width
  - Observed pulse width =\_\_\_\_\_

EXPERIMENT .NO.9

### R-2R Ladder Type Digital to Analog Converter

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#### AIM

To design and setup a 3 bit R-2R ladder type DAC using op-amp IC 741

#### THEORY

A DAC(Digital to Analog Converter) accepts an  $n$ -bit input word  $b_1 b_2 \dots b_n$  with fractional binary value  $D_I$ , and produces an analog output proportional to  $D_I$  (Here  $b_1$  is the MSB and  $b_n$  is the LSB)

The output of a voltage-output DAC is,

$$v_O = KV_{REF}D_I = V_{FSR}(b_12^{-1} + b_22^{-2} + \dots + b_n2^{-n})$$

Where  $K \rightarrow$  scale factor;  $V_{REF} \rightarrow$  A reference voltage;  $V_{FSR} \rightarrow$  full-scale range

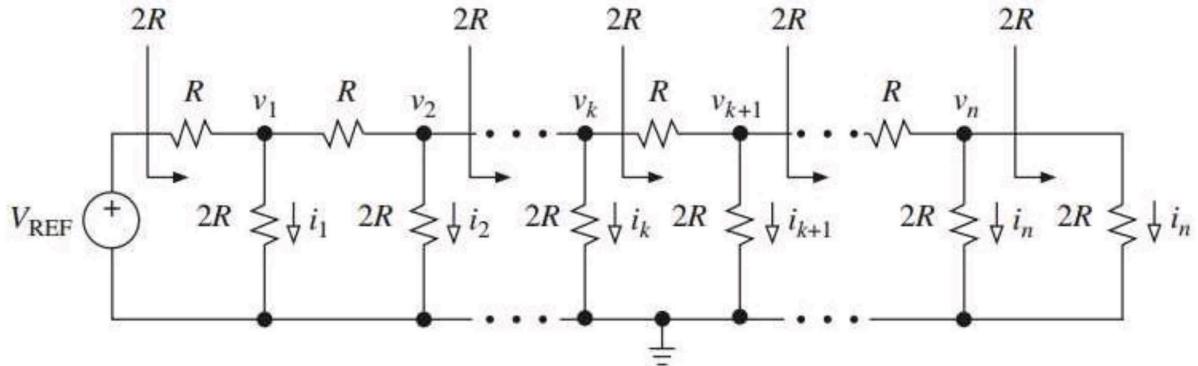
Depending on the input bit pattern,  $v_O$  can assume  $2^n$  different values ranging from 0 to the *full-scale value*  $V_{FSV} = (1 - 2^{-n})V_{FSR}$

Note that  $V_{FSV}$  is always 1 LSB short of  $V_{FSR}$

The quantity  $DR = 20\log_{10}(2^n)$  is called the *dynamic range* of the DAC

#### R-2R LADDER TYPE DAC

Most DAC architectures are based on the popular *R-2R* ladder shown below

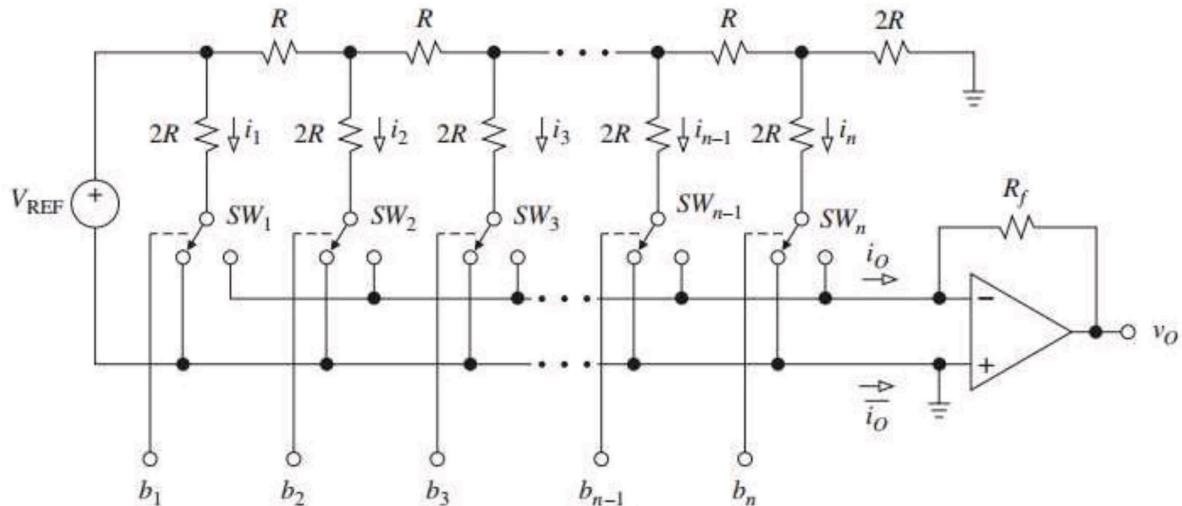


Starting from the right and working toward the left, it can be proven that the equivalent resistance to the right of each labeled node equals  $2R$ . Hence, the current flowing downward, away from each node, is equal to the current flowing toward the right; moreover, twice this current enters the node from the left.

Thus, the currents and, hence, the node voltages are binary-weighted,

$$i_{k+1} = \frac{1}{2} i_k \quad \text{and} \quad v_{k+1} = \frac{1}{2} v_k \quad \text{where } k = 1, 2, \dots, n-1$$

With a resistance spread of only 2-to-1,  $R - 2R$  ladders can be fabricated monolithically to a high degree of accuracy and stability.



**DAC using a current mode R-2R ladder**

We have  $i_1 = \frac{V_{REF}}{R} (2^{-1})$ ;  $i_2 = \frac{V_{REF}}{R} (2^{-2})$ ; ...;  $i_n = \frac{V_{REF}}{R} (2^{-n})$

These currents are diverted either to the ground bus ( $i_O^-$ ) or to the virtual-ground bus ( $i_O^+$ ) using the switches  $SW_k$  controlled by the bits  $b_k$

Thus we have,

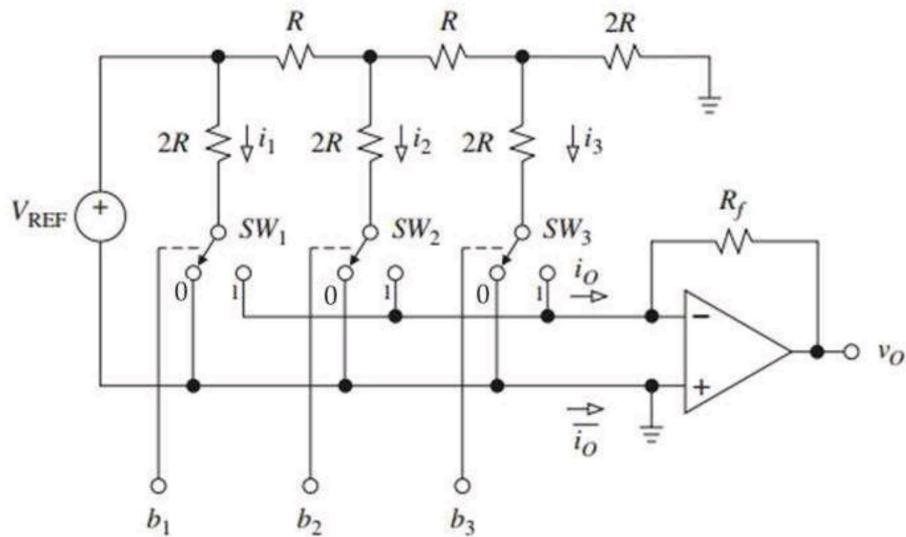
$$v_O = -i_O R_f = -\frac{R_f}{R} V_{REF} (b_1 2^{-1} + b_2 2^{-2} + \dots + b_n 2^{-n})$$

Which indicates that  $K = -\frac{R_f}{R}$

We can rewrite the above expression as,

$$v_O = -\frac{R_f V_{REF}}{2^n} (b_1 2^{n-1} + b_2 2^{n-2} + \dots + b_n) = -\frac{R_f V_{REF}}{2^n} D$$

Where  $D$  is the decimal representation for the  $n$  bit digital input word  $b_1 b_2 \dots b_n$



**3 bit DAC using a current mode R-2R ladder**

## DESIGN

For the 3 bit R-2R ladder DAC shown above, we have,

$$v_O = -\frac{R_f}{R} \frac{V_{REF}}{2^3} (b_1 2^2 + b_2 2^1 + b_3 2^0) = -\frac{R_f}{R} \frac{V_{REF}}{2^3} D$$

Let  $V_{REF} = 15V, R = 5K$  (Use two  $10k$  in parallel),  $2R = 10K, R_f = 3.3k$

Then  $v_O = -\frac{3.3k}{5k} \frac{15}{8} D = -1.2375D$

### PROCEDURE

- Setup the circuit and give supply voltages to the op-amp and the reference voltage to the R-2R ladder
- Set the input digital word  $b_1 b_2 b_3$  to 000 and note down the output voltage. Repeat this step for all 3 bit digital values up to 111 and tabulate the measurements. (To set a bit to 1, connect it to the non-inverting terminal of the op-amp, and to set the bit to 0, connect it to the inverting terminal)

### OBSERVATIONS

<b><math>b_1 b_2 b_3</math></b>	<b>Expected <math>v_o</math></b>	<b>Observed <math>v_o</math></b>
000	0V	
001	-1.24V	
010	-2.48V	
011	-3.71V	
100	-4.95V	
101	-6.19V	
110	-7.43V	
111	-8.66V	

### RESULTS

Designed and setup a 3 bit R-2R ladder type DAC using op-amp IC 741

EXPERIMENT .NO.10

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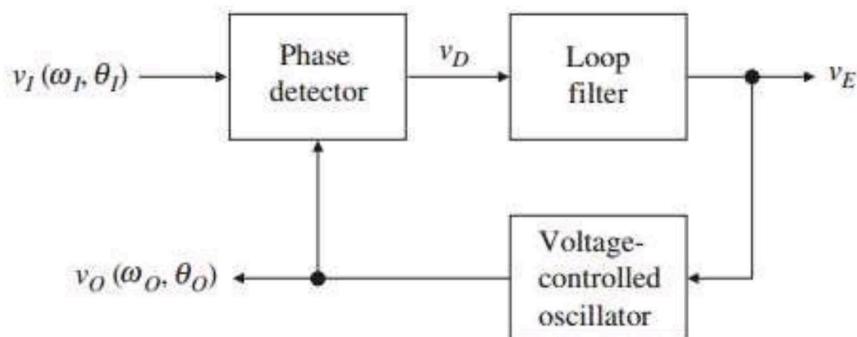
## Familiarization of PLL IC 565

### AIM

To familiarize the PLL IC NE565 and to measure its lock and capture range for a free running frequency of  $f_0 = 1.36\text{kHz}$

### THEORY

Phase-locked loop (PLL) is a frequency-selective circuit designed to synchronize with an incoming signal and maintain synchronization in spite of noise/variations in the incoming signal frequency. They are widely used as modulators, demodulators, oscillators, synthesizers, clock signal recovery circuits etc.



Basic PLL system comprises a phase detector, a loop filter, and a voltage-controlled oscillator (VCO). The phase detector compares the phase  $\theta_I$  of the incoming signal  $v_I$  against the phase  $\theta_O$  of the VCO output  $v_O$ , and develops a voltage  $v_D$  proportional to the difference  $\theta_I - \theta_O$ .  $v_D$  is sent through a low-pass filter to suppress high-frequency ripple and noise, and the result, called the *error voltage*  $v_E$ , is applied to the control input of the VCO to adjust its frequency  $\omega_O$ .

The VCO is designed so that with  $v_E = 0$  it is oscillating at some initial frequency  $\omega_0$  called the free-running frequency, so its characteristic is,

$\omega_O(t) = \omega_0 + K_o v_E(t)$  where  $K_o$  is the sensitivity of the VCO,  
in radians-per-second per

volt.

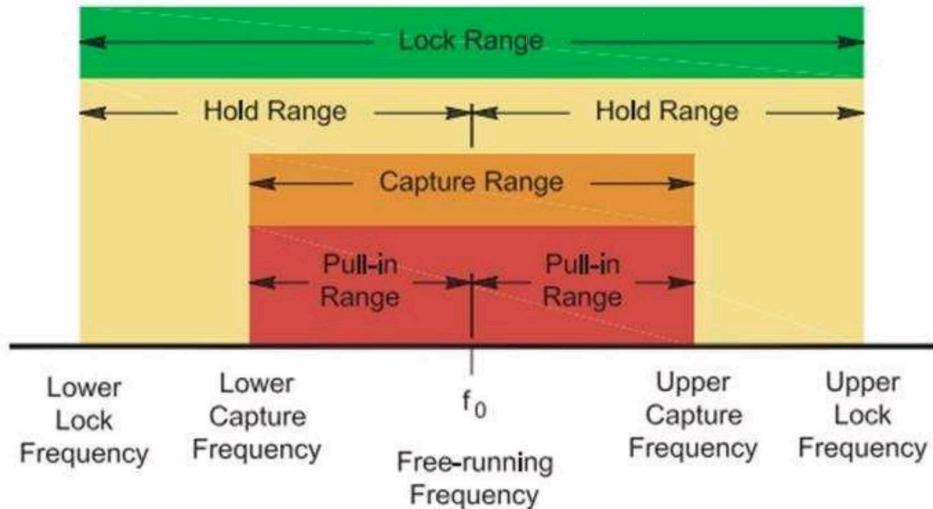
If an input is applied to the PLL with frequency  $\omega_I$  sufficiently close to  $\omega_0$ , an error voltage  $v_E$  will develop, which will adjust  $\omega_O$  until  $v_O$  is synchronized with  $v_I$ , i.e., until *for every input cycle there is one, and only one, VCO cycle*

PLL is now said to be *locked* on the incoming signal, and it gives  $\omega_O = \omega_I$  exactly

Should  $\omega_I$  change, the phase shift between  $v_O$  and  $v_I$  will start to increase, changing  $v_D$  and, hence, the control voltage  $v_E$ . This change in  $v_E$  is designed to adjust the VCO until  $\omega_O$  is brought back to the same value as  $\omega_I$

This self-adjusting ability by the feedback loop allows the PLL, once locked, to track input frequency changes. Since a change in  $\omega_I$  is ultimately reflected by a change in  $v_E$ , we use  $v_E$  as the output of the PLL whenever we wish to detect changes in  $\omega_I$ , as in FM and FSK demodulation

A PLL can be designed to lock on the incoming signal in spite of noise. A noisy input will generally cause the phase-detector output  $v_D$  to jitter around some average value. However, if the filter cutoff frequency is low enough to suppress this jitter,  $v_E$  will emerge as a clean signal, in turn resulting in a stable VCO frequency and phase

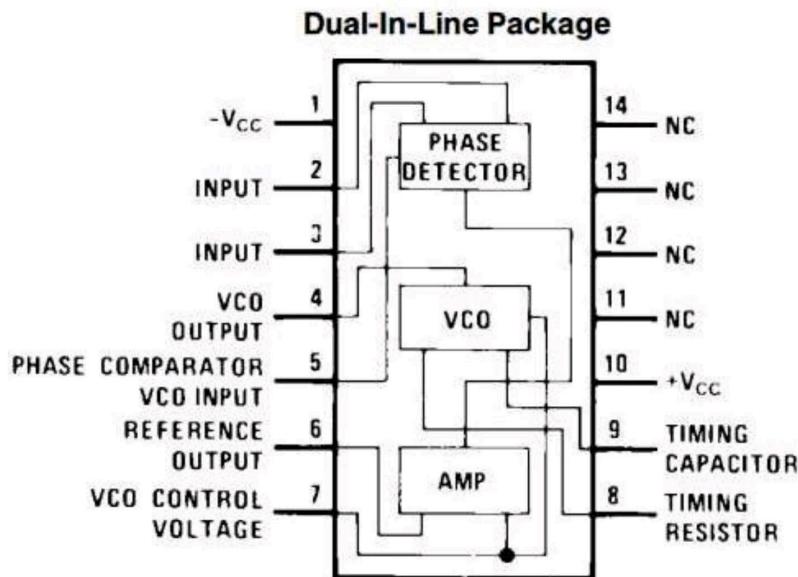


The capture range is the frequency range  $\pm\Delta\omega_C$ , centered about  $\omega_0$ , over which the loop can acquire lock. This range is affected by the filter characteristics, and gives an indication of how close  $\omega_I$  must be to  $\omega_0$  to acquire lock

The lock range(Hold-in range) is the frequency range  $\pm\Delta\omega_L$ , also centered about  $\omega_0$ , over which the loop can track the input once lock has been established. The lock range is affected by the operating range of the phase detector and the VCO.

Lock range shows how far the PLL frequency can track an input signal. Capture range shows how far from the free running frequency the VCO will move to lock onto an input signal. The capture range is never greater than the lock range.

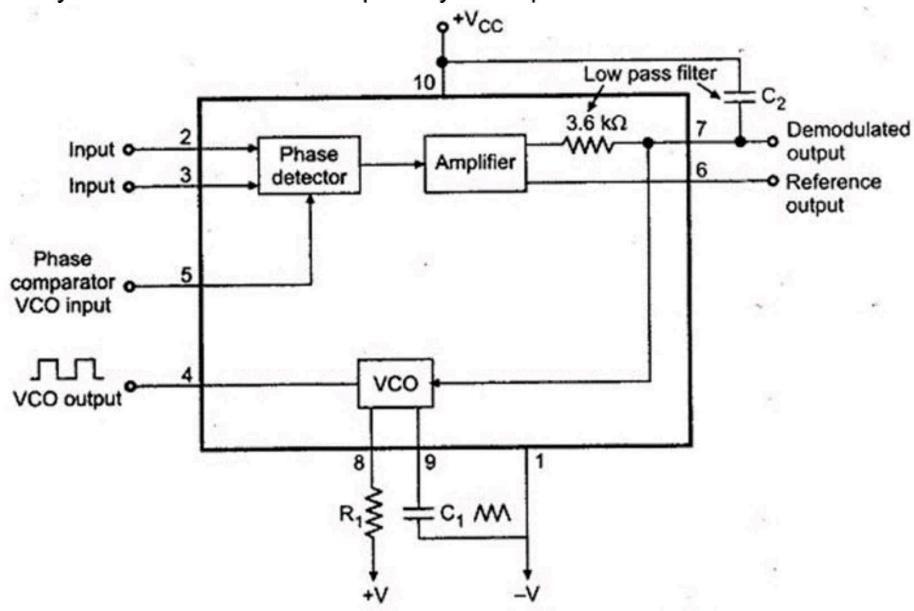
## PLL IC 565



The SE/LM565 are general purpose PLLs containing a stable, highly linear voltage controlled oscillator for low distortion FM demodulation, and a double balanced phase detector with good carrier suppression

The VCO frequency is set with an external resistor and capacitor. The output of VCO is capable of producing TTL compatible square wave.

The loop may be broken between the VCO and the phase detector for insertion of a digital frequency divider to obtain frequency multiplication.



Block diagram of IC 565 PLL

The free running frequency of the VCO(when i/p's 2 & 3 are shorted) is  $f_o = \frac{0.3}{R_T C_T}$  where  $R_T$  &  $C_T$  are the external resistor and capacitor connected to pins 8 & 9 respectively.

$R_T$  should be within the range  $2k\Omega < R_T < 20k\Omega$

An externally connected link between pins 4&5 connects the VCO o/p to the phase detector input, so as to compare  $f_i$  &  $f_o$

The  $3.6k\Omega$  internal resistance together with the external capacitor between pins 7 & 10 forms an RC filter

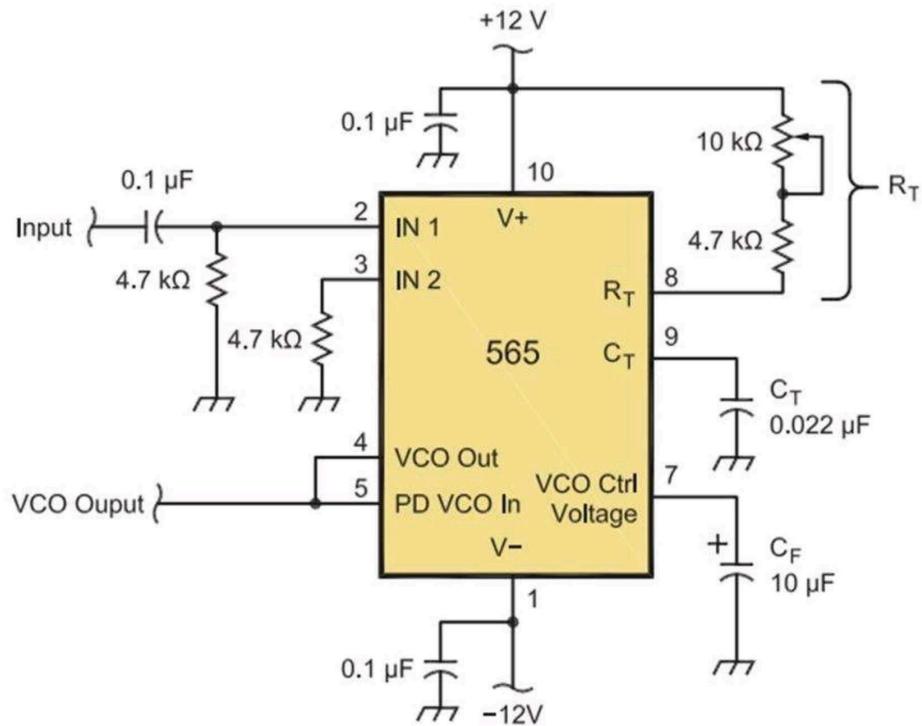
The VCO free running frequency  $f_o$  is adjusted externally with  $R_T$  &  $C_T$ , to be at the center of the i/p frequency range

565 IC is capable of locking to and tracking an i/p signal over  $\pm 60\%$  bandwidth wrt  $f_{out}$

The lock range of the PLL is,  $f_L = \pm \frac{8f_o}{V_S}$  where  $V_S = (+V) - (-V)$  is the total supply voltage

Capture range is,  $f_c = \pm \left( \frac{f_L}{2\pi * 3.6 * 10^3 * C} \right)^{0.5}$

## CIRCUIT DIAGRAM FOR MEASURING LOCK AND CAPTURE RANGE



## DESIGN

We have  $f_o = 1.36\text{kHz}$

$$\text{Let } C_T = 0.022\mu\text{F}, \text{ Then } R_T = \frac{0.3}{1.36k \times 0.022\mu} = 10k\Omega$$

The total supply voltage  $V_S = (+V) - (-V) = 24V$

$$\text{Expected Lock range } f_L = \pm \frac{8f_o}{V_S} = \pm \frac{8 \times 1360}{24} = \pm 453\text{Hz}$$

## PROCEDURE

- Setup the circuit and provide supply voltages
- Without applying any input signal, observe the output of the VCO at pin no.4 and measure the free-running frequency,  $f_0$  of the VCO.
- Now apply an input **square** wave signal of 1 Vpp with a frequency equal to the measured value of  $f_0$  to the PLL input
- Observe the input and the VCO output simultaneously on the CRO. The waveforms on both channels should be stable (because they are locked in frequency) but will be somewhat out of phase.
- Gradually reduce the input frequency till the PLL loses lock(which can be seen as one trace suddenly becoming unstable). Note down this frequency which is the **lower limit of the PLL's lock range**.
- Return the input frequency to  $f_0$  and then increase it until the PLL loses lock again at the **upper limit of the lock range**. Note down this frequency. Total lock range is the difference between these two frequencies.
- Slowly reduce the generator frequency until the PLL suddenly captures the input signal and locks again - both traces will be stable. Note down this frequency, which is the **upper limit of the PLL capture range** (It will be somewhat lower than the upper lock range limit)
- Change the generator frequency to something below the lower limit of lock range you measured previously. Slowly increase frequency until the PLL captures the input signal at the **lower limit of capture range**. Note down this value. The total capture range is the difference between these two frequencies.

## **OBSERVATIONS**

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## **RESULTS**

The PLL IC NE565 was familiarized by designing a PLL for a free running frequency of  $f_0 = 1.36\text{kHz}$

- Observed Value of free running frequency = \_\_\_\_\_
- Expected Lock range = \_\_\_\_\_
- Observed Lock range = \_\_\_\_\_
- Observed Capture range = \_\_\_\_\_