ECT301-LINEAR INTEGRATED CIRCUITS

S5 EC (B)

RINJU RAVINDRAN

Textbooks

1. Linear integrated circuits by Roy Choudhary and S.B. Jain 3/e
2. Op amps and linear integrated circuits by Gaykwad 4/e

Module 1:

Operational amplifiers(Op Amps):

- The 741 Op Amp
- Block diagram
- Ideal op-amp parameters
- Typical parameter values for 741
- Equivalent circuit
- Open loop configurations
- Voltage transfer curve
- Frequency response curve.

Differential Amplifiers:

- Differential amplifier configurations using BJT
- DC Analysis- transfer characteristics;
- AC analysis- differential and common mode gains, CMRR, input and output resistance, Voltage gain.
- Concept of current mirror-the two transistor current mirror, Wilson and Widlar current mirrors.

Module 2

Op-amp with negative feedback:

- Voltage Series, Voltage Shunt, current series and current shunt negative feedback
- Op Amp circuits with voltage series and voltage shunt feedback
- Virtual ground Concept

Op-amp applications:

- Summer, Voltage Follower-loading effects, Differential and Instrumentation Amplifiers, Voltage to current and Current to voltage converters, Integrator, Differentiator, Precision rectifiers, Comparators, Schmitt Triggers, Log and antilog amplifiers.

Module 3

Op-amp Oscillators and Multivibrators:

- Phase Shift and Wien-bridge Oscillators, Triangular and Sawtooth waveform generators, Astable and monostable multivibrators.

Active filters:

Comparison with passive filters, First and second order low pass, High pass, Band pass and band reject active filters, state variable filters.

Module 4

Timer and VCO:

- Timer IC 555- Functional diagram, Astable and monostable operations;. Basic concepts of Voltage Controlled Oscillator and application of VCO IC LM566

Phase Locked Loop :

Operation, Closed loop analysis, Lock and capture range, Basic building blocks, PLL IC 565, Applications of PLL.

Module 5

Voltage Regulators:

Fixed and Adjustable voltage regulators, IC 723 – Low voltage and high voltage configurations, Current boosting, Current limiting, Short circuit and Fold-back protection.

Data Converters:

Digital to Analog converters, Specifications, Weighted resistor type and R-2R Ladder type.

Analog to Digital Converters: Specifications, Flash type and Successive approximation type.

Integrated Circuits(ICs)

- A simple electronic circuit can be designed easily because it requires few discrete electronic components and connections.
- Designing a complex electronic circuit is difficult, as it requires more number of discrete electronic components and their connections.
- It is also time taking to build such complex circuits and their reliability is also less.
- If multiple electronic components are interconnected on a single chip of semiconductor material, then that chip is called as an **Integrated Circuit (IC)**. It consists of both active and passive components.
- Advs: compact size, lesser weight, low P consumption, reduced cost, increased reliability, improved operating speeds.

Types of Integrated Circuits

1. Analog Integrated Circuits

ICs that operate over an entire range of continuous values of the signal amplitude

- **Linear Integrated Circuits** – An analog IC is said to be Linear, if there exists a linear relation between its voltage and current.

  Eg: IC 741

- **Radio Frequency Integrated Circuits** – An analog IC is said to be Non-Linear, if there exists a non-linear relation between its voltage and current.
- A Non-Linear IC is also called as Radio Frequency IC.

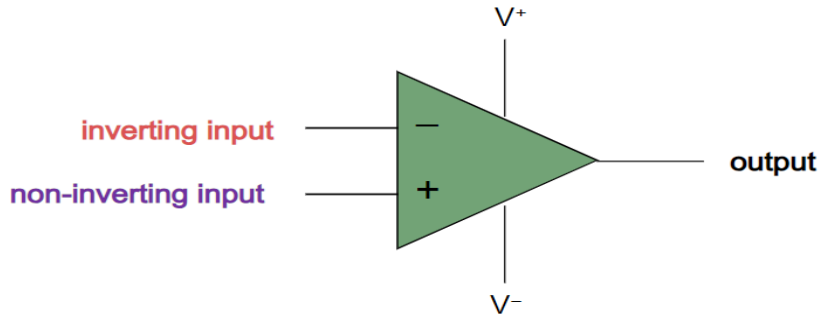
2. Digital Integrated Circuits

- If the ICs operate only at a few pre-defined levels instead of operating for an entire range of continuous values of the signal amplitude.

MODULE-1

OPERATIONAL AMPLIFIERS

Symbol of Operational Amplifier:



V+ ↔ $+V_{CC}$
V- ↔ $-V_{EE}$ or $-V_{cc}$

The Gain of OP-AMP is denoted by "A".

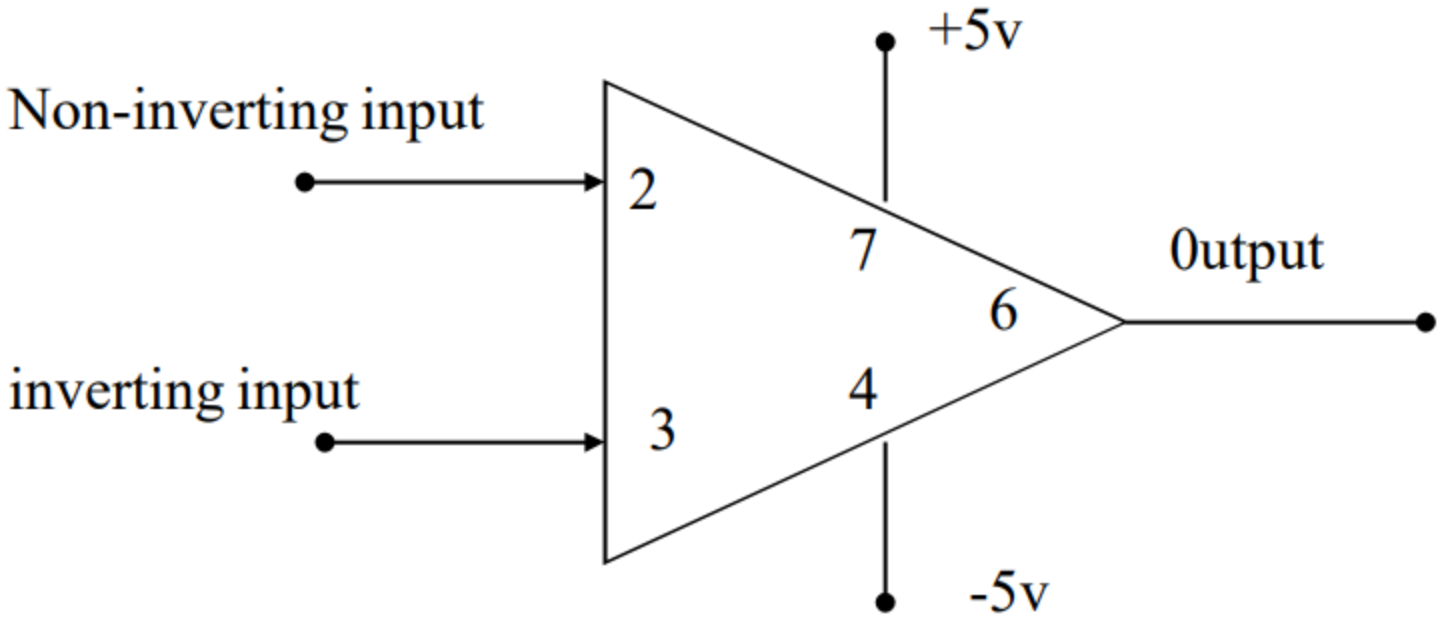
A = (Output/Difference Between Two Input Signals)

$= Vo / (V_1 - V_2)$

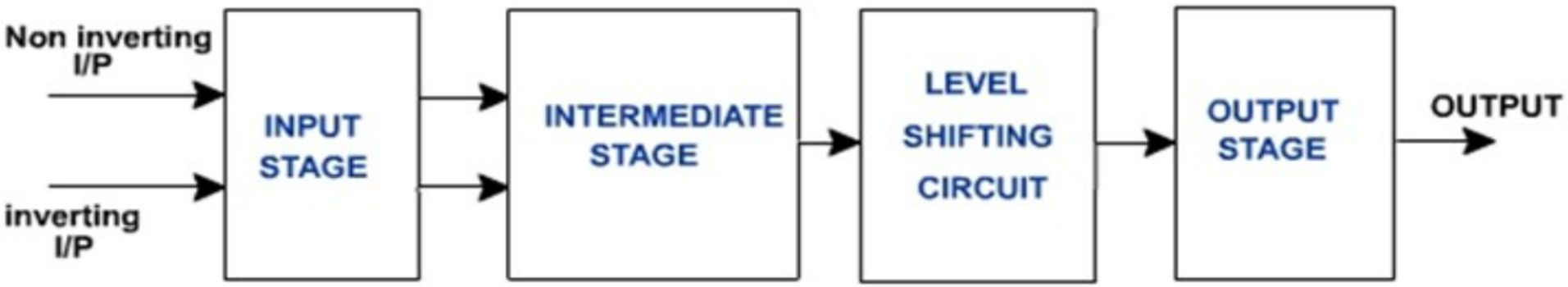
Where,

V_1 = Voltage Applied at Non-Inverting input
V_2 = Voltage Applied at Inverting input
V_o = Output Voltage

- An ac s/g or DC voltage applied to non inverting i/p (+)produces an inphase or same polarity s/g at o/p.
- An ac s/g or DC voltage applied to inverting i/p (-)produces an 180 deg out of phase or opposite polarity s/g at o/p.



Block Diagram of OP-AMP:



Input stage: It consists of a dual input, balanced output differential amplifier. Its function is to amplify the difference between the two input signals. It provides high differential gain, high input impedance and low output impedance.

Intermediate stage: The overall gain requirement of an Op-Amp is very high. Since the input stage alone cannot provide such a high gain. Intermediate stage is used to provide the required additional voltage gain.

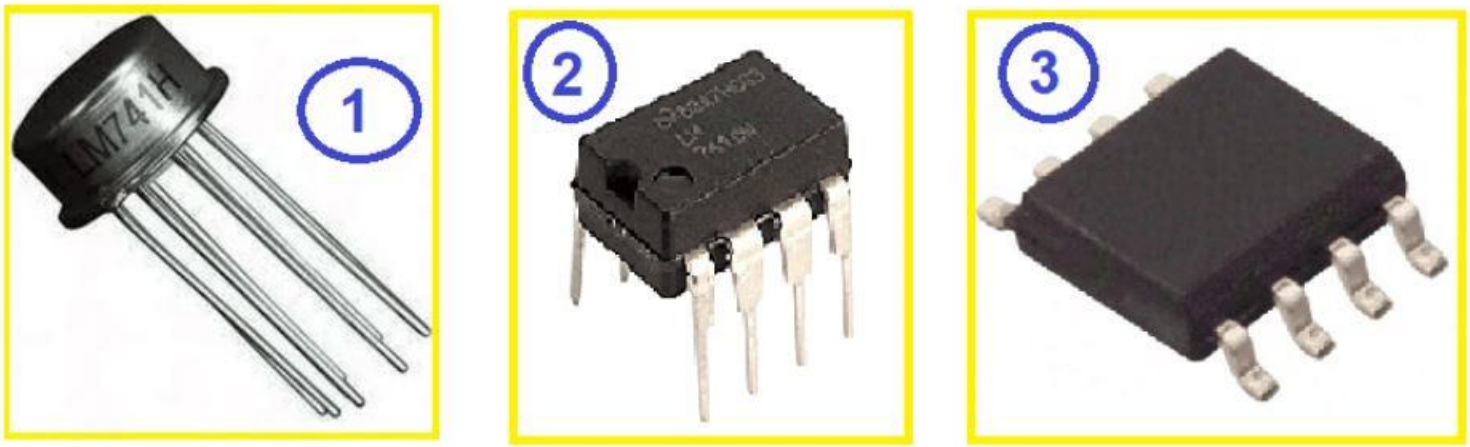
It consists of another differential amplifier with dual input, and unbalanced (single ended) output.

Buffer and Level shifting stage: As the Op-Amp amplifies D.C signals also, the small D.C. quiescent voltage level of previous stages may get amplified and get applied as the input to the next stage causing distortion the final output.

Hence the level shifting stage is used to bring down the D.C. level to ground potential, when no signal is applied at the input terminals. Buffer is usually an emitter follower used for impedance matching.

Output stage: It consists of a push-pull complementary amplifier which provides large A.C. output voltage swing and high current sourcing and sinking along with low output impedance.

IC 741 comes in the following form:

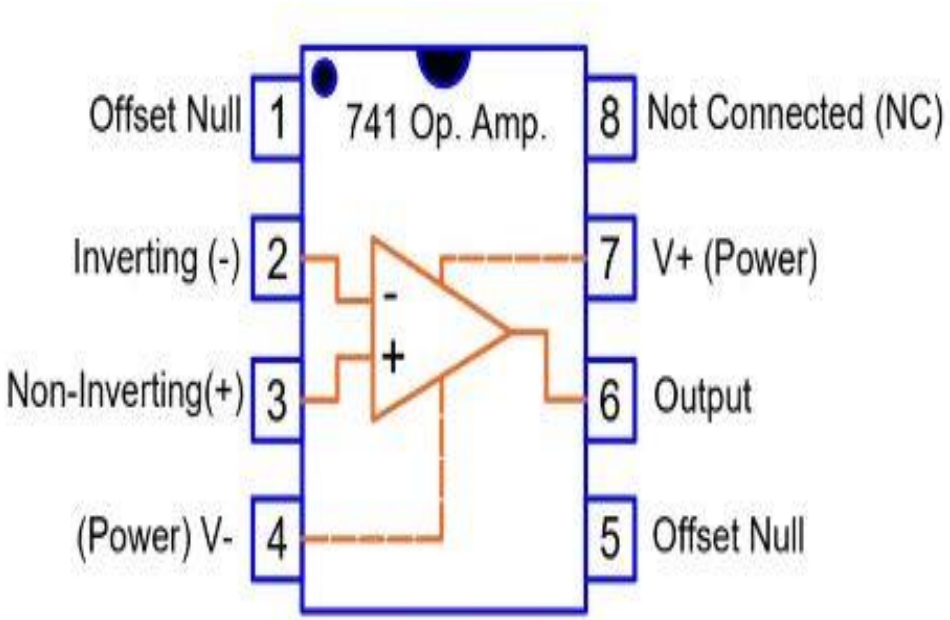


Different IC 741 Package

1.The metal can (TO) package or transistor pack
2.The dual-in-line package (DIP)
3. Flat pack

The selection of an IC package depends on the application.

IC 741


Offset Null
1
741 Op. Amp.
8
Not Connected (NC)
Inverting (-)
2
7
V+ (Power)
-
+
Non-Inverting(+)
3
6
Output
(Power) V-
4
5
Offset Null

- General purpose operation amplifier.
- The no. 741 indicates that the op amp has **7** functional pins, **4** input pins, and **1** output pin.
- It has high voltage gain.
- Used in wide range of applications like integrators, summing amplifier and general feedback applications.

Pin Description of IC 741

Pin 4 & 7: Power Supply

- Pin 7 is the (+)power supply terminal.
- Pin 4 is the (-) power supply terminal.
- The voltage between these two pin will be between 5V and 18V. Usually the supply at $+V_{CC}$ is +15V and that at $-V_{EE}$ is -15V.
- These power supply voltages must be with referenced to a common point or ground.

Pin 6: Output Pin

- The o/p from the op-amp is delivered to this pin.
- The voltage output received here depends on the feedback used and the voltage input given to the op-amp.
- When a high voltage is received at pin 6, it means the output voltage received is similar to the +ve supply voltage.
- If the output is said to be low, then the voltage at pin 6, corresponds to the -ve supply voltage.

Pin 2 & 3 : Input Pins

- Pin2 is the inverting input of the op-amp. Pin 3 is the non-inverting input of the op-amp.
- When the voltage at pin 2 is greater than the voltage at pin 3, it means that the inverting terminal has higher voltage. So, the output signal would be low.
- When the voltage value at pin 3 is higher than the voltage at pin 2, the voltage level at non-inverting input is high. So, the output signal obtained would be high.

Pin 1 & 5: Offset Null

- Op-amp 741 provides high gain.
- Thus, minor differences in voltages at the inverting and non-inverting terminals can influence output.
- To nullify this influence, an offset voltage may be applied to the op-amp. This offset voltage is applied at pin 1 and 5.
- It is usually done by using a potentiometer.

Pin 8: Not Connected

- It is not connected to any part inside the IC 741. It is a dummy lead that is used to fill the void space in standard 8 pin packages.

Op amp Parameters

DC characteristics

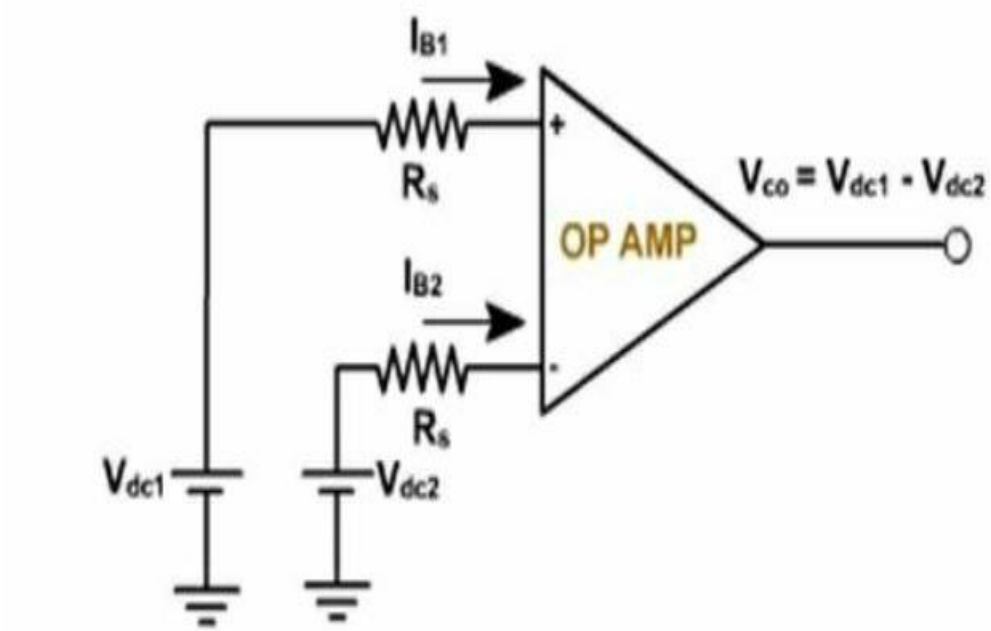
- In an ideal op-amp, we assume that no current is drawn from the source.
- Its response is also indep of temp.
- However a real op amp will draw current from the source into the op amp i/ps
- Respond differently to I and V due to mismatch in transistors.
- Shifts its opr. with temp.

- These non ideal DC characteristics that add error components to the dc o/p V are:
  - i/p bias current
  - i/p offset current
  - i/p offset voltage
  - Thermal drift

  These will affect steady state (DC) response of op amp only.

1. Input offset Voltage V_{io}

- It is the voltage that must be applied between the two input terminals of the op amp to obtain zero volts at the output.
- In an ideal op-amp, the DC voltage of the $V_{(+)}$ and $V_{(-)}$ terminals match exactly when the input voltage (V_i) is 0 V.
- But in reality, there are diff.s in input impedance and input bias current between the $V_{(+)}$ and $V_{(-)}$ terminals, causing a slight diff in their voltages.
- This diff called input offset voltage is multiplied by a gain, appearing as an output voltage deviation from the ideal value.
- It is necessary to select an op-amp with low input offset voltage.



$$V_{io} = V_{dc1} - V_{dc2}$$

The input offset is typically 2mV to <6mV.

2. Input offset Current I_{io}

- The input terminals conduct a small value of dc current to bias the input transistors.
- Since the input transistors cannot be made identical, there will always be some small diff btw the currents into inv and non inv terminals.
- There exists a difference in bias currents.
- This algebraic diff is called as I_{io}

$$I_{io} = | I_{B1} - I_{B2} |$$

- The difference between the bias currents at the input terminals of the op- amp is called as input offset current.
- $I_{io(max)}$ for 741 IC is 200nA .

3. Input bias current I_B

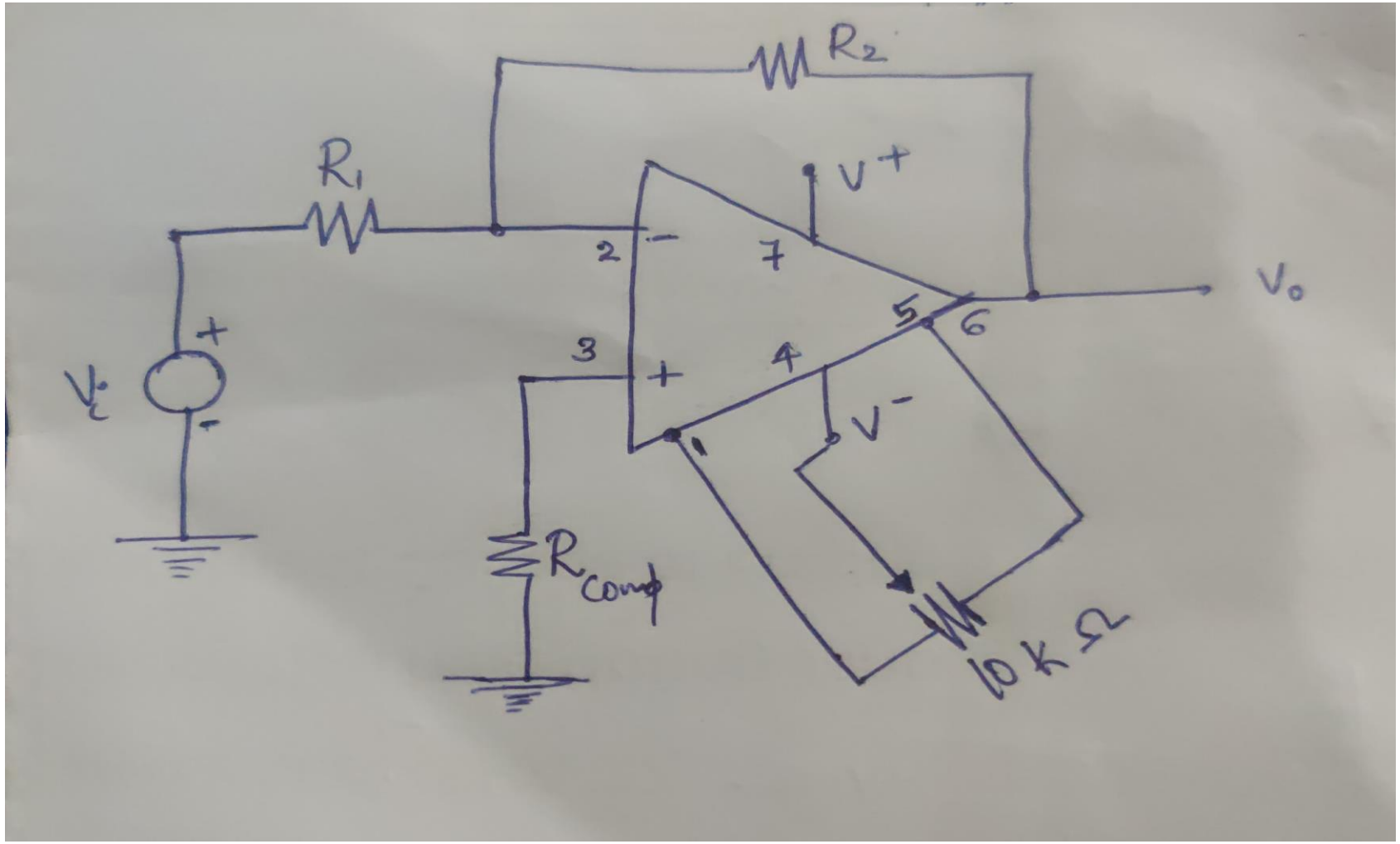
- Op amp input stage is a differential amplifier made of BJT or FET
- In either case, the i/p transistors must be biased into the linear region by supplying I into base by ext ckt.
- In ideal opamp, we assume no I is drawn from i/p terminals
- But practically i/p terminals do conduct a small value of dc current to bias the i/p transistors.
- I_B is the avg of currents that flow into inv & non inv i/p terminals of op amp.

$$I_B = (I_{B1}+I_{B2})/2$$

- $I_{B\,(max)} =$ 700nA for 741 IC

4. Output offset Voltage

- It is the V that appears at o/p for 0 i/p.
- May be due to i/p offset V or i/p bias current or both.
- Many op amp provide offset compensation pin to nullify offset V.
- For 741 op amp, a 10Kohm potentiometer is connected btw offset null pins 1 &5 and wiper connected to –ve supply pin 4.
- Position of wiper is adjusted to nullify the o/p offset V.


R2
R1
V+
2
7
Vo
5
6
+
Vi
-
3
+
4
V-
1
Rcomp
10 kΩ

5.Thermal drift

- Bias current, offset V & I change with temp.
- A ckt nulled at 25 deg may not remain so when temp rises to 35 deg
- This is called drift.
- Offset I drift in nA/deg C
- Offset V drift in mV/deg C

AC characteristics

- For small signal sinusoidal applications, we must know AC characteristics.

1.Frequency Response

* Magnitude plot and phase plot

- Gain of op amp is a fn of freq.
- At a given freq, the gain will have a specific magnitude as well as a phase angle.
- Graph of mag. of gain vs freq------ magnitude response plot.
- Graph of phase shift vs freq-------- phase response plot.
- To accommodate large range, freq(Hz) is in log scale & gain in dB.

Generally for an amplifier, as operating freq. increases,

1. Gain of ampr decreases
2. Phase shift btw o/p and i/p signals increases to **negative**.

- **Change in gain or phase as a fn of freq**. is bcoz of the internally integrated capacitor or stray capacitances.
- These capacitance are due to :

1. <u>Physical characteristics of semicondr devices (BJTs or FETs)</u>

✓ BJTs /FETs contains junction capacitors.

$$X_c = 1/2\pi f_c$$

✓ at low freqs, X_c is high. So act as Open ckt.

✓ at high freqs, X_c is low. So there will be a finite value of capacitance.

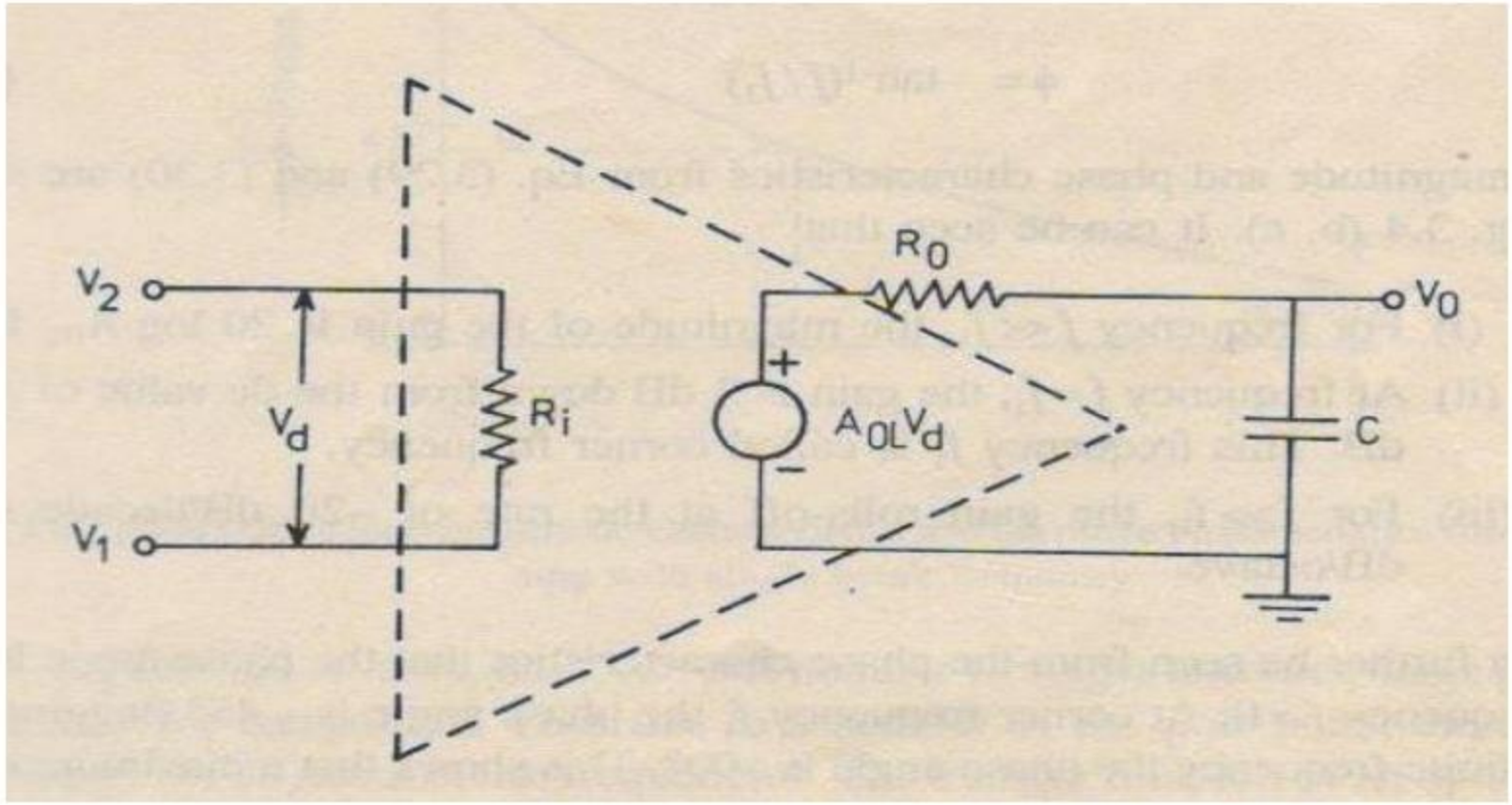
2. Internal construction of an op amp.

- In op amp, many transistor, resistors, sometimes capacitor are integrated on same material----substrate-----act as insulator & separates the components.
- Various components are connected by conducting path and the paths are separated by insulators.
- But 2 conducting paths separated by an insulator ------act as capacitor.

Phase shift increases to negative wrto freq.

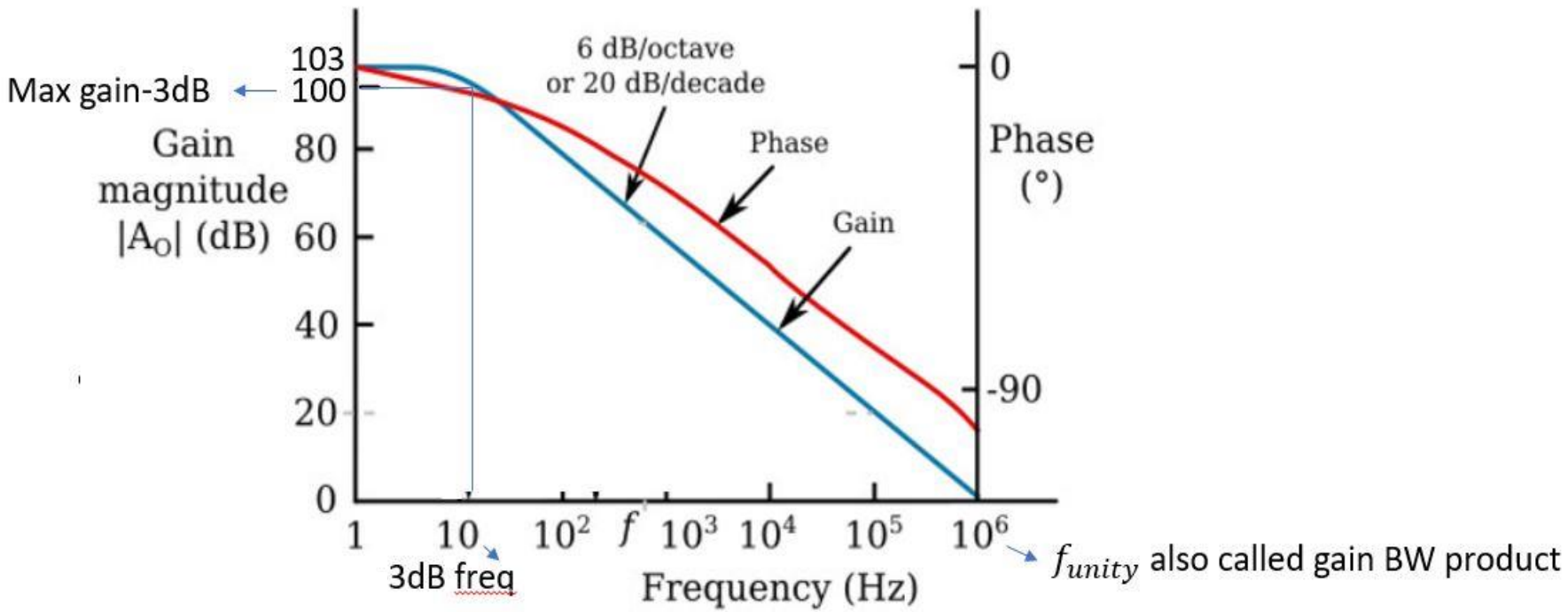
- Due to inherent characteristics of components and the way they interact within the ckt.
- As the freq of i/p s/g increases, behaviour of components like capacitors, transistors starts to dominate the ckt's response.
- Eg: capacitors can introduce a phase shift btw V across them and I flowing thru them.
- This phase shift becomes more pronounced as the freq increases.
- The cumulative phase shift caused by these components can lead to an overall –ve phase shift wrto freq.
- That is, o/p signal's phase lags behind i/p signal's phase.

High Freq model of an Op Amp

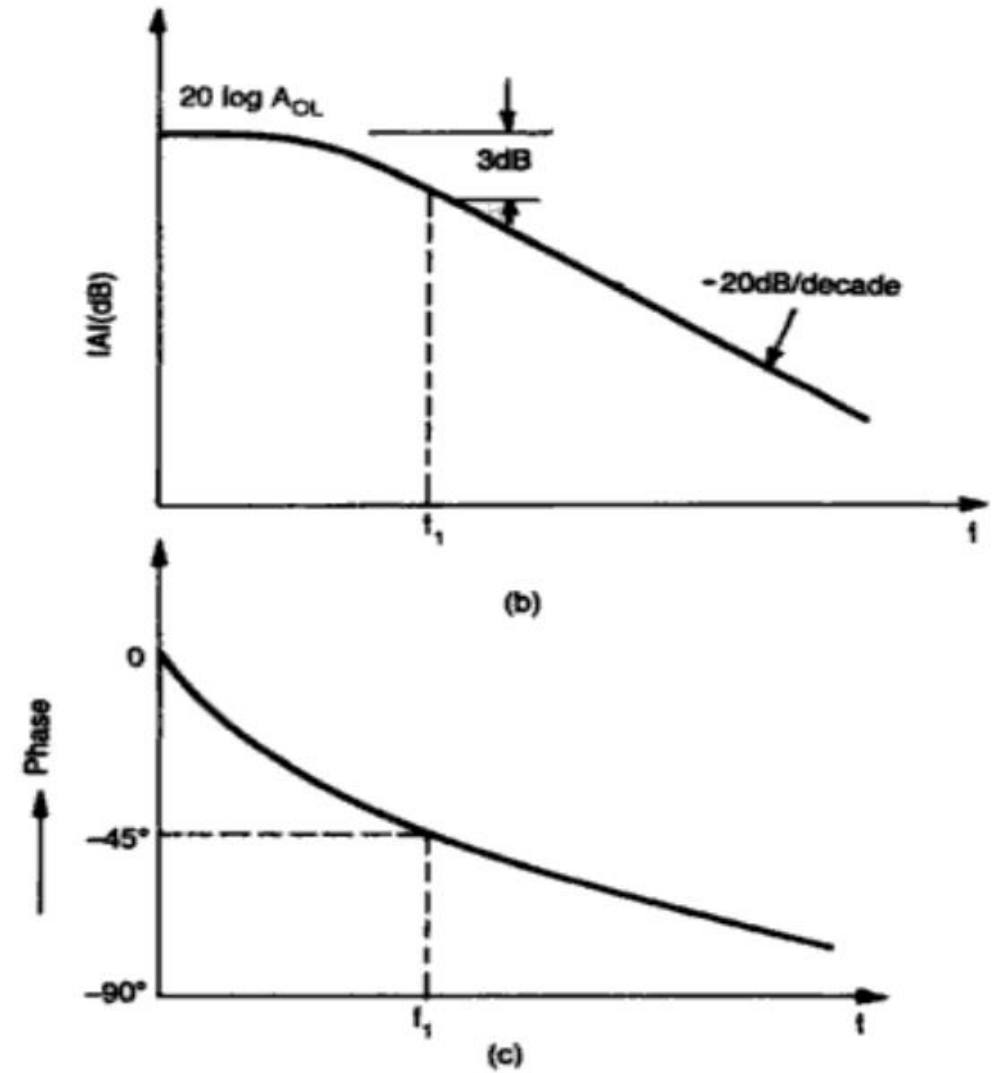


*For an op amp with only 1 corner freq, all cap. effects can be represented as single capacitor

Frequency response of op amp: magnitude and phase responses.



Frequency response of typical operational amplifier.


20 log A_{OL}
3dB
-20dB/decade
|A|(dB)
f_1
f
(b)
0
Phase
-45°
-90°
f_1
f
(c)

- 741 IC has upper cut off freq of 10Hz. Beyond this point, gain decreases at the rate of 20 dB/decade until it reaches unity at 1 MHz.
- OL gain is approx. constant from 0Hz to break freq or corner freq fc.
- When i/p s/g freq = break freq fc, gain is 3dB less than max value. So fc is called -3dB freq.
- At some point, OL gain in dB =0

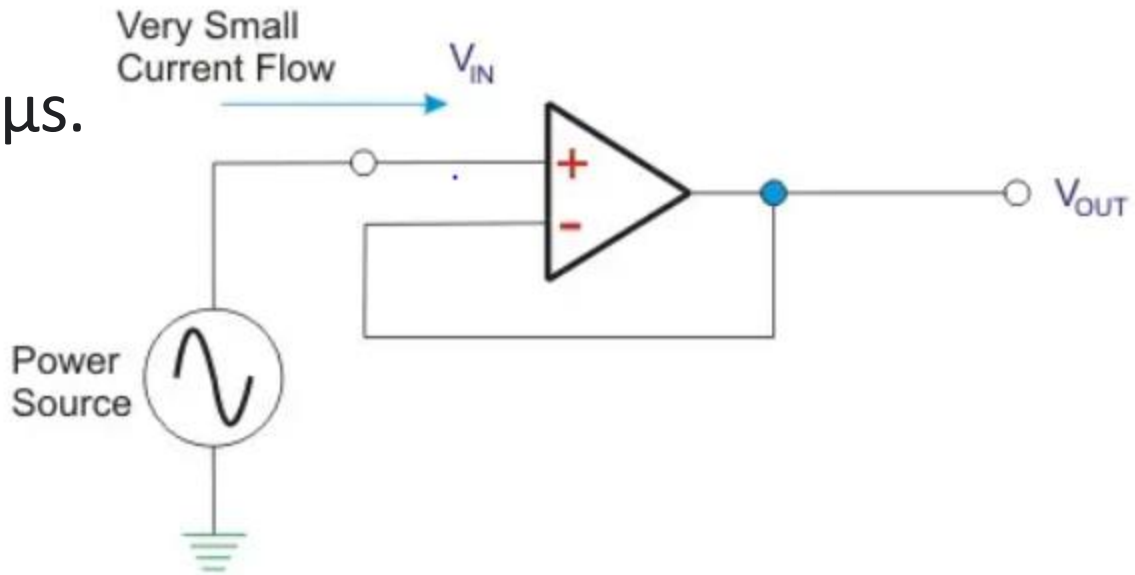
ie, gain =1. this freq is unity gain bandwidth or gain bandwidth product

2.Slew Rate

- Slew rate is defined as the maximum rate of change of an op amps output voltage, and is given in units of V/µs.
- It is measured by applying a large signal step, such as 1V, to the input of the op amp, and measuring the rate of change from 10% to 90% of the output signal's amplitude.
- Slew rate of 10 V/ µs means that when a large step change is placed on the input, the electronic device would be able to provide an output 10 V change in 1 µs.

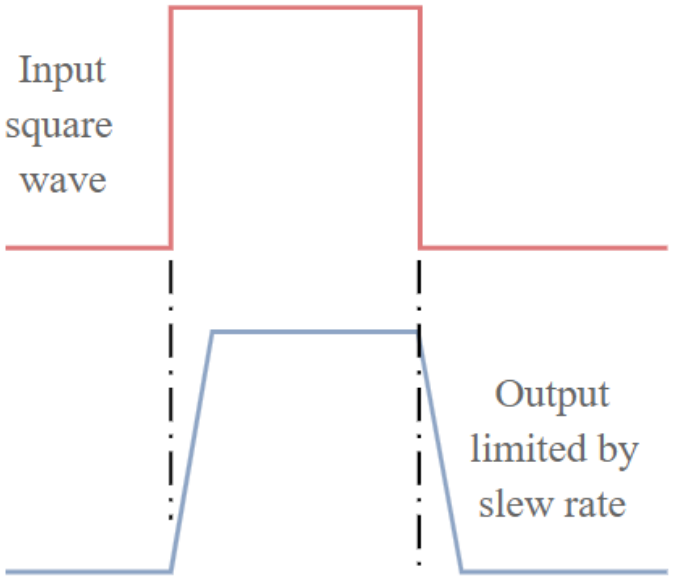
$$S = \frac{dV_0}{dt}|_{maximum}\ Volts/\mu S$$

- The SR changes with the voltage gain change. Therefore, it is generally specified at unity (+1) gain condition.
- Consider a unity gain ckt .
- Here o/p V follows changes in i/p V --- V follower.
- But if rate of change of i/p is greater than SR, o/p will not be able to change fast and o/p gets distorted.
- Ideal SR = ∞
- Practically for 741 IC, SR is 0.5 V/µs.

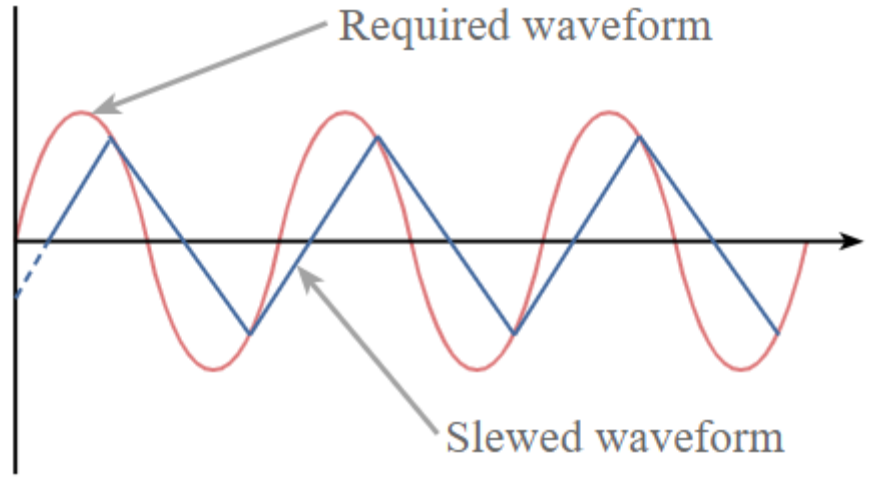


- The main causes for the slew rate limitations are caused by the

1. internal frequency compensation included in most op amps to provide stability, especially at HFs.
2. the small internal drive currents, as well as any limitations in the output stage. These all combine together to limit the rate at which o/p can change from 1 level to another.



Effect of op amp slew rate



Op amp slewing distortion (limit)

- There is usually a capacitor within or outside op amp to prevent oscillations.
- If it is a part of IC, opamp is internally compensated.
- If not, need to provide ext compensation for stability of op amp.
- This cap. prevents the o/p V from responding to a fast changing i/p.
- If i/p is a large amp sine wave,

$V_s = V_m \sin \omega t$,

then o/p voltage $V_o = V_m \sin \omega t$

Then dV/dt = $\omega V_m \cos \omega t$

This has max value when cos ωt=1.

SR= max of dV/dt = $\omega V_m = 2\pi f V_m$ volts/sec = = $\frac{2\pi f V_m}{10^6}$ volts/ μs

- Max freq at which we can obtain an undistorted o/p V of peak value V_m is

$$f_{max}\ (\text{Hz}) = \frac{\text{SR}}{2\pi\ V_m} = \frac{\text{SR}}{6.28\ V_m}$$

f_{max} is the full power response.

3.Common mode rejection ratio (CMRR)

- CMRR is a measure of the capability of an op-amp to reject a signal that is common to both inputs.
- Ideally, CMRR is ∞
- the ratio of the differential-mode gain to common-mode gain .
- DA amplifies diff btw 2 i/p s/gs
- Since noise is undesirable and appears equally at both i/ps of op amp, DA cancel out or reject these signals.

$$\text{CMRR} = 20 \log |A_d / A_c|$$

- The common mode signal is when both of the inputs of the amplifier have the same voltage or they have a “common voltage” across them.
- Under this condition, the output of the amplifier should be zero or the amplifier should reject the signal and not amplify it.
- DA with 2 i/ps V1 & V2

difference s/g $V_d = V_1 - V_2$----------(1)

common mode s/g $V_c = \frac{V_1+V_2}{2}$ ----------(2)

- Eventhough DA is symmetric ckt, mismatch of transistor causes gain at o/p wrt inv to be diff wrt non inv terminal.

$$V_o = A_1\ V_1 + A_2 V_2$$ ----------(3)

A1 is the voltage amplification (gain) from i/p 1 to o/p under the cond i/p 2 is grnded

A2 is the voltage amplification (gain) from i/p 2 to o/p under the cond i/p 1 is grnded

From (1) & (2)

$V_1 = V_c + \frac{V_d}{2}$ ----------(4)

$V_2 = V_c - \frac{V_d}{2}$ ----------(5)

(4) & (5) in (3)

$V_0 = A_c\, V_c + A_d V_d$

A_c : common mode gain

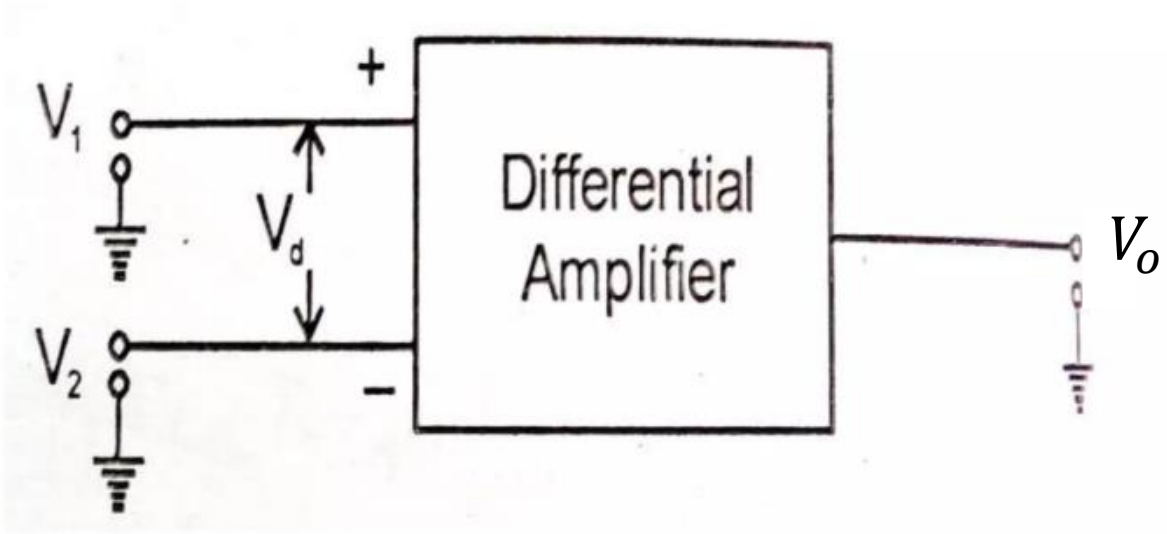
A_d : differential mode gain

Ideally A_c =0; CMRR = ∞

Practically CMRR is large

For 741 IC, CMRR= 90 dB

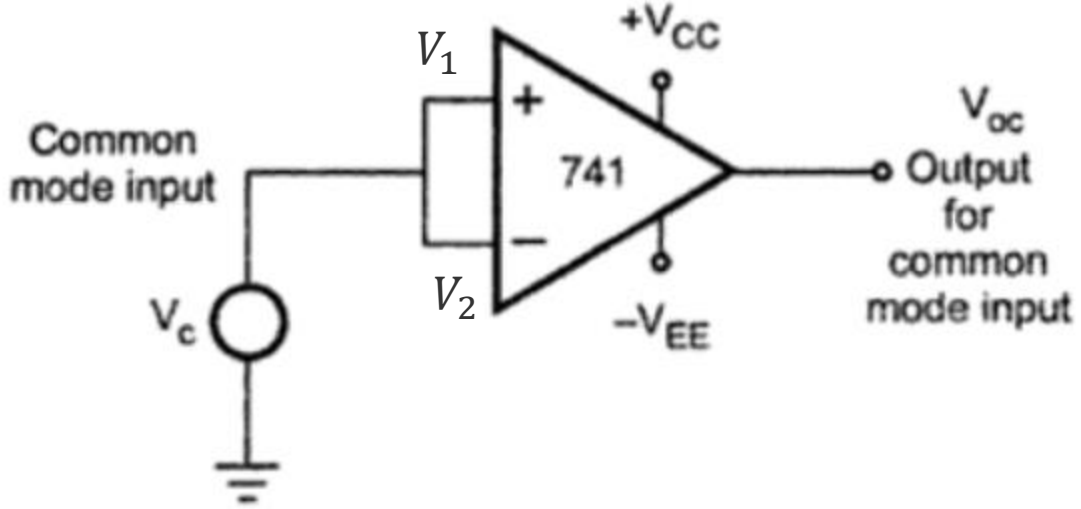
Block diagram of differential amplifier



Measurement of A_c

A_d is Open loop voltage gain A_{OL}

A_c is measured using the given ckt.



The common mode input V_c is applied to both the terminals of op-amp & o/p V_{oc} is measured.

$$A_c = \frac{V_{oc}}{V_c}$$

4. Supply Voltage Rejection Ratio(SVRR)

- Also called as power supply RR(PSRR) or power supply sensitivity (PSS).
- Ratio of change in i/p offset voltage to the change in supply voltage.
- It will adversely affect the performance of an op amp
- So SVRR should be as low as possible.

$$SVRR = \Delta V_{io} / \Delta V$$

For 741 IC, SVRR is 150 µV/ V.

Input capacitance

- Eqvt capacitance that can be measured at eithr inv or non inv i/p with other terminal connected to grnd.
- For 741 IC, value is 1.4pF

Output resistance

- Eqvt res measured btw o/p & grnd.
- For 741, i/p res is relatively low $75\boldsymbol{\Omega}$

Differential i/p resistance

Eqvt res that can be measured at either inv or non inv i/p with other terminal connected to grnd.

For 741, i/p res is relatively high 2M$\boldsymbol{\Omega}$

Input Voltage Range

- It is the range of a common mode i/p s/g for which a differential ampr remains linear.
- used to determine the degree of matching btw inv and non inv i/p terminals.
- For 741, range of i/p common mode V is $\pm 13V$.
- ie, common mode voltage applied at both i/p terminals can be as high as +13V or as low as -13V.

Gain Bandwidth Product

- Gain bandwidth product (GB) is the bandwidth of the op-amp when the open loop voltage gain is reduced to 1.
- For 741 op-amp, GB is 1MHz. GB is also known as closed-loop bandwidth, unity gain bandwidth and small signal bandwidth.
- 3dB freq or cut off freq is 10Hz.
- GBW pdt is a constant value for an op amp. As gain increases, BW decreases and vice-versa.

Output Voltage Swing

- The difference between positive saturation voltage and negative saturation voltage is called output voltage swing.
- The ac o/p V swing is the max unclipped peak to peak o/p V that an op amp can produce.

Output Short-Circuit Current

- Value of output current that is allowed to flow by the internal short circuit protection circuitry, if the output is shorted to ground. It is denoted by $I_{SC.}$

Characteristics of an ideal op amp

An ideal op-amp would exhibit the following electrical characteristics.

1. **Infinite input resistance** ($R_i=\infty$) so that almost any signal source can drive it and there is no loading of the preceding stage.
2. **Zero output resistance** ($R_O=0$) so that the output can drive an infinite number of other devices.
3. **Infinite voltage gain** ($A= \infty$).
4. **Zero offset voltage** ($V_{io}=0$) so that zero output voltage when input voltage is zero.

5. Infinite bandwidth (BW=∞) so that any frequency signal from 0 to ∞ Hz can be amplified without attenuation.

6. Infinite common-mode rejection ratio (CMRR=∞) so that the output common-mode noise voltage is zero.

7. Zero Supply Voltage Rejection Ratio (SVRR=0) so that output voltage does not change due to fluctuation in supply voltage.

8. Infinite slew rate (SR=∞) so that output voltage changes occur simultaneously with input voltage changes.

Ideal and Typical Values of IC LM741

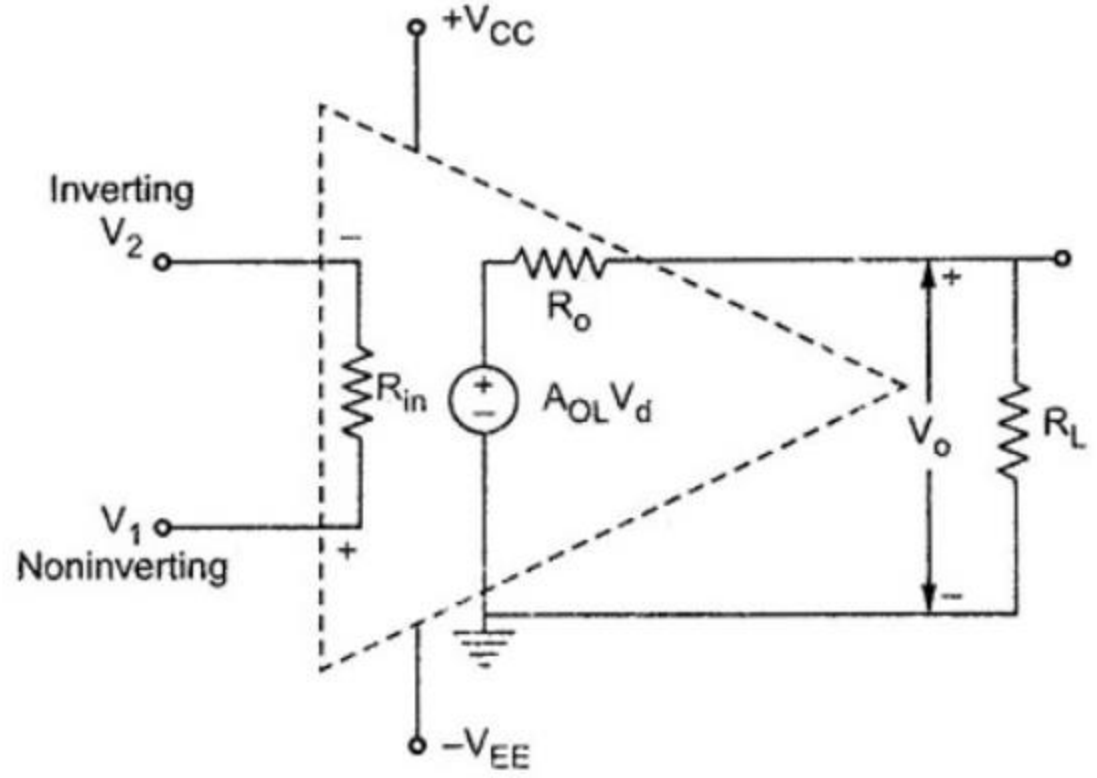
Sr. No.	Characteristics	Ideal Value	Typical Value
1	Input Resistance	∞	2MΩ
2	Output resistance	0	75Ω
3	Voltage gain	∞	200000
4	Bandwidth	∞	1 MHz
5	CMRR	∞	90 dB
6	Slew rate	∞	0.5 V/μs
7	Offset voltage	0	2 mV
8	SVRR/ PSRR	0	30 μV/V

Parameters of op amp

- Differential Input Resistance
- Input Capacitance
- Output Resistance
- Input Offset Voltage
- Input Offset Current
- Input Bias Current
- Common-Mode Rejection Ratio (CMRR)
- Supply Voltage Rejection Ratio (SVRR)
- Output Voltage Swing
- Slew rate
- Gain Bandwidth Product
- Output short ckt current

Equivalent Circuit of Practical Op Amp:

- The Circuit which represents op-amp parameters in terms of physical components, for the analysis purpose is called equivalent circuit of an op-amp.
- The Equivalent Circuit of Practical Op Amp is shown in the Fig.



- The Eqvt Ckt of Practical Op Amp shows the op-amp parameters like input resistance, output resistance, the open loop V gain in terms of ckt components like R_{in}, R_o etc.
- The op-amp amplifies the difference between the two input voltages.

$$\mathbf{V_o = A_{OL}\, V_d = A_{OL}\,(V_1 - V_2)}$$

where

- A_{OL} = Large signal open loop voltage gain.
- V_d = Difference voltage $V_1 - V_2$
- V_1 = Noninverting input voltage with respect to ground
- V_2 = Inverting input voltage with respect to ground
- R_{in} = Input resistance of op-amp
- R_o = Output resistance of op-amp
- $A_{OL}\, V_d$ = Thevenin eqvt V source
- R_o=Thevenin's equivalent resistance looking back into the output terminals.

In practical op amp,

$R_{in} \neq \infty$

$A_{OL} \neq \infty$

$R_o \neq 0$

The output voltage is directly proportional to the difference voltage V_d.

Thus the output polarity gets decided by the polarity of the difference voltage V_d.

Open loop op amp configurations

- Open-loop means no feedback in any form is fed to the input from the output.
- that is no connection btw i/p & o/p.

- $V_o = A_{OL} V_d$
- Practically $A_{OL} \neq \infty$

Eg : if V_d = v1-v2 = 1µV, $A_{OL} = 10^6$,

then V_o =1 V

But if V_d =v1-v2 = 1V, $A_{OL} = 10^6$,

then o/p can never be 10^6

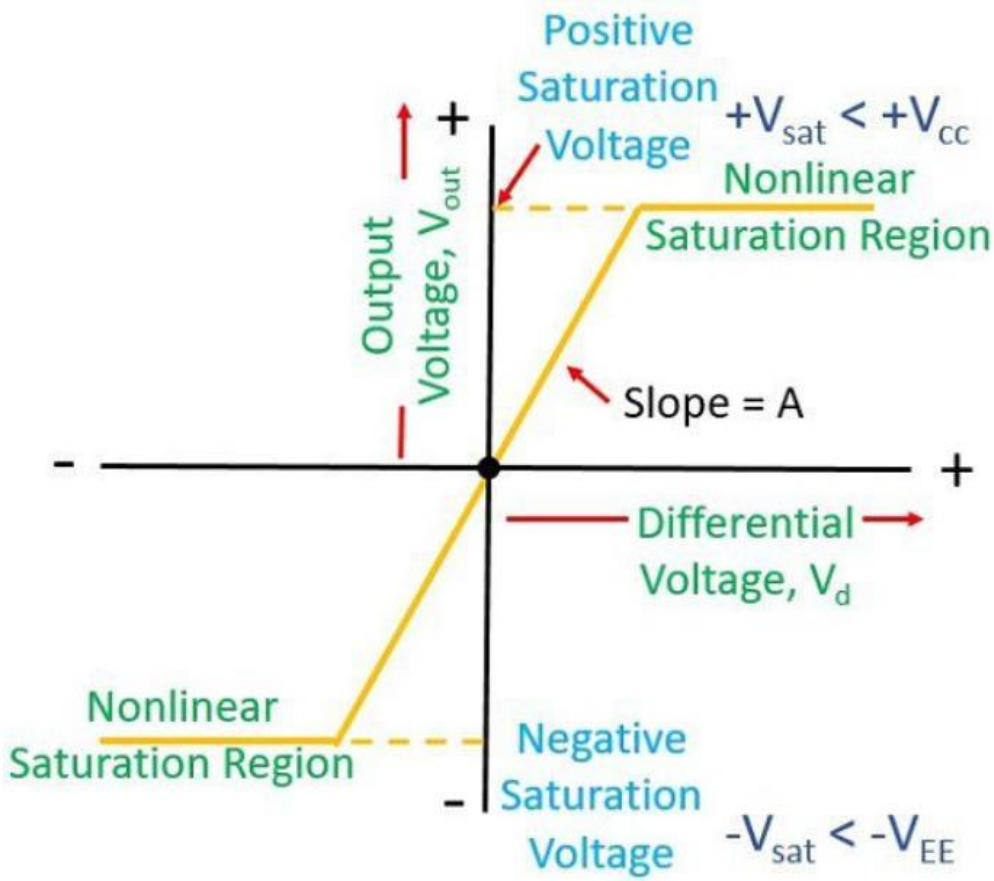
By increasing the input voltage, we find that the output voltage is limited by the dc supply voltages + V_{CC} and -V_{EE}.

The op-amp cannot give out any more than about 85% of the voltage, it is being supplied with (±15 V). We say that the op-amp saturates. (active region to saturation region).

For supply Voltages of ±15 V, µA741 IC, o/p V cannot go beyond $\pm 13V$. This is called o/p saturation voltages.

Ideal Voltage transfer Curve of op amp

This curve is drawn between the output voltage V_{out} and difference input voltage V_d where gain A is kept constant.
It is ideal because while drawing the curve we assume that **output offset voltage =0**.



- the output voltage V_{out} increases in direct proportion to the differential input voltage V_d until it attains **saturation value**, after which it becomes **constant**.
- V_{out} cannot exceed positive and negative saturation voltage.

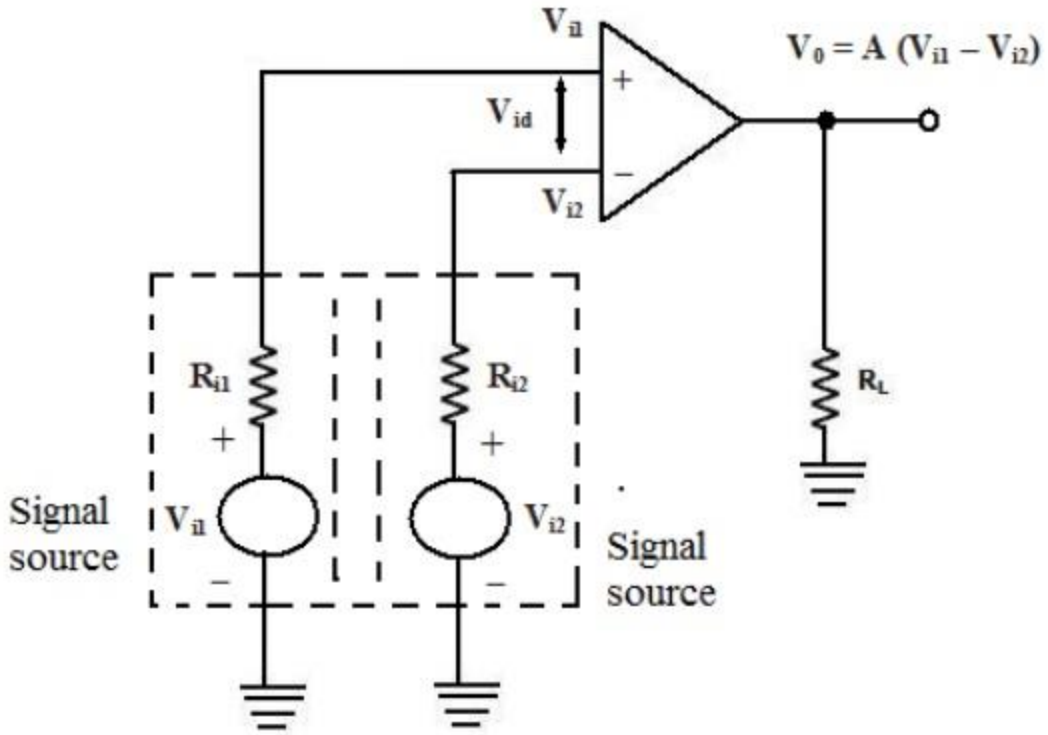
So when connected in open loop, the op-amp functions as a very high gain amplifier.

There are 3 OL configurations of op-amp :

1. differential amplifier
2. Inverting amplifier
3. Non-inverting amplifier

- The above classification is made based on the no. of inputs used and the terminal to which the input is applied.
- The op-amp amplifies both ac and dc input signals. Thus, the input signals can be either ac or dc voltage.

1.Differential Amplifier



Open - loop Differential Amplifier

- The input voltages are V_{i1} and V_{i2}.
- The source res Ri1 and R_{i2} are negligibly small in comparison with the very high input res offered by the op-amp, and thus the V drop across these source resistances is assumed to be 0.
- Therefore $V_1 = V_{i1}$

  $V_2 = V_{i2}$

- The output voltage V_0 is given by

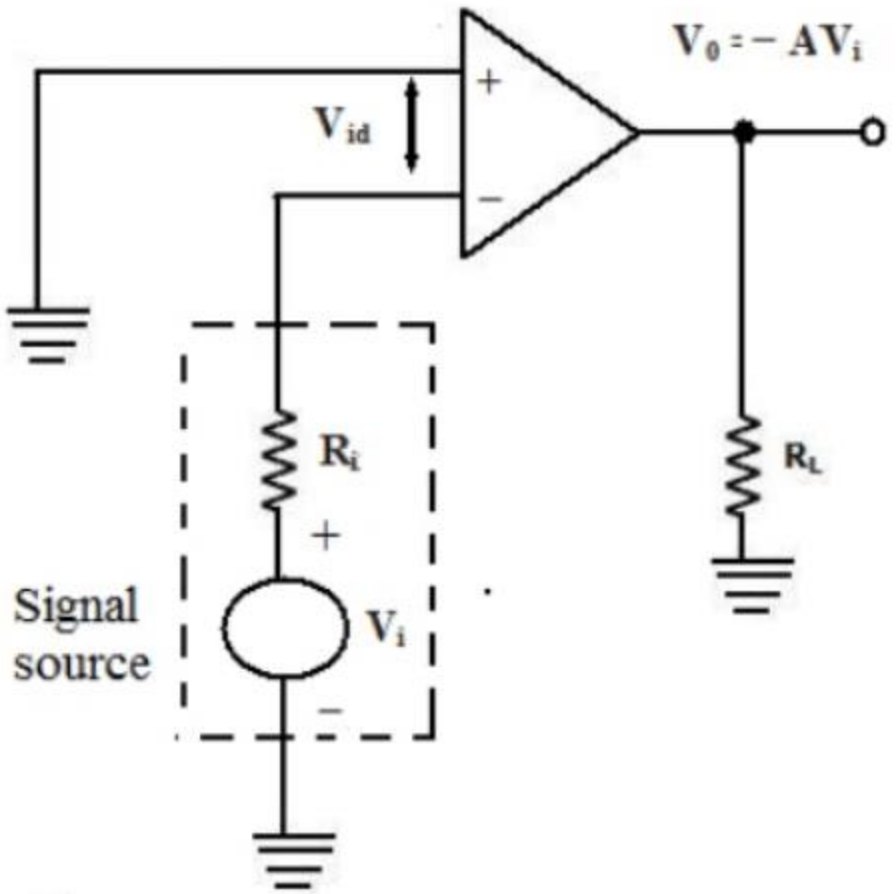
$$V_0 = A(V_{i1} - V_{i2})$$

where A is the large signal V gain. Thus the V_0 is equal to the voltage gain A times the diff btw the two input voltages.

This is the reason why this configuration is called a differential amplifier.

In open – loop configurations, the large signal voltage gain A is also called open-loop gain .

2.Inverting Amplifier



Open - loop Inverting Amplifier

- In this configuration the input signal is applied to the inverting input terminal of the op-amp and the non-inverting input terminal is connected to the ground.)

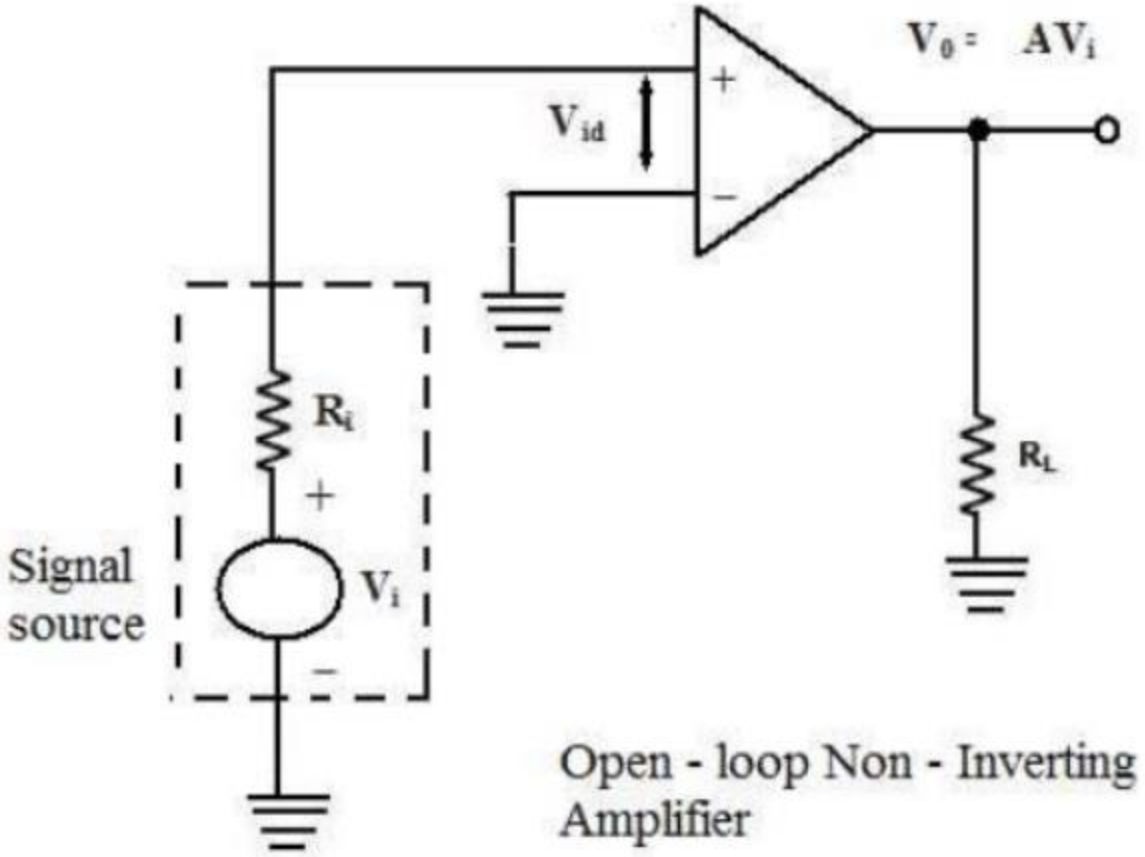
$$V_1 = 0 \ \& \ V_2 = V_i$$

$$V_0 = A(V_1 - V_2) = A(0 - V_i)$$

$$V_0 = -AV_i$$

- The output voltage is 180^0 out of phase with respect to the input.
- Thus, in an inverting amplifier, the input signal is amplified by the open-loop gain A and –ve sign shows that o/p s/g is out of phase wrt i/p by 180^0

3. Non-inverting Amplifier



Open - loop Non - Inverting Amplifier

- The input signal is applied to the non-inverting input terminal of the op-amp and the inverting input terminal is connected to the ground.
- The input signal is amplified by the open loop gain A and the output is in-phase with input signal.

$$V_1 = V_i \ \& \ V_2 = 0$$

$$V_0 = AV_i$$

- In all the above open-loop configurations, only very small values of input voltages can be applied.
- Even for voltages levels slightly greater than zero, the output is driven into saturation, which is observed from the ideal transfer characteristics of op-amp.
- Thus, when operated in the open-loop configuration, the output of the op-amp is either in negative or positive saturation, or switches between positive and negative saturation levels.
- This prevents the use of open – loop configuration of op-amps in linear applications.

Limitations of OL Opamp configurations:

1. In OL configurations, clipping of the o/p waveform can occur when the o/p voltage exceeds the saturation level of op-amp. In all the above open-loop configurations, only very small values of input voltages can be applied.
2. The OL gain of the op amp is not a constant and it varies with changing temperature and variations in power supply. Also, the bandwidth of most of the OL op amps is negligibly small. This makes the OL configuration of op-amp unsuitable for ac applications.

- For the reason stated, the open – loop op-amp is generally not used in linear applications. However, the OL op amp configurations find use in certain nonlinear applications such as comparators, square wave generators and astable multivibrators.
- To increase the utility of op amp, we use –ve feedback which will reduce gain and prevent o/p from going to saturation resulting in linear operation.
- Op amp with f/b is called as closed loop amplifier.

Numerical Problems

1. The SR of an op amp is 6V/µs when closed loop gain is unity. The amplified o/p s/g is observed to be a pure sinusoid. $V_{out} = V_{max}\cos \omega t$ provided the frequency of this signal doesnot exceed a certain limit. Find the value of this limiting freq before the o/p s/g is distorted by slew rate limit if (i) V_{max}=1V (ii) V_{max}=10 V
2. For a typical op amp if the compensating capacitor is 35pF & this internal capacitor charging current is 15µA, find the slew rate. If peak value of i/p is 12 V, determine the max possible frequency of i/p V that can be applied to get undistorted o/p?

3. An op amp has a differential gain of 5000 and CMRR of 80 dB. If common mode i/p V is 2 V, calculate o/p V due to common mode i/p.
4. An op amp has a GBW pdt of 1MHz. Calculate max achievable gain when op amp is operating at a freq of 10KHz
5. A 741 IC is used as inverting ampr with a gain of 50. Volt gain vs freq curve of IC is flat upto 20KHz. What max peak to peak i/p signal can be applied without distorting the o/p?

Answers

1. SR = 2πfV_m

   f_{max}= SR/ 2πV_m

   In first case V_{max}= 1V ---------- f_{max}=0.955MHz

   In second case V_{max}= 10V ------- f_{max}=95.5KHz

2. C=35pF

   I=15µA

   we have capacitive current I = C dv/dt

   SR = dv/dt = I/C = 0.4285 V/µs

   V_m=12V ---------- f_{max}= SR/ 2πV_m = 5.684KHz

3. CMRR = 80dB $= 20log_{10}(A_d/A_c)$

$A_c = A_d$/ CMRR = 0.5

$V_{out\_cm} = A_c * V_{cm} = A_c * 2 = 1V$

4. $A_{max=}$GBW/f =100

5. Gain =50

SR=0.5V/µs

SR = 2πf$V_m/10^6$ V/µs ---------- V_m=3.98V peak

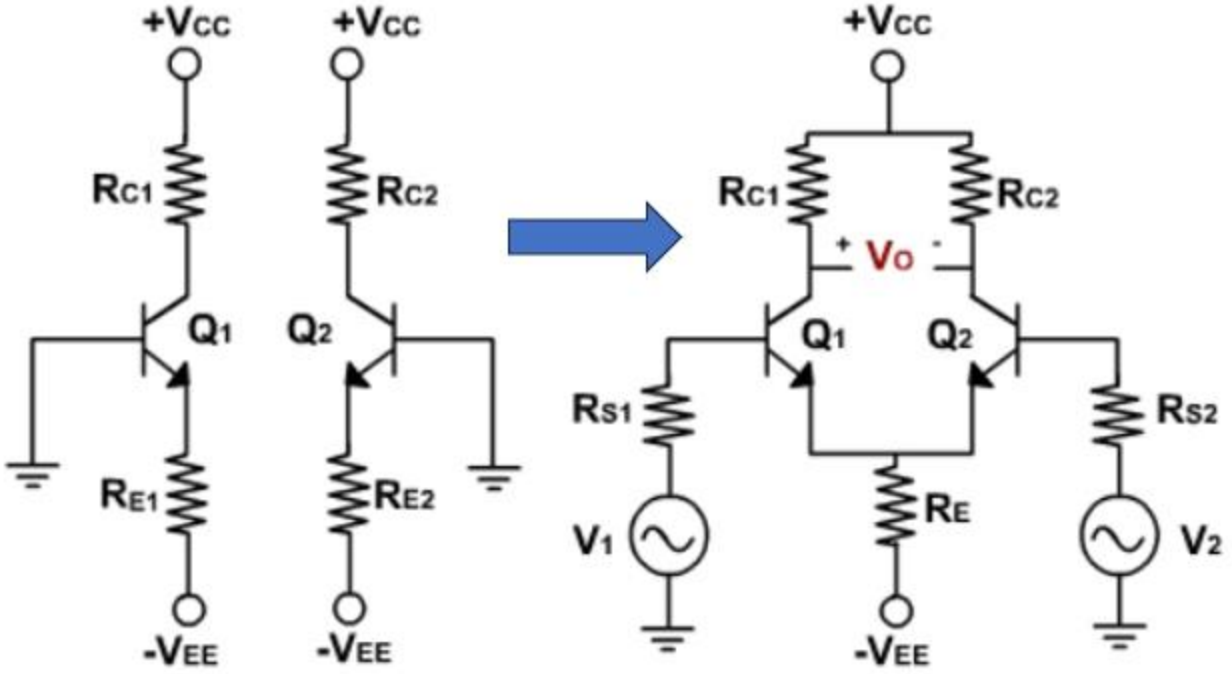
so o/p V_0= 7.96 V peak to peak

Hence for the o/p to be undistorted sine wave, max i/p s/g shud be < 7.96/50

= 159 mV peak to peak

DIFFERENTIAL AMPLIFIERS

- Basic building block of an op-amp.
- The function is to amplify the difference between two input signals.



- The two transistors Q_1 and Q_2 have identical characteristics.
- The res.s of the ckts are equal, i.e. $R_{E1} = R_{E2}$, $R_{C1} = R_{C2}$ and the magnitude of $+V_{CC}$ is equal to the magnitude of $-V_{EE}$. These voltages are measured wrt ground.
- To make a DA, the two ckts are connected as shown in **fig.**
- The two $+V_{CC}$ and $-V_{EE}$ supply terminals are made common bcz they are same.
- The two emitters are also connected and the parallel combination of R_{E1} and R_{E2} is replaced by a res R_E.
- The two i/ps v_1 & v_2 are applied at the base of Q_1 and at the base of Q_2.
- The o/p V is taken between two collectors. The collector resistances are equal $R_C = R_{C1} = R_{C2}$.
- Ideally, the o/p V is 0 when the two inputs are equal. When $v_1 > v_2$, the output voltage with the same polarity appears. When $v_1 < v_2$, the output voltage has the opposite polarity.

- The Diff ampr.s are of different configurations.

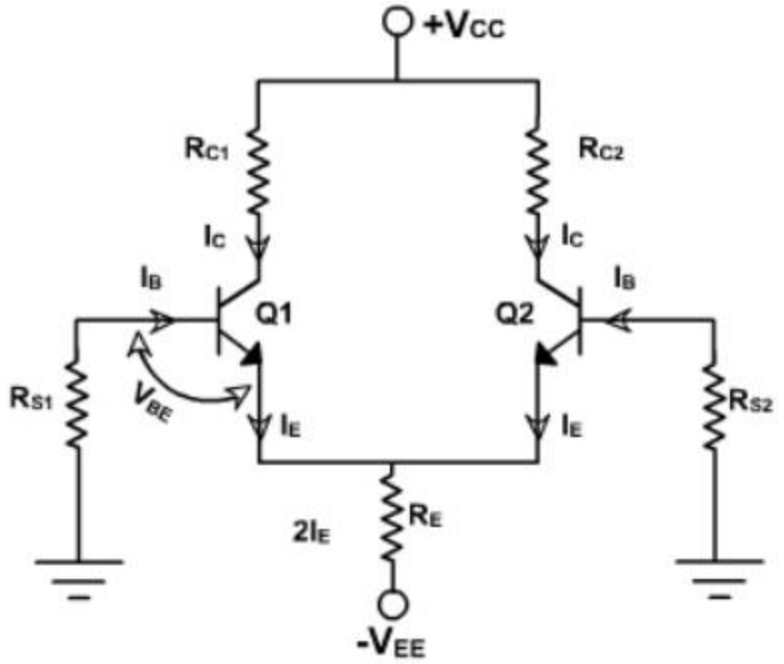
1. Dual input, balanced output(DIBO) differential amplifier.
2. Dual input, unbalanced output(DIUO) differential amplifier.
3. Single input balanced output(SIBO) differential amplifier.
4. Single input unbalanced output (SIUO)differential amplifier.

- If use two input signals, the configuration is said to be dual input, otherwise it is a single input configuration.
- On the other hand, if the output voltage is measured between two collectors, it is referred to as a balanced output because both the collectors are at the same dc potential w.r.t. ground.
- If the output is measured at one of the collectors w.r.t. ground, the configuration is called an unbalanced output.

- Performance of DA depends on ideal matching characteristics of transistor pair Q1 & Q2.
- Ampr uses both +ve & -ve power supply.
- i/p V1 is connected to Base of Q1
- i/p V2 is connected to Base of Q2
- o/p is taken btw collectr terminals

DC analysis

- To obtain the operating point (I_{CQ} and V_{CEQ}) for differential amplifier, dc equivalent circuit is drawn by reducing the input voltages v_1 and v_2 to 0
- ie, making the ac i/ps 0



- We assume Q1 and Q2 are ideally matched
- β »1
- The internal resistances of the input signals are denoted by R_S because $R_{S1}= R_{S2}$.
- Since both emitter biased sections of the different amplifier are symmetrical in all respects, therefore, the operating point for only one section need to be determined.
- The same values of I_{CQ} and V_{CEQ} can be used for second transistor Q_2.
- Applying KVL to the base emitter loop of the transistor Q_1.

- $R_s\ I_B + V_{BE} + 2I_E R_E = V_{EE}$
- $\beta = I_C / I_B$
- I_C approx. $= I_E$
- $\beta = I_E / I_B$
- Practically $R_s / \beta \ll 2R_E$
- $I_E = I_C = (V_{EE} - V_{BE}) / 2R_E$

- Neglecting the drop across R_S , apply KVL to collectr base loop

- $V_C = V_{CC} - I_C R_C$
- $V_{BE} = V_B - V_E = 0 - V_E$ ---------- $V_E = -V_{BE}$

$V_{CE} = V_C - V_E$

$= V_{CC} - I_C R_C + V_{BE}$

$V_{CE} = V_{CC} + V_{BE} - I_C R_C$

Q pt(V_{CE}, I_C)

The Q point, also known as the operating point, is a steady-state DC voltage and current level that a transistor operates at. It determines the amount of power the transistor will use and the level of amplification it will provide.

AC analysis of emitter coupled pair

- To analyze the ac signal operation of an amplifier, an ac equivalent circuit is developed.

1. The capacitors are replaced by effective shorts because their values are selected so that X_c is negligible at the signal frequency and can be considered to be 0 V.
2. The dc source is replaced by ground.

In the a.c. analysis, we will calculate the differential gain A_d, common mode gain A_C, input resistance Ri and the output resistance R_0 of the differential amplifier circuit, using the h-parameters.

- hfe- is forward current gain
- hie - Input Impedance
- hre - reverse voltage gain
- hoe – Output conductance

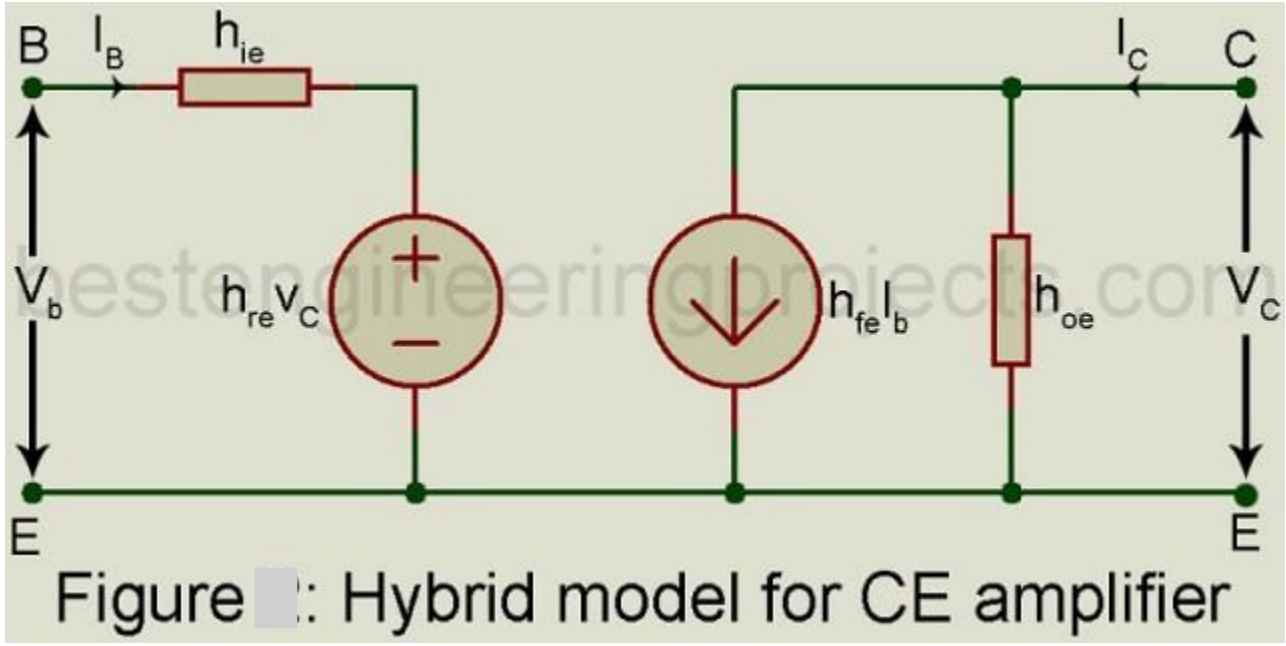


Figure : Hybrid model for CE amplifier

$$h_{ie} = \frac{V_{be}}{I_b}\bigg|_{V_{CE}} \qquad h_{re} = \frac{\Delta V_{BE}}{\Delta V_{CE}}\bigg|_{I_B}$$

$$h_{fe} = \frac{I_c}{I_b}\bigg|_{V_{CE}} \qquad h_{oe} = \frac{I_c}{V_{ce}}\bigg|_{I_B}$$

1. Differential gain A_d

- For this calculation, the two input signals must be different from each other.
- Let the two a.c. input signals be equal in magnitude but having 180" phase difference in between them.
- The magnitude of each a.c. input voltage V_{S1} and V_{S2} be Vs /2.
- The two a.c. emitter currents $I e_1$ and $I e_2$ are equal in magnitude and 180' out of phase. Hence they cancel each other to get resultant a.c. current through the emitter as zero.

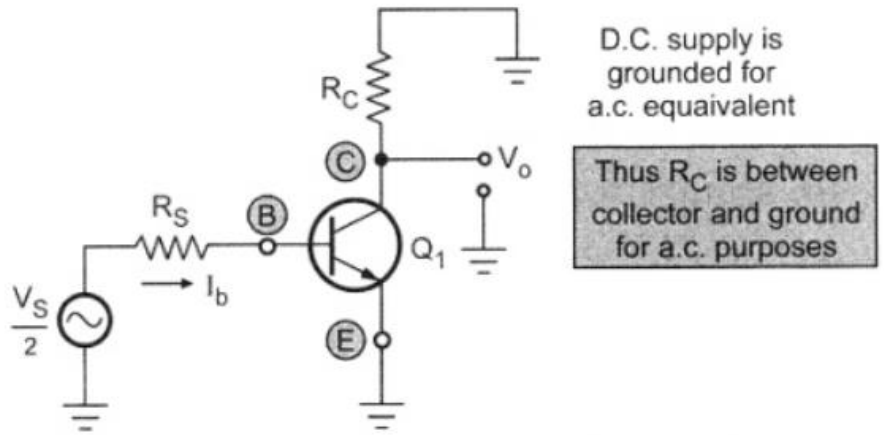


Fig: Ac equivalent for differential operation

- For the a.c. purposes emitter terminal can be grounded.
- The a.c. small signal differential amplifier circuit with grounded emitter terminal is shown in the Fig.
- As the two transistors are matched, the a.c. equivalent circuit for the transistors are identical.
- Thus the circuit can be analyzed by considering only one transistor. This is called as half circuit concept of analysis.

- The approximate hybrid model for the above circuit can be shown as below, neglecting ho_e,

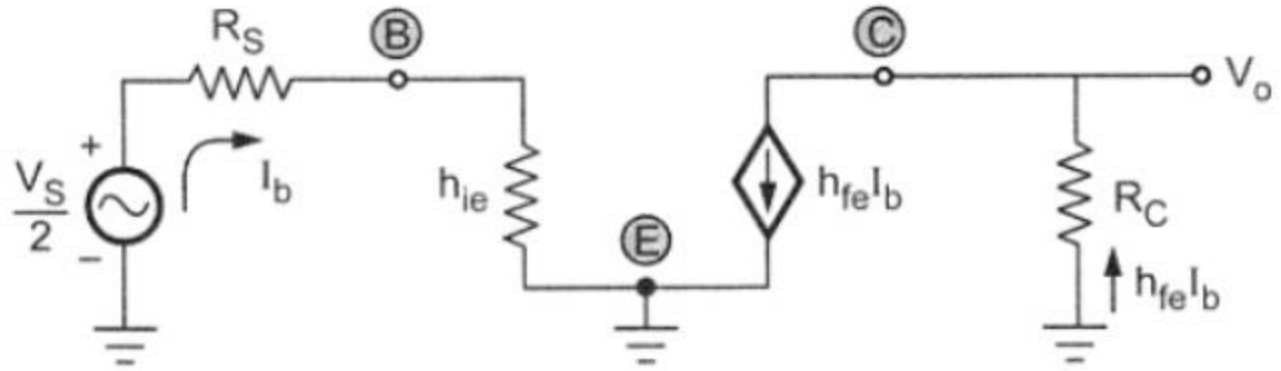


Fig: Approximate hybrid model

Apply KVL to i/p loop

$I_bR_s + I_bh_{ie} - V_s/2 = 0$ ----------(1)

$I_b = V_s / 2(R_s + h_{ie})$ ----------(2)

Apply KVL to o/p loop

$V_o = - h_{fe}I_bR_c$----------(3)

(2) in (3)

$V_o = - h_{fe} R_c * V_s / 2(R_s + h_{ie})$

$V_o/V_s = - h_{fe} R_c / 2(R_s + h_{ie})$ ----------(4)

-ve sign indicates the phase difference between input and output.

two input signal magnitudes are V_S /2 but they are opposite in polarity, as 180" out of phase.

$V_d = V_1 - V_2$

$= \frac{Vs}{2} - (- \frac{Vs}{2})$

$= V_S$

Magnitude of differential gain **$A_d = \frac{V_o}{V_s}$**

V_s is the differential i/p

- the expression for magnitude of A_d
- **$|A_d| = h_{fe}R_c / 2(R_s + h_{ie})$ for unbalanced o/p**
- the expression for magnitude of A_d with balanced output changes as
- $|A_d| = \{ h_{fe}R_c / 2(R_s + h_{ie})\} * 2$
- **$|A_d| = h_{fe}R_c / (R_s + h_{ie})$ for balanced o/p**
- This is the differential gain for balanced output dual input differential amplifier circuit.

2. Common Mode Gain (A_C)

- Let the magnitude of both the a.c. input signals be V_s and are in phase with each other.
- Hence the differential input $V_d = 0$ while the common mode input Vc is the average value of the two.
- $V_c=(V_1+V_2)/2 = V_s$
- output $V_o=A_cV_s$
- $Ac=V_o/V_s$

But now both the emitter currents flows through R_E in the Same direction. Hence the total current flowing through R_E is $2I_e$. considering only one transistor, as in the Fig

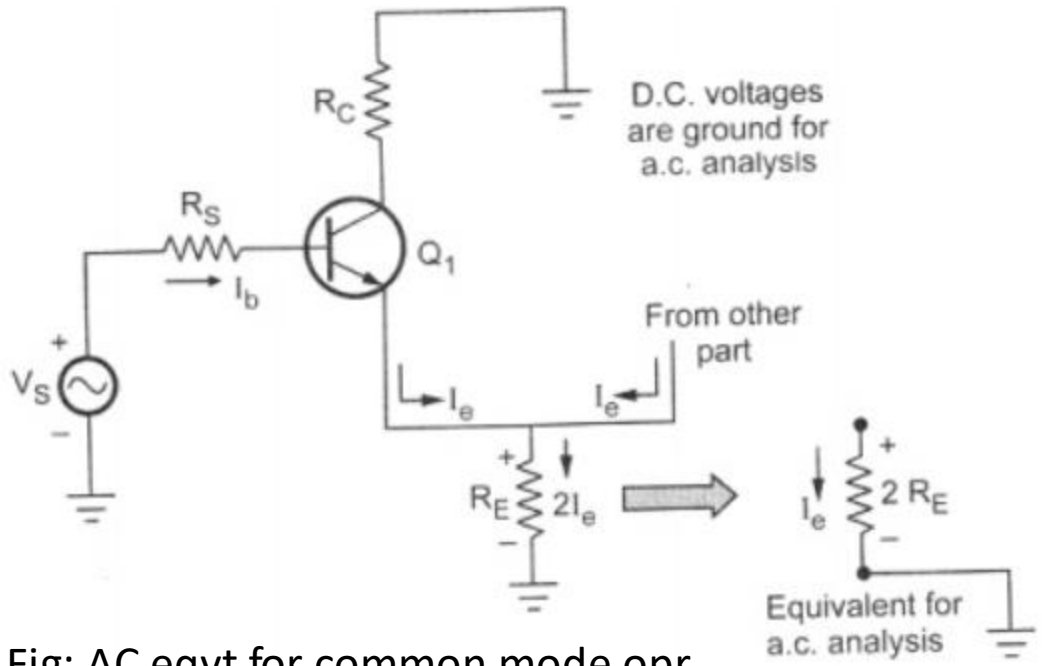


Fig: AC eqvt for common mode opr.

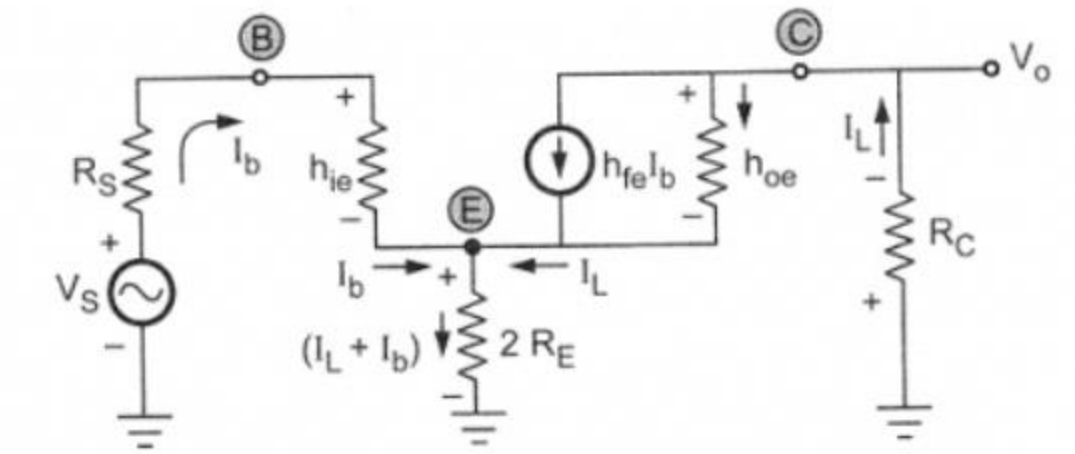


Fig. Approximate hybrid model

I thru R_c=load current I_L
effective emitter res = $2R_E$
I thru E res = $I_L + I_b$
I thru $h_{oe} = I_L - h_{fe}\ I_b$

Apply KVL to i/p loop,

- $I_bR_S+ I_bh_{ie}+2R_E(I_L+I_b) = V_s$
- $V_s= I_b(R_s+h_{ie}+2R_E) +2R_EI_L$

  $=I_b(R_s+h_{ie}+2R_E) +2R_Eh_{fe}I_b$

$V_s = I_b(R_s+h_{ie}+2R_E+2R_Eh_{fe})$

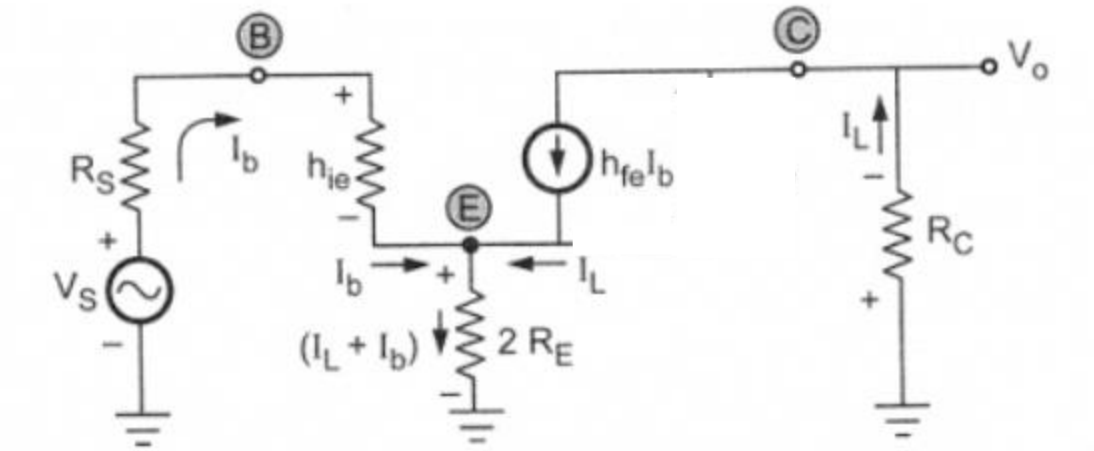


Fig. Approximate hybrid model

Apply KVL to o/p loop,

- hoe is the conductance of the output. So 1/hoe is the resistance parallel to it. More the value of 1/hoe, better is the current source. So for a good transistor the value of hoe is very small. h_{oe} is generally neglected.

- $V_0 = -I_L R_c$

  $= -h_{fe} I_b R_c$

$A_c = V_0 / V_s$

$$\mathbf{A_c = -h_{fe} R_c / (R_s + h_{ie} + 2R_E(1 + h_{fe}))}$$

$$\mathbf{|A_c| = h_{fe} R_c / (R_s + h_{ie} + 2R_E(1 + h_{fe}))}$$

3. Common Mode rejection Ratio (CMRR)

- Once the differential and common mode gains are obtained, the expression for the CMRR can be obtained as,
- CMRR = $\left|\frac{Ad}{Ac}\right|$
- CMRR = $\frac{R_s + h_{ie} + 2RE(1+h_{fe})}{R_s + h_{ie}}$

- This is CMRR for **dual input balanced output** differential amplifier circuit.

4. Input impedance R_i

- Eqvt res btw any 1 of the i/ps and grnd, when other i/p is grnded.
- Considering hybrid model used for differential gain analysis,

From (1)

$$I_b(R_s+h_{ie}) = V_s/2$$

$$R_i = V_s/I_b$$

$R_i = 2 (R_s+h_{ie})$ ---------- for dual i/p ckt

$R_i = R_s+h_{ie}$---------- for single i/p ckt

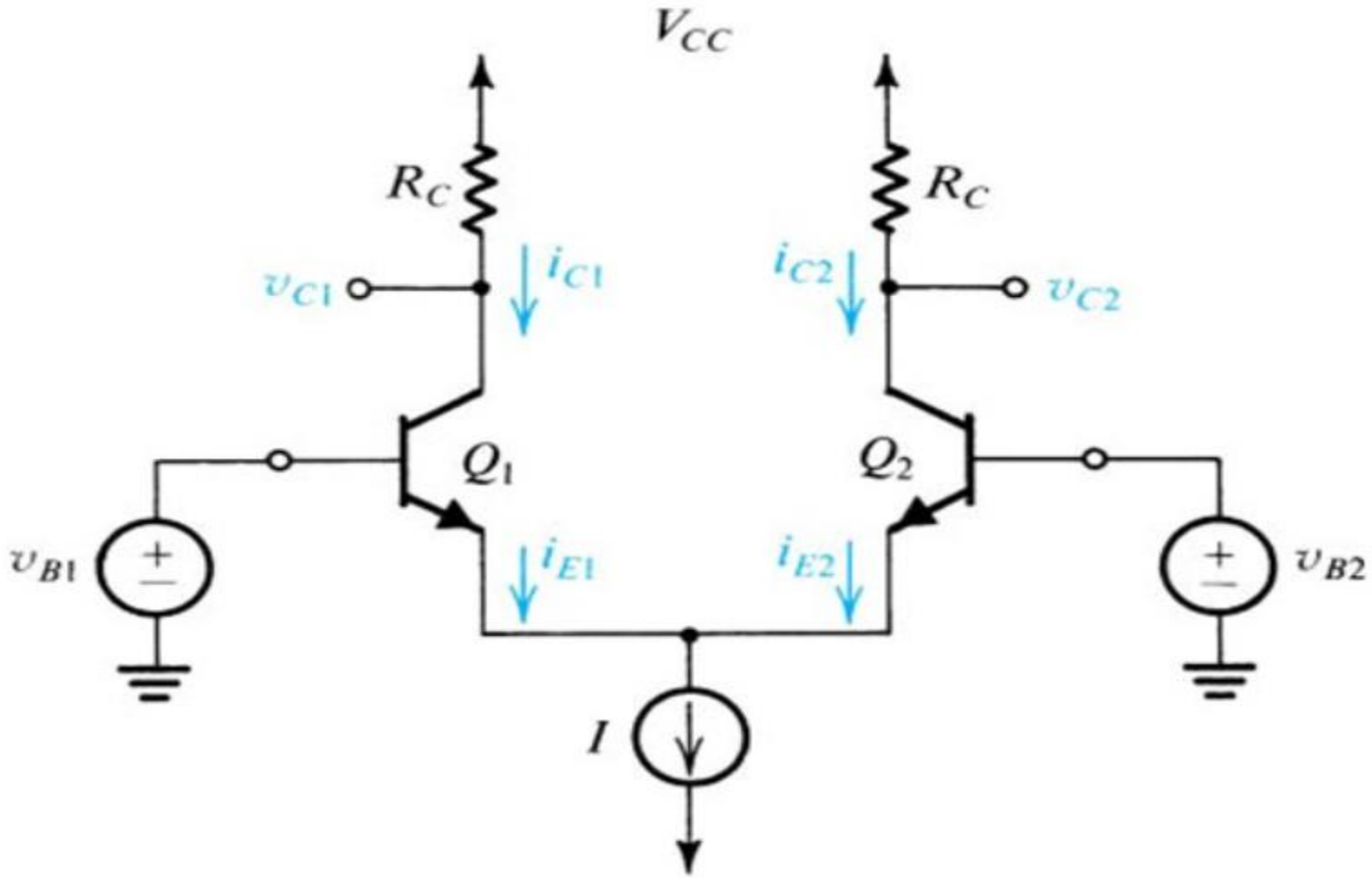
5. Output impedance R_0

- Eqvt resistance btw any 1 of the o/ps and ground
- So from the hybrid model

$$R_0 = R_c$$

Transfer characteristics of BJT differential pair

- Basic BJT differential pair configuration



Assumptions

- R_E will be replaced by a constant current source. Resistance of this current source will be infinitely high . So it act as OC.
- R_s=0

- For a basic npn transistor, collector current

$$i_c = i_s\, e^{\frac{V_{BE}}{V_T}}$$

i_s is the saturation current

V_T is the thermal Voltage

$i_E = i_c / \alpha$

$$i_E = i_s / \alpha * e^{\frac{V_{BE}}{V_T}}$$

applying this eqn to the ckt

$$i_{E1} = i_s / \alpha * e^{\frac{(V_{B1} - V_E)}{V_T}}$$

$$i_{E2} = i_s / \alpha * e^{\frac{(V_{B2} - V_E)}{V_T}}$$

- $\frac{i_{E1}}{i_{E2}} = e^{\frac{(V_{B1} - V_{B2})}{V_T}}$
- $\frac{i_{E2}}{i_{E1}} = e^{\frac{(V_{B2} - V_{B1})}{V_T}}$
- $\frac{i_{E1}}{i_{E1}+i_{E2}} = \frac{1}{1+\frac{i_{E2}}{i_{E1}}} = \frac{1}{1+e^{\frac{(V_{B2} - V_{B1})}{V_T}}}$ $\frac{i_{E2}}{i_{E1}+i_{E2}} = \frac{1}{1+\frac{i_{E1}}{i_{E2}}} = \frac{1}{1+e^{\frac{(V_{B1} - V_{B2})}{V_T}}}$

- $i_{E1} + i_{E2} = I$ I is the bias current

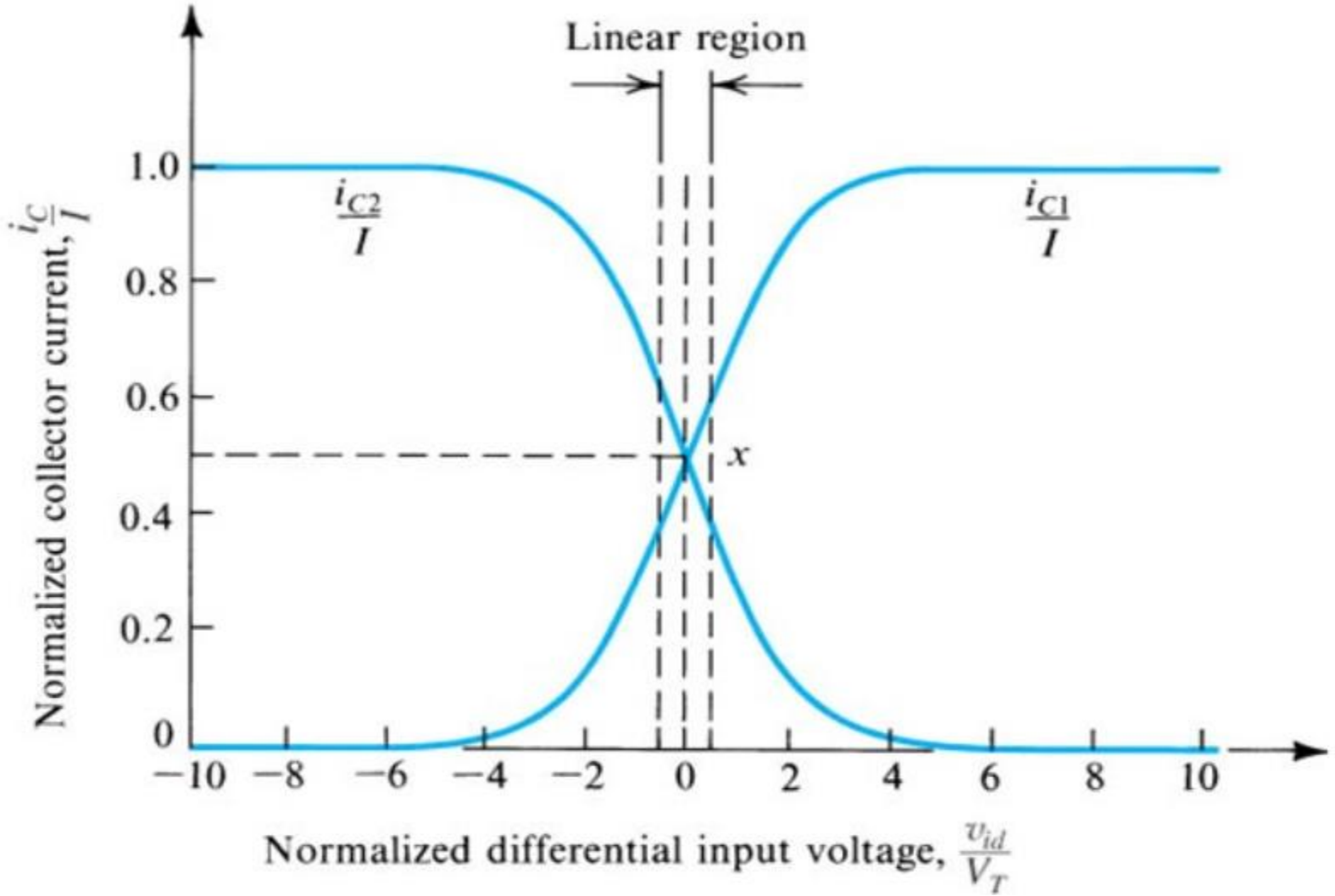
- $\frac{i_{E1}}{I} = \frac{1}{1+e^{\frac{(V_{B2}-V_{B1})}{V_T}}}$

- $i_{E1} = \frac{I}{1+e^{\frac{(V_{B2}-V_{B1})}{V_T}}}$ $i_{E2} = \frac{I}{1+e^{\frac{(V_{B1}-V_{B2})}{V_T}}}$

- $i_c = \alpha\, i_E$
- So we get i_{c1} and i_{c2} from this
- The eqn suggest that the differential amplifier respond to only difference signal , hence the transfer chara can be plotted as shown

- When differential i/p voltage is large, non linear transfer characteristics are seen. By limiting the difference i/p s/g to less than $V_T/2$, we may be able to operate on a linear segment of the characteristics arnd the midpoint x.

Transfer characteristics of BJT differential pair assuming α =1



How to improve CMRR of BJT differential amplifier

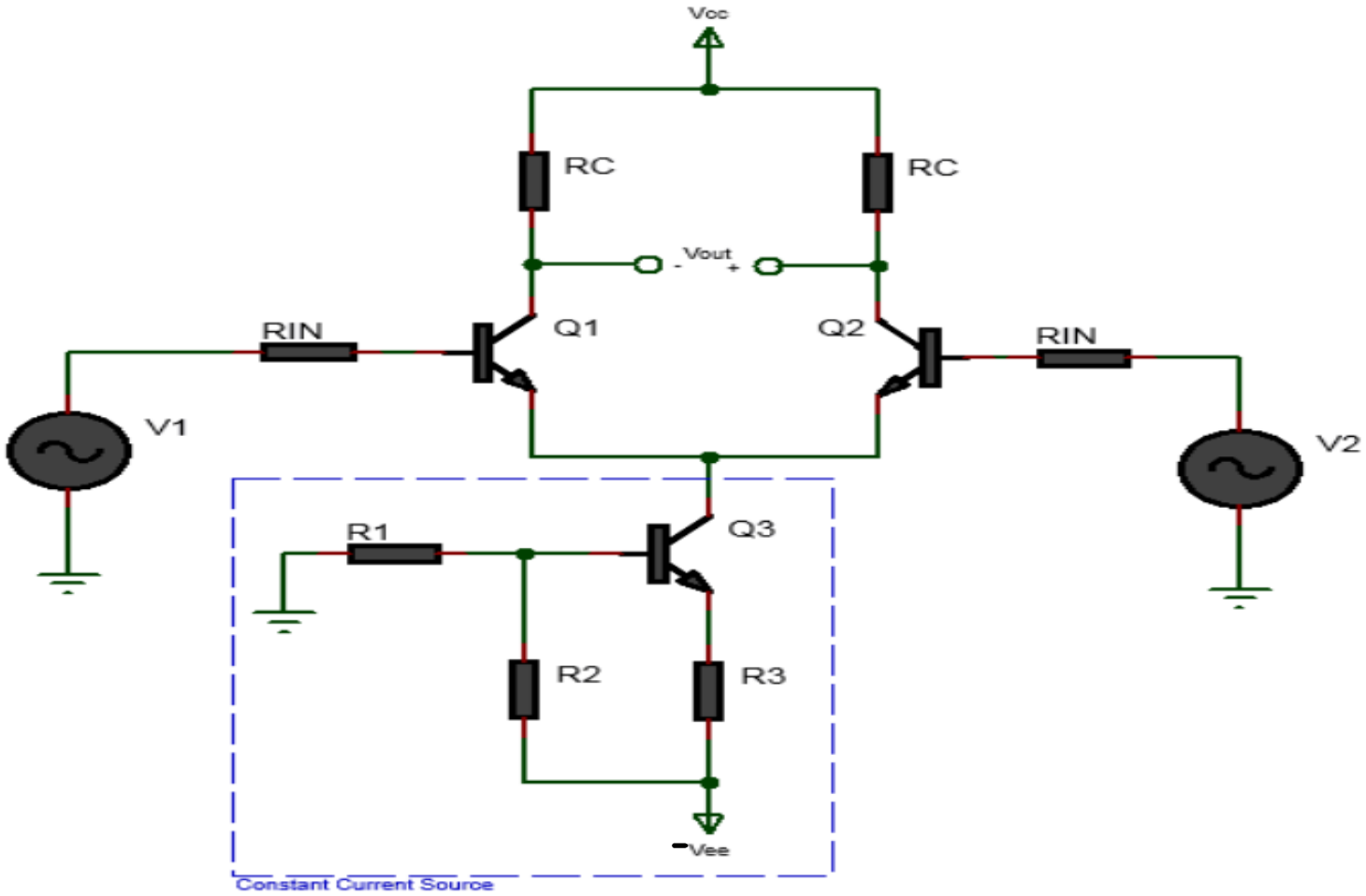
- The CMMR of a differential amplifier is an important parameter that measures the ability of the amplifier to reject common-mode signals.
- A high CMMR is desirable for most applications, and it is typically expressed in dB.
- To improve CMRR---- Ac should be very small.
- If A_c =0 -----CMRR = ∞
- **$A_c = -h_{fe}R_c / (R_s + h_{ie} + 2R_E(1+h_{fe}))$**
- R_E =∞, then A_c = 0, then CMRR = ∞
- The problem of improving CMRR is to increase emitter resistance but increasing emitter resistance will disturb the biasing point.
- Solution to increasing emitter biasing resistance and at the same time provide stability is either to use constant current bias, current mirror circuit or active load

- So in order improve the CMMR we need other ways such as constant current source to provide stable biasing current. The following are popular methods to improve the CMRR value of a differential amplifier.
- Constant Current Bias
- Current Mirror Circuit

Constant current bias

- A constant current source is a circuit or device whose internal resistance is very high compared with the load resistance it is giving power to. Because its internal resistance is so high, it can supply a constant current to a load whose resistance value varies, even over a wide range.
- designed to produce a steady, constant current regardless of changes in load resistance or supply voltage

Transistor used is Q3 , res values R1,R2,R3 are selected so as to give the same operating point values for the transistors Q1 and Q2.



Working of constant current source

The resistors R1 and R2 are used to bias the transistor Q3 properly. The dc collector current IC3 of the transistor Q3 is setup by the resistors R1, R2 and R3.
The voltage at the Q3 base is,

$$V_{B3} = \frac{-R_1 V_{EE}}{R_1 + R_2} \qquad \text{------->(1)}$$

The voltage at the Q3 emitter is,

$$V_{E3} = V_{B3} - V_{BE3}$$

using (1) we have,

$$V_{E3} = -\frac{R_1 V_{EE}}{R_1 + R_2} - V_{BE3} \quad \text{------->(2)}$$

The emitter current of Q3 is,

$$I_{E3} = \frac{V_{E3}-(-V_{EE})}{R_3}$$

$$\text{or, } I_{E3} = \frac{V_{E3}+V_{EE}}{R_3}$$

Substituting V_{E3} from(2) we get,

$$I_{E3} = \frac{-\frac{R_1 V_{EE}}{R_1+R_2} - V_{BE3} + V_{EE}}{R_3}$$

$$\text{or, } I_{E3} = \frac{V_{EE}-[\frac{R_1 V_{EE}}{R_1+R_2}]-V_{BE3}}{R_3} \quad \text{------->(3)}$$

Since for identical transistors and in general, the collector current is nearly equal to emitter current we have,

$$I_{C3} \approx \frac{V_{EE}-[\frac{R_1 V_{EE}}{R_1+R_2}]-V_{BE3}}{R_3} \quad \text{------->(4)}$$

- In equation(4) we see that the right hand side contains only constant terms. Thus equation(4) shows that the constant current source provides constant current I_{C3} that is independent on any current or voltage variable.
- Furthermore, since this Q3 collector current is sourced equally to the emitters of Q1 and Q2, we have,

$$I_{E1} = I_{E2} = \frac{I_{C3}}{2} \quad \text{------->(5)}$$

That is,

$$I_{E1} = I_{E2} = \frac{V_{EE} - [\frac{R_1 V_{EE}}{R_1 + R_2}] - V_{BE3}}{2R_3} \quad \text{------->(6)}$$

Thus the constant current source circuit provides constant emitter current to both the differential amplifier bipolar transistors Q1 and Q2.

- In addition to providing stabilized current to the BJT differential amplifier, the constant current source also provides high impedance to the differential amplifier.
- This is because in ac operation, the dc current source is effectively open circuit. Since it is open circuit in ac operation, the impedance is high and so the common mode gain is ideally zero and the CMRR is ideally infinity, since CMRR is the ratio of differential mode gain to common mode gain.

Applications of BJT Differential Amplifier with Constant Current Bias

- In Instrumentation Amplifiers: to amplify small differential signals from sensors and transducers. It is used in applications such as temperature sensing, pressure sensing, and strain gauges.
- In Audio Amplifiers: used in audio amplifiers to amplify the difference between left and right audio channels. It is used in high-fidelity audio systems, home theater systems, and automotive audio systems.
- In Analog Signal Processing: The BJT differential amplifier is used in analog signal processing circuits to amplify, filter, and process analog signals. It is used in instrumentation systems, medical equipment, and control systems.
- In Communication Systems: to amplify differential signals and reject common mode signals. It is used in applications such as radio transmitters, receivers, and modems.

Assignment – 1

(Date of submission: 04.09.23)

1. a)Explain the concept of current mirror in differential amplifier configurations using BJT.

   b)Explain Wilson and Widlar current mirrors.

   c) What are the advantages and limitations of Wilson and Widlar current mirrors ?

[CO1]

2. What is 555 timer IC ? Explain with pin diagram and functional diagram. [CO4]