dress of the instruction to be fetched and the access phase (A) which reads the address of the operand and modify the auxiliary registers and stack pointer if required.

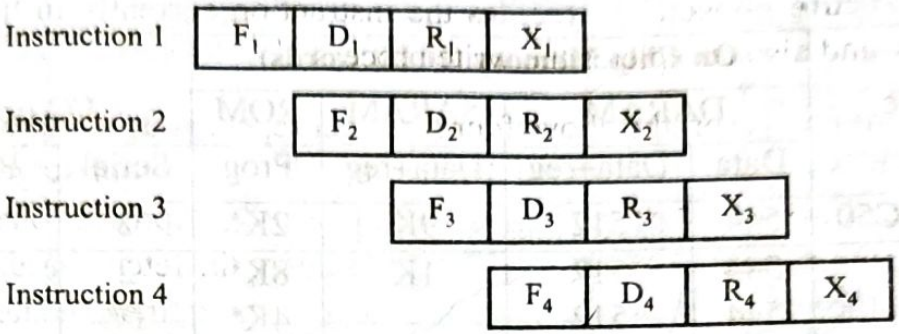

Fig. 11.4 Four stages of TMS320C54x

Table 11.2 Pipeline in different TMS320 Processors

DSP processor	Pipeline phases
TMS320C2000	F-D-R-X (4 levels)
TMS320C3x	F-D-R-X (4 levels)
TMS320C5x	F-D-R-X (4 levels)
TMS320C54x	PF-F-D-A-R-X (6 levels)

Pipelining leads to dramatic improvements in system performance. The more stages that we can break the pipeline into, the more theoretical speed we can get from it. For example, let's suppose it takes 12 clock cycles to handle all the steps to process an instruction. In theory, if you use a 4-stage pipeline, your maximum throughput is 1 instruction every 3 cycles. But if you use a 6-stage pipeline, maximum throughput is 1 instruction every 2 cycles.