ECT304
VLSI CIRCUIT DESIGN

SYLLABUS

MODULE-1

Module 1: VLSI Design Methodologies. (11 Hrs)		
1.1	Introduction: Moore slaw .ASIC design, Full custom ASICs, Standard cell based ASICs, Gate array based ASICs,	3
1.2	SoCs, FPGA devices	2
1.3	ASIC and FPGA Design flows Top-Down and Bottom-Up design methodologies.	3
1.4	Logical and Physical design. Speed power and area considerations in VLSI design	3

SYLLABUS

MODULE-2

Module 2:Static CMOS Logic Design (9 Hrs)		
2.1	**MOSFET Logic Design** - NMOS logic (Static analysis of Basic gates only)	3
2.2	CMOS logic, Static and transient analysis of CMOS inverter Switching power dissipation and delays	3
2.3	Realization logic functions in static CMOS logic, Pass transistor logic, and transmission gate logic (Static analysis only)	3

SYLLABUS

MODULE-3

Module 3: Dynamic logic Design and Storage Cells (8 Hrs)		
3.1	Dynamic Logic Design-Pre charge- Evaluate logic, Domino Logic, NP domino logic.	3
3.2	**Read Only Memory**-4x4 MOS ROM Cell Arrays(OR,NOR,NAND)	2
3.3	**Random Access Memory** –SRAM-Six transistor CMOS SRAM cell, DRAM –Three transistor and One transistor Dynamic Memory Cell.	3

SYLLABUS

MODULE-4

Module 4: Arithmetic circuits (5 Hrs)		
4.1	**Adders**- Static adder, Carry-Bypass adder, Linear Carry- Select adder, Square- root carry- select adder.	3
4.2	**Multipliers**-Array multiplier.	2

SYLLABUS

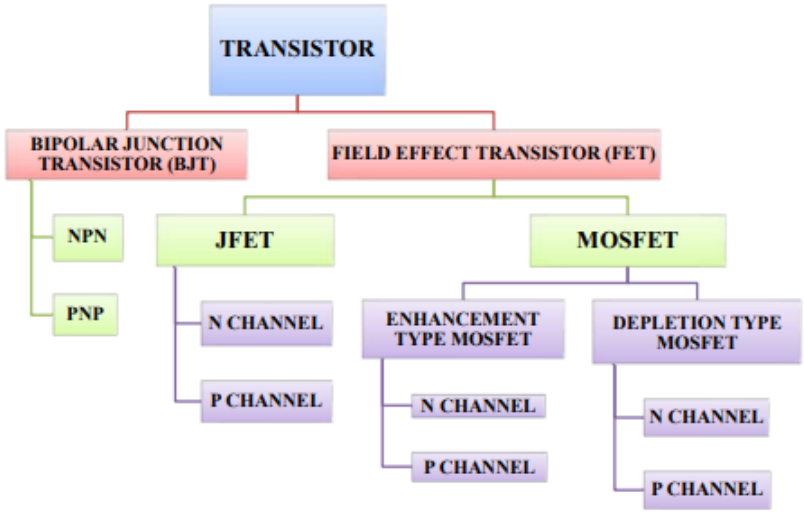
MODULE-5

Module 5: MOSFET physical Design and Fabrication techniques (13 Hrs)		
5.1	**Material Preparation** (qualitative analysis only) Purification and Crystal growth (CZ process), wafer preparation.	2
5.2	**Thermal Oxidation**- Growth mechanisms, Dry and Wet oxidation. Diffusion and ion implantation techniques.	3
5.3	**Epitaxy :** Molecular beam epitaxy. **Lithography-** Photo lithographic sequence, Electron Beam Lithography, Etching and metal deposition techniques	3
5.4	**MOSFET Fabrication techniques**(*qualitative analysis only*) Twin-Tub fabrication sequence, Fabrication process flow.	2
5.5	**Layout Design and Design rules**, Stick Diagram and Design rules- micron rules and Lambda rules. Layout of CMOS Inverter, two input NAND and NOR gates,	3

MODULE-2
Static CMOS logic design

ECT304
VLSI CIRCUIT DESIGN

TRANSISTOR CLASSIFICATION

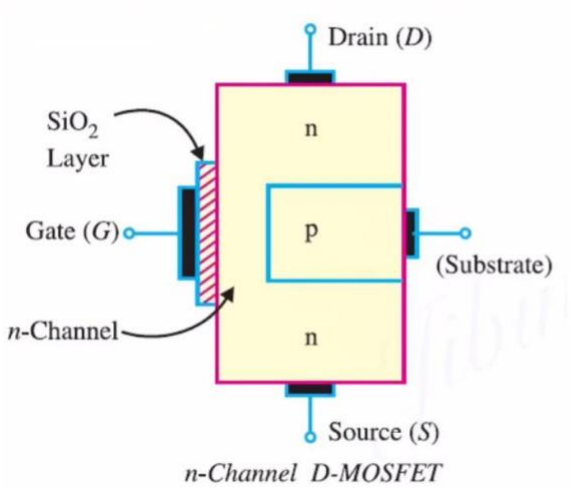


- BJT is a Current Controlled Device. i.e., output characteristics of the device is controlled by input current and not by input voltage.
- FET is a Voltage Controlled Device. i.e., output characteristics of the device is controlled by input voltage and not by input current.
- Two types of FET (Field effect Transistors)
  - Junction Field effect Transistors (JFET)
  - Metal Oxide Semiconductor/Silicon Field effect Transistors (MOSFET)

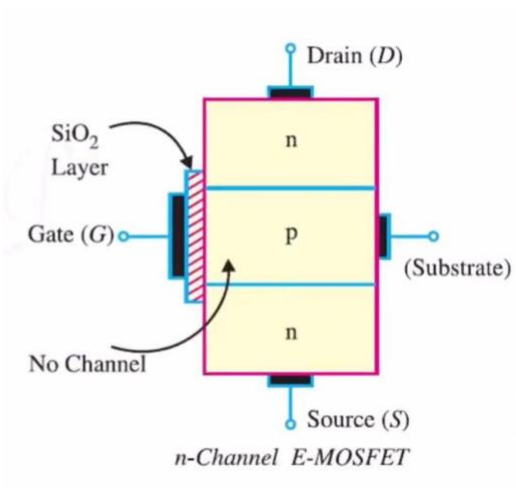
CLASSIFICATION OF MOSFET

- **DEPLETION TYPE MOSFET OR D-MOSFET**
- Operated in both depletion/enhancement mode.
- Sometimes called as depletion/enhancement MOSFET
- **ENHANCEMENT TYPE MOSFET OR E-MOSFET**
- Can operate in Enhancement mode only

CONSTRUCTION OF MOSFET



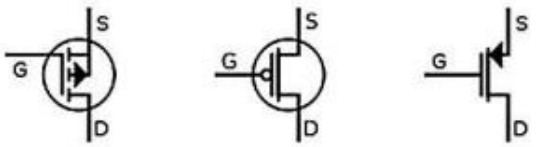
n-Channel D-MOSFET



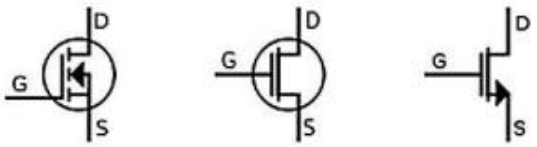
n-Channel E-MOSFET

E-MOSFET SYMBOL

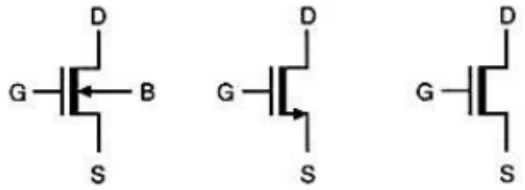
P CHANNEL



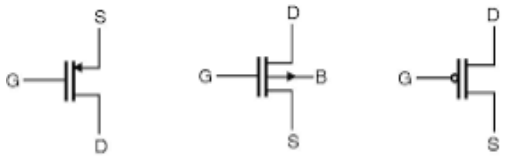
N CHANNEL



DEPLETION-MOSFET SYMBOL

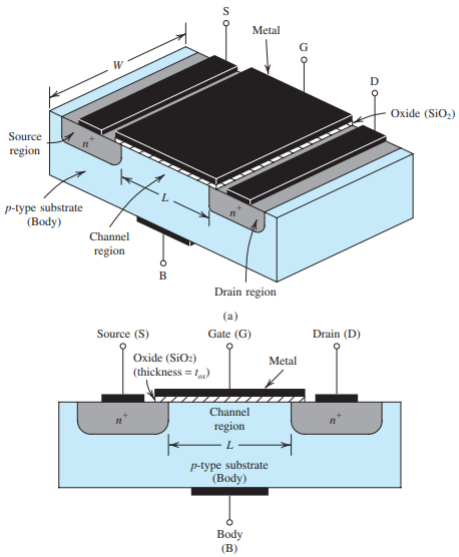


N CHANNEL DEPLETION TYPE MOSFET



P- CHANNEL DEPLETION TYPE MOSFET

MOS TRANSISTOR OPERATION



Vgs < 0 ➔ **ACCUMULATION MODE**

Vt > Vgs > 0 ➔ **DEPLETION MODE**

Vgs > Vt ➔ **INVERSION MODE**

Vgs < Vt ➔ **CUT OFF REGION**

Vgs > Vt & Vds < (Vgs – Vt) ➔ **LINEAR REGION**

Vgs > Vt & Vds > (Vgs – Vt) ➔ **SATURATION REGION**

MOS TRANSISTOR OPERATION

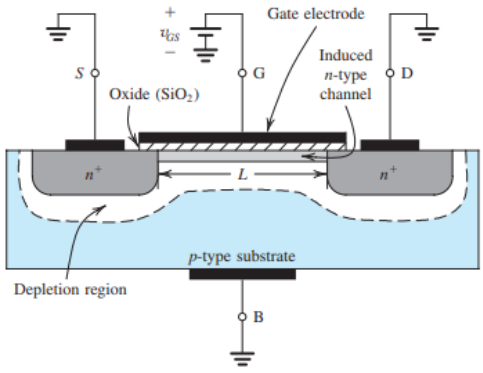


Figure 5.2 The enhancement-type NMOS transistor with a positive voltage applied to the gate. An *n* channel is induced at the top of the substrate beneath the gate.

- The induced n region thus forms a channel for current flow from drain to source
- The channel is created by inverting the substrate surface from p type to n type. Hence the induced channel is also called an **inversion layer.**
- The value of V_{GS} at which a sufficient number of mobile electrons accumulate in the channel region to form a conducting channel is called the **threshold voltage** and is denoted **Vt**.
- **Vt** for an n-channel MOSFET is positive.
- The value of Vt is controlled during device fabrication and typically lies in the range of 0.3 V to 1.0 V.

MOS TRANSISTOR OPERATION

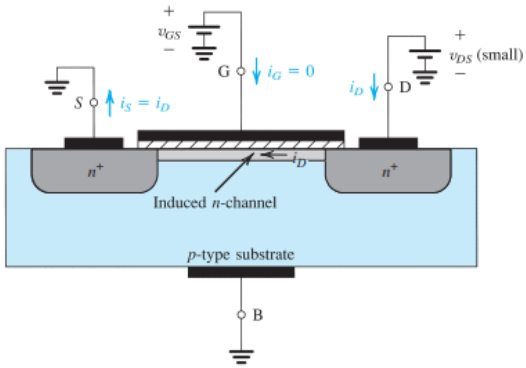
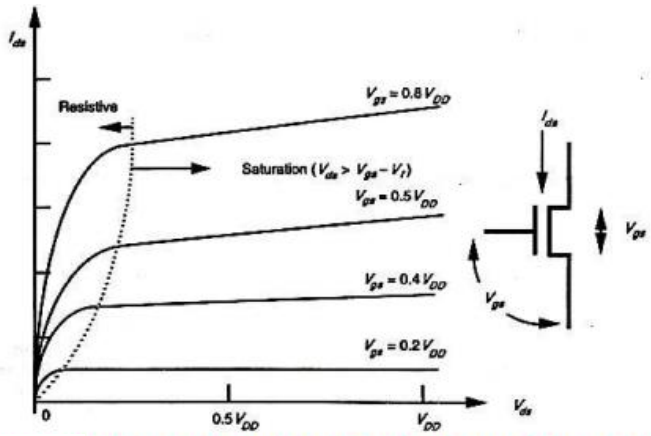


Figure 5.3 An NMOS transistor with $v_{GS} > V_t$ and with a small v_{DS} applied. The device acts as a resistance whose value is determined by v_{GS}. Specifically, the channel conductance is proportional to $v_{GS} - V_t$, and thus i_D is proportional to $(v_{GS} - V_t)v_{DS}$. Note that the depletion region is not shown (for simplicity).

MOS TRANSISTOR CHARACTERISTICS



OUTPUT CHARACTERISTICS OF N CHANNEL EMOS

MOS TRANSISTOR CHARACTERISTICS

- Three regions of operation

1. Cut Off Region

   $V_{GS} < V_{TH}$

   I_{DS} will be 0. i.e., no current flow

2. Ohmic or Resistive or Triode or Non-Saturated Region

   $V_{GS} > V_{TH}$ and $V_{DS} < (V_{GS} - V_{TH})$

   I_{DS} greater than 0

3. Saturation Region

   $V_{GS} > V_{TH}$ and $V_{DS} \geq (V_{GS} - V_{TH})$

   I_{DS} greater than 0

MOS TRANSISTOR CURRENT EQUATIONS

✓ Drain Current of EMOSFET is given by

$I_{DS} = 0$, Cut Off region

$I_{DS} = \mu C_{ox} \frac{W}{L} \left[V_{DS}(V_{GS} - V_{TH}) - \frac{V_{DS}^2}{2} \right]$, Ohmic region

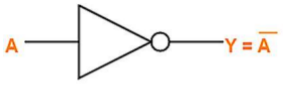
$I_{DS} = \mu C_{ox} \frac{W}{L} \left[\frac{(V_{GS} - V_{TH})^2}{2} \right]$, Saturation Region

- C_{ox} is the Gate/Channel Capacitance per unit area (F/cm^2)
- μ is the mobility of majority carrier (electron or hole mobility)
- $\frac{W}{L}$ is the channel width to channel length ratio of MOS
- V_{TH} is the threshold voltage

BASIC INVERTER CIRCUITS

INVERTER CIRCUITS

- The basic requirement for producing a complete range of logic circuits is the inverter.
- Inverter is needed for restoring logic levels for NAND and NOR gates and for sequential and memory circuits of various forms.
- **CLASSIFICATION**
  - **NMOS INVERTER**
    - **RESISTIVE LOAD**
    - **DEPLETION TYPE LOAD**
    - **ENHANCEMENT TYPE LOAD**
    - **PSEUDO NMOS LOAD**
  - **CMOS INVERTER**

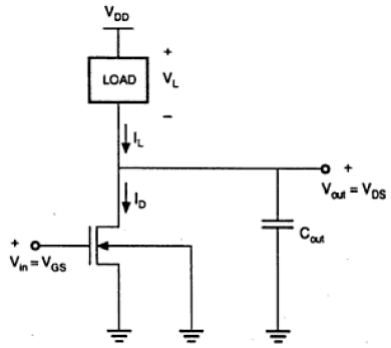


NOT Gate

Figure 2.1: Inverter Symbol

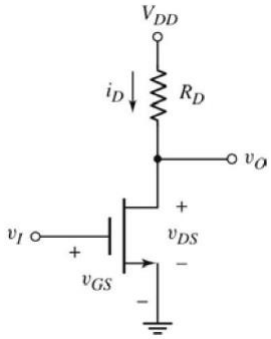
NMOS INVERTER

- The basic inverter circuit requires a transistor with source connected to ground and a load resistor of some sort connected from the drain to the positive supply rail $V_{DD.}$
- The output is taken from the drain and the input applied between gate and ground.
- NMOS acts as a switch



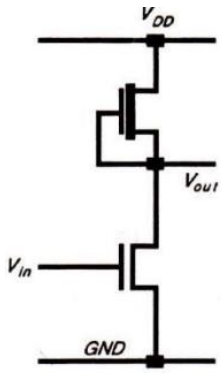
RESISTIVE LOAD NMOS INVERTER

- Here the load used is a resistor.
- This arrangement is not often used because of the large space requirements of resistors produced in a silicon substrate.
- Also standby leakage is more, poor noise margin
- Resistors are not conveniently produced on the silicon substrate; even modest values occupy excessively large areas so that some other form of load resistance is required.
- A convenient way to solve this problem is to use a transistor as the load.



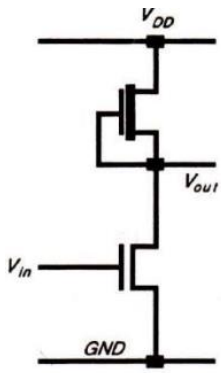
DEPLETION TYPE LOAD NMOS INVERTER

- With no current drawn from the output, the currents Ids for both transistors must be equal.
- For the depletion mode transistor, the **gate is connected to the source** so it is **always on** and only the characteristic curve Vgs = 0 is relevant.
- In this configuration the **depletion mode device** is called the **pull-up (p.u.)** and the **enhancement mode device the pull-down (p.d.) transistor**.
- The D-MOS here acts as a nonlinear resistor (as always on)
- D-MOS work in either in Linear region or in saturation region.



DEPLETION TYPE LOAD NMOS INVERTER

- The maximum voltage across the enhancement mode device corresponds to minimum voltage across the depletion mode transistor.
- When Vin (= Vgs p.d. transistor) exceeds the p.d. threshold voltage current begins to flow.
- The output voltage Vout, thus decreases and the subsequent increases in Vin will cause the p.d. transistor to come out of saturation and become resistive.
- The p.u. transistor is initially resistive



DEPLETION TYPE LOAD NMOS INVERTER

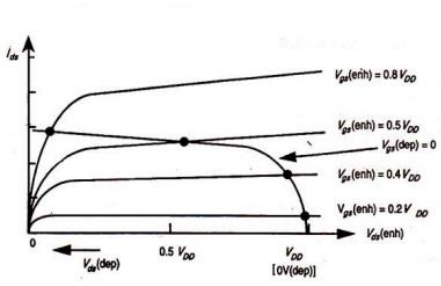


Figure 2.4: Derivation of NMOS Inverter transfer characteristics

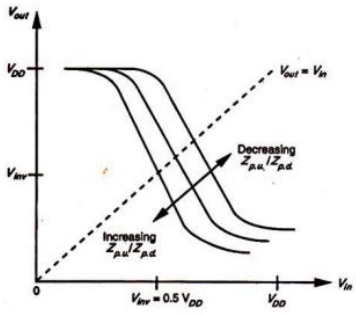
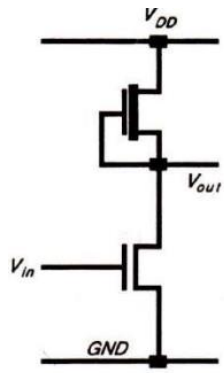


Figure 2.5: NMOS Inverter transfer characteristics

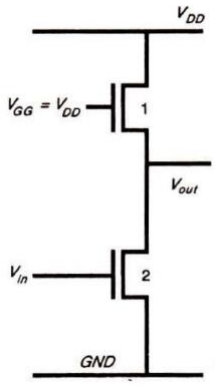
DEPLETION TYPE LOAD NMOS INVERTER

- Dissipation is high, since rail to rail current flows when Vin = logical 1.
- Switching of output from 1 to 0 begins when Vin exceeds V_{TH} of pull down device.
- When switching the output from 1 to 0, the pull up device is non- saturated initially and this presents lower resistance through which to charge capacitive loads.



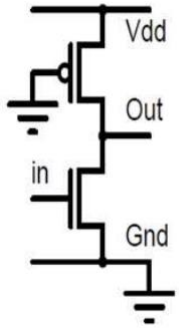
ENHANCEMENT TYPE LOAD NMOS INVERTER

- Dissipation is high since current flows when Vin = logical 1 (VGG is returned to VDD).
- Vout can never reach VDD (logical 1) if VGG = VDD as is normally the case.



PSEUDO NMOS LOAD NMOS INVERTER

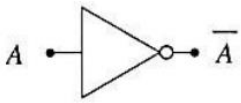
- The inverter that uses a p-device pull-up or load that has its gate permanently ground



CMOS INVERTER

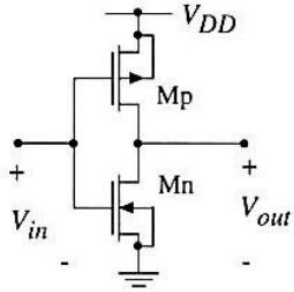
CMOS INVERTER

- A CMOS inverter consists of two opposite polarity MOSFETs M_n (nMOS) and M_p (pMOS) with their gates connected together at the input.
- The applied voltage is denoted by V_{in}
- The inverter output voltage V_{out} is taken from the common drain terminals.



A	$\overline{A}$
0	1
1	0

(a) Logic symbol



(b) CMOS circuit

CMOS INVERTER

- An nMOS - pMOS group with a common gate is called a **complementary pair,** which gives us the "C" in "CMOS."
- The transistors are connected in a manner that ensures that only one of the MOSFETs conducts when the input is stable at a low or high voltage.
- This is due to the use of the complementary arrangement.
- From the circuit we have

$$\mathbf{V_{GSn} = V_{in}}$$
$$\mathbf{V_{SGp} = V_{DD} - V_{in}}$$

- where $\mathbf{V_{in}}$ is assumed to be in the voltage range $\mathbf{[0, V_{DD}]}$ with $\mathbf{V_{DD}}$ the power supply.

CMOS INVERTER – DC OPERATION

- When $V_{in} = V_{DD}$, i.e., high input voltage (Logic 1)

$$\mathbf{V_{GSn} = V_{DD}}$$
$$\mathbf{V_{SGp} = 0}$$

- pMOS M_p is in Cut off while nMOS M_n is conducting in the non-saturated mode.
- M_n provide a current path to ground, resulting in an output voltage of

$$\mathbf{min(V_{out}) = V_{OL} = 0}$$

- where V_{OL} is called the output low voltage, and represents the smallest voltage available at the output.

CMOS INVERTER – DC OPERATION

- When $V_{in} = 0$, i.e., low input voltage (Logic 0)

$$\mathbf{V_{GSn} = 0}$$
$$\mathbf{V_{SGp} = V_{DD}}$$

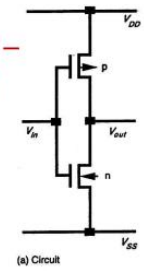
- nMOS M_n is in Cut off while pMOS M_p is conducting in the non-saturated mode.
- The pMOS M_p provides a conductive path to the power supply and gives

$$\mathbf{max(V_{out}) = V_{OH} = V_{DD}}$$

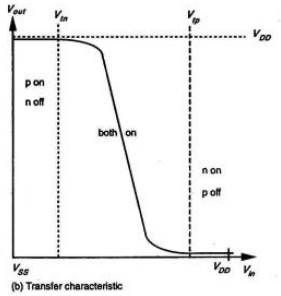
- which defines the output high voltage $\mathbf{V_{OH}}$ of the circuit
- $\mathbf{V_{OH}}$ is the largest value of $\mathbf{V_{out}}$

CMOS INVERTER – DC OPERATION

CMOS INVERTER – DC OPERATION



(a) Circuit



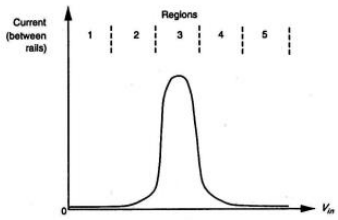
(b) Transfer characteristic

: CMOS Inverter

(a) Circuit

(b) Transfer Characteristics

(c) Current v/s Voltage



(c) CMOS inverter current versus V_{in}

CMOS INVERTER – DC OPERATION

✓ The Current - Voltage relationships for the MOSFET is given by

$$I_D = \beta\left[V_{DS}(V_{GS} - V_{TH}) - \frac{{V_{DS}}^2}{2}\right]$$

➢ in the resistive region or

$$I_D = \frac{\beta}{2}(V_{GS} - V_{TH})^2$$

➢ in the Saturation.

➢ where $\beta = \mu C_{ox}\frac{W}{L}$

✓ CMOS inverter has five distinct regions of operation.

CMOS INVERTER – DC OPERATION

✓ Region 1

- V_{in} = logic 0, we have the pMOS fully turned on while the nMOS is fully turned off.
- Thus no current flows through the inverter and the output is directly connected to V_{DD} through the p-transistor.
- A good logic 1 output voltage is thus present at the output.

✓ Region 5

- V_{in} = logic 1, the nMOS is fully on while the pMOS is fully off.
- Again, no current flows and a good logic 0 appears at the output.

CMOS INVERTER – DC OPERATION

✓ Region 2

- The input voltage has increased to a level which just exceeds the threshold voltage of the nMOS.
- The nMOS conducts and has a large voltage between source and drain; so it is in saturation.
- The pMOS is also conducting but with only a small voltage across it, it operates in the unsaturated resistive region.
- A small current now flows through the inverter from V_{DD} to V_{SS}.

CMOS INVERTER – DC OPERATION

✓ Region 4

- Region 4 is similar to region 2 but with the roles of the p- and n-transistors reversed.
- The input voltage has increased to a level which just exceeds the threshold voltage of the pMOS.
- The pMOS conducts and has a large voltage between source and drain; so it is in saturation.
- The nMOS is also conducting but with only a small voltage across it, it operates in the unsaturated resistive region.
- A small current now flows through the inverter from V_{DD} to V_{SS}.

CMOS INVERTER – DC OPERATION

✓ Region 3

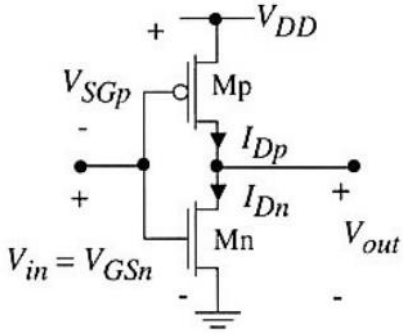
- The current magnitudes in regions 2 and 4 are small and most of the energy consumed in switching from one state to the other is due to the larger current which flows in region 3.
- Region 3 is the region in which the inverter exhibits gain and in which both transistors are in saturation.
- The currents in each device must be the same since the transistors are in series i.e., $\mathbf{I_{dsn} = -I_{dsp}}$

$$I_{dsp} = \frac{\beta_p}{2}(V_{in} - V_{DD} - V_{tp})^2 \qquad \text{and} \qquad I_{dsn} = \frac{\beta_n}{2}(V_{in} - V_{tn})^2$$

- Hence $$V_{in} = \frac{V_{DD} + V_{tp} + V_{tn}(\beta_n/\beta_p)^{1/2}}{1 + (\beta_n/\beta_p)^{1/2}}$$
- If $\boldsymbol{\beta_n = \beta_p}$ and if $\mathbf{V_{tn} = -V_{tp}}$, then $\mathbf{V_{in} = 0.5V_{DD}}$

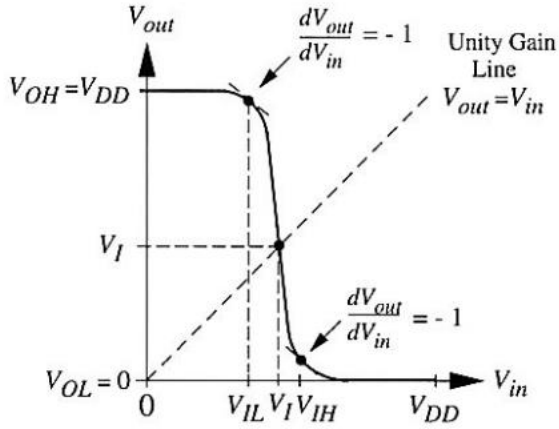
CMOS INVERTER

- Because of the placement and operation of each MOSFET, M_n is called a pull-down transistor, while M_p is termed a pull-up device.



CMOS Inverter – Input and Output Voltages

CMOS INVERTER – DC CHARACTERISTICS



Voltage Transfer Characteristics of CMOS Inverter

CMOS INVERTER – DC CHARACTERISTICS

- The DC input-output characteristics are portrayed graphically using the Voltage-Transfer Curve (or VTC)
- This is simply a plot of $\mathbf{V_{out}}$ as a function of $\mathbf{V_{in}}$
- When $\mathbf{V_{in}}$ is small, $\mathbf{V_{out}}$ is large, and vice-versa.
- The sharpness of the transition is a measure of how well the circuit is able to perform digital operations.
- The VTC itself gives a set of critical voltages to work with in creating the defined ranges.
- The important values are the output voltages ($\mathbf{V_{OH}}$ and $\mathbf{V_{OL}}$), the input voltages ($\mathbf{V_{IH}}$ and $\mathbf{V_{IL}}$), and and the inverter threshold voltage ($\mathbf{V_I}$).
- Assume that the MOSFETs have known device transconductance values of

$$\beta_n = k'_n \left(\frac{W}{L}\right)_n \quad \text{and} \quad \beta_p = k'_p \left(\frac{W}{L}\right)_p$$

CMOS INVERTER – DC CHARACTERISTICS

- This means that the layout has been completed and the aspect ratios $\mathbf{(W/L)_n}$ and $\mathbf{(W/L)_p}$ are known quantities.
- The critical voltages are established by the MOSFET parameters and characterize the DC response of the circuit.
- These are directly related to the method we use to define logic 0 and logic 1 levels.
- In CMOS circuit design, only the device aspect ratios $\mathbf{(W/L)_n}$ (for nMOS) and $\mathbf{(W/L)_p}$ (for the pMOS) can be adjusted in the design phase.
- The other electrical parameters such as $\boldsymbol{k'}$ and $\mathbf{V_{TH}}$ and are a result of the fabrication and cannot be changed.
- The critical voltages may be computed by setting the input voltage to the desired value and then equating the drain currents $\mathbf{I_{Dn}} = \mathbf{I_{Dp}}$ at the output node.

CMOS INVERTER – DC CHARACTERISTICS

✓ OUTPUT HIGH VOLTAGE (V_{OH})

- The output-high voltage $\mathbf{V_{OH}}$ is the largest value of $\mathbf{V_{out}}$.
- It may be calculated by applying an input voltage $\mathbf{V_{in}<V_{THn}}$ which insures that the nMOS is in cut off while the pMOS is biased into the active region.
- Ideally, the simplified MOSFET equations give $\mathbf{I_{Dp}=0}$, which implies that the source-drain voltage $\mathbf{V_{SDp}=0}$.
- Since the source of the pMOS is connected to the power supply voltage $\mathbf{V_{DD}}$, KVL gives

$$V_{out} = V_{DD} - V_{SDp} \quad = V_{DD} \quad = V_{OH}$$

CMOS INVERTER – DC CHARACTERISTICS

✓ OUTPUT LOW VOLTAGE (V_{OL})

- The output-low voltage $\mathbf{V_{OL}}$ represents the smallest value of $\mathbf{V_{out}}$ from the circuit.
- Setting the input voltage to a value $\mathbf{V_{in} = V_{DD} > (V_{DD} - |V_{THp}|)}$ places M_p in cut off and defines the condition needed to calculate the value of $\mathbf{V_{out}=V_{OL}}$
- Since M_n is biased active but has $\boldsymbol{I_{Dn}=0}$,the drain-source voltage across the nMOS is $\boldsymbol{V_{DSn}=0}$.
- The inverter output is given by

$$V_{out} = V_{DSn} \quad = 0 \quad = V_{OL}$$

CMOS INVERTER – DC CHARACTERISTICS

- An important property of CMOS is that the output logic swing V_L is given by

$$V_L = V_{OH} - V_{OL}$$
$$= V_{DD}$$

- This shows that the CMOS inverter exhibits a **full-rail** output voltage swing, i.e., the entire power supply range.

- This helps provide well-defined logic 0 and logic 1 voltages.

CMOS INVERTER – DC CHARACTERISTICS

✓ **INPUT LOW VOLTAGE (V_{IL})**

- The input low voltage V_{IL} represents the largest value of V_{in} that can be interpreted as a logic 0 input.
- If the input voltage satisfies $V_{in}<V_{IL}$ then the output voltage V_{out} is either at V_{DD} or close to it, indicating that the output can be interpreted as a logic 1.
- If V_{in} is increased above V_{IL}, the circuit moves into the transition region.
- Using stability arguments, we define V_{IL} as the point where the slope of the VTC has a value of -1, i.e.,

$$\frac{dV_{out}}{dV_{in}} = -1$$

CMOS INVERTER – DC CHARACTERISTICS

✓ **INPUT LOW VOLTAGE (V_{IL})**

- At this point, the M_n is saturated while the M_p is conducting in the non-saturated mode.
- Equating currents $\mathbf{I_{Dn} = I_{Dp}}$ gives

$$\frac{\beta_n}{2}(V_{in} - V_{THn})^2 = \frac{\beta_p}{2}\left[2(V_{DD} - V_{in} - |V_{THp}|)(V_{DD} - V_{out}) - (V_{DD} - V_{out})^2\right]$$

EQN 2.13

- The derivative condition is applied by first writing the functional relationship

$$I_{Dn}(V_{in}) = I_{Dp}(V_{in}, V_{out})$$

- Taking differentials of both sides gives

CMOS INVERTER – DC CHARACTERISTICS

✓ **INPUT LOW VOLTAGE (V_{IL})**

- Substituting and calculating the derivatives yields

$$V_{in}\left(1 + \frac{\beta_n}{\beta_p}\right) = 2V_{out} - V_{DD} - |V_{THp}| + \frac{\beta_n}{\beta_p} V_{THn}$$

CMOS INVERTER – DC CHARACTERISTICS

✓ INPUT HIGH VOLTAGE (V_{IH})

- The input high voltage $\mathbf{V_{IH}}$ is the smallest value of $\mathbf{V_{in}}$ that can be interpreted as a logic 1 level.
- An input voltage of $\mathbf{V_{in} \geq V_{IH}}$ gives an output voltage that is either 0V or close to it.
- To calculate $\mathbf{V_{IH}}$, we use the current flow equations and the unity slope condition as in finding $\mathbf{V_{IL}}$.
- Now, M_n is non-saturated while M_p is saturated so that equating currents gives

$$\frac{\beta_n}{2}[2(V_{in} - V_{THn})V_{out} - V_{out}^2] = \frac{\beta_p}{2}(V_{DD} - V_{in} - |V_{THp}|)^2$$

CMOS INVERTER – DC CHARACTERISTICS

✓ INPUT HIGH VOLTAGE (V_{IH})

- Substituting the current equations and differentiating equation

$$V_{in}\left(1 + \frac{\beta_p}{\beta_n}\right) = 2V_{out} + V_{THn} + \frac{\beta_p}{\beta_n}(V_{DD} - |V_{THp}|)$$

CMOS INVERTER – DC CHARACTERISTICS

✓ INVERTER THRESHOLD (MIDPOINT) VOLTAGE (V_I)

- The voltage $\mathbf{V_I}$ is called the **inverter gate threshold voltage**, and is defined by the point where the voltage transfer curve intersects the unity gain line defined by $\mathbf{V_{out}=V_{in}}$
- $\mathbf{V_I}$ is the midpoint between the borders of the logic 0 and logic 1 input voltages $\mathbf{V_{IL}}$ and $\mathbf{V_{IH}}$ and is a very useful parameter that characterizes the entire VTC.
- This gives rise to the alternate notation and terminology in the literature for this voltage as $\mathbf{V_M}$, **the midpoint voltage**.

CMOS INVERTER – DC CHARACTERISTICS

✓ INVERTER THRESHOLD (MIDPOINT) VOLTAGE (V_I)

- The value of $\mathbf{V_I}$ can be found by definition,

$$\mathbf{V_{out} = V_{in} = V_I}$$

- so that

$$\mathbf{V_{GSn} = V_I = V_{DSn}}$$
$$\mathbf{V_{SGp} = V_{DD} - V_I = V_{SDp}}$$

- holds for the MOSFET voltages.
- These equations show that both the nMOS and the pMOS are operating in the saturation region.
- Equating currents gives

$$\frac{\beta_n}{2}(V_I - V_{THn})^2 = \frac{\beta_p}{2}(V_{DD} - V_I - |V_{THp}|)^2$$

CMOS INVERTER – DC CHARACTERISTICS

✓ INVERTER THRESHOLD (MIDPOINT) VOLTAGE (V_I)

- so that

$$V_I = \frac{V_{DD} - |V_{THp}| + \sqrt{\frac{\beta_n}{\beta_p}} V_{THn}}{1 + \sqrt{\frac{\beta_n}{\beta_p}}} = V_M$$

- gives the desired result.
- Note that the device ratio $\frac{\beta_n}{\beta_p}$ is the important quantity that determines the value of V_I for a given circuit.

CMOS INVERTER – DC CHARACTERISTICS

✓ INTERPRETATION OF CRITICAL VOLTAGES

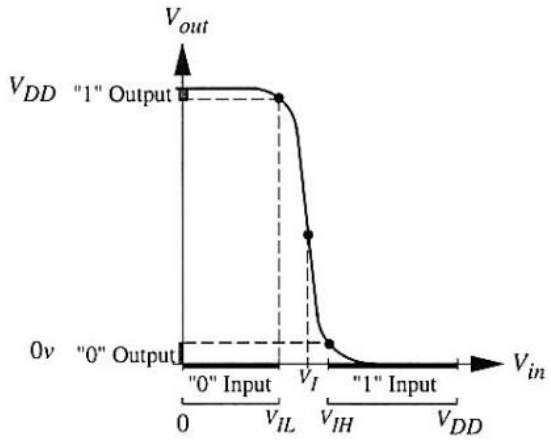


Figure 2.12: Interpretation Of Critical Voltages

CMOS INVERTER – DC CHARACTERISTICS

✓ INTERPRETATION OF CRITICAL VOLTAGES

- Consider the input voltage $\mathbf{V_{in}}$ as it is increased from 0V.
- For input voltages in the range $\mathbf{0 \leq V_{in} \leq V_{IL}}$, the output voltage is high at either a perfect logic 1 voltage $\mathbf{V_{out} = V_{DD}}$ or very close to it.
- This then allows us to identify this range of voltages as logic 0 input values.
- When $\mathbf{V_{in}}$ is in the high range defined by $\mathbf{V_{IH} \leq V_{in} \leq V_{DD}}$, then the output voltage is either at a perfect logic 0 value $\mathbf{V_{out} = 0V}$ or very close to it.
- We thus identify these values of $\mathbf{V_{in}}$ as corresponding to logic 1 inputs.

CMOS INVERTER – DC CHARACTERISTICS

✓ INTERPRETATION OF CRITICAL VOLTAGES

- The inverter threshold voltage always has the characteristic that $\mathbf{V_{IL} \leq V_I \leq V_{IH}}$
- We may thus interpret this as the midpoint voltage $\mathbf{V_M = V_I}$ such that

  $\mathbf{V_{in} < V_M}$ ➔ **Input is probably a logic 0**

  and

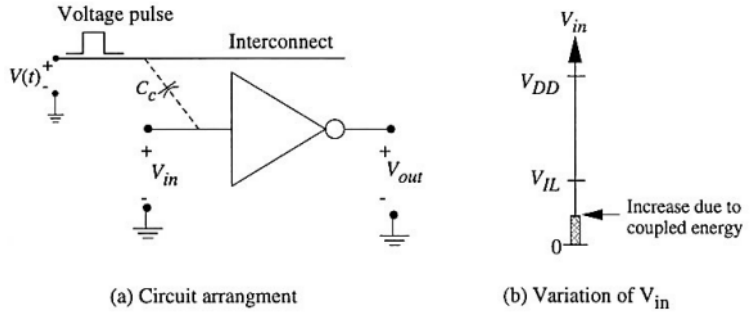
  $\mathbf{V_{in} > V_M}$ ➔ **Input is probably a logic 1**

- with $\mathbf{V_{IL}}$ and $\mathbf{V_{IH}}$ providing more precise limits.

CMOS INVERTER – DC CHARACTERISTICS

✓ **NOISE MARGINS**

- The meaning of the critical input and output voltages gains greater significance when coupled to the concept of noise margins.
- Consider the situation in Figure 2.13a where the input of an inverter is close to a neighbouring interconnect line.



(a) Circuit arrangment (b) Variation of V_{in}

Figure 2.13: Noise Margin

CMOS INVERTER – DC CHARACTERISTICS

✓ **NOISE MARGINS**

- A parasitic coupling capacitance C_C exists between the two, so that applying a voltage pulse to one line will cause a change in the voltage in the other.
- Suppose that the input to the inverter is initially at 0v.
- With this type of electric coupling, the value of V_{in} can jump to a voltage as shown in Figure 2.13b.
- If the increase is large, then an incorrect switching event may occur.
- However, so long as the input voltage remains below V_{IL}, then the input will still be correctly interpreted as a logic 0 voltage.
- ***Noise margins provide a quantitative measure of how resistant a circuit is to false switches.***

CMOS INVERTER – DC CHARACTERISTICS

✓ **NOISE MARGINS**

- We define the voltage noise margin for logic 1 (high) voltages as

$$VNM_H = V_{OH} - V_{IH}$$
$$= V_{DD} - V_{IH}$$

- Similarly, the voltage noise margin for logic 0 (low) voltages as

$$VNM_L = V_{IL} - V_{OL}$$
$$= V_{IL} \qquad \text{EQN 2.25}$$

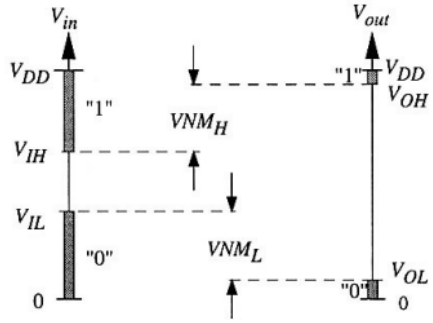


Figure 2.14: Noise Margins

CMOS INVERTER – DC CHARACTERISTICS

✓ **NOISE MARGINS**

- For a functional digital circuit, we must have $\mathbf{VNM_L > 0}$ and $\mathbf{VNM_H > 0}$
- Noise margins are particularly important when designing low voltage circuits, i.e., those with small power supply values.
- This is because as $\mathbf{V_{DD}}$ shrinks, the definitions of logic 0 and 1 voltage ranges also shrink, and the gates are more susceptible to spurious signals from neighboring lines.