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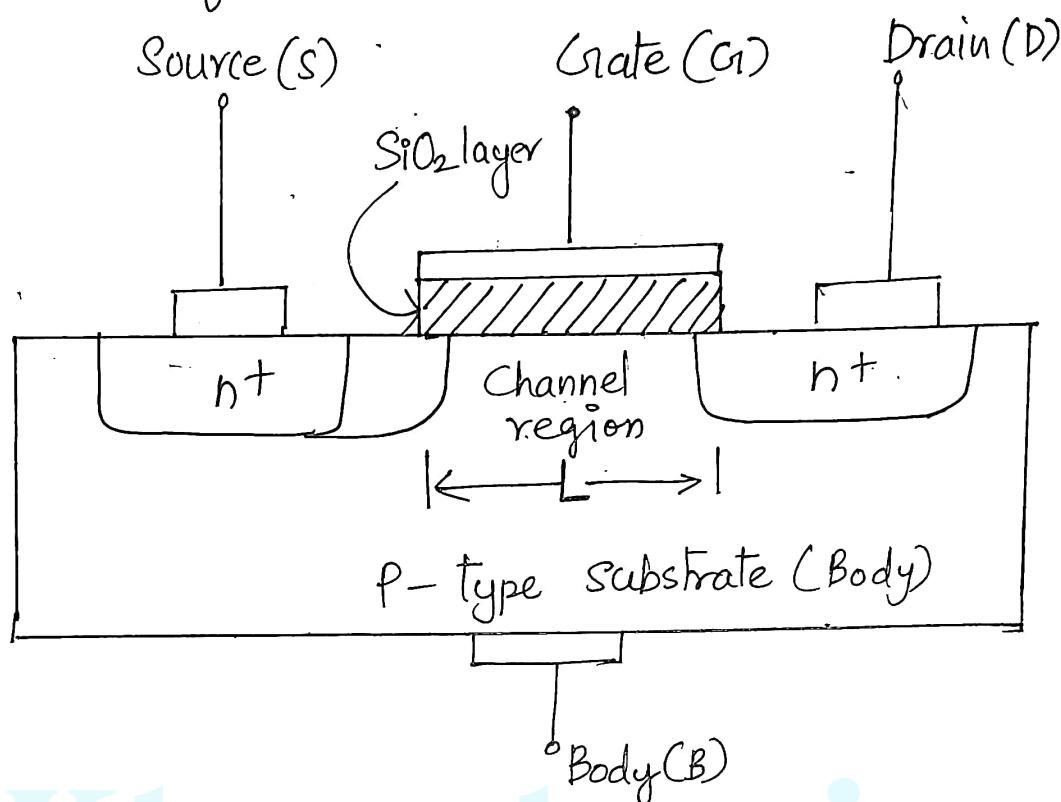
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## MOSFET Amplifier

### Structure of n-channel Enhancement type of MOSFET

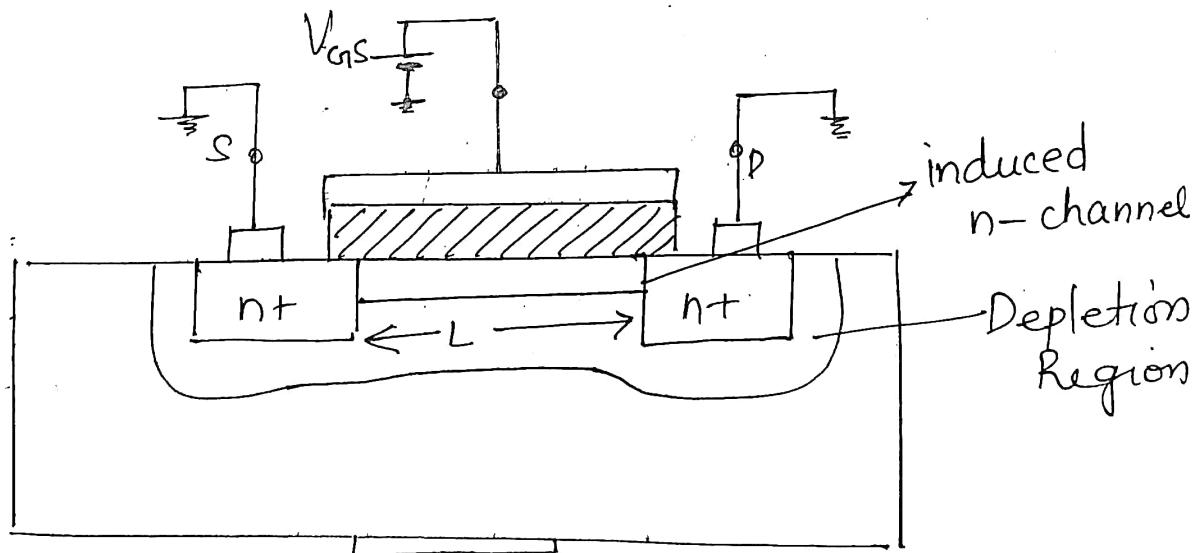


The enhancement type MOSFET is the most widely used FET. The transistor is fabricated on a p-type substrate. Two heavily doped n-regions (n+) are created in the substrate (source and drain). A thin layer of SiO<sub>2</sub> insulates gate terminal from the body. Another name for MOSFET is IGFET (Insulated Gate FET). In a MOSFET the current flows in the longitudinal direction from drain to source through the channel region. L and W are the length and width of channel. Typical values L: 0.1 to 0.3 μm. W: 0.2 to 100μm. MOSFET is a symmetrical device, in the source and drain can be interchanged with no changes in device

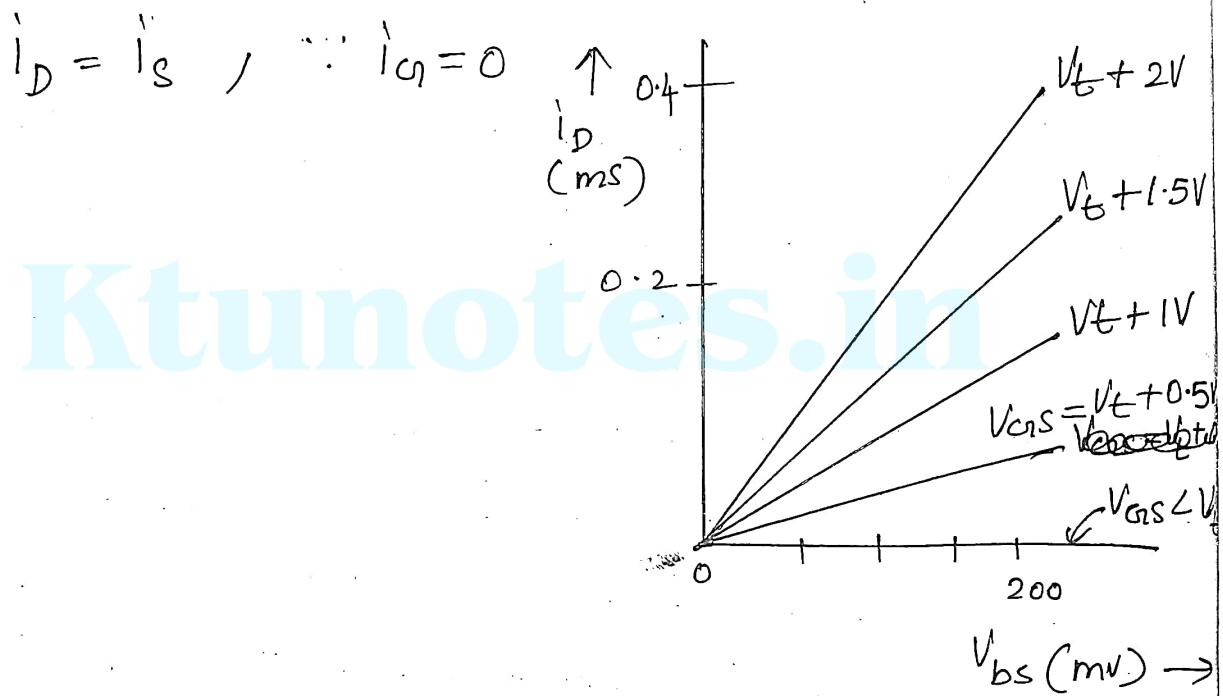
characteristics.

When a positive voltage is applied to the gate, an n-channel is induced at the top of the substrate beneath the gate. The value of  $V_{GS}$  at which sufficient no. of mobile electrons accumulate in the channel region to form a conducting channel is called the threshold voltage ( $V_t$ ). It is controlled during fabrication typically 0.5 to 1 V.

The gate and the channel region of the MOSFET form a parallel plate capacitor, with the oxide layers as dielectric. +ve gate voltage causes positive charge to accumulate on the top of the plate. The corresponding negative charge on the bottom plate is formed by electrons in the induced channel. The gate field controls the amount of charge in the channel and thus determines the channel conductivity and, in turn the channel current when  $V_{DS}$  is applied.

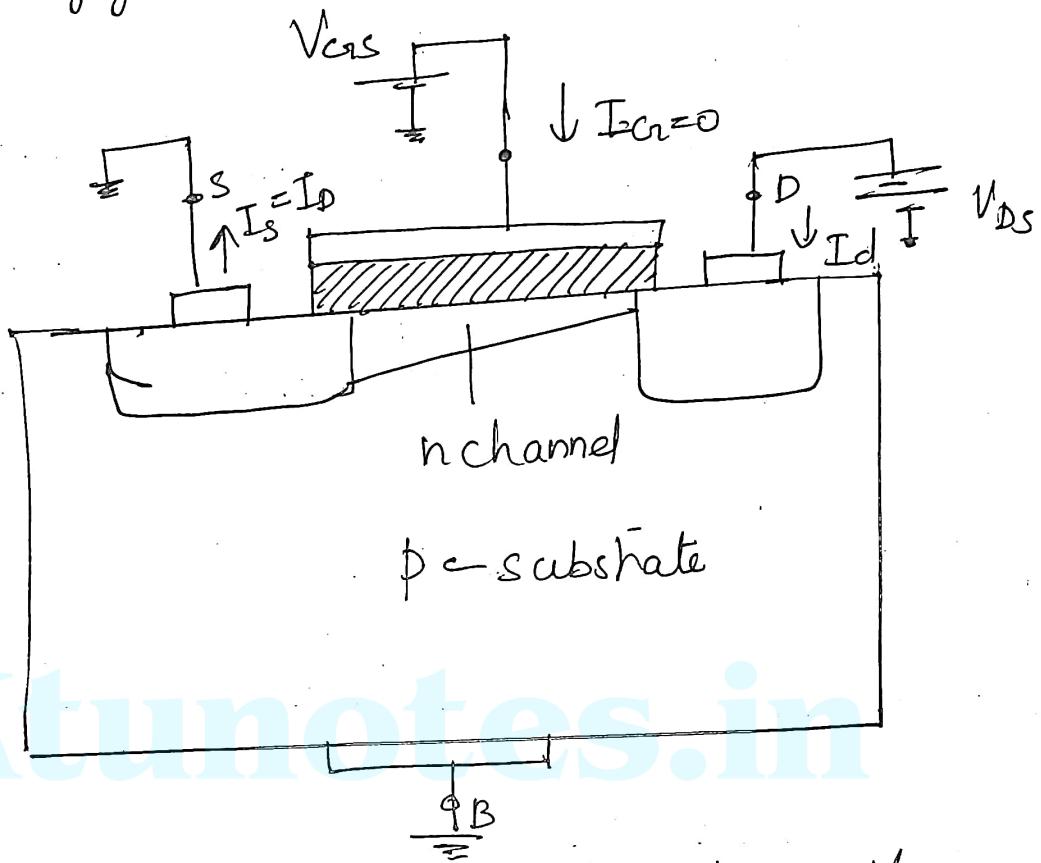


When  $V_{GS} > V_t$  and a small  $V_{DS}$  is applied, the device acts as a resistance whose value is determined by  $V_{GS}$ . The channel conductance is proportional to excess gate voltage ( $V_{GS} - V_t$ ) and it is proportional to  $(V_{GS} - V_t)V_{DS}$ . Increasing  $V_{GS}$  above the threshold voltage enhances the channel, hence enhancement mode operation or enhancement type MOSFET.



When  $V_{DS}$  is increased by keeping  $V_{GS} > V_t$ ,  $V_{DS}$  appears as a voltage drop across the channel from source to drain. Hence the voltage b/w gate and points along the channel decreases from  $V_{GS}$  at the source end to  $V_{GS} - V_{DS}$  at the drain end.

Since the channel depth depends on this voltage, the channel will no longer be at uniform width. It gets tapered. As  $V_{DS}$  is increased, the channel becomes more tapered and its resistance increases correspondingly.



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Curve bends because  
channel resistance  
increases with  $V_{BS}$

Almost straight  
line with slope  
proportional to  
 $V_{GDS} - V_t$

current saturation because  
the channel is pinched off  
at the drain end and  $V_{DS}$   
no longer affects the channel

$$V_{GDS} > V_t$$

$$V_{DS_{sat}} = V_{GS} - V_t$$

For every value of  $V_{GS} > V_t$ , there is corresponding value of  $V_{DS_{sat}}$ .

Saturation Region:  $V_{DS} > V_{DS_{sat}}$

$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$$

~~$\epsilon_{ox}$~~   $\epsilon_{ox}$  — permittivity of  $\text{SiO}_2$   
 $t_{ox}$  — thickness of oxide layer.

$$\epsilon_{ox} = 3.9 \epsilon_0 = 3.9 \times 8.854 \times 10^{-12} = 3.45 \times 10^{-11} \text{ F/m}$$

$$I_D = \frac{1}{2} \times k_n' \frac{W}{L} (V_{GS} - V_t)^2 \quad \text{— saturation region.}$$

$k_n'$  = ~~Mn~~  $C_{ox}$  — process transconductance parameter.

$\frac{W}{L}$  = aspect ratio.

For a MOSFET,  $\frac{W}{L} = \frac{8 \mu\text{m}}{0.8 \mu\text{m}}$ ,  $k_n' = 194 \mu\text{A/V}^2$ ,

$V_t = 0.7 \text{ V}$ . Calculate the value of  $V_{GS}$  and  $V_{DS_{min}}$  needed to operate the transistor in the saturation region with ~~as~~ a dc current  $I_D = 100 \mu\text{A}$ .

$$I_D = \frac{1}{2} k_n' \frac{W}{L} (V_{GS} - V_t)^2$$

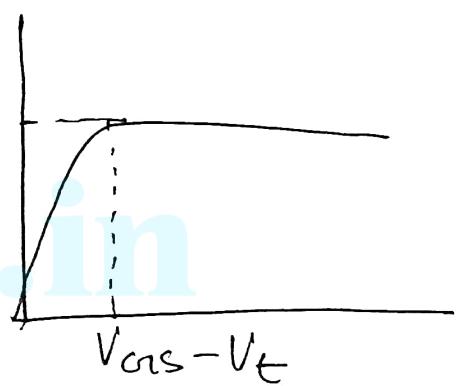
$$100 \times 10^{-6} = \frac{1}{2} \times 194 \times 10^{-6} \times \frac{8}{2} (V_{GS} - 0.7)^2$$

$$(V_{GS} - 0.7)^2 = 0.103$$

$$V_{GS} - 0.7 = 0.32$$

$$V_{GS} = \underline{\underline{1.02V}}$$

$$V_{DSmin} = V_{GS} - V_T = \underline{\underline{0.32V}}.$$

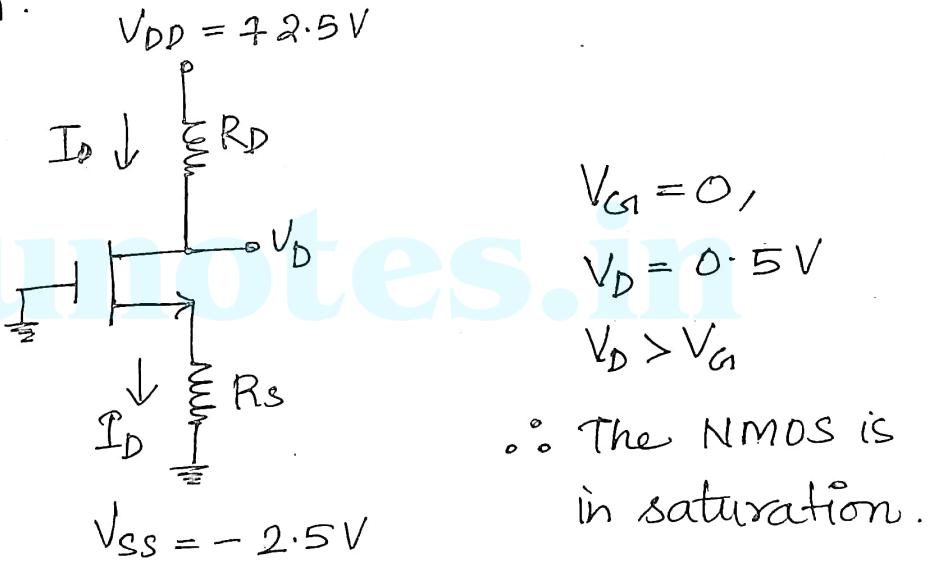


## MOSFET Circuits at D.C

over drive voltage  $V_{ov} = V_{gs} - V_t$

- Design the following circuit so that the transistor operates at  $I_D = 0.4 \text{ mA}$  and  $V_D = 0.5 \text{ V}$ .  $V_t = 0.7 \text{ V}$ ,  $MnCox = 100 \text{ MA/V}^2$ ,  $L = 1 \mu\text{m}$ ,  $W = 32 \mu\text{m}$ . Neglect channel length modulation.

Ans:-



$$I_D = \frac{1}{2} MnCox \frac{W}{L} (V_{gs} - V_t)^2$$

$$0.4 \times 10^{-3} = \frac{1}{2} \times 100 \times 10^6 \times \frac{32}{1} (V_{gs} - V_t)^2$$

$$(V_{GDS} - V_t)^2 = 0.25$$

$$V_{GDS} - V_t = 0.5$$

$$V_{GDS} = 0.5 + V_t = 0.5 + 0.7 = \underline{\underline{1.2V}}$$

$$V_{GDS} = V_G - V_S = 0 - V_S = 1.2V$$

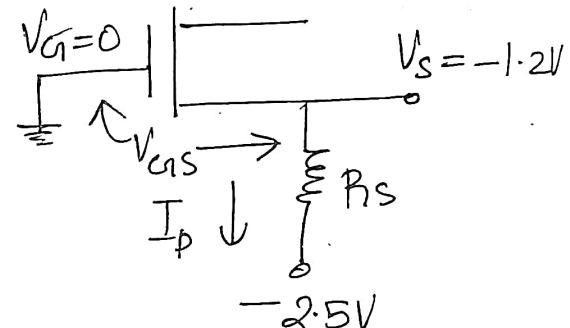
$$V_S = \underline{\underline{-1.2V}}$$

$$R_S = \frac{V_S - V_{SS}}{I_D}$$

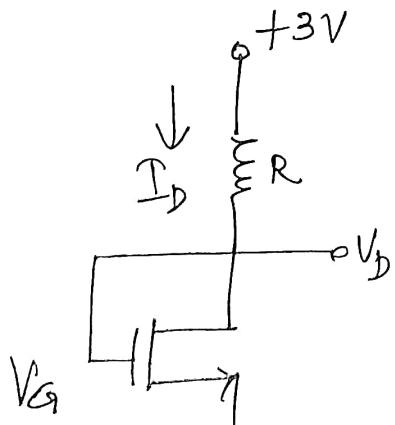
$$= \frac{-1.2 - (-2.5)}{0.4 \times 10^{-3}}$$

$$R_S = \underline{\underline{3.25k\Omega}}$$

$$R_D = \frac{V_{DD} - V_D}{I_D} = \frac{2.5 - 0.5}{4 \times 10^{-3}} = \underline{\underline{5k\Omega}}$$



2. Design the circuit to obtain an  $I_D = 80\text{ }\mu\text{A}$ . Find  $R$  and  $V_D$ . Given :  $V_t = 0.6V$ ,  $M_n C_{ox} = 200\text{ }\mu\text{A/V}^2$ ,  $L = 0.8\text{ }\mu\text{m}$ ,  $W = 4\text{ }\mu\text{m}$ .



$$V_{DGS} = 0$$

$$V_D = V_G$$

$$V_{DS} > (V_{GDS} - V_t)$$

$\therefore$  Saturation region

$$k_m' = M_n C_{ox} = 200\text{ }\mu\text{A/V}^2$$

$$I_D = \frac{1}{2} \times k_n' \frac{W}{L} (V_{GS} - V_t)^2$$

$$\Rightarrow \frac{1}{2} \times 200 \times 10^{-6} \times \frac{4}{0.8} (V_{GS} - V_t)^2 = 80 \times 10^{-6}$$

$$(V_{GS} - V_t)^2 = \frac{2 \times 80 \times 10^{-6}}{200 \times 10^{-6} \times \frac{4}{0.8}} = \underline{\underline{0.16}}$$

$$\therefore V_{GS} - V_t = \underline{\underline{0.4V}}$$

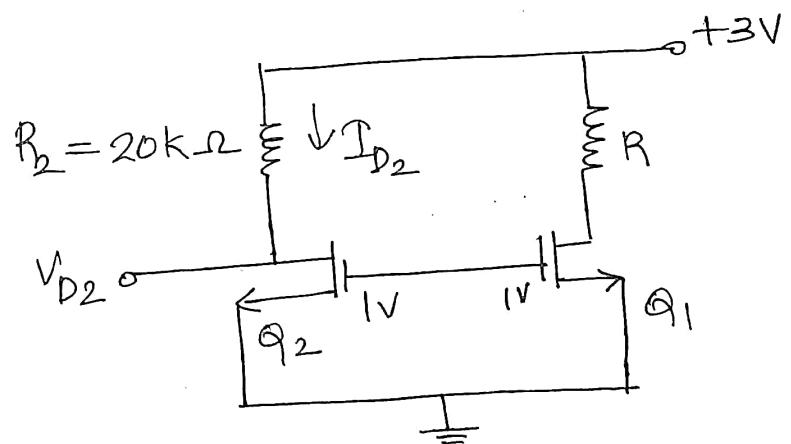
$$V_{GS} = V_t + 0.4V = 0.6 + 0.4 = 1V$$

~~As~~ Drain is shorted to gate,  $V_D = V_G = 1V$

$$R = \frac{V_{DD} - V_D}{I_D} = \frac{3 - 1}{80 \times 10^{-6}} = \underline{\underline{25k\Omega}}$$

3. Find the drain current and voltage of  $Q_2$  assuming  $Q_1$  identical to  $Q_2$ .  $k_n' = 200 \mu A/V^2$ ,  $\frac{W}{L} = \frac{4 \text{ Ms}}{0.8 \mu m}$ ,  $V_t = 0.6V$ ,  $V_{GS1} = 1V$ .

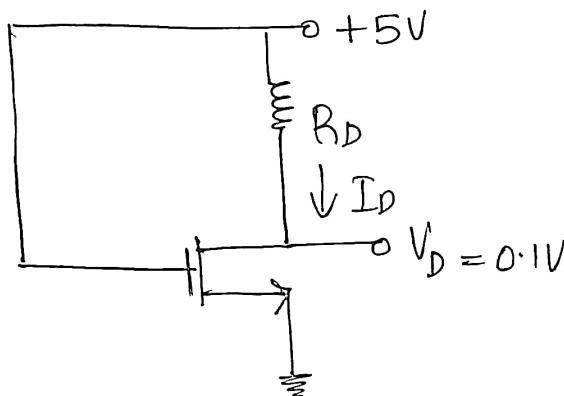
$$\begin{aligned} I_{D2} &= \frac{1}{2} k_n' \frac{W}{L} (V_{GS} - V_t)^2 \\ &= \frac{1}{2} \times 200 \times 10^{-6} \times \frac{4}{0.8} (1 - 0.6)^2 \\ &= \underline{\underline{80 \text{ mA}}} \end{aligned}$$



$$\begin{aligned} V_{D2} &= \cancel{V_{DD}} - I_{D2} R_2 \\ &= 3 - 80 \times 10^{-6} \times 20 \times 10^3 \\ &= \underline{\underline{1.4V}} \end{aligned}$$

4. Design the circuit to establish a drain voltage of 0.1V. What is the effective resistance between drain and source at this operating point?

$$V_t = 1V, k_n' \frac{W}{L} = 1mA/V^2$$



$$V_{DS} = 0.1V$$

~~$V_{DD} = 5V$~~

$V_{GS} = 5V$

$\therefore V_D < V_{GS}$ , the MOSFET is in the triode region

$$I_D = k_n' \frac{W}{L} \left[ (V_{GS} - V_t) V_{DS} - \frac{1}{2} V_{DS}^2 \right]$$

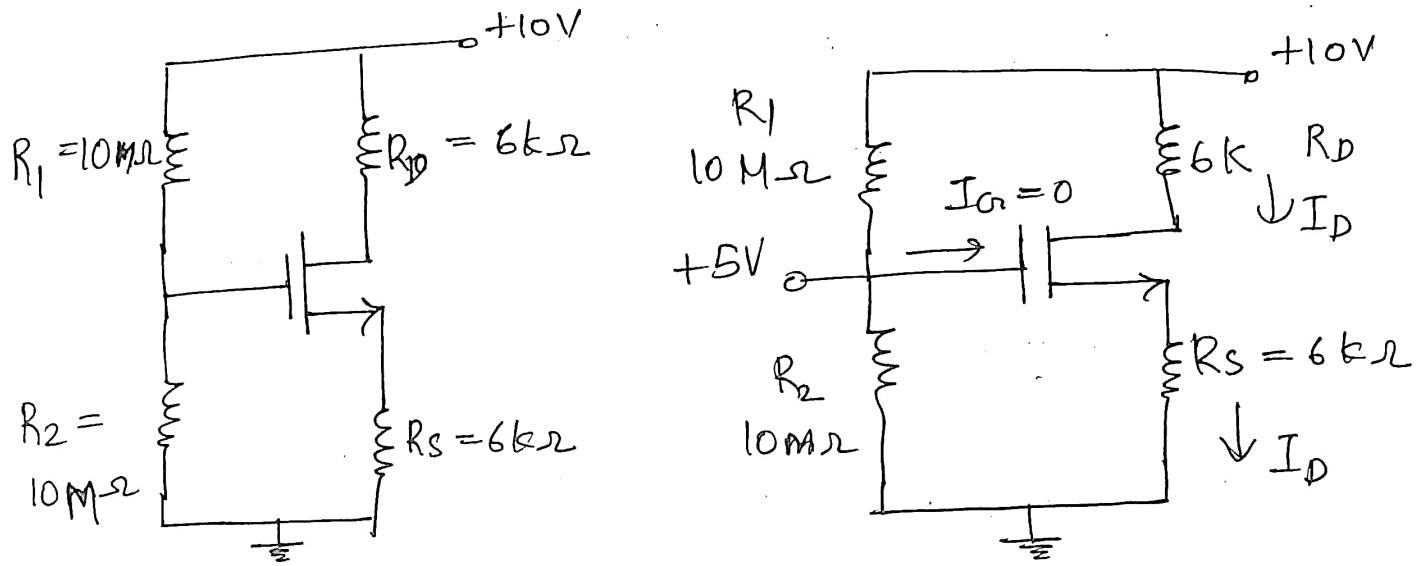
$$= 1 \times 10^{-3} \left[ (5 - 1) 0.1 - \frac{(0.1)^2}{2} \right]$$

$$= 0.395 \mu A$$

$$R_D = \frac{V_{DD} - V_{DS}}{I_D} = \frac{5 - 0.1}{0.395 \times 10^{-3}} = 12.4k\Omega$$

$$r_{DS} = \frac{V_{DS}}{I_D} = \frac{0.1}{0.395 \times 10^{-3}} = 253\Omega$$

5. Analyse the circuit to determine the voltages at all nodes and the currents through all branches.  $V_t = 1V, k_n' \frac{W}{L} = 1mA/V^2$ .



$$V_{R_2} = \frac{10 \times 10 \times 10^6}{(10 \times 10^6 + 10 \times 10^6)} = \frac{10 \times 10 \times 10^6}{2 \times 10 \times 10^6} = 5V$$

$$I_D = \frac{V_{DD}}{R_1 + R_2} = \frac{10}{(10 + 10) \times 10^6} = 0.5 \times 10^{-6} = 0.5 \text{ mA}$$

$\therefore V_{DS}$  is not known; we will here assume the operating region either saturation region or triode.

Assuming saturation,

$$V_{DS} = V_G - V_S = 5 - 6 \times 10^3 I_D \quad \text{--- (1)}$$

In saturation,

$$\begin{aligned} I_D &= \frac{1}{2} k n^1 \frac{W}{L} (V_{DS} - V_t)^2 \\ &= \frac{1}{2} \times 1 \times 10^{-3} (5 - 6 \times 10^3 I_D - 1)^2 \\ &= \frac{10^{-3}}{2} [4 - 6 \times 10^3 I_D] \\ &= \frac{10^{-3}}{2} [16 + 36 \times 10^6 I_D^2 - 48 \times 10^3 I_D] \\ &\approx 8 \times 10^{-3} + 18 \times 10^3 I_D^2 - 24 I_D \end{aligned}$$

$$I_D = \frac{25 \pm \sqrt{25^2 - 4 \times 18 \times 10^3 \times 8 \times 10^{-3}}}{2 \times 18 \times 10^3} = \frac{25 \pm \sqrt{49}}{36 \times 10^3}$$

$$= \frac{25 \pm 7}{36 \times 10^3}$$

$$= 0.89 \text{mA}, \quad 0.5 \text{mA}$$

If  $I_D = 0.89 \text{mA}$ ,  $V_S = 6 \times 0.84 = 5.04 \text{V} > V_A$

$\therefore$  The Mos tr will be cut off.  $\therefore$  This  $I_D$  - does not make sense

$$\text{Hence, } I_D = 0.5 \text{mA}$$

$$V_S = 6 \times 10^3 I_D = 6 \times 10^3 \times 0.5 \times 10^{-3} = 3 \text{V}$$

$$V_{GS} = V_A - V_S = 5 - 3 = 2 \text{V}$$

$$V_D = 10 - 6 \times 10^3 I_D = 10 - 6 \times 10^3 \times 0.5 \times 10^{-3} \\ = 7 \text{V}$$

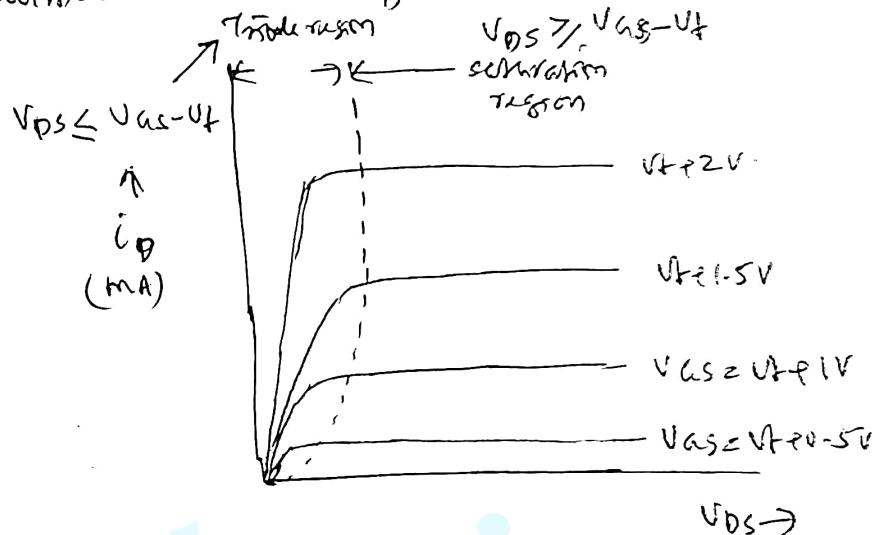
$$V_{GS} = V_A - V_S = 5 - 3 = 2 \text{V}$$

$$V_{DS} = V_D - V_S = 7 - 3 = 4 \text{V}$$

$\therefore V_{DS} > (V_{GS} - V_t)$ , the transistor is in saturation

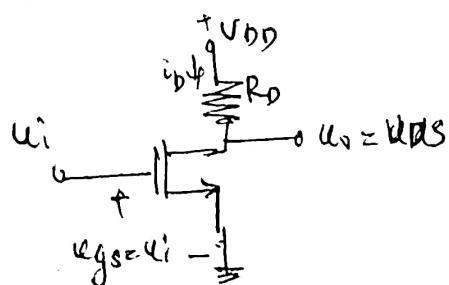
MOSFET as an amplifier.

When operated in the saturation region, the MOSFET acts as a voltage controlled current source. Change in  $V_{GS}$  causes change in  $i_D$ .



Thus a saturated MOSFET can be used to implement a transconductance amplif'.  $A = \frac{R_o}{V_T}$ . By keeping  $V_{GS}$  small, the change in drain current  $i_D$  can be made proportional to  $V_{GS}$ .

Large signal operation of MOSFET amplif'



From the op circuit,

$$V_{DS} = V_{DD} - i_D R_D$$

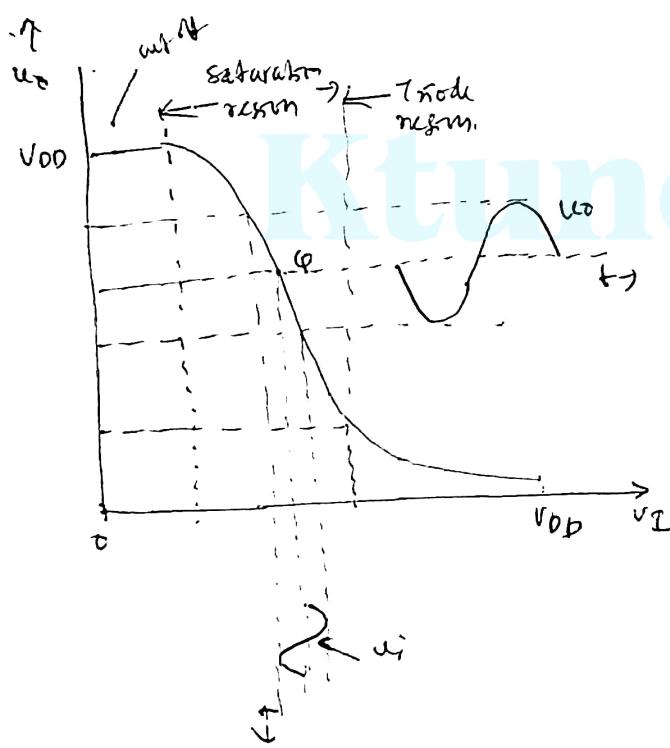
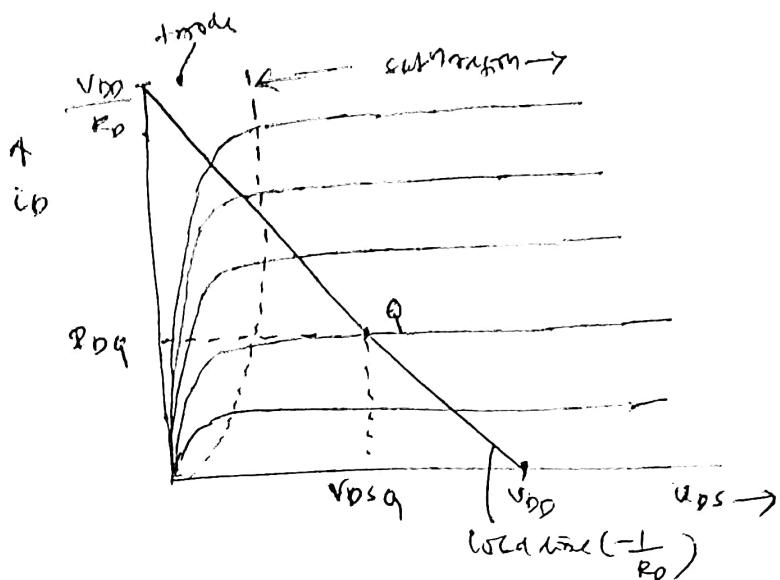
$$i_D = \frac{V_{DD}}{R_D} - \frac{1}{R_D} \cdot V_{DS}$$

Figure shows an CS amplifier circuit. When  $V_{GS} = V_i$  is

Variety,  $i_D$  varies and  $R_D$  is used to obtain drain voltage.

$$U_D = U_{DS} = V_{DD} - i_D R_D$$

This way the draininduced amplifier is converted into a voltage amplifier.



From the transfer char.  
It is clear that when a small  $i_D$  is applied it gets amplified.

Transfer characteristic showing operation as amplifier.

The load line is marked in the drain char. It passes through  $(0, \frac{V_{DD}}{R_D})$  and  $(V_{DD}, 0)$ . Slope of the line is  $-\frac{1}{R_D}$ .

Once an operating point is selected at Q, when  $i_D$  voltage

is applied; during positive half cycle if operating point moves up along the load line,  $i_D$  increases and  $V_{DS}$  decreases. During -ve half cycle, the operating point moves down,  $i_D$  decreases and  $V_{DS}$  increases. The transistor characteristics clearly explains the amplification operation.

### Biasing of MOSFET amplifier

An important step in the design of a MOSFET amplifer is the selection of operating point. This is done by proper biasing of the transistor. For proper operation of the amplifier, the operating point must remain in the saturation region for all expected input signal levels.

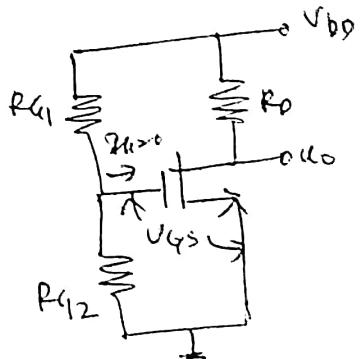
#### I. Biasing by fixing $V_{GS}$ (fixed bias)

The straight forward approach of biasing a MOSFET is to fix its gate to source voltage  $V_{GS}$  to the required value to provide desired  $i_D$ . Required  $V_{GS}$  can be derived from  $V_{DD}$  using a voltage divider as shown in the circuit.

$$V_{GS} = V_{DD} \times \frac{R_{G2}}{R_{G1} + R_{G2}}$$

$$V_S = 0, R_{G2} = 0.$$

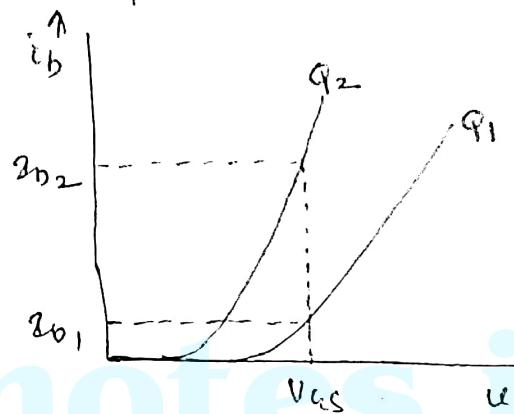
$R_{G1}$  and  $R_{G2}$  must be in M.L.s.



$$I_D = \frac{1}{2} g_m C_{ox} \frac{W}{L} (V_{GS} - V_t)^2$$

The values of threshold voltage  $V_t$ , oxide capacitance  $C_{ox}$

and drain-to-source aspect ratio  $\frac{W}{L}$  vary widely among devices of the same type. Also both  $V_F$  and  $\mu_m$  depend on temperature.



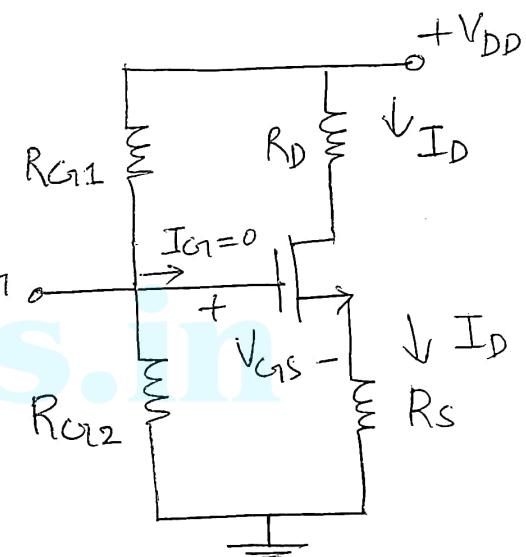
The  $i_D, V_{DS}$  char. of two MOSFETs of the same type is shown above. If the device is biased by fixing  $V_{DS}$ , when transistors replaced with another, there will be a wide variation in the value of  $i_D$ . Also if temperature changes the operating point will vary. Hence this is not a good method for MOSFET biasing.

→ Method by fixing  $V_G$  and connecting a resistance in the

2. Biasing by fixing  $V_{G1}$  and connecting a resistance in the source.

$$V_{G1} = V_{DD} \times \frac{R_{G12}}{R_{G11} + R_{G12}} \quad \text{--- (1)}$$

$V_{G1}$  is fixed and a resistance is connected at the source.



$$V_{G1} = V_{GS} + I_D R_S \quad \text{--- (2)}$$

$$I_D = \frac{V_{G1} - V_{GS}}{R_S} \quad \text{--- (3)}$$

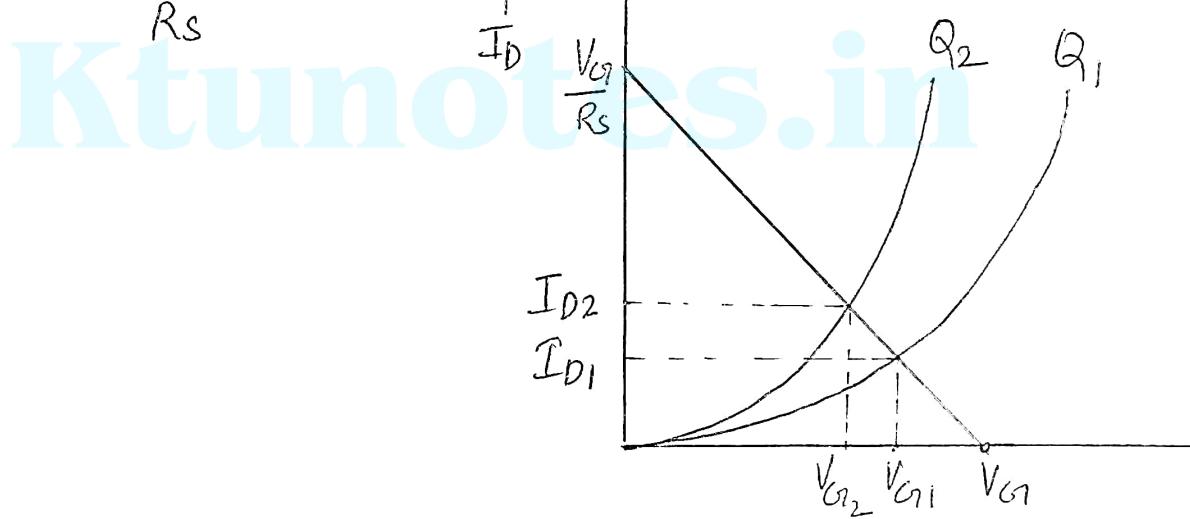
$R_s$  helps to stabilise the bias current  $I_D$  but provides negative F.B. If  $I_D$  increases,  $I_D R_s$  increases. Since  $V_{G1}$  is constant,  $V_{DS} = V_{G1} - I_D R_s$  decreases. When  $V_{DS}$  decreases,  $I_D$  decreases. Thus  $R_s$  helps to keep  $I_D$  as constant as possible. Due to negative FB,  $R_s$  is known as degeneration resistance.

$$V_{DS} = V_{G1} - I_D R_s$$

$$\therefore \text{When } I_D = 0, V_{DS} = V_{G1} \quad (V_{G1}, 0)$$

$$V_{DS} = 0 \Rightarrow V_{G1} - I_D R_s = 0 \quad (0, \frac{V_{G1}}{R_s})$$

$$\text{or } I_D = \frac{V_{G1}}{R_s}$$



Reduced variability at  $I_D$ .

From the characteristics it is clear that compared to the case of fixed  $V_{DS}$ , the variability of  $I_D$  is much smaller.

In the circuit, since  $I_{G1}=0$ ,  $R_{G1}$  and  $R_{G2}$  can be selected to be very large (in MΩ range)

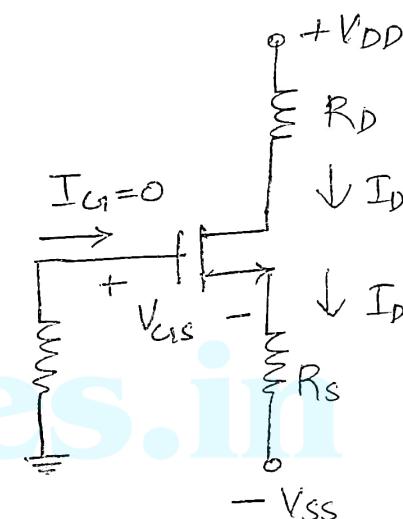
for large input resistance.

When  $R_D$  increases the o/p voltage swing increases and gain increases.  $R_D$  must be selected such that the gain is sufficient and also for the desired input signal swing, the MOSFET remains in saturation at all times.

Next fig. shows a 2nd circuit two power supplies. Since  $I_{G1}=0$ ,  $V_{G1}=0$ .

$$V_{G1}=0, \quad V_S = I_D R_S - V_{SS}$$

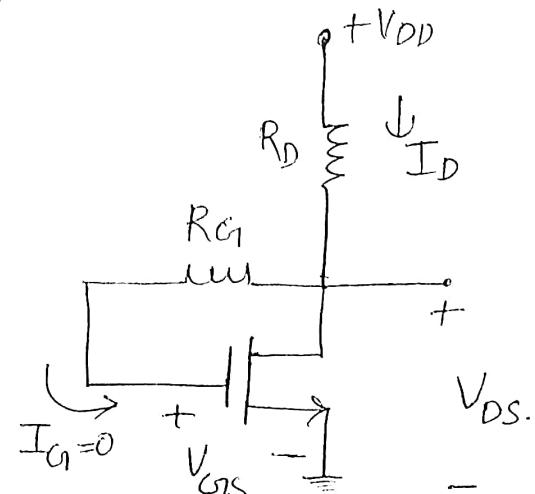
$$\begin{aligned} \therefore V_{GS} &= V_G - V_S \\ &= 0 - (I_D R_S - V_{SS}) \\ &= \underline{\underline{V_{SS} - I_D R_S}} \end{aligned}$$



In this circuit  $V_G$  is replaced by  $V_{GS}$ . Resistance  $R_{G1}$  establishes a dc ground and presents a high i/p resistance to the i/p source.

### 3. Biasing using a Drain to Gate FB resistance.

This circuit uses a large FB resistance b/w drain and gate.  $R_{G1}$  is in the M2s range. Since  $I_{G1}=0$ , the DC voltage at the gate will be equal to the drain voltage.



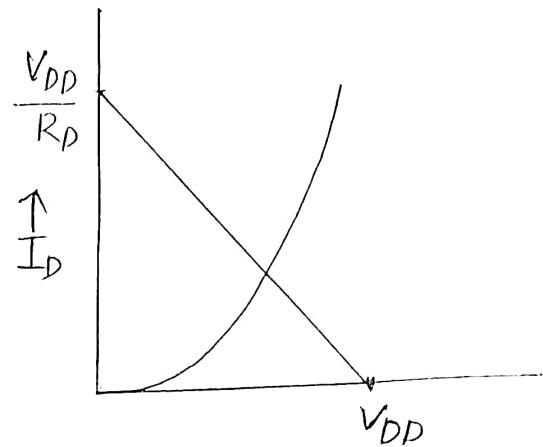
$$V_{DD} = I_D R_D + V_{DS} \quad \text{--- (1)}$$

$$V_{DS} = I_D R_S + V_{GS}$$

$$\therefore I_G = 0, \quad V_{DS} = V_{GS}$$

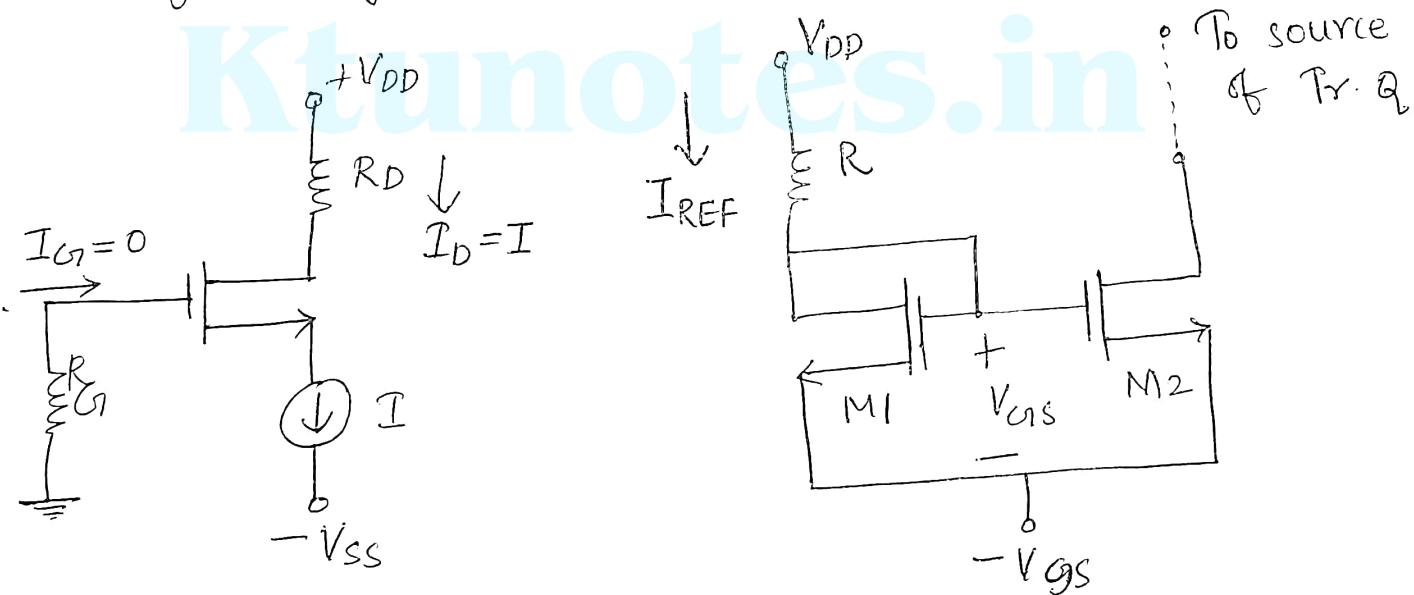
$$\therefore (1) \quad V_{DD} = I_D R_D + V_{GS}$$

$$\text{or} \quad V_{GS} = V_{DD} - I_D R_D \quad \text{--- (2)}$$



If  $I_D$  increases due to some reason,  $V_{GS}$  decreases. The reduction in  $V_{GS}$  in turn causes reduction in  $I_D$ . Thus the negative FB or degeneration provided by  $R_S$  keeps the value of  $I_D$  as constant as possible.

#### 4. Biasing using a constant current source.



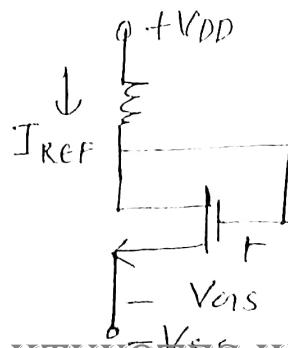
Implementation of constant current source of I using a current mirror.

Applying KVL,

$$V_{DD} - I_{REF} R - V_{GS} = -V_{SS}$$

$$I_{REF} R = V_{DD} + V_{SS} - V_{GS}$$

$$I_{REF} = \frac{V_{DD} + V_{SS} - V_{GS}}{R}$$



$\therefore$  Drain of M is shorted to Gate,  $V_{DS} = V_{GS}$

$\therefore V_{DS} > V_{GS} - V_t$  ( $V_{GS} > V_{GS} - V_t$ )

Hence M<sub>1</sub> will be in

saturation.  $\therefore V_{G1S1} = V_{GS2}$ ,  $I_{D2} = I_{D1}$  or  $I_{D1} = I_{REF}$  will be mirrored into  $I_{D2}$ .

This is the most effective scheme for biasing a MOSFET amplifier. The Q pt. value of  $I_D$  remains constant at I, the constant current provided by the constant current source.  $R_{G1}$  is M<sub>1</sub>  $\Omega$  range establishes a dc ground at the gate and provides a large input resistance to the amplifier.

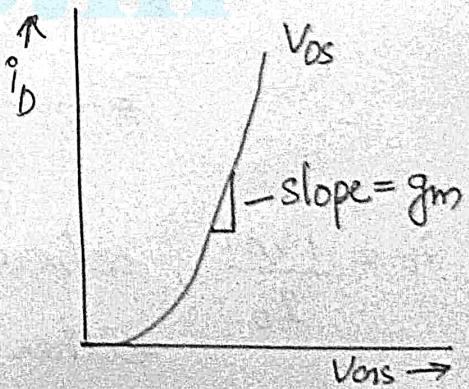
$R_D$  establishes an appropriate dc voltage at the drain.  $R_D$  should be selected such that ~~this is~~ it provides the required gain or o/p voltage and also keeps the transistor operation in the saturation region.

## MOSFET Small Signal models.

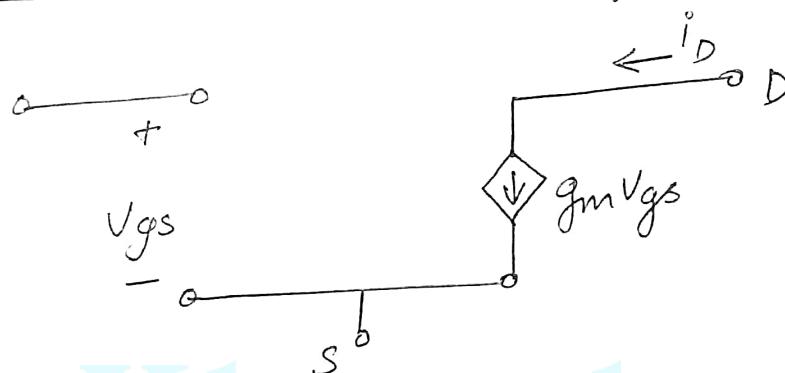
Linear amplification can be obtained by biasing the MOSFET to operate in the saturation region and by keeping the input signal small. The parameter  $g_m$  relates  $i_d$  with  $V_{gs}$ .

$$g_m = \frac{i_d}{V_{gs}} = \frac{\Delta i_d}{\Delta V_{gs}} \Big|_{V_{ds}}$$

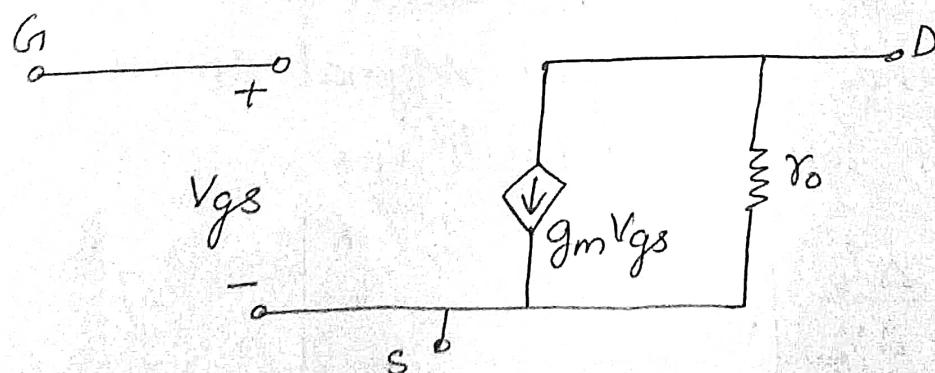
$g_m$  is the slope of the ~~isots~~  
 $i_d - V_{gs}$  char. at the operating point.



MOSFET behaves as a voltage controlled current source. It accepts a signal  $V_{gs}$  between gate and source and provides a current  $g_m V_{gs}$  at the drain. The input resistance of this controlled source is very high - ideally infinite. Thus we arrive at the following circuit which represents the small signal operation of the MOSFET and is thus a small signal model or small signal equivalent circuit.

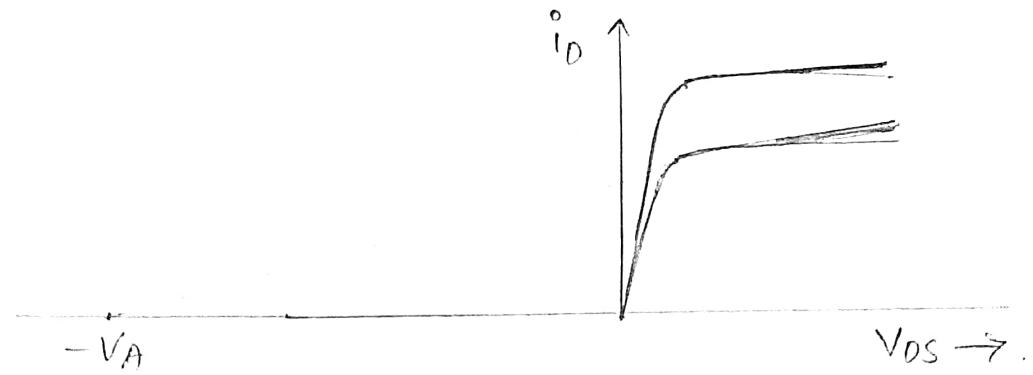


In the above equivalent circuit, it is assumed that the drain current in saturation is independent of drain voltage. But  $i_D$  depends on  $V_{ds}$  on a linear manner. This can be modelled by a finite resistance  $r_0$  between drain and source.



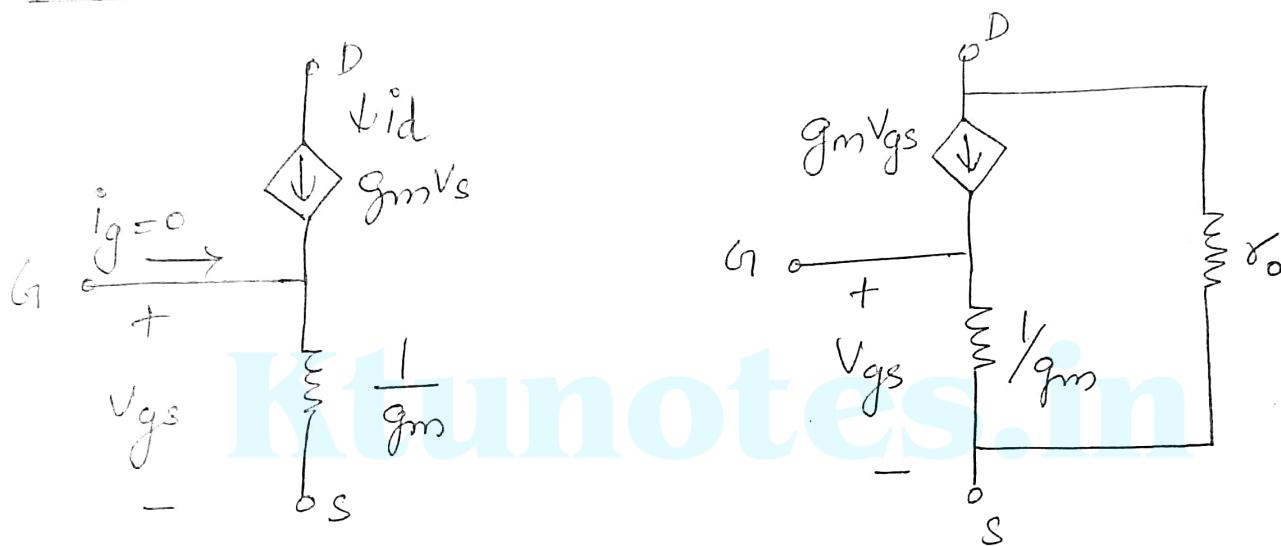
Small signal model including the effect of channel length modulation.

$r_0 = \frac{|V_A|}{I_D}$ , where  $V_A$  is a MOSFET parameter that is either specified or can be measured.

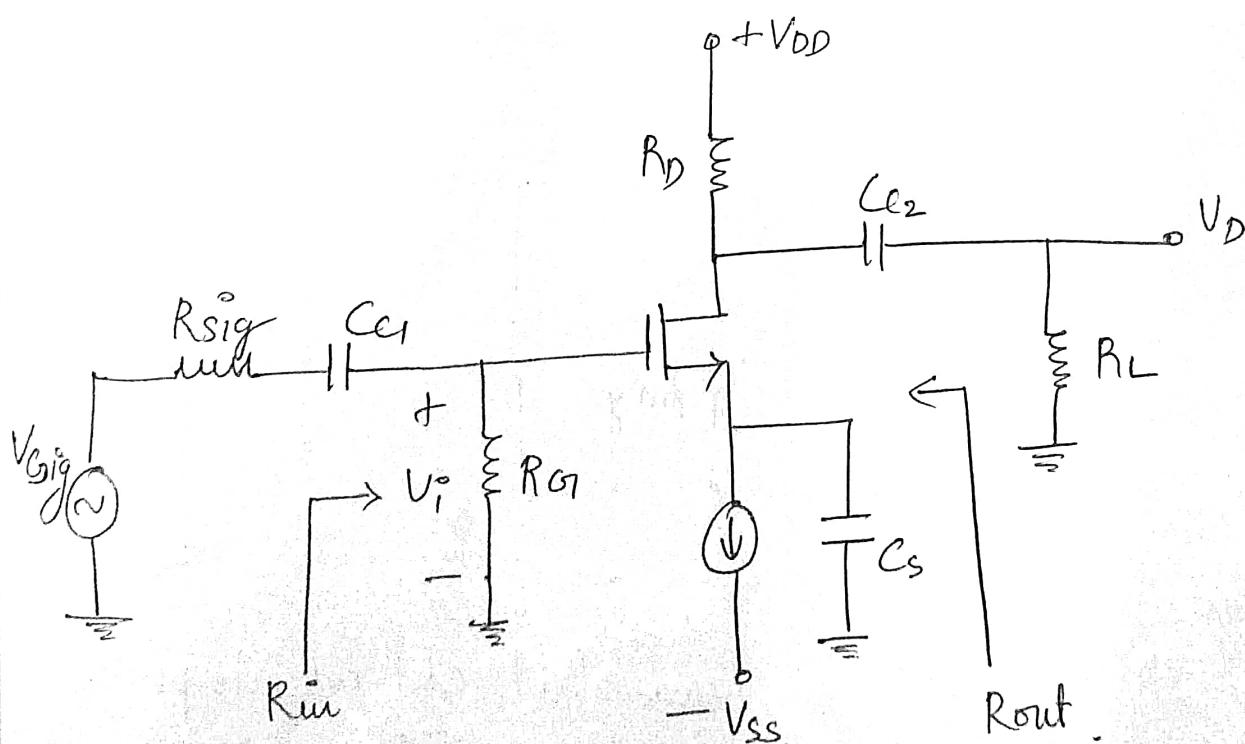


$i_D$  is typically in the range of  $10k\Omega$  to  $1M\Omega$ .  
Typical value of  $g_m = 1ms$ .

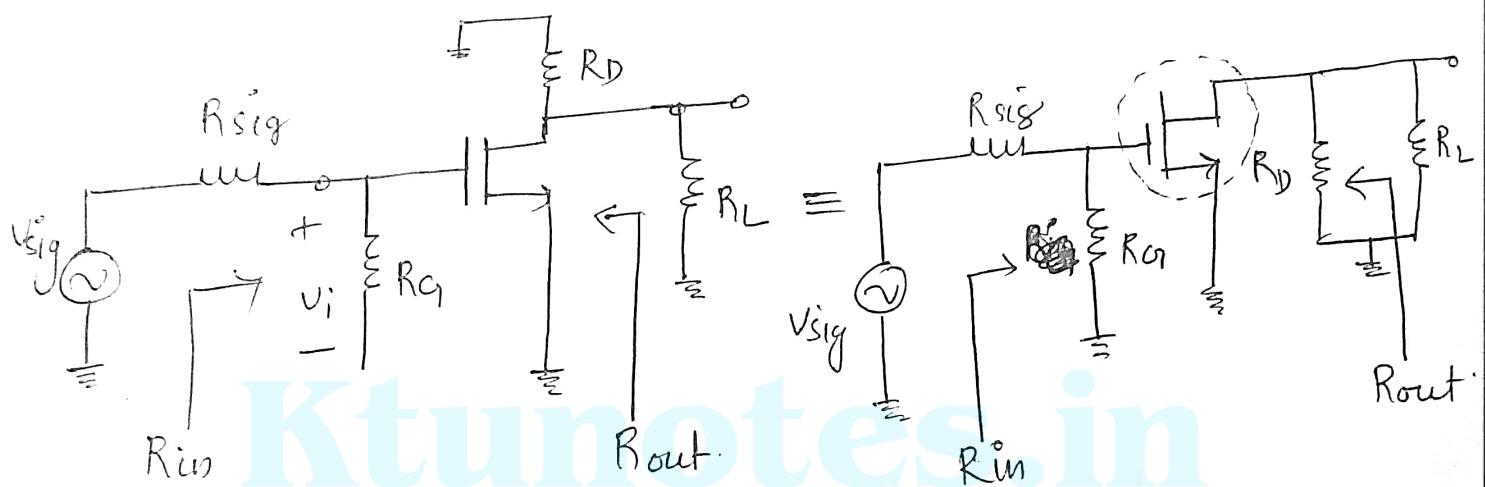
### The T-model of MOSFET



### Common Source Amplifier (CS ampl).

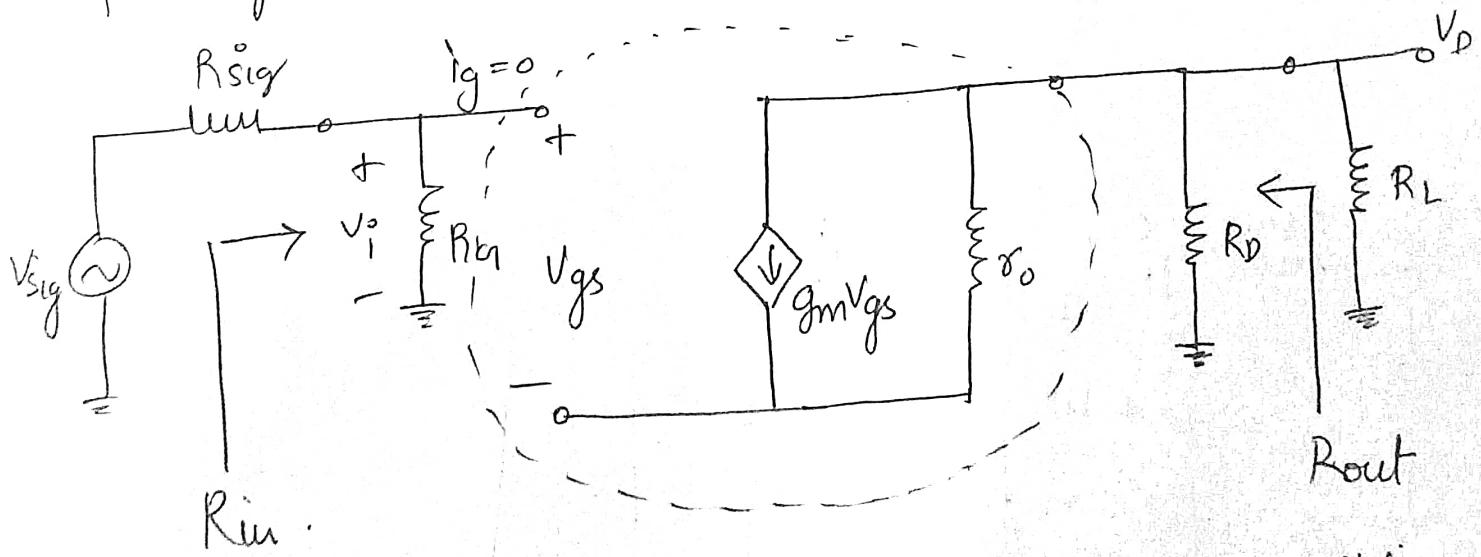


The common source (cs) or grounded source configuration is the most widely used of all MOSFET amplifier circuits. To establish an ac ground at the source, a bypass capacitor  $C_S$  is used.  $C_1$  and  $C_2$  are coupling capacitors. The drain voltage is coupled to the load resistance  $R_L$  via the coupling capacitor  $C_2$ .



Ac Equivalent

Replacing the MOSFET with the small signal equivalent.



$$i_g = 0$$

$$V_i = V_{gs}$$

Equivalent ckt at amplifier  
for small signal analysis.

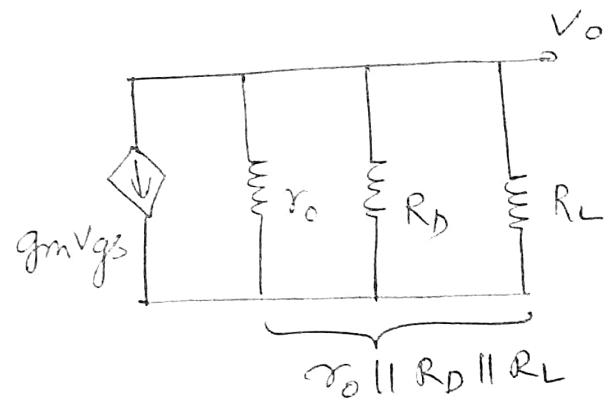
## Input Resistance ( $R_{in}$ )

$$R_{in} = R_{CA}$$

## Voltage Gain ( $A_v$ )

$$V_D = -g_m V_{GS} (\tau_0 \parallel R_D \parallel R_L)$$

$$A_v = \frac{V_o}{V_i} = \frac{V_o}{V_{GS}} \\ = -g_m (\tau_0 \parallel R_D \parallel R_L)$$



The open circuit voltage gain  $A_{v0}$  with  $R_L = \infty$

$$A_{v0} = \underline{-g_m (\tau_0 \parallel R_D)}$$

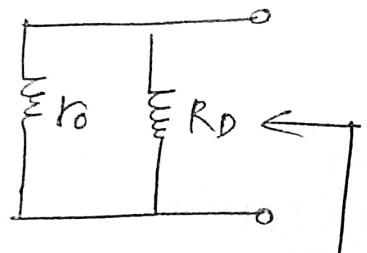
## O/P Resistance ( $R_{out}$ )

Set  $V_{sig}$  to zero, disconnect the load and look through the O/P terminals

$$R_{out} = \tau_0 \parallel R_D$$

$$\approx \underline{\underline{R_D}}$$

$$\because \tau_0 \gg R_D$$

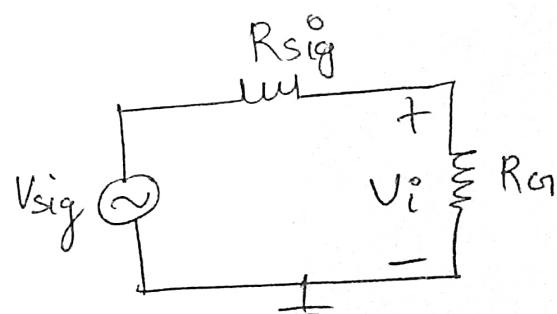


## Overall voltage gain ( $G_V$ ) [From source to load]

$$G_V = \frac{V_o}{V_{sig}} = \frac{V_o}{V_i} \times \frac{V_i}{V_{sig}}$$

$$= A_v \times \frac{R_{in}}{R_{sig} + R_{in}}$$

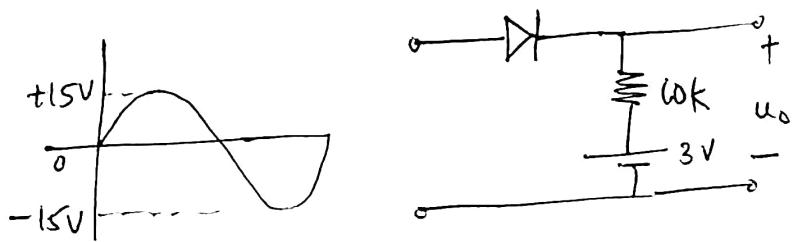
$$= -g_m (\tau_0 \parallel R_L \parallel R_D) \frac{R_{in}}{R_{sig} + R_{in}}$$



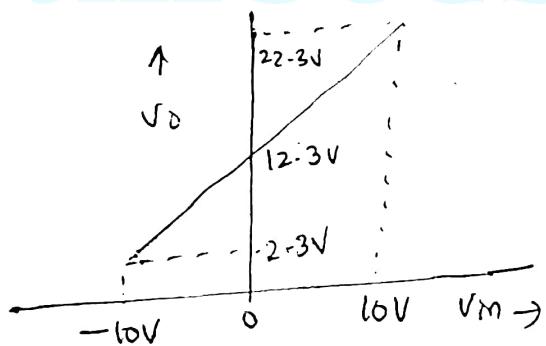
$$V_i = V_{sig} \times \frac{R_{in}}{R_{sig} + R_{in}}$$

## TUTORIAL - I

1. Draw the AC waveform and transfer characteristics of the following circuit. Cut off voltage of the diode is  $0.7V$ .

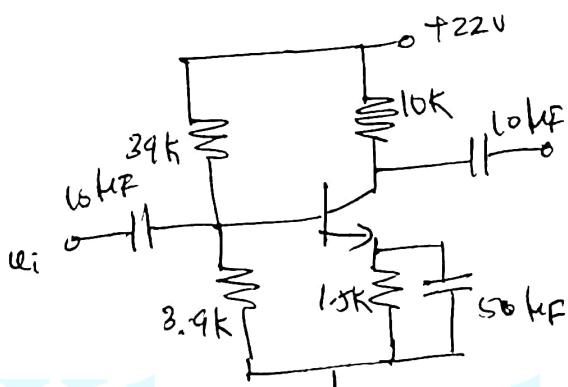


2. Design a clapper circuit to get the following transfer characteristics, assuming voltage drop across the diode  $0.7V$ .  
Also draw the input and output waveforms.

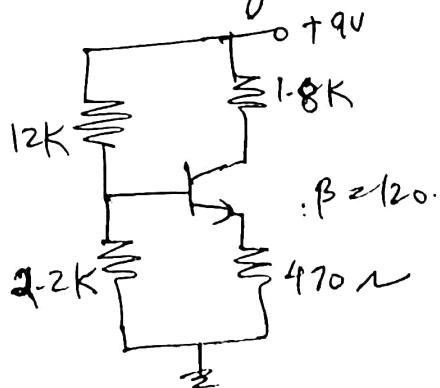


## TUTORIAL - 2

1. Draw the load line and mark the Q pt of the following circuit. A transistor with  $\beta = 100$  is used.

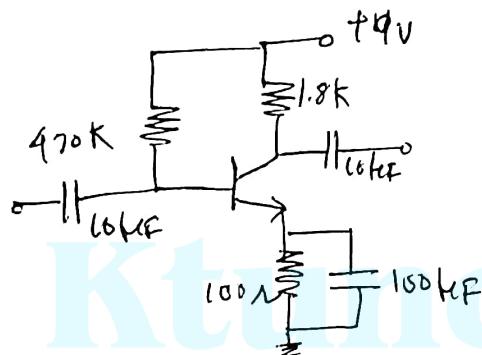


2. Find the stability factor of the following circuit.



### TUTORIAL - 3

1. Find  $R_{in}$ ,  $A_v$  and  $R_{out}$  of the following amplifier.

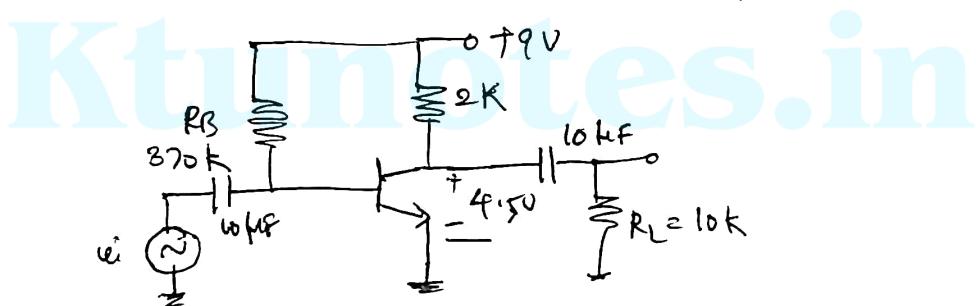


$\text{Si-TR} : \beta = 150, V_{BE} = 0.6\text{ V}$   
 $I_C = 2.4\text{ mA}, V_T = 25\text{ mV}$ .

2. From the above amplifier circuit, the bypass capacitor is removed. Find  $R_{in}$ ,  $A_v$  and  $R_{out}$ .

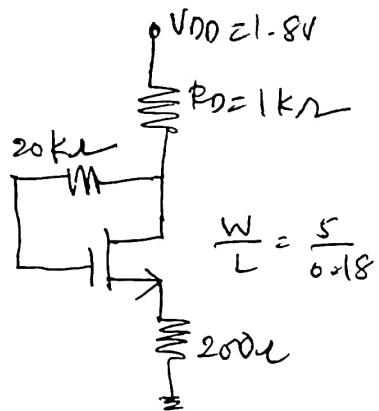
### TUTORIAL - 4

1. In a BJT amplifier  $I_c = 2 \text{ mA}$ ,  $\beta_0 = 125$ ,  $C_{\pi} = 8 \text{ pF}$ ,  $WV_B = 80 \text{ mV/rad/s}$ . calculate  $f_T$  and  $C_M$ .
2. Calculate the upper cut off frequency of the given amplifier. Given that  $\beta_2 100$ ,  $C_{\pi} 10 \text{ pF}$  and  $C_M = 0.2 \text{ pF}$ .



## TUTORIAL-5

- i. calculate H<sub>FE</sub> drain current  $I_D$ ,  $k_n C_{ox} = 100 \text{ MA/V}^2$ ,  $V_{TH} = 0.5 \text{ V}$ , and  $\lambda = 0.1$ .



2. In the following circuit MOSFET operates in saturation.  $V_T = 1 \text{ V}$ ,  $k = 0.1 \text{ MA/V}^2$ . Calculate  $I_D$ ,  $V_{DS}$  and verify the region of operation.

