Ext. No. 6

Date: 18/07/22

FEEDBACK AMPLIFIERS

AIM:

To design, set up and study feedback amplifiers

COMPONENTS REQUIRED:

Transistors, resistors, capacitors, signal generator, breadboard, dc power source and CRO

THEORY:

Many desirable characteristics can be obtained by employing the negative feedback in the amplifiers at the cost of reduction in gain. An open loop amplifier suffers from many limitations such as frequency and phase distortions, non-linear distortion and noise. These limitations can be considerably rectified in the feedback amplifiers. Though the gain is reduced in the negative feedback amplifiers, bandwidth of operation is greater than that of an amplifier without feedback.

The output voltage or current is sampled and fed back to the input of the amplifier in series or in shunt to the input signal source. There are four important topologies of negative feedback, namely voltage series, voltage shunt, current series and current shunt. First term in the nomenclature indicates the way in which the parameter sampled and the second term indicates the way in which the sampled signal is fed back to the input.

Current series feedback amplifier:

A common emitter RC coupled amplifier without emitter bypass capacitor C_E is an example of current series amplifier. Here the sampled signal is current and the feedback signal is voltage. Emitter resistance R_E samples the output current and feeds a voltage back to the input side as a voltage. Its feedback factor $\beta = -R_E$.

Voltage series feedback amplifier:

Emitter follower is a good example of voltage series feedback. Here sampled signal is voltage and feedback signal is current. Its feedback factor $\beta = 1$

DESIGN:

DC biasing conditions:

In order to keep the operating point at the centre of load line, take

$V_{CC} = 12V \quad I_C = 2mA$

$V_{RC} = 40\%$ of $V_{CC} = 4.8$

$V_{RE} = 10\%$ of $V_{CC} = 1.2V$

$V_{CE} = 50\%$ of $V_{CC} = 6V$

Design of RC:

$V_{RC} = I_C \times R_C = 4.8V$

$R_C = 2.4K$

Use 2.2k (std)

Design of R_E:

$V_{RE} = I_E \times R_E = 1.2V$

$I_E \simeq I_C$

$R_E = 600\Omega \approx 680\Omega$ (std)

Design of voltage divider R_1 and R_2:

Assume the current through $R1 = 10I_B$ and that through $R_2 = 9I_B$ to avoid loading of potential divider network R_1 and R_2 by the base current

V_{R2} = Voltage across $R_2 = V_{BE} + V_{RE}$

$V_{R2} = V_{BE} + V_{RE} = 0.7 + 1.2$

$= 1.9V$

$V_{R2} = 9I_B R_2$

$= 1.9V$

$I_B = I_C/h_{FE} = \frac{2mA}{100}$

$= 20\mu A$

Then $R2 = \frac{1.9}{9 \times 20 \times 10^{-6}}$

$= 10.6k$ Use 10k (std)

$V_{R1} = V_{CC} - V_{R2} = 12 - 1.9$

$= 10.1V$

$V_{R_1} = 10I_B R_1 = 10.1$

$R_1 = \frac{10.1}{10 \times 20 \times 10^{-6}} = 50k$. Select 47k std

Design of coupling capacitors cc_1 and cc_2

Xc_1 should be less than the input impedance of the transistor. Here R_{in} is the series impedance

Then $X_{C1} \leq R_{in}/10$

Here $R_{in} = R_1 // R_2 // R_{PE}$

We get $R_{in} = 1.1k$

$X_{C1} \leq 110\Omega$

So, $C_{C1} \geq \frac{1}{2\pi f_L \times 110} = 14\mu F$ Use $10\mu F$ (Std)

Similarly,

$X_{C2} \leq R_{out}/10$

$R_{out} = R_C$

$X_{CE} \leq 240\Omega$

So, $C_{C2} \geq \frac{1}{2\pi \times 240} = 6.6\mu F$ Use $10\mu F$ (Std)

PROCEDURE:

1. Set up the current series amplifier circuit after testing the components
2. Feed the input signal and note down the output amplitude by varying the input frequency. Draw the frequency response characteristics
3. Repeat the above step without feedback by connecting an emitter bypass capacitor of $10\mu F$.
4. Repeat the experiment for other feedback amplifiers with feedback and without feedback.

RESULT:

Designed and setup feedback amplifier.

Current series feedback amplifier:

Lower cut off frequency f_L = 78 Hz

Higher cut-off frequency $f_H = 720\,kHz$

Bandwidth $= f_H - f_L$

$= 720 \times 10^3 - 78$

$= 719.922\,kHz$

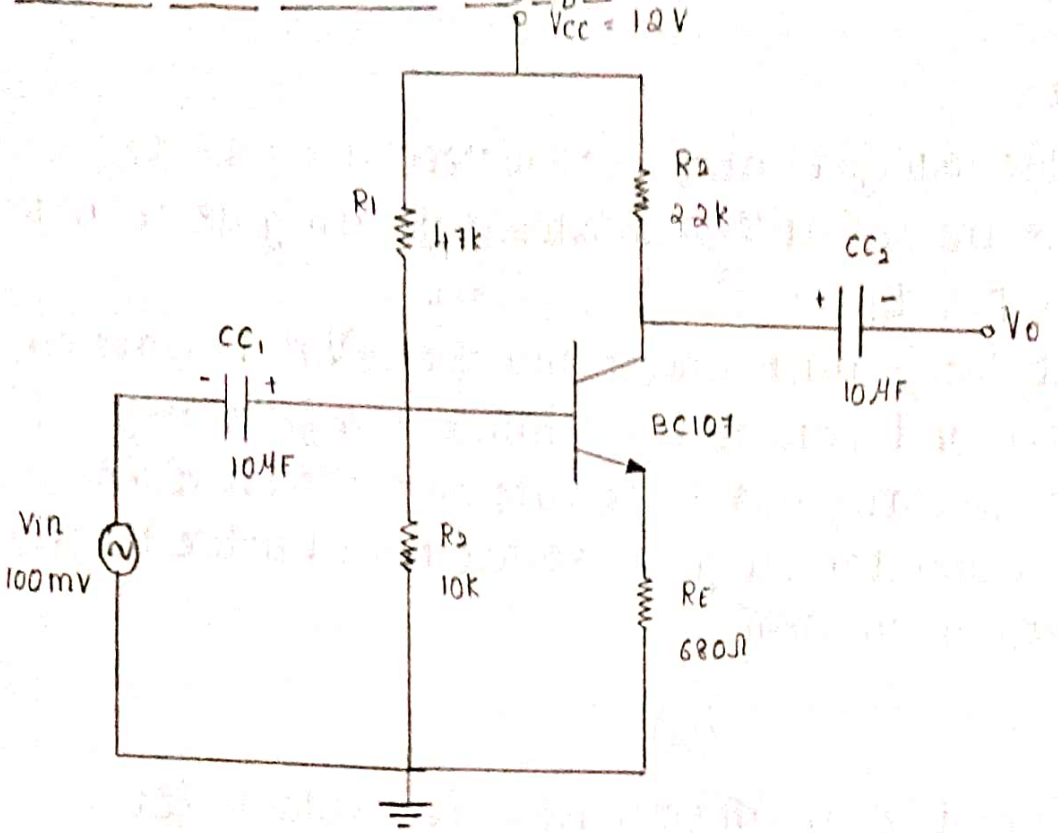
Voltage series feedback amplifier :

Sine wave with peak to peak value 102 mV.

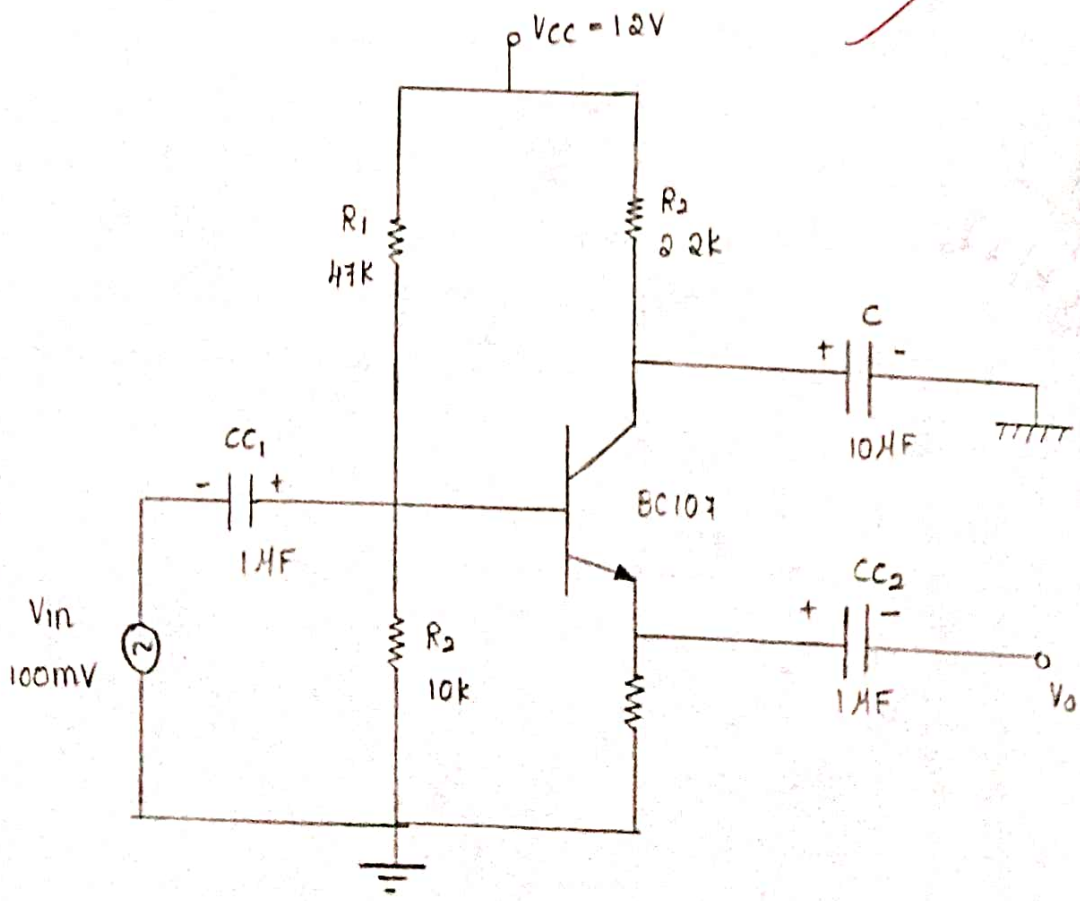
21/03/22

CIRCUIT DIAGRAM

Current Series feedback amplifier



Voltage Series feedback Amplifier



OBSERVATION :

V_i = 500 mV pp

freq (Hz)	V_o	V_o/V_i	$20\log(V_o/V_i)$
10	0.400	0.8	-1.94
20	0.600	1.2	1.584
50	0.800	1.6	4.082
80	1.20	2.4	7.604
90	1.40	2.8	8.943
100	1.60	3.2	10.103
200	1.60	3.2	10.103
300	1.60	3.2	10.103
500	1.60	3.2	10.103
600	1.60	3.2	10.103
700	1.60	3.2	10.103
800	1.60	3.2	10.103
1k	1.60	3.2	10.103
2k	1.60	3.2	10.103
5k	1.60	3.2	10.103
8k	1.60	3.2	10.103

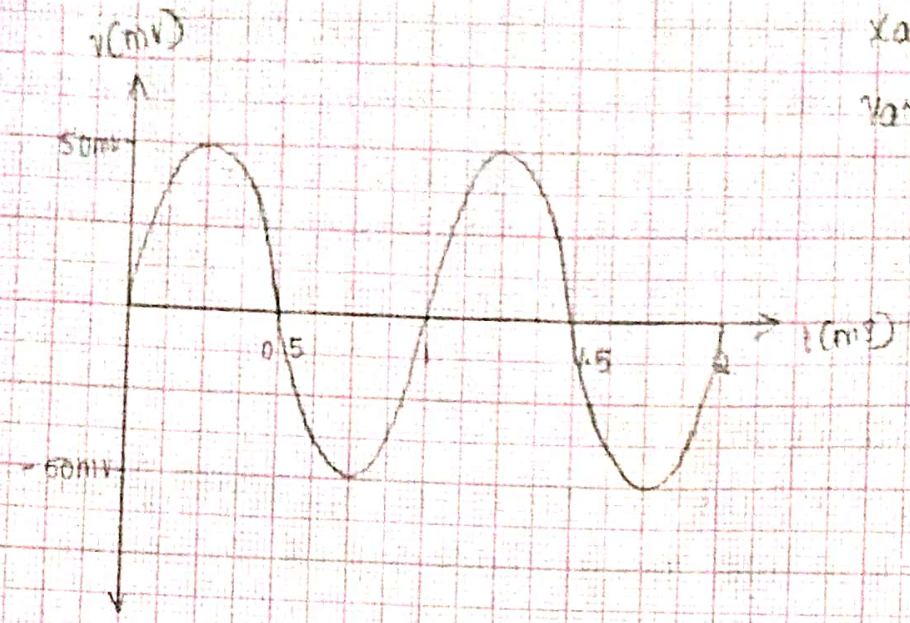
freq (Hz)	V_o	V_o/V_i	$20\log(V_o/V_i)$
10k	1.60	3.2	10.103
20k	1.60	3.2	10.103
50k	1.60	3.2	10.103
100k	1.60	3.2	10.103
200k	1.60	3.2	10.103
300k	1.40	2.8	8.943
400k	1.40	2.8	8.943
500k	1.20	2.4	7.604
600k	1.20	2.4	7.604
700k	1.18	2.36	7.46
800k	1	2	6.021
900k	1	2	6.021
1M	1	2	6.021

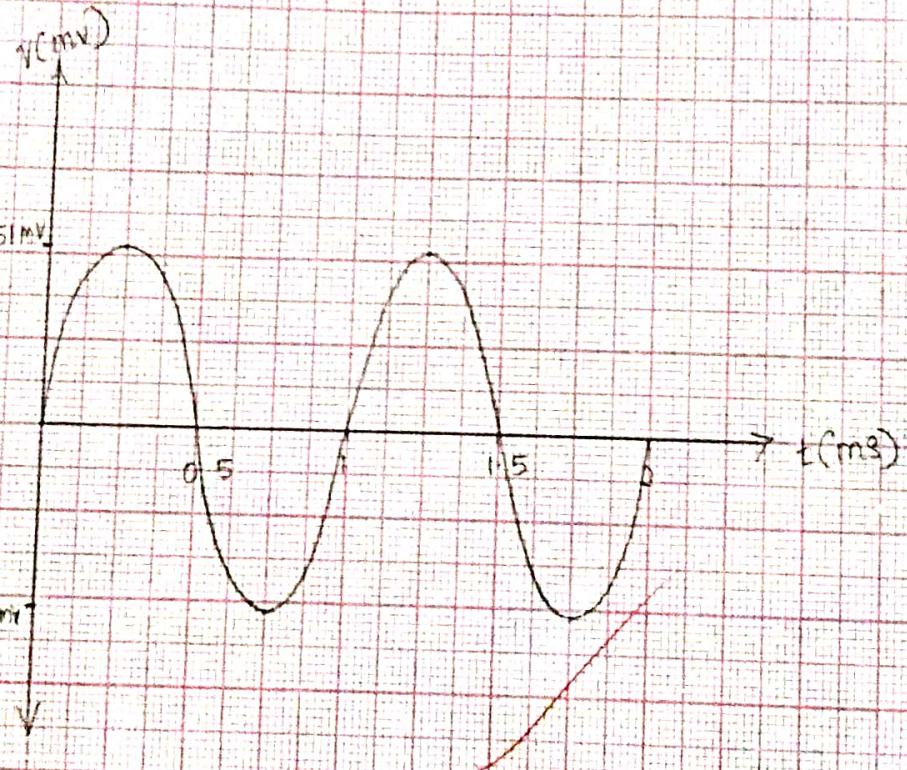
VOLTAGE SHUNT FEEDBACK AMPLIFIER

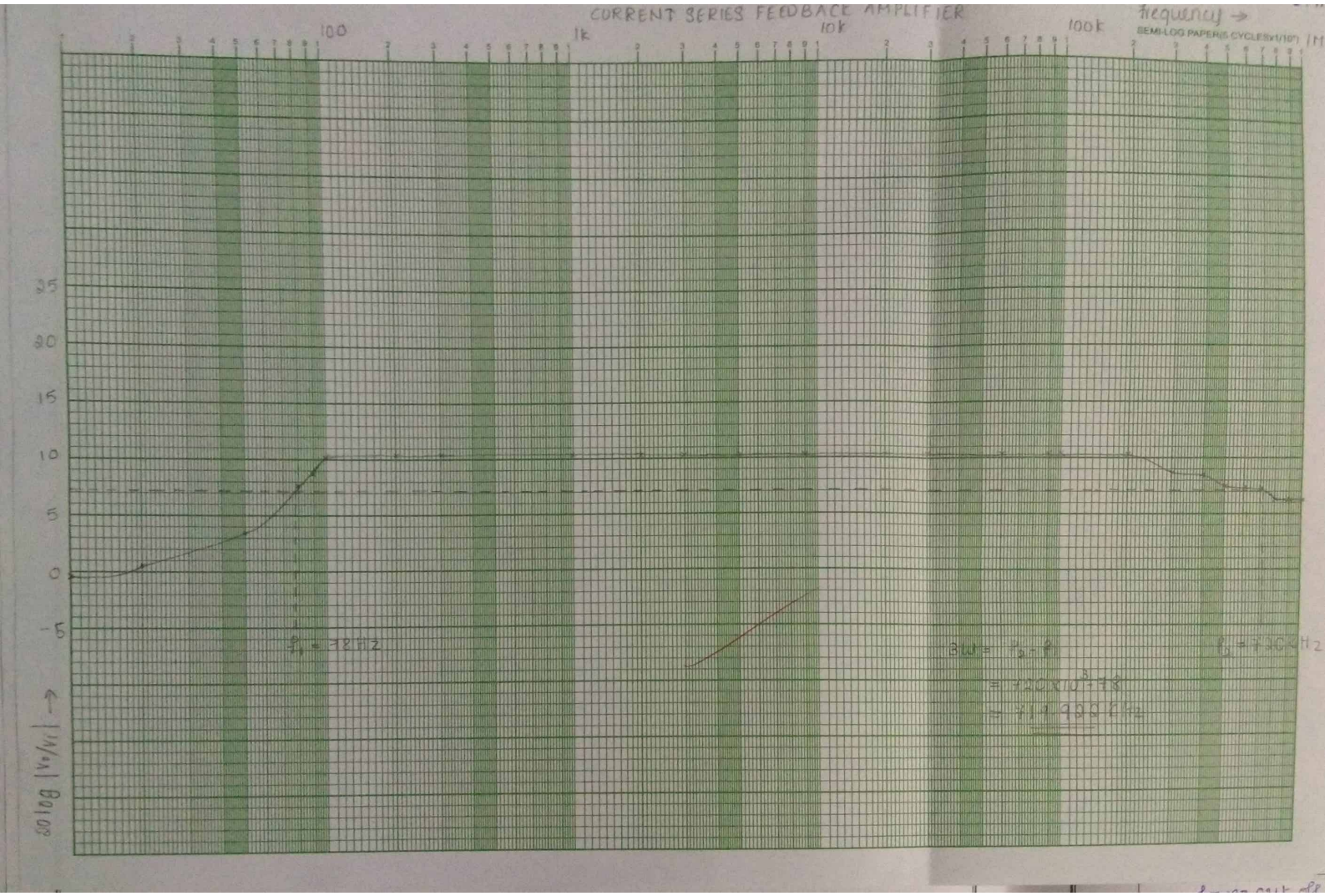
Echelle

Xaxis - 20 div - 0.5 ms

Yaxis - 20 div - 50 mV






CURRENT SERIES FEEDBACK AMPLIFIER
frequency →
SEMI-LOG PAPER(5 CYCLES x1/10/1)
100
1k
10k
100k
1M
25
20
15
10
5
0
-5
20log|Vo/Vi| →
fL = 32 Hz
BW = fH - fL
fH = 730 kHz
= 730 x 10^3 - 32
= 729.968 kHz