MODULE-2

1. Static CMOS logic realization

2. Pass Transistor logic

3. Transmission gates

ECT304

VLSI CIRCUIT DESIGN

STATIC LOGIC REALIZATION

- Static logic realization can be done using NMOS and CMOS
  - ***Static NMOS logic***
  - ***Static CMOS logic***
- Static CMOS logic gates are relatively easy to design and use.

STATIC NMOS LOGIC REALIZATION

- Consist of a **pull up load (Resistive)** and a **pull down NMOS** network.

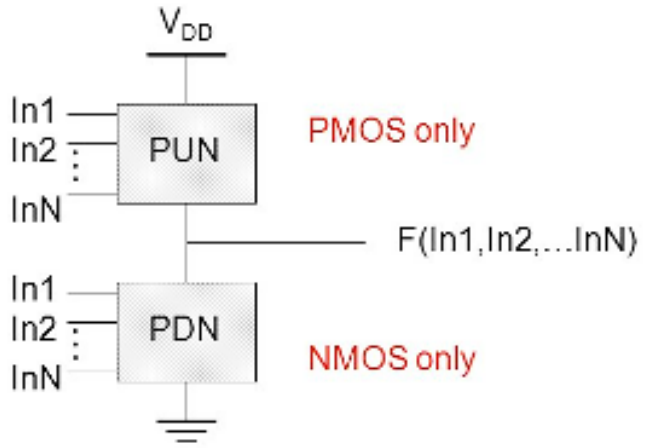
NMOS in series indicates AND operation

NMOS in parallel indicates OR operation.

- **Output will be complement of resultant logic.**

STATIC CMOS

- The static CMOS style is really an extension of static CMOS inverter to multiple inputs.
- The advantage of the CMOS structure is **robustness, good performance and low power consumption with no static power dissipation.**
- The complementary CMOS circuit falls under a class of logic circuits called static circuits, in which at every point in time, each Gate output is connected to either V_{DD} or V_{SS} via a low resistance path.
- A static CMOS is a combination of 2 networks – the **Pull up network (PUN)** and the **Pull down network (PDN)**



PUN and PDN are logically dual logic networks

STATIC CMOS

- The function of the PUN is to provide a connection between the **output and V_{DD}**, anytime when the output of logic gate is 1.
- The function of PDN is to connect the **output (F) to V_{SS}** when the output of the logic gate is O.
- The PUN and PDN are constructed in a **mutually exclusive fashion** such that **one and only one of the network is Conducting in steady state.**
- An NMOS switch is ON, when the controlling high and is OFF when the controlling signal is low.
- A PMOS transistor switch act as an inverse switch, that is ON when the controlling signal is low and OFF when the controlling signal is high.
- **A PDN is constructed using NMOS devices and PMOS are used in PUN.**
- The reason for this choice is that **NMOS produce "Strong Zeros" and PMOS generate "Strong Ones".**
- When PMOS is ON, the capacitor will charge. ie, why it is used in PUN
- When NMOS is ON, capacitor will discharge, ie why it is used PDN.

STATIC CMOS LOGIC REALIZATION

- Consist of a pull up PMOS and a pull down NMOS network.

NMOS in series indicates AND operation

NMOS in parallel indicates OR operation

PMOS in series indicates OR operation

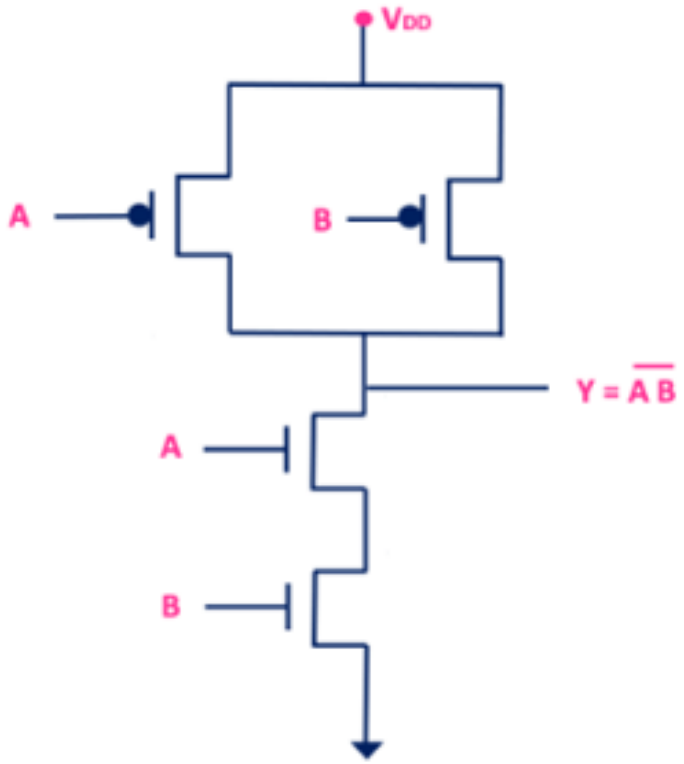
PMOS in parallel indicates AND operation.

- **Output will be complement of resultant logic.**

STATIC CMOS LOGIC REALIZATION

- Consist If a logic function is given
  - *Take the complement of logic function.*
  - *Draw the pull down NMOS network*
  - *Take the dual of NMOS expression and draw the pull up PMOS network*

STATIC CMOS LOGIC –NAND GATE



$$Y = \overline{A.B}$$

- *Take the complement of logic function.*

$$Y = A.B$$

- *Draw the pull down NMOS network*

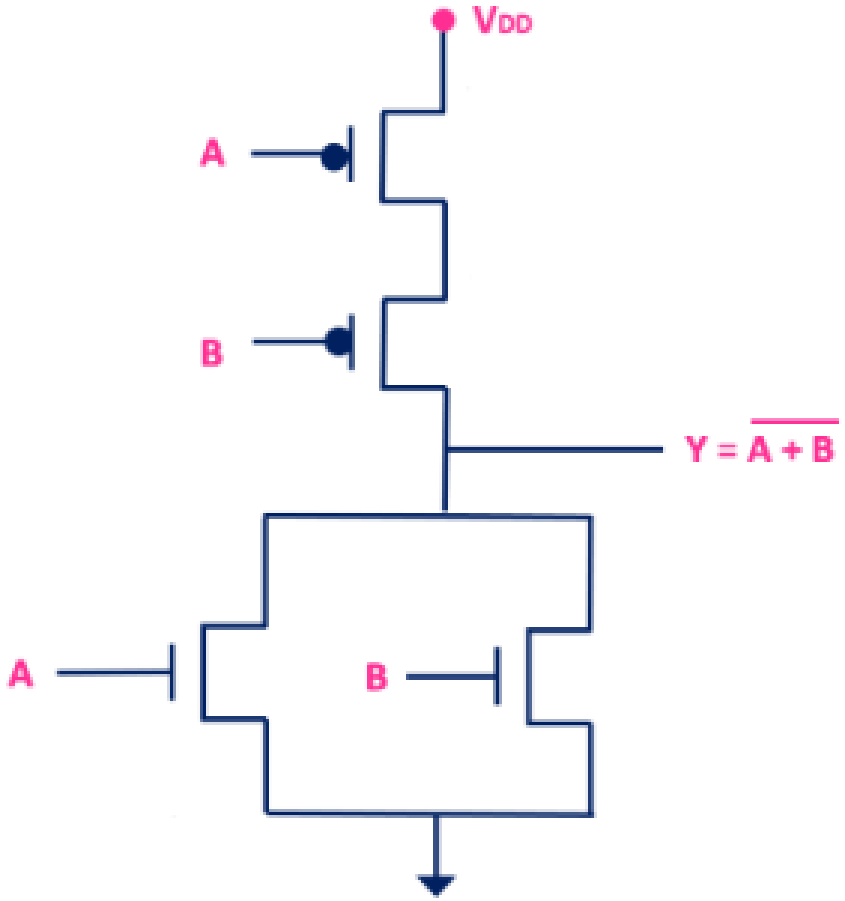
NMOS in series indicates AND operation

NMOS in parallel indicates OR operation

- *Take the dual of NMOS expression and draw the pull up PMOS network*

$$Dual \rightarrow Y = A + B$$

STATIC CMOS LOGIC –NOR GATE

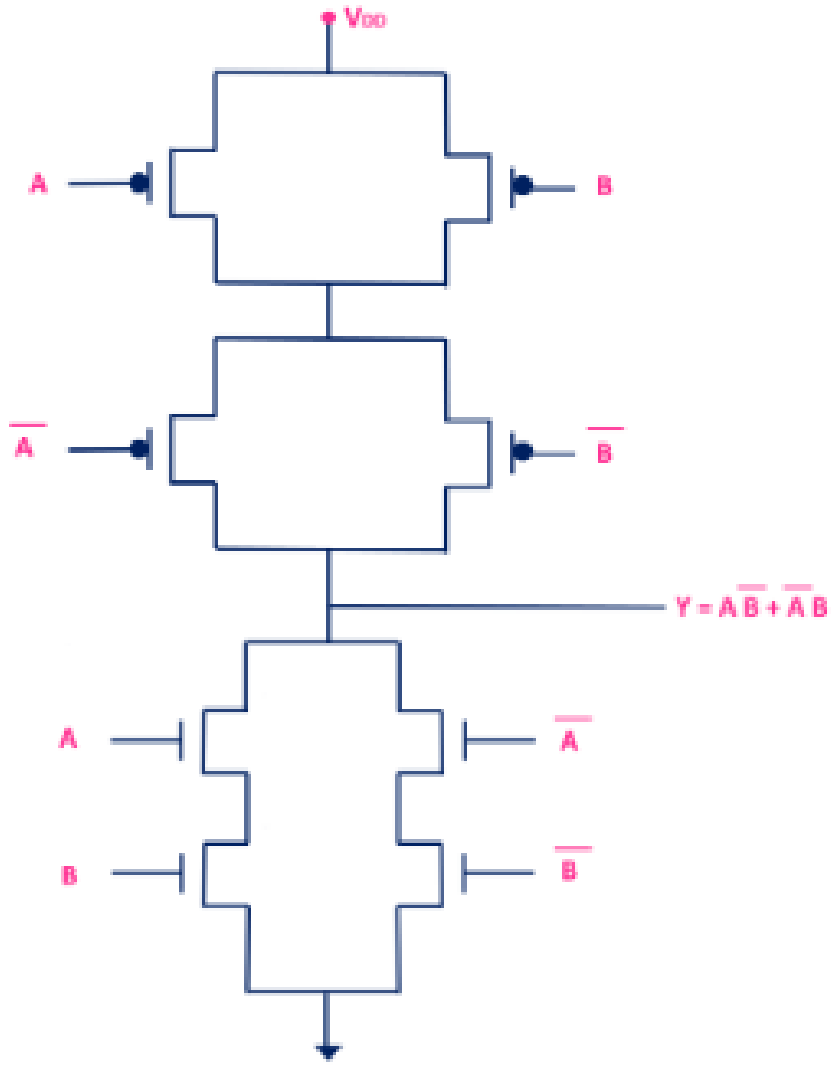


$$Y = \overline{A + B}$$

$Y = A + B$ ➔ Complement

$Y = A.B$ ➔ Dual

STATIC CMOS LOGIC –XOR GATE

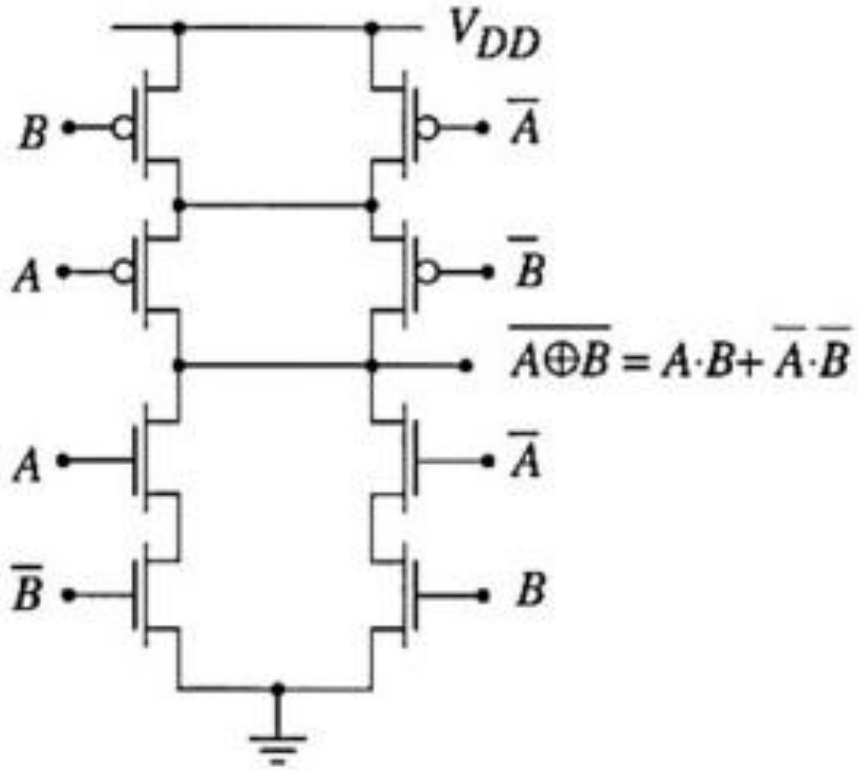


$$Y = \bar{A}B + A\bar{B}$$

$$Y = AB + \bar{A}\bar{B}$$ ➔ Complement

$$Y = (A + B).(\bar{A} + \bar{B})$$ ➔ Dual

STATIC CMOS LOGIC –XNOR GATE

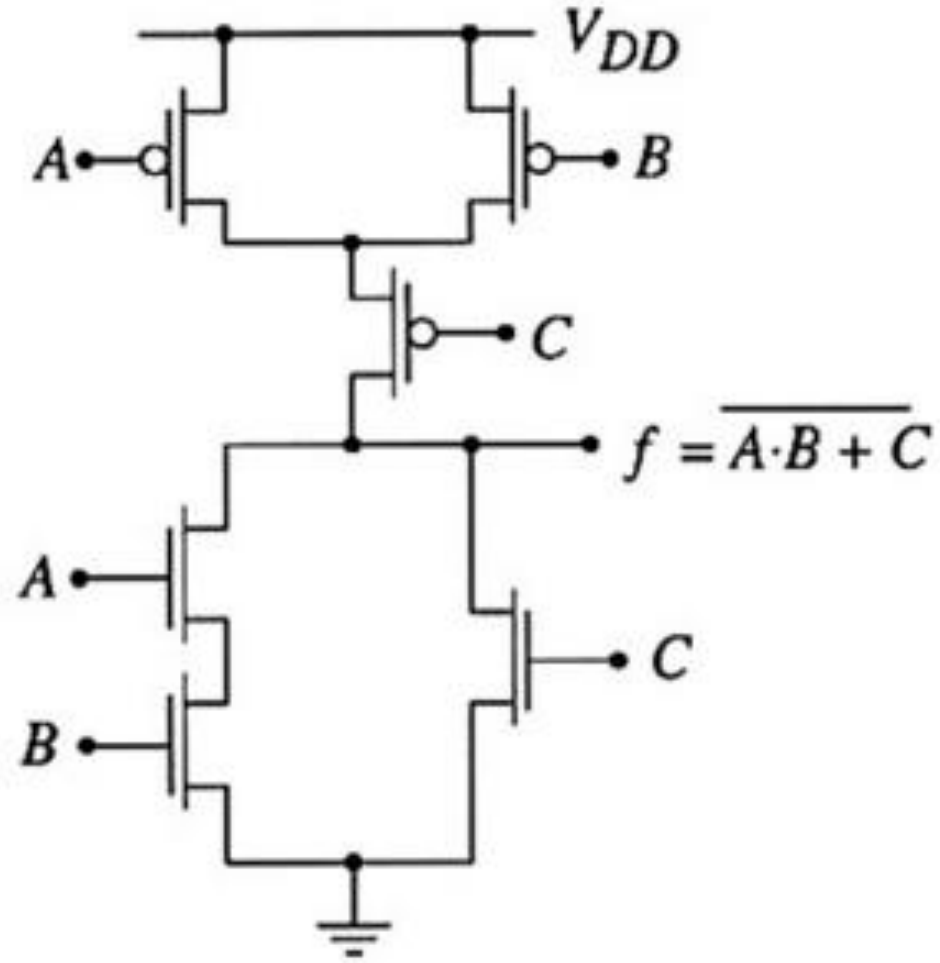


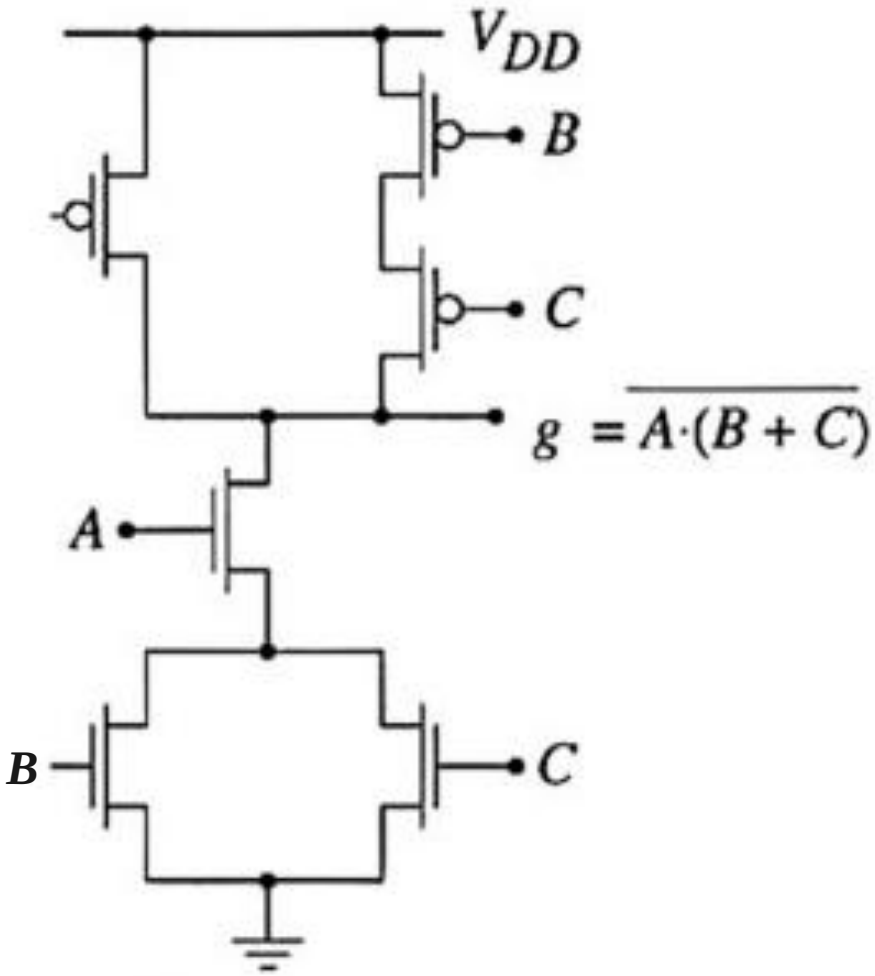
$$Y = AB + \bar{A}\bar{B}$$

$$Y = \bar{A}B + A\bar{B}$$ ➔ Complement

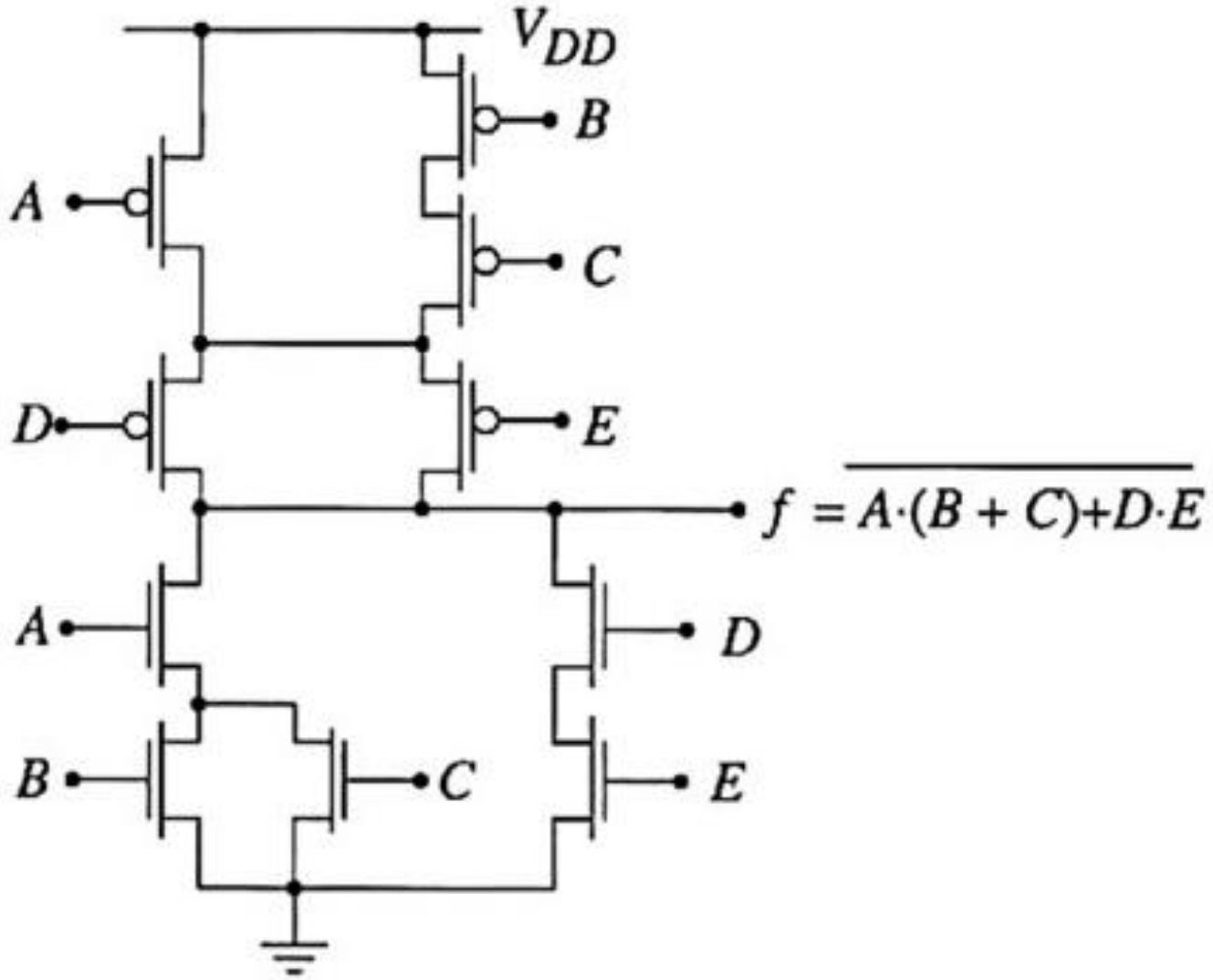
$$Y = (\bar{A} + B).(A + \bar{B})$$ ➔ Dual

STATIC CMOS LOGIC

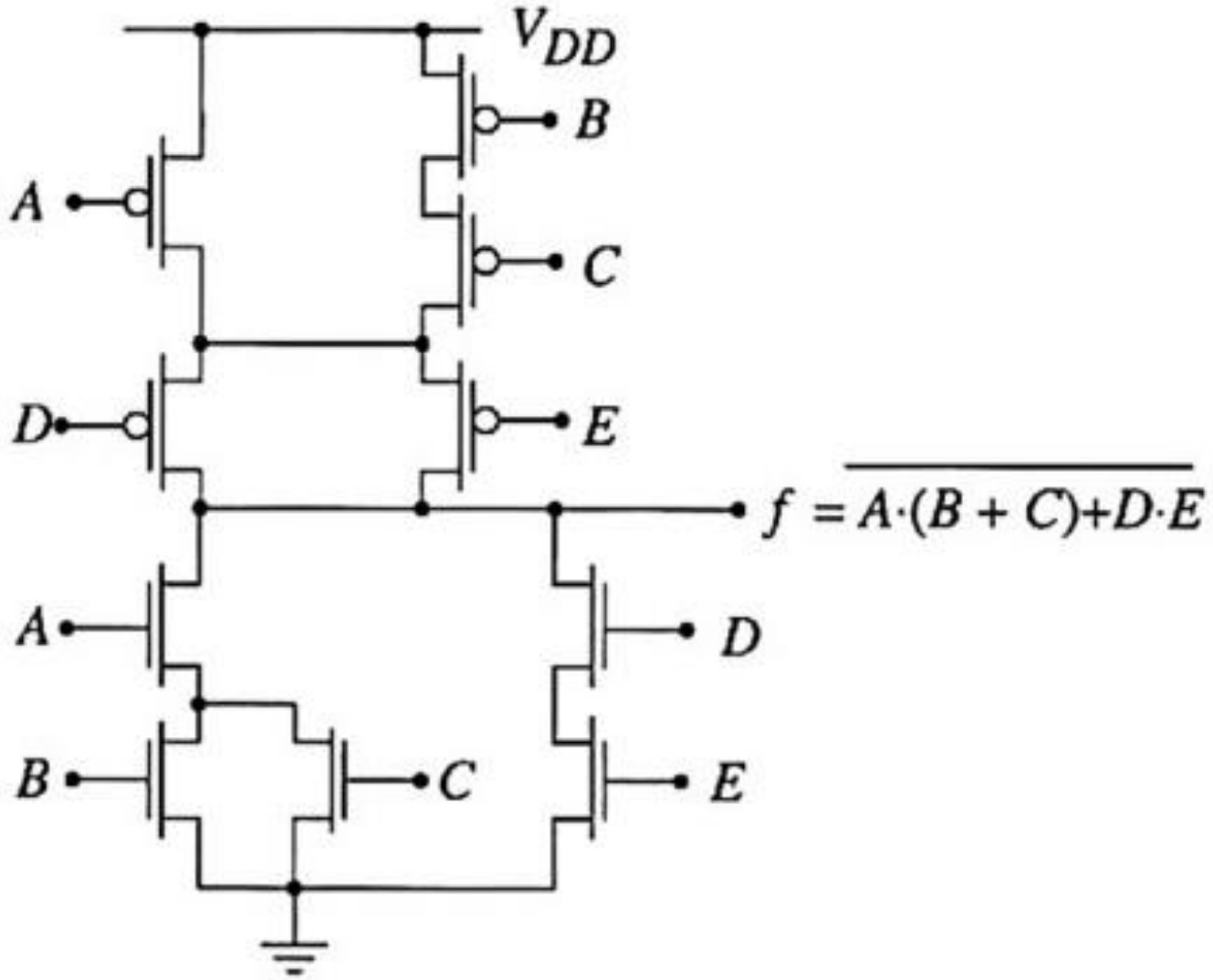




STATIC CMOS LOGIC



STATIC CMOS LOGIC



PROPERTIES OF COMPLEMENTARY CMOS GATES

1) High noise margins

- VOH and VOL are at VDD and GND , respectively.

2) No static power consumption

- There never exists a direct path between VDD and VSS (GND) in steady-state mode.

3) Comparable rise and fall times:

- (under the appropriate scaling conditions)

COMPLEMENTARY CMOS GATES

Advantages over other inverters

- steady state power dissipation of CMOS inverter circuit is negligible small
- VTC exhibits a full output voltage swing between 0V and VDD

Limitations

- CMOS process is more complex than standard NMOS only process
- Due to parasitic effect chance of occurring latch up condition

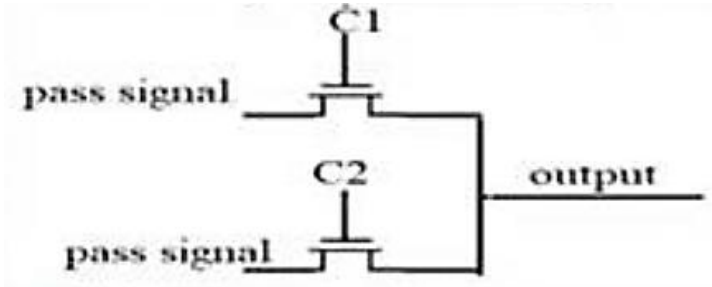
The static and transient performance strongly depend upon the availability of an high quality switch with low parasitic resistance and capacitance

PASS TRANSISTOR LOGIC (PTL)

- A popular and widely used alternative to complementary CMOS is **Pass Transistor logic**

- **Advantages**

  - Here the number of transistors required to implement logic is reduced by allowing **the primary inputs to drive gate terminals as well as source/drain terminals.**
  - While CMOS allow primary inputs to drive the gate terminals of MOSFETS.
  - Pass transistor logic often **uses fewer transistors**, **runs faster**, and **requires less power** than the same function implemented with the same transistors in fully complementary CMOS logic.

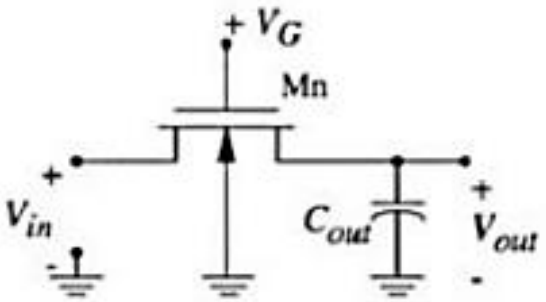


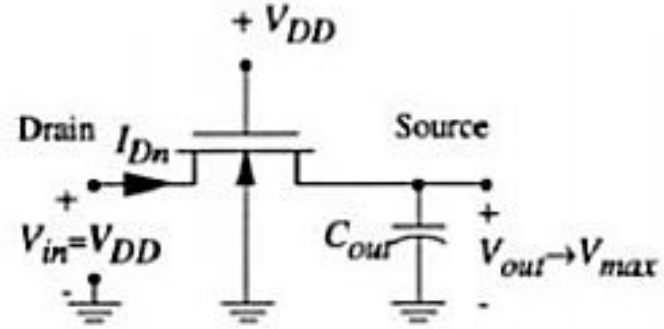
PASS TRANSISTOR LOGIC (PTL)

- The pass transistor is an NMOS used as a switch-like element to connect logic and storage.

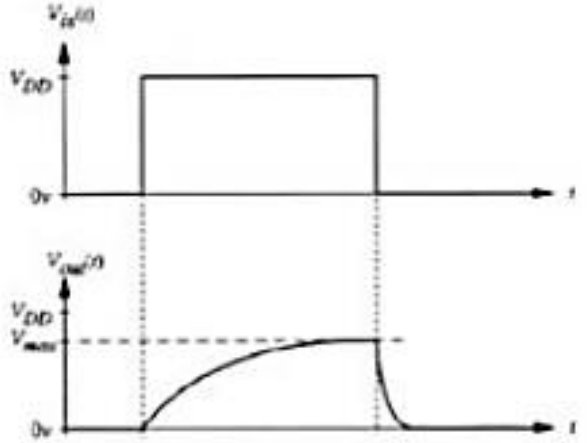
- Used in NMOS; sometimes used in CMOS to reduce cost.
- The voltage on the gate, V_C, determines whether the pass transistor is "**open**" or "**closed**" as a switch.
  - If V_C = H, it is "closed" and connects Vout to Vin.
  - If V_C = L, it is "open" and Vout is not connected to Vin.
- Consider V_{in} = L and V_{in} = H with V_C = H. With V_{in} = L, the Vout, becomes L.
- But, for V_{in} = H, the output becomes the effective source of the FET.
- When $V_{GS} = V_{DD}-V_{OUT} = V_{Tn}$, the NMOS in cuts off. The High level of $V_{OUT} = V_{DD}-V_{Tn}$.

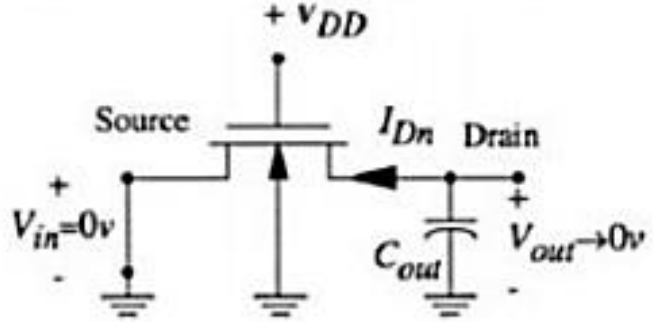
NMOS PASS TRANSISTOR





(a) Logic 1 input



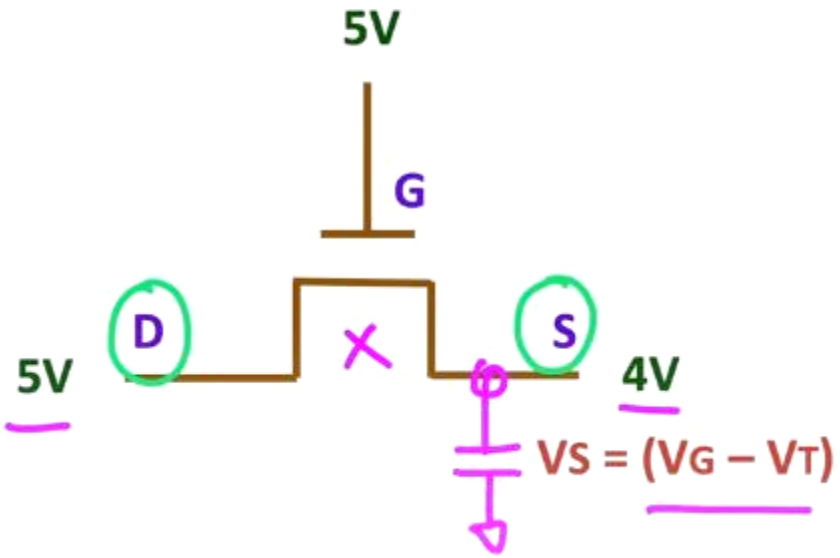


(b) Logic 0 input

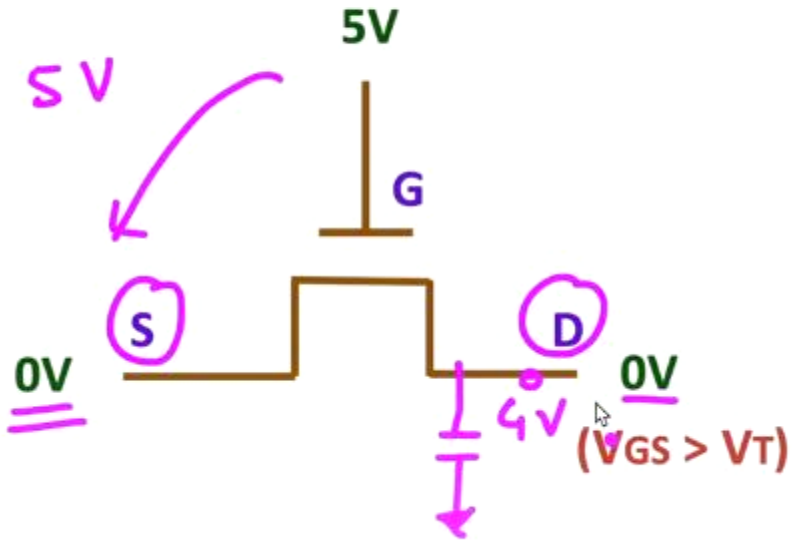
$$V_{max} = V_{DD} - V_{Tn}$$

NMOS PASS TRANSISTOR

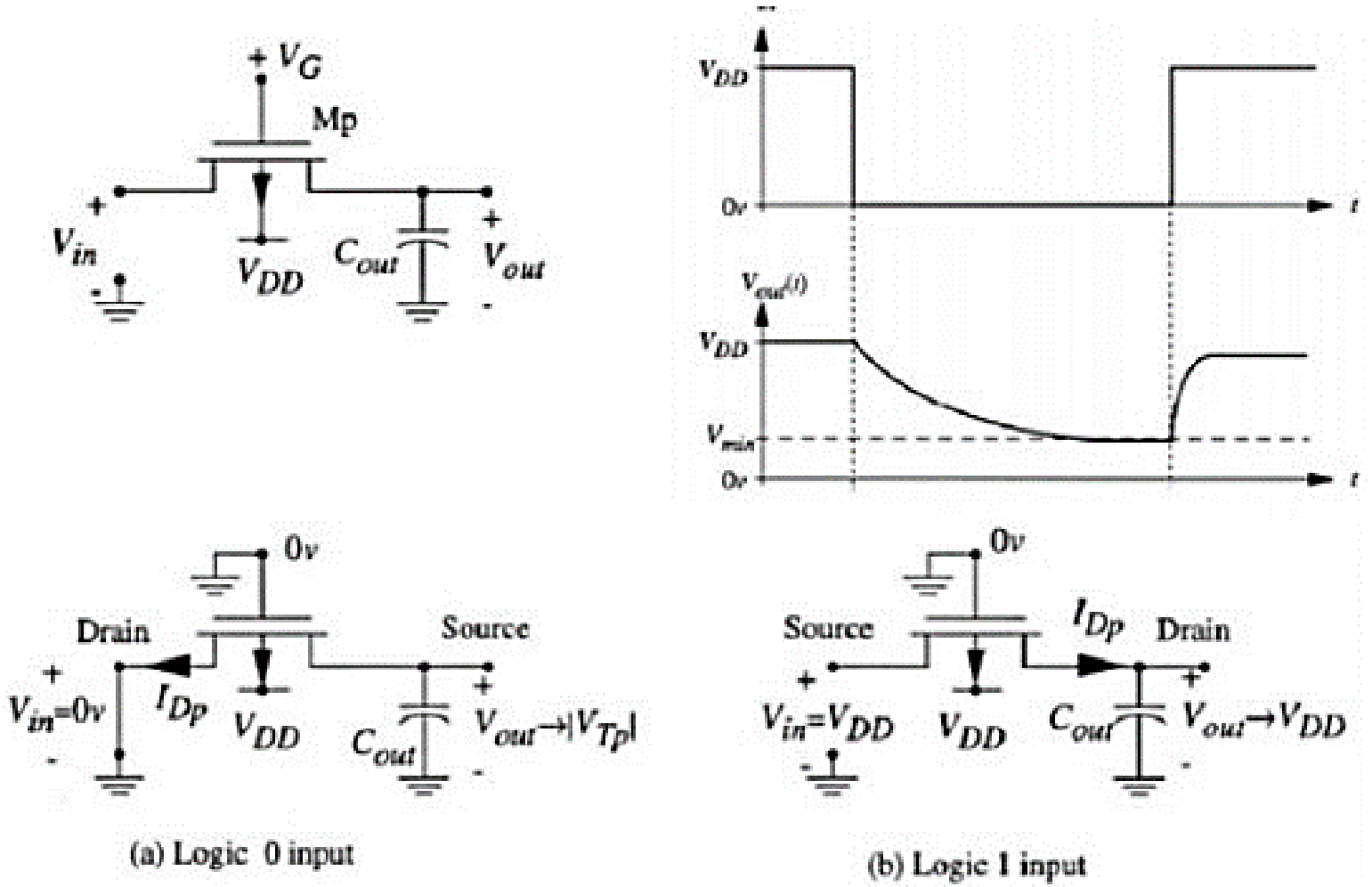
NMOS passes weak logic '1'



NMOS passes strong logic '0'



PMOS PASS TRANSISTOR

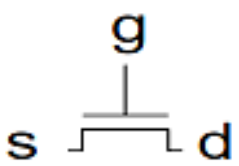


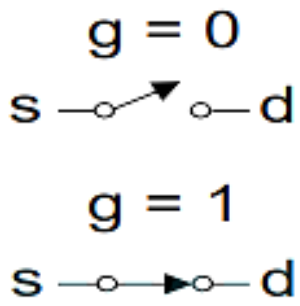
(a) Logic 0 input

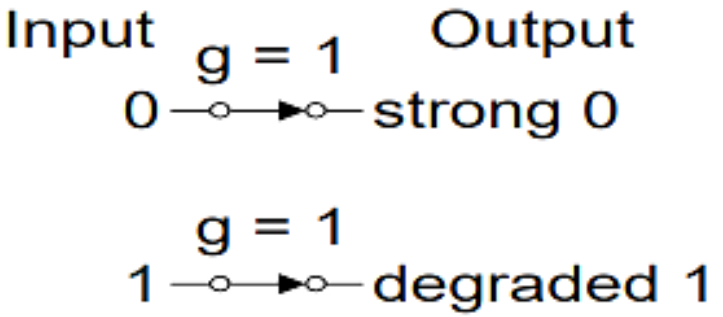
(b) Logic 1 input

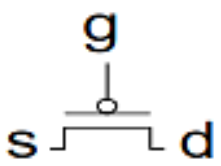
PASS TRANSISTORS

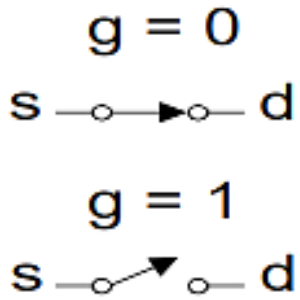
- Transistors can be used as switches

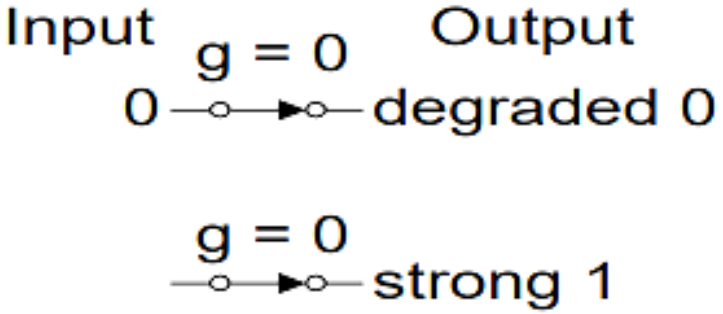






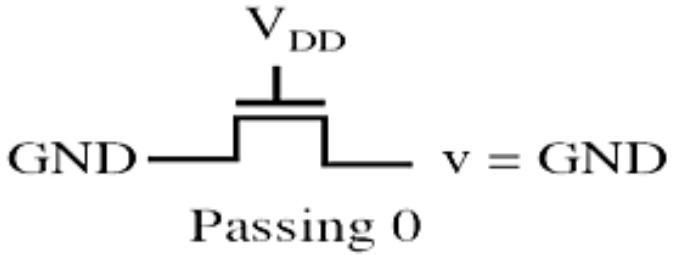




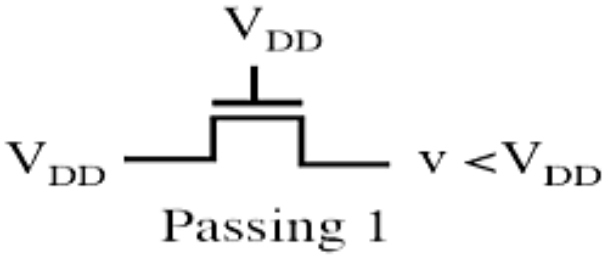


PASS TRANSISTORS

- N-Channel MOS Transistors pass a 0 better than a 1

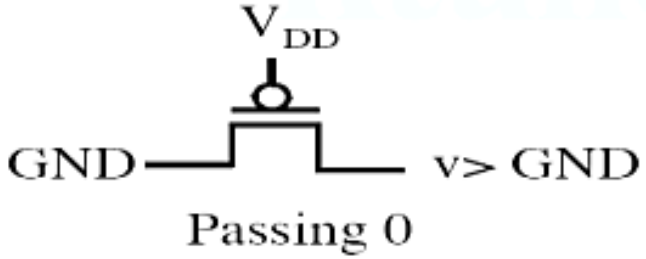


Passing 0

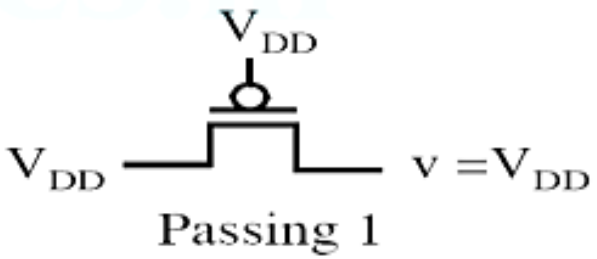


Passing 1

- P-Channel MOS Transistors pass a 1 better than a 0



Passing 0

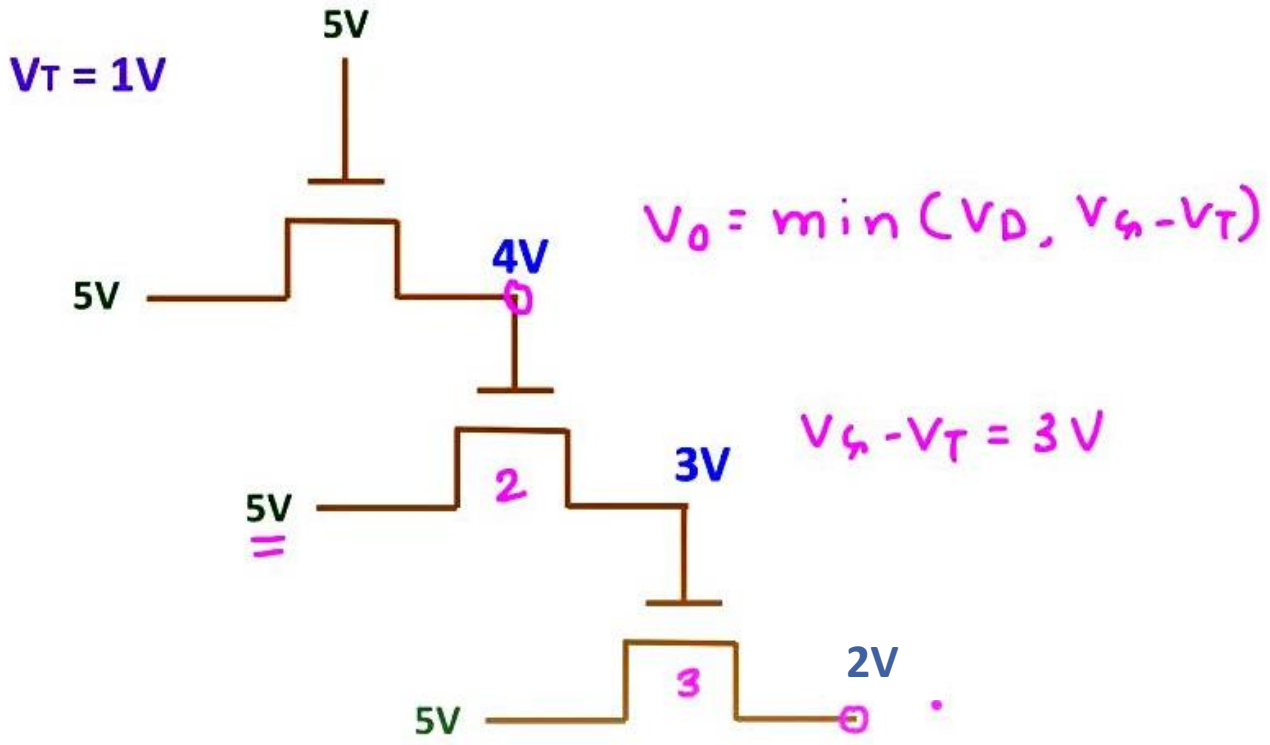


Passing 1

- This is the reason that N-Channel transistors are used in the pull-down network and P-Channel in the pull-up network of a CMOS gate. Otherwise the noise margin would be significantly reduced.

PASS TRANSISTOR LOGIC

- No pass transistor gate may be driven through one or more pass transistor.
- Logic levels propagated through pass transistors are degraded by threshold voltage effects



PASS TRANSISTOR LOGIC- AND GATE

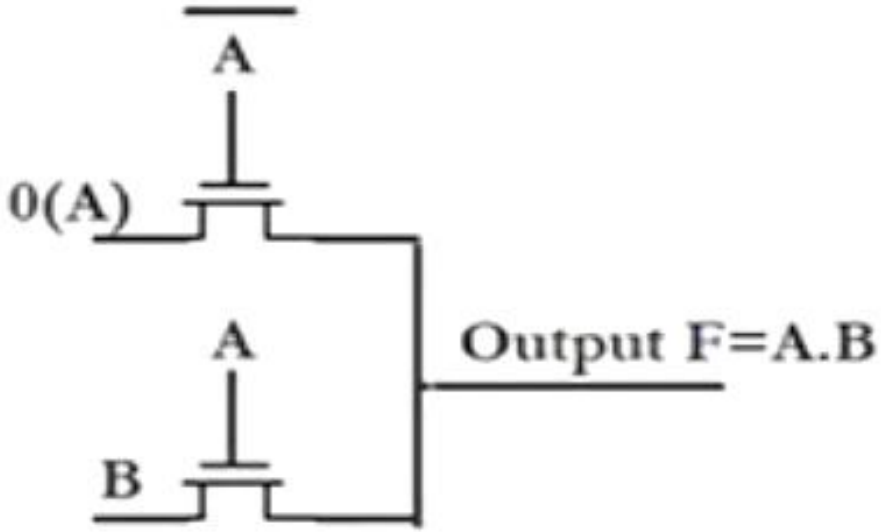
A	B	Output
0	0	0
0	1	0
1	0	0
1	1	1

- We have to design two NMOS which works on VGS low and VGS High

A – Control input

When A=0 ➔ Y = 0

When A=1 ➔ Y = B



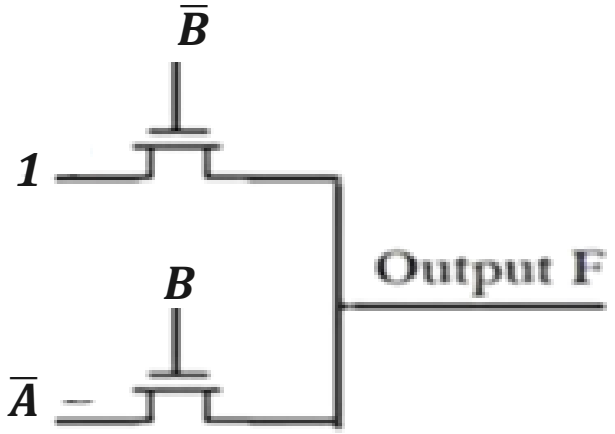
PASS TRANSISTOR LOGIC- NAND GATE

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

B – Control input

When B=0 ➔ Y = 1

When B=1 ➔ Y = $\overline{A}$



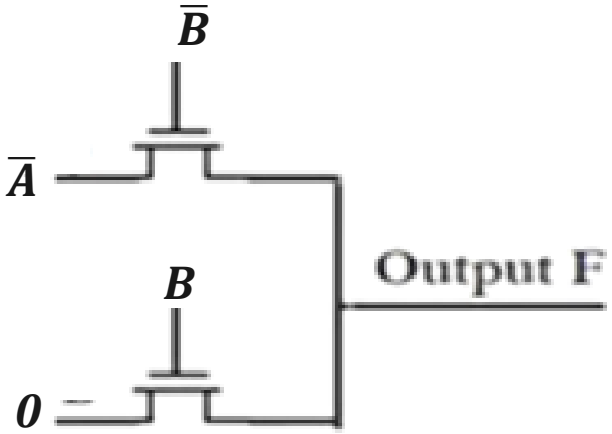
PASS TRANSISTOR LOGIC- NOR GATE

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

B – Control input

When B=0 ➔ Y = $\overline{A}$

When B=1 ➔ Y = 0



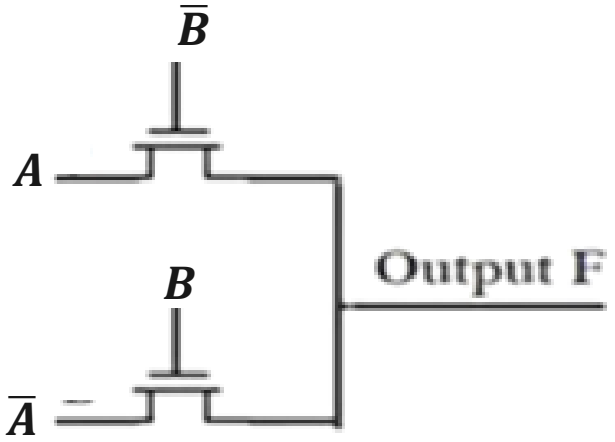
PASS TRANSISTOR LOGIC- XOR GATE

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

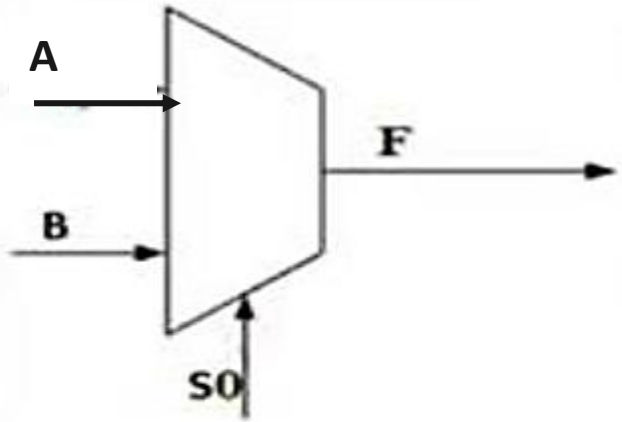
B – Control input

When B=0 ➔ Y = A

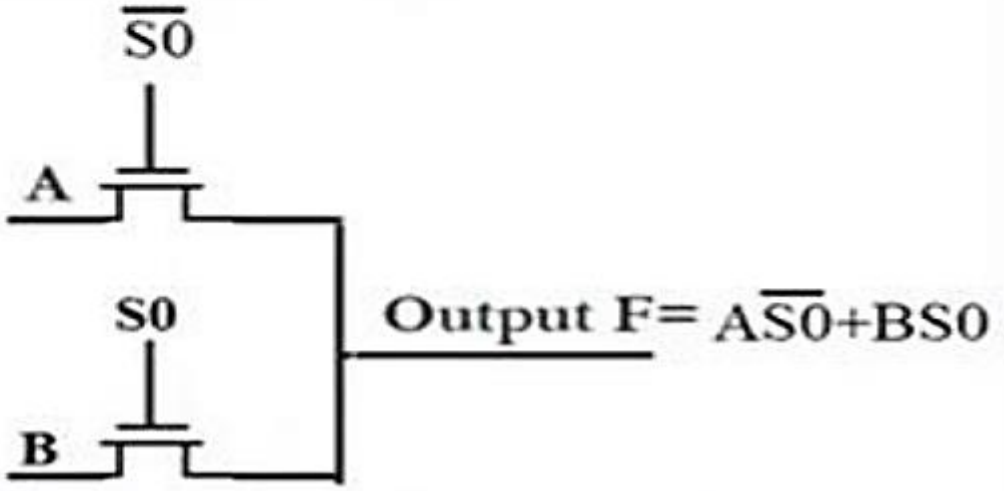
When B=1 ➔ Y = $\overline{A}$



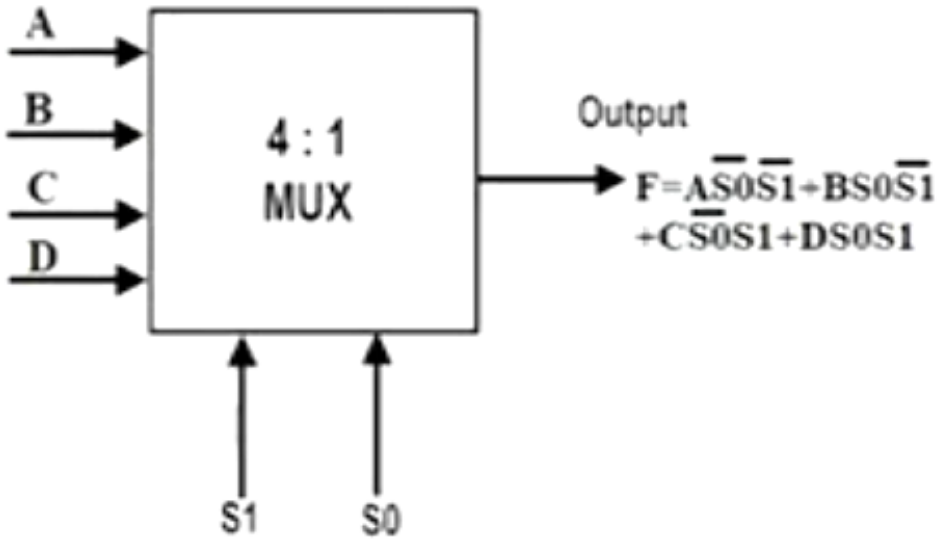
PASS TRANSISTOR LOGIC- 2:1 MUX



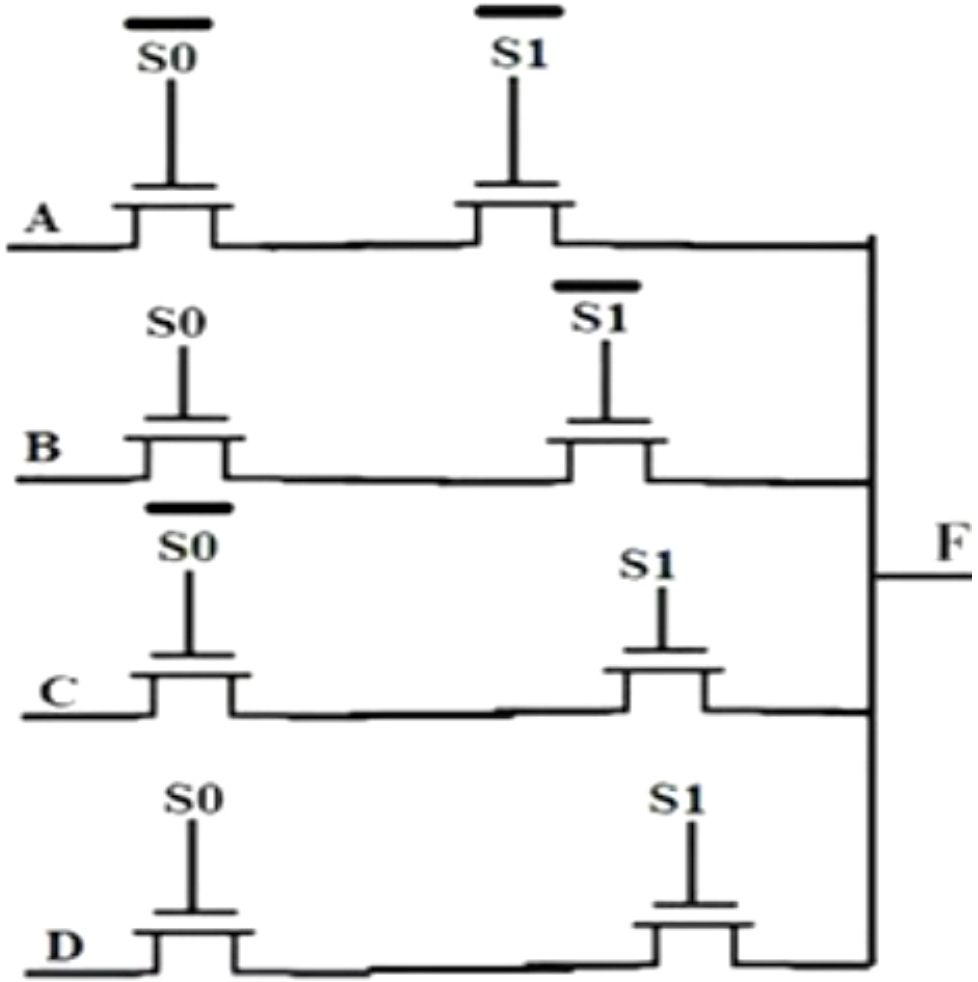
Truth Table	
S0	F(output)
0	A
1	B



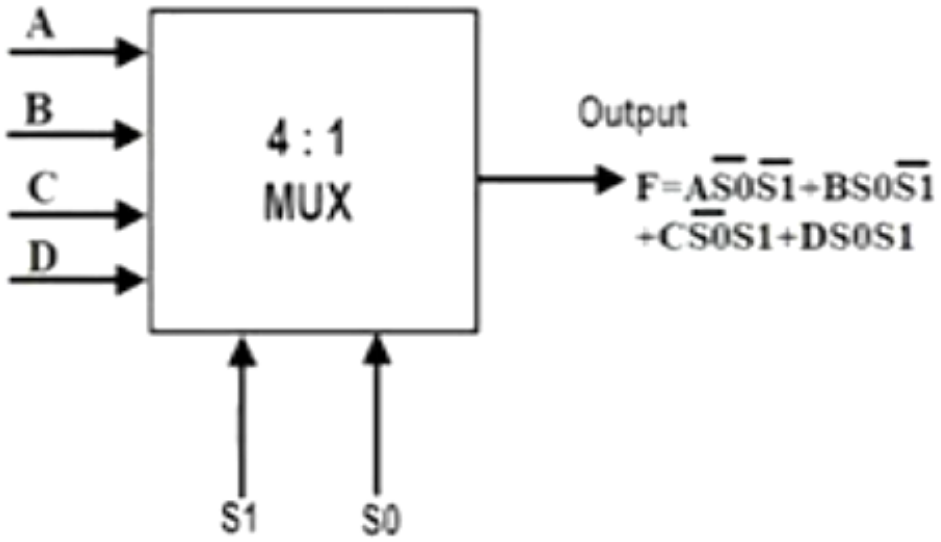
PASS TRANSISTOR LOGIC- 4:1 MUX



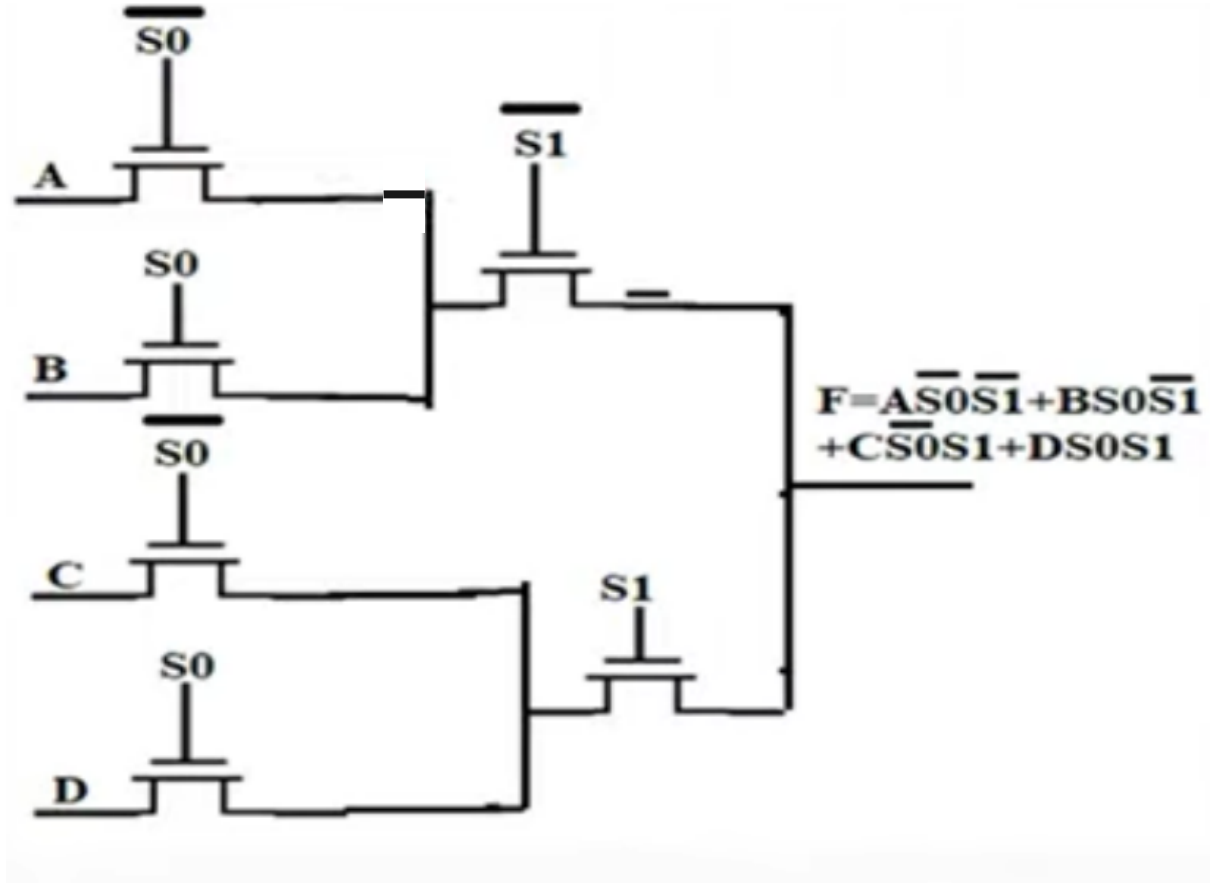
Truth Table		
S1	S0	F
0	0	A
0	1	B
1	0	C
1	1	D



PASS TRANSISTOR LOGIC- 4:1 MUX

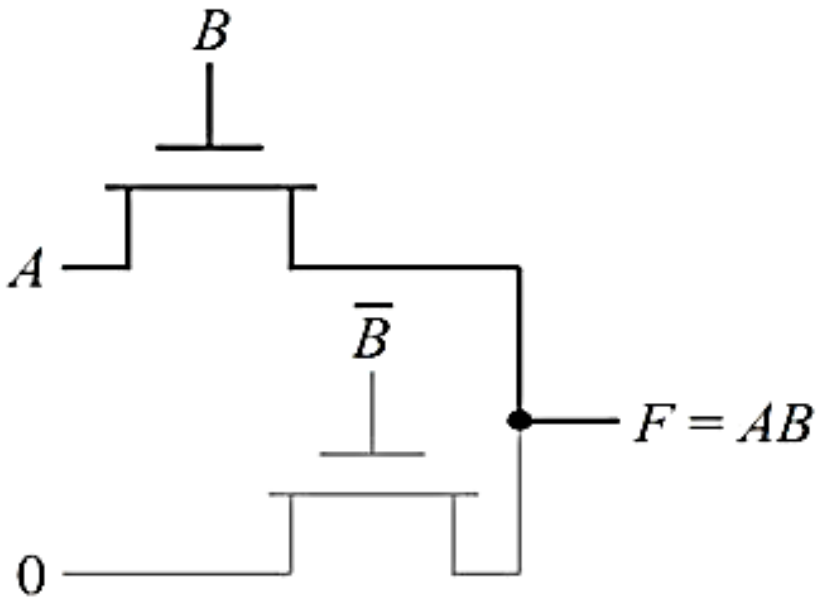


Truth Table		
S1	S0	F
0	0	A
0	1	B
1	0	C
1	1	D



Advantages of pass transistor logic

- Fewer devices to implement the logical functions as compared to CMOS
- Example AND gate.
- When B is “1”, top device turns on and copies the input A to output F.
- When B is low, bottom device turns on and passes a “0”.

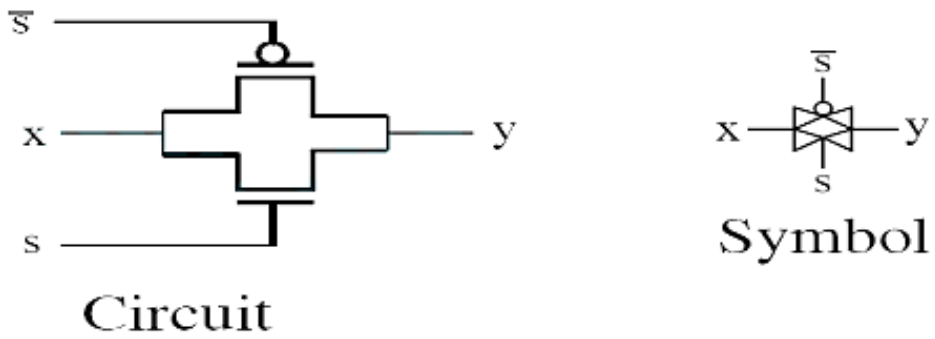


TRANSMISSION GATES

- The NMOS pass transistor passes a strong 0 and a weak 1.
- PMOS pass transistor passes a strong 1 and a weak 0.
- Combine the two to make a CMOS pass gate which will pass a strong 0 and a strong 1.
- Pass transistors produce degraded outputs
- ***Transmission gates pass both 0 and 1 well***

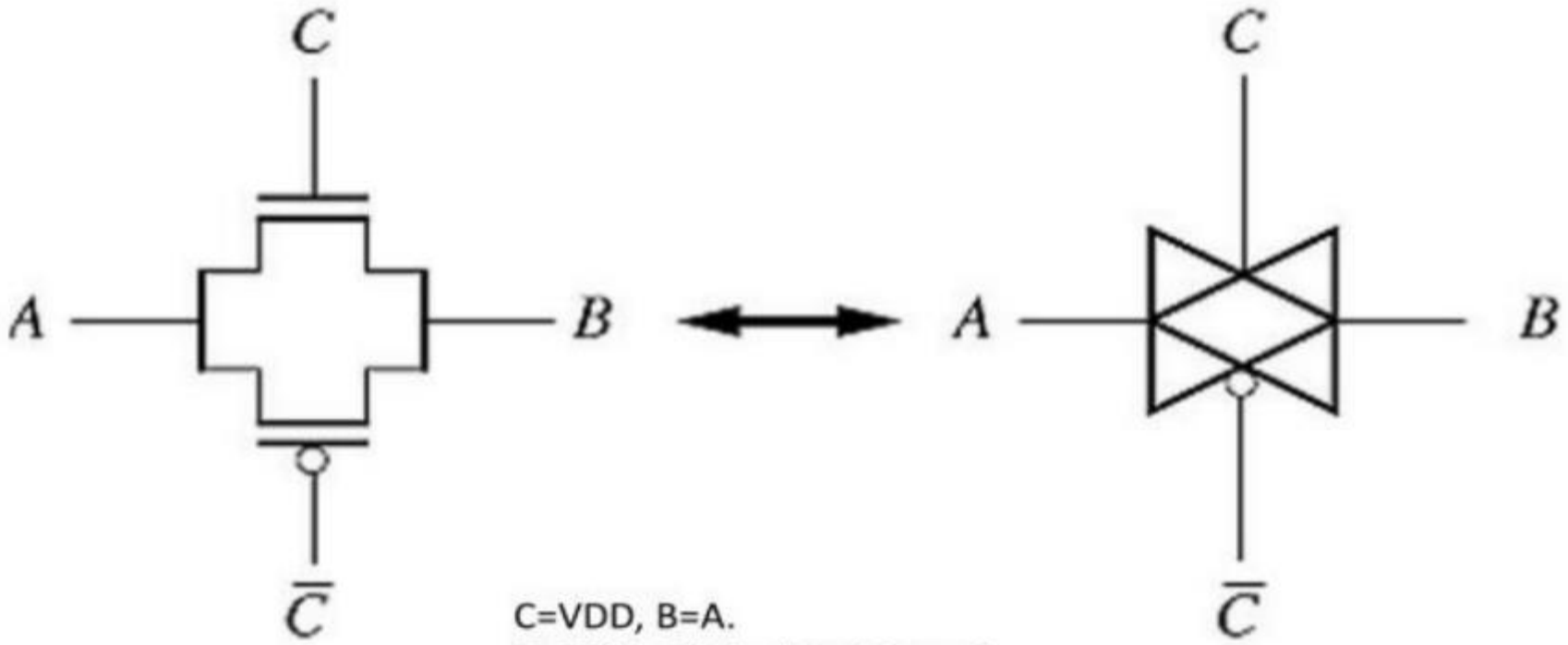
TRANSMISSION GATES

- A transmission gate is a essentially a switch that connects two points.
- In order to pass 0's and 1's equally well, a pair of transistors (one N-Channel and one P-Channel) are used as shown below:



- When s = 1 the two transistors conduct and connect x and y
  - The top transistor and the bottom transistor passes x when S= 1
- When s = 0 the two transistor are cut off disconnecting x and y

TRANSMISSION GATES



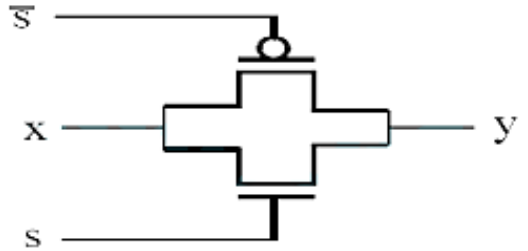
C=VDD, B=A.
C=GND, B is isolated from A.

Transistors: 4=2 (transmission gate)+2 (inverter)

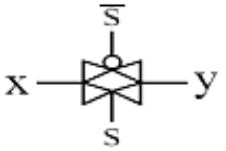
TRANSMISSION GATES

Operation

- S is logic high ➔Both transistors are turned on and provide a low-resistance ➔current path between nodes X and Y.
- S is logic low ➔ Both transistors will be off, and the path between nodes X and Y will be open circuit. This condition is called the high-impedance state.
- With the parallel PMOS added, it can transfer a full V_{DD} from X to Y (or Y to X). It can also charge driven capacitance faster.
- The substrates of NMOS and PMOS are connected to ground and VDD, respectively. Therefore, the substrate-bias effect must be taken into account.



Circuit

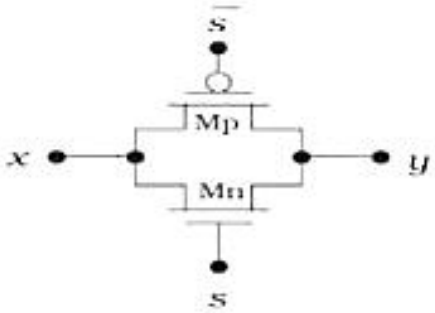


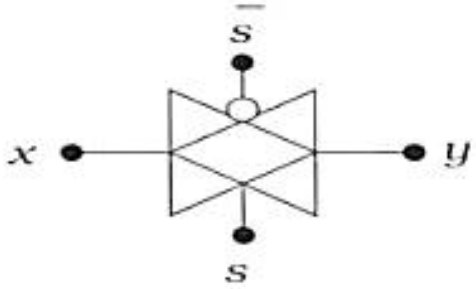
Symbol

TRANSMISSION GATES

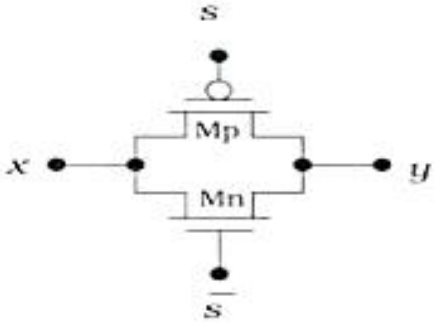
- Bi-directional
- Transmit the entire voltage range [0, V_{DD}]

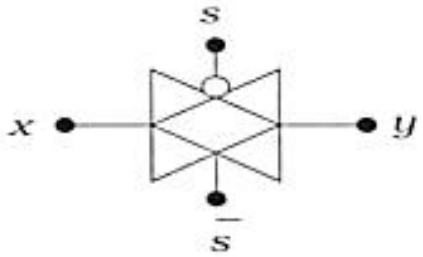
$$y = x \cdot s \quad iff \quad s = 1$$





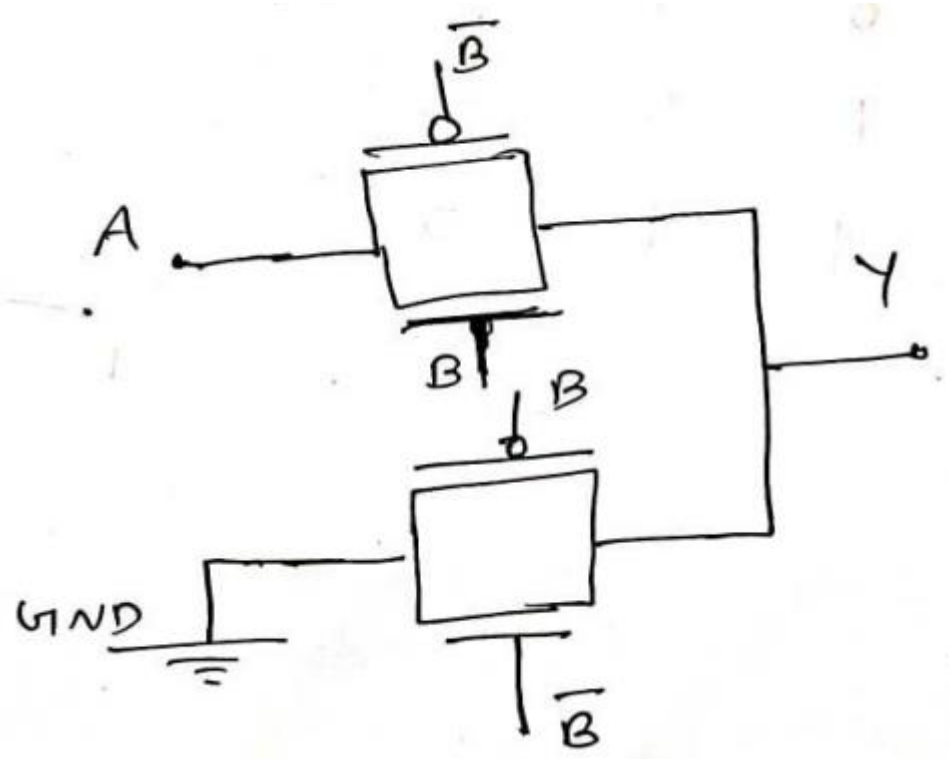
$$y = x \cdot \bar{s} \quad iff \quad \bar{s} = 1$$





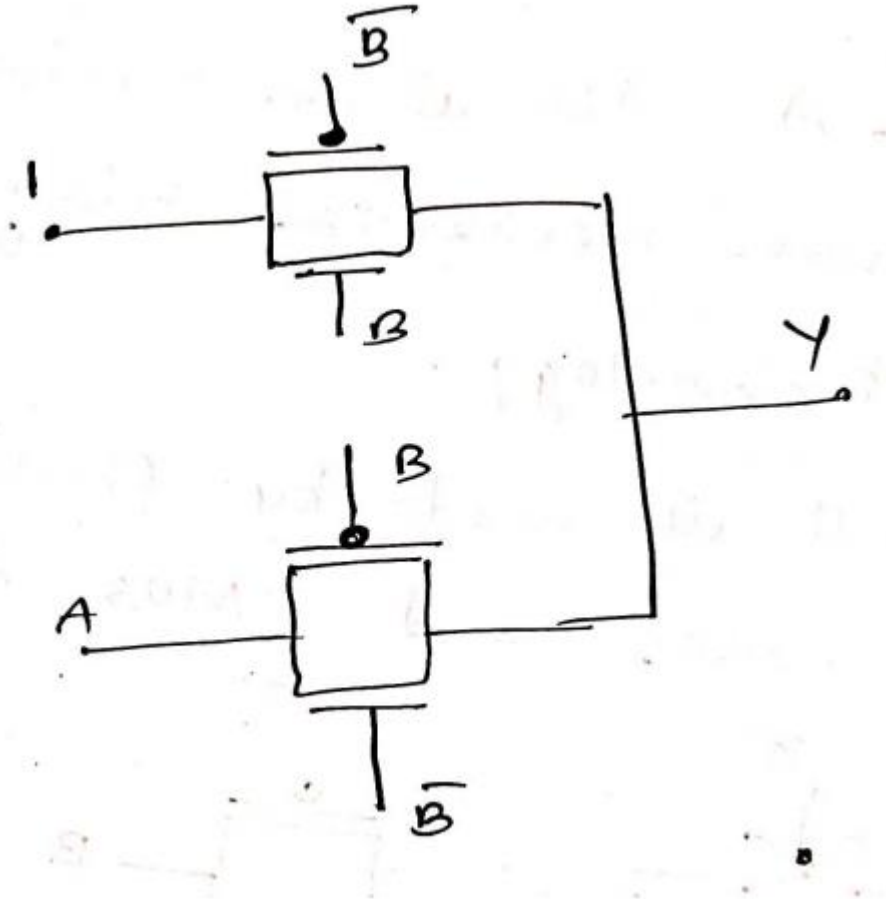
TRANSMISSION GATES- AND GATE

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1



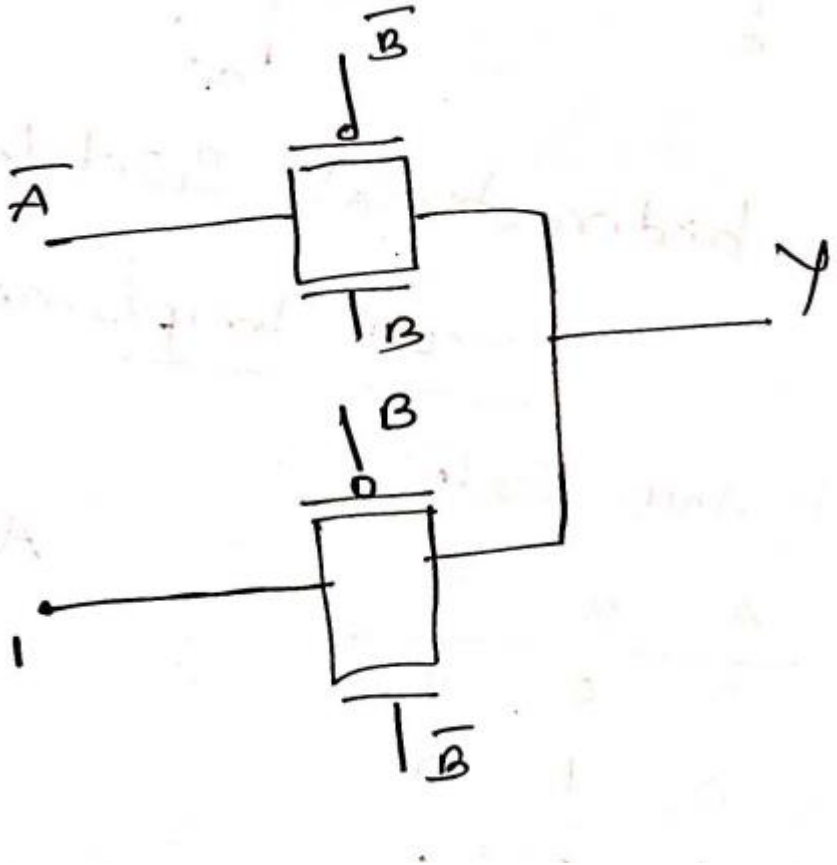
TRANSMISSION GATES- OR GATE

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0



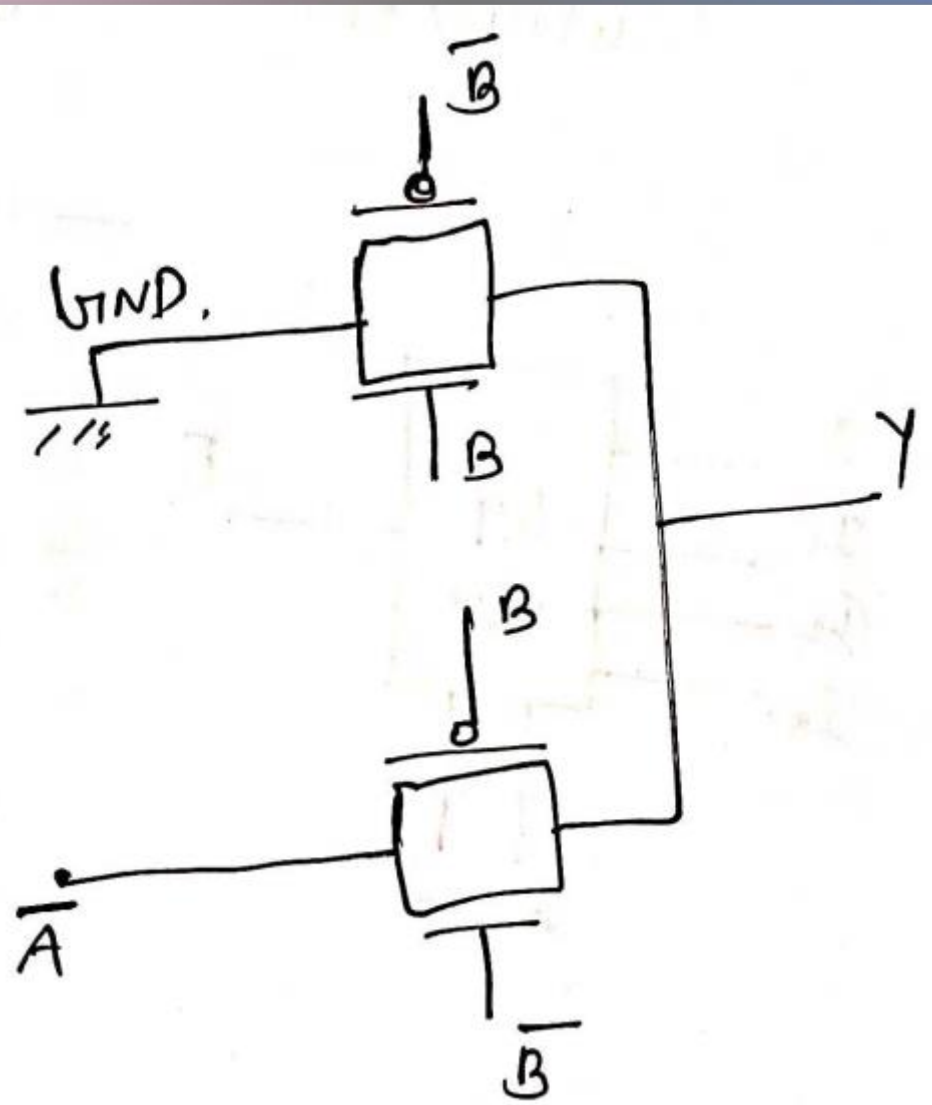
TRANSMISSION GATES- NAND GATE

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0



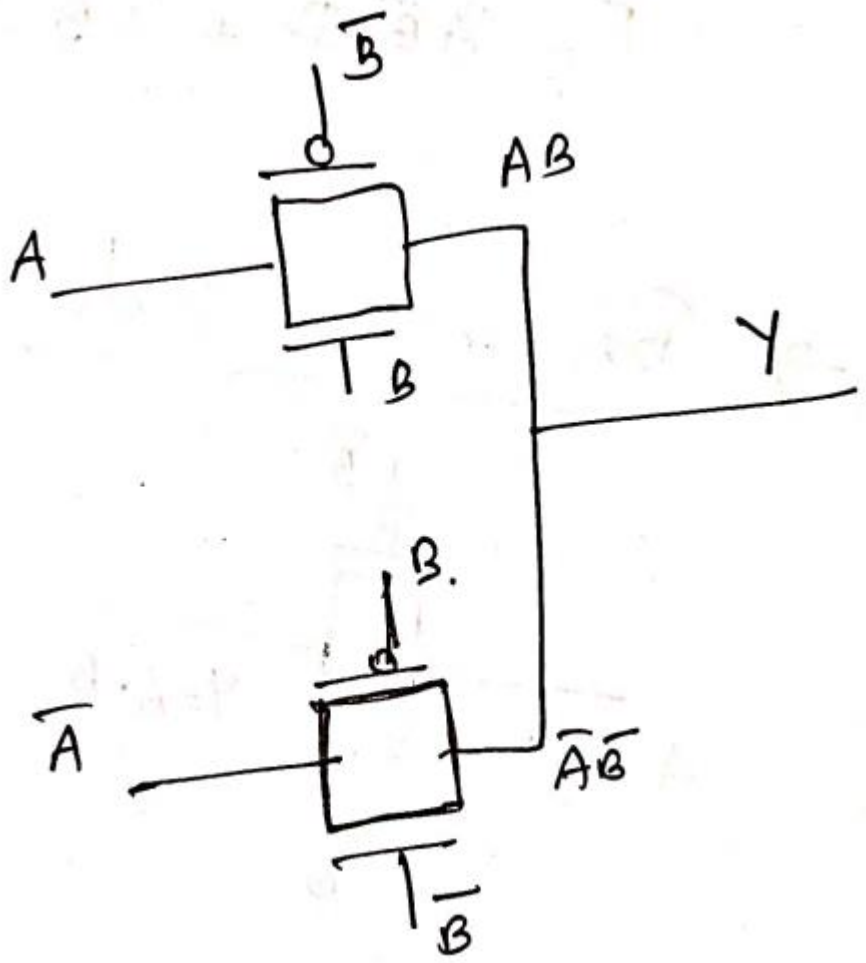
TRANSMISSION GATES- NOR GATE

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

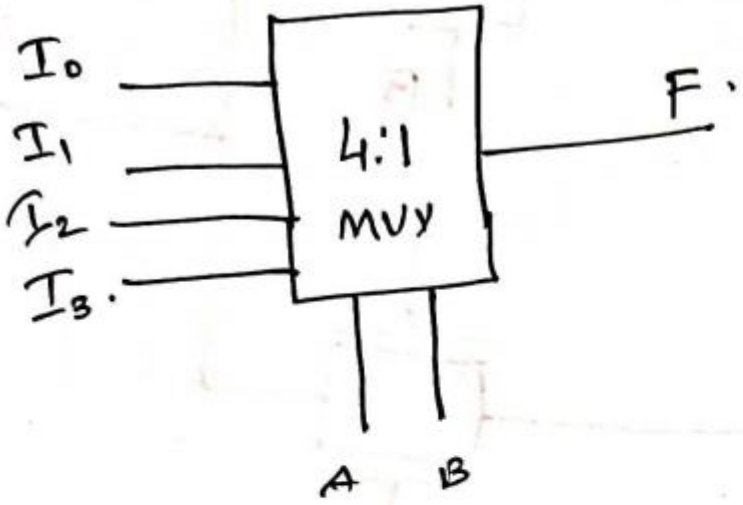


TRANSMISSION GATES- XNOR GATE

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1



TRANSMISSION GATES- 4:1 MUX

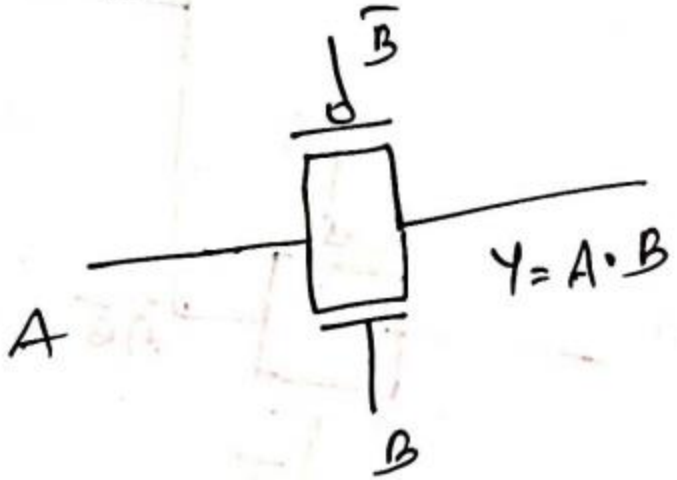


A	B	F
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3

$$F = \bar{A}\bar{B}I_0 + \bar{A}BI_1 + A\bar{B}I_2 + ABI_3$$

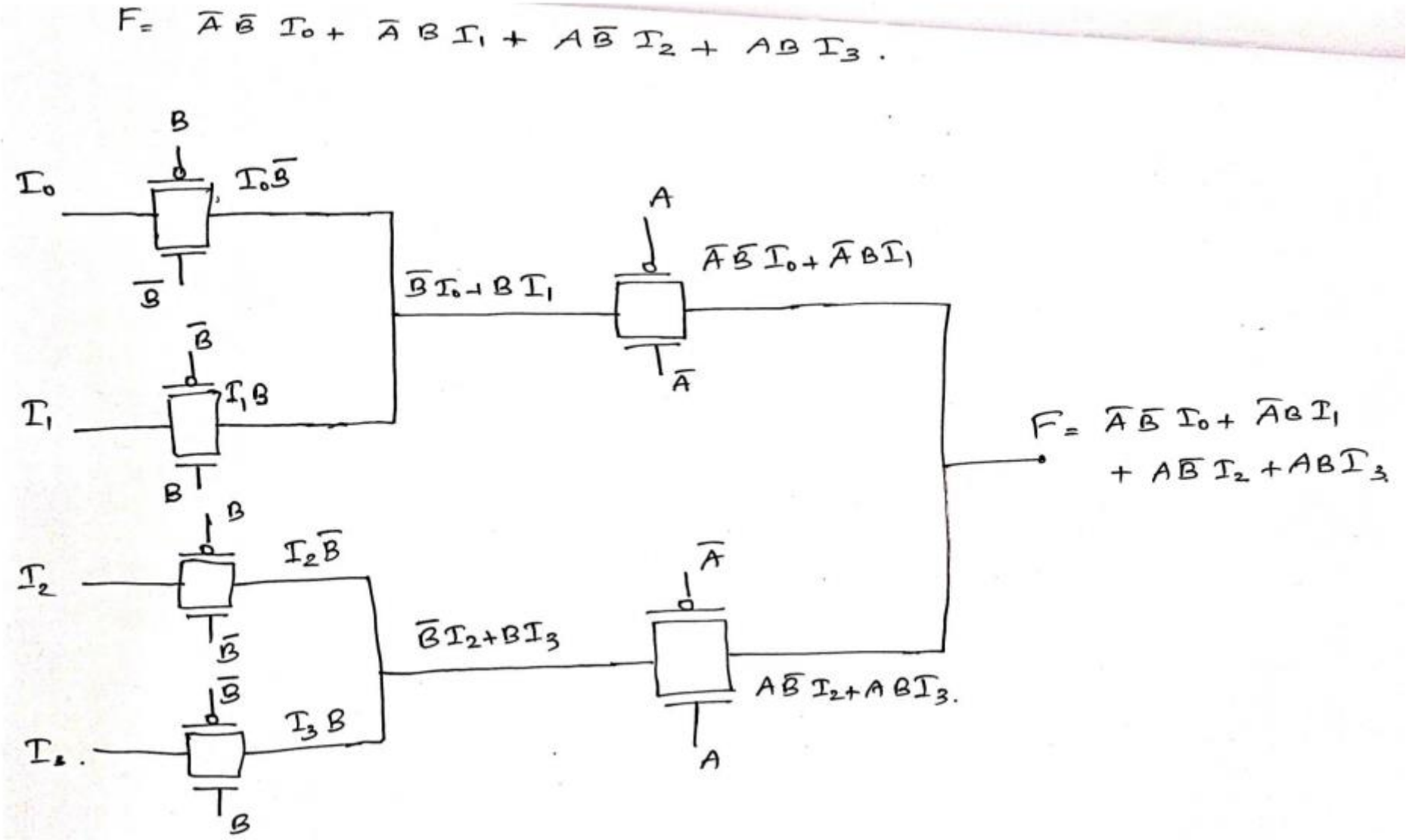
TRANSMISSION GATES- 4:1 MUX

→ Transmission Gate.



A	B	Y
0	0	H.I
0	1	0
1	0	H.I
1	1	1

TRANSMISSION GATES- 4:1 MUX



TRANSMISSION GATES- 4:1 MUX

- The 2:1 MUX can be modified to produced other useful function, such as XOR & XNOR circuits.