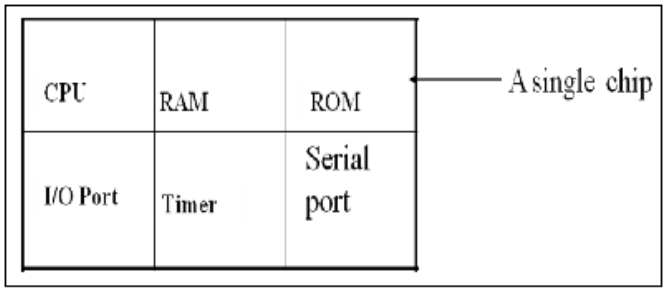
MicroProcessor	MicroController
Microprocessor is heart of Computer System.	Micro Controller is heart of an embedded System
CPU is Stand alone. RAM, ROM, I/O & timer are separate.	CPU, RAM, ROM,I/O & timer all are on single chip.
It is just a processor. Memory and I/O components have to be connected externally	Micro Controller has external processor along with internal memory and I/O components
Since memory and I/O has to be connected externally, the circuit becomes large	Since memory and I/O present internally, the circuit is small
Cannot be used in compact systems and hence inefficient	Can be used in compact systems and hence it is an efficient technique
RAM, ROM, I/O Ports, and Timers can be added externally and can vary in numbers.	RAM, ROM, I/O Ports, and Timers cannot be added externally. These components are to be embedded together on a chip and are fixed in numbers.
Designers can decide the amount of RAM, ROM, & I/O ports needed.	Fixed amount of on-chip RAM, ROM, & I/O ports.
Cost of the entire system increases	Cost of the entire system is low
Due to external components, the entire power consumption is high. Hence it is not suitable to use with devices running on	Since external components are low, total power consumption is less and can be used with devices running on stored power like batteries
Most of the microprocessors do not have power saving features	Most of the micro controllers have power saving modes like idle mode and power saving mode. This helps to reduce power consumption even further
Since memory and I/O components are all external each instruction will need external operation, hence it is relatively	Since components are internal, most of the operations are internal instruction, hence speed is fast.
Microprocessor have less number of registers, hence more operations are memory based.	Micro controller have more number of registers, hence the programs are easier to write.
Microprocessors are based on von Neumann model/architecture where program and data are stored in	Micro controllers are based on Harvard architecture where program memory and data memory are separate
General Purpose	Single Purpose
Mainly used in personal computers	Used in washing machine, MP3 players
E.g. 8085,8086,80286	E.g. 8051, PIC

3.3 MICROCONTROLLER

- A microcontroller is a programmable digital processor with necessary peripherals.
- The design has all the features found in microprocessor CPU: ALU,PC, SP and registers. It also has other features needed to make a complete computer: ROM, RAM, Parallel I/O, serial I/O, Counters and clock circuits.
- Block diagram of a typical Microcontroller which is a true computer on a chip is shown in fig
- The prime use of microcontroller is to control the operation of a machine using a fixed program that is stored in ROM and that does not change over the lifetime of the system.



fig

Microprocessors versus Microcontrollers:

MICROPROCESSORS	MICROCONTROLLERS
Contains ALU, general purpose registers, stack pointer, program counter, clock timing circuit and interrupt circuit.	Contains the circuitry of microprocessor and in addition it has built in ROM, RAM, I/O devices, timers and counters.
Have many instructions to move data between memory and CPU.	Have one or two instructions.
Have one or two bit handling instructions.	Have many instructions for handling the memory.
Access times for memory and I/O devices are more.	Less access times for built in memory and I/O devices.
Microprocessor based systems require more hardware.	Microcontroller based system require less hardware, reducing the PCB size and increasing the reliability.
They are more flexible in design point of view.	Less flexible from the design point of view.
Has single memory map for data and code.	Has separate memory map for data and code.
Less number of pins is multifunctional.	More number of pins are multifunctional.

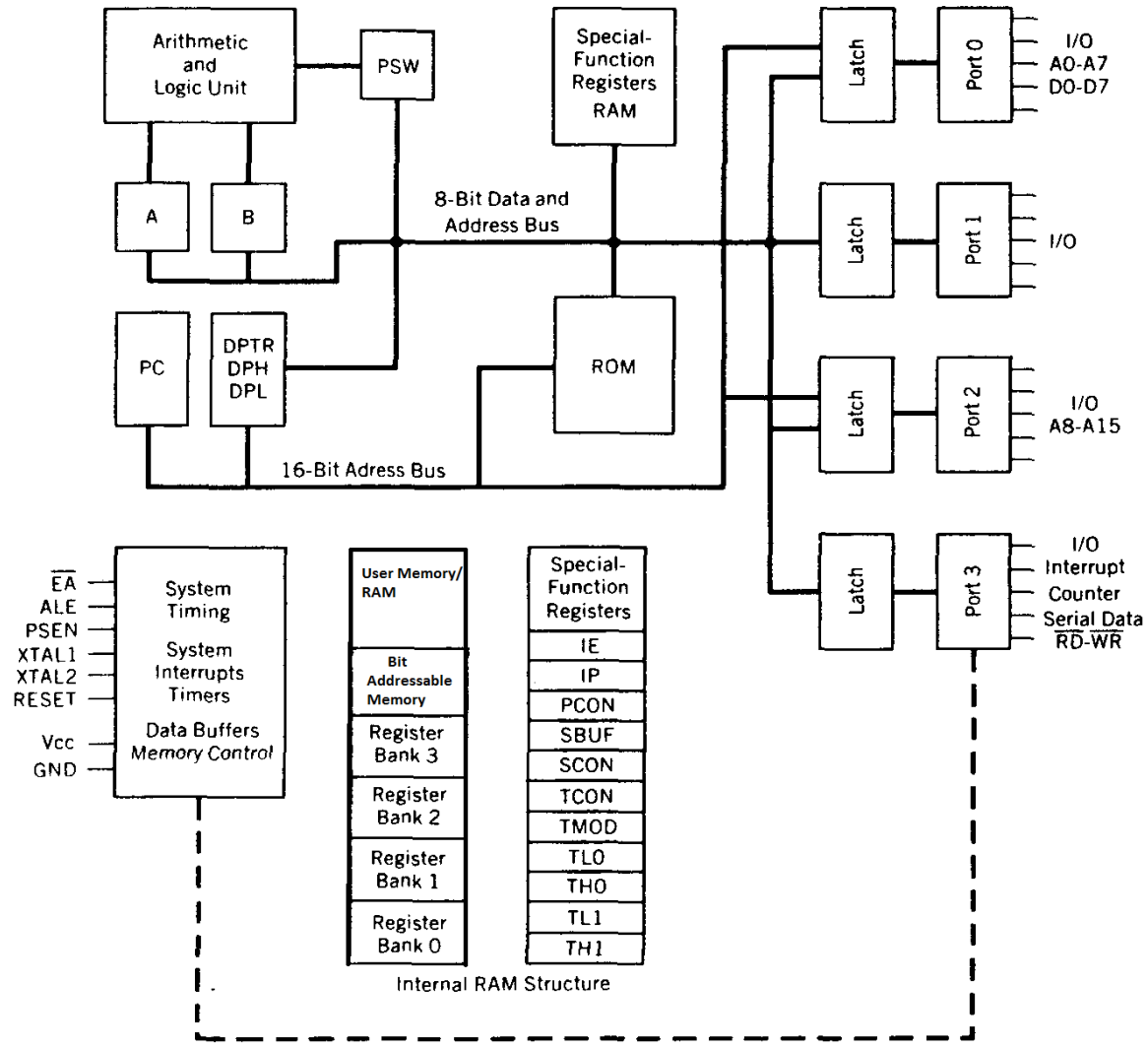
3.4 8031/8051 MICROCONTROLLER

Features of 8051

The salient features of the 8051 architecture are as follows:

- Eight bit CPU with registers A (Accumulator) and B
- 16 bit Program counter (PC) and a data pointer (DPTR)
- 8 Bit Program Status Word (PSW)
- 8 Bit Stack Pointer
- 4K Code Memory (Internal ROM or EPROM)
- Internal Memory of 128 Bytes (RAM)
    - 4 register each with 8 registers $R_0 - R_7$. Each of 8 byte size.
    - 16 bytes which may be addressed at the bit level.
    - 80 bytes of general purpose data memory.
- 32 I/O Pins arranged as 4 , 8 Bit ports
- Two 16 Bit Timer/Counter :T0, T1
- Full Duplex serial data receiver/transmitter
- Control Registers : TCON,TMOD,SCON,PCON,IP and IE
- Two External and three Internal Interrupt sources

3.5 ARCHITECTURE OF 8031/8051 MICROCONTROLLER



Description:

1. ALU:

- It performs the arithmetic operations such as addition, subtraction, multiplication and division.
  - The unit can perform logical operations such as AND, OR; and Exclusive-OR, as well as rotate, clear, and complement.
  - The ALU can also manipulate one bit as well as eight-bit data types.
  - Individual bits may be set, cleared, complemented, tested, and used in logic computation.

2. Accumulator:

- It is an 8-bit register.
- It holds a data for arithmetic and logical operations.
- Results of arithmetic and logical operations are stored in accumulator.

3. B register:

- An 8-bit general-purpose register.
- Used for direct multiplication and division along with accumulator

4. Program Status Word:

- Many instructions implicitly or explicitly affect (or are affected by) several status flags, which are grouped together to form the Program Status Word (Flag register).
- It also used to select the memory bank.

B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0
CY	AC	F0	RS1	RS0	OV	-	P

Program Status Word

CY, *the carry flag*

- This flag is set whenever there is a carry out from the D7 bit.

AC, the auxiliary carry flag

- If there is a carry from D3 to D4 during an ADD or SUB operation, this bit is set; otherwise, it is cleared.

P, the parity flag

- The parity flag reflects the number of 1 s in the A (accumulator) register only. If the A register contains an odd number of Is, then P = 1. Therefore, P = 0 if A has an even number of Is.

OV, the overflow flag

- This flag is set whenever the result of a signed number operation is too large.

F0, *User flag*

- This flag is user defined flag. Programmer can use this flag as per the requirements.

RS1 and RS0 are used to select the register bank as follows:

RS1	RS0	BANK SELECTION	
0	0	00H - 07H	Bank 0
0	1	08H - 0FH	Bank 1
1	0	10H - 17H	Bank 2
1	1	18H - 1FH	Bank 3

5. Stack Pointer (SP):

- The stack pointer register is 8 bit wide.
- It is incremented before data is stored during PUSH and CALL instructions.
- After reset the value of SP is 07H.

6. Data Pointer (DPTR):

- The data pointer is a 16-bit register used to hold the 16-bit address of external data memory.
- This can also be used as two numbers of 8-bit data pointer namely DPH and DPL.
- The 8-bit data pointers are used for accessing internal RAM and SFR.
- The 16-bit data pointer is used for accessing external data memory.

7. Program Counter (PC):

- It is a 16 bit register.
- PC is used, as address pointer to access program instructions and it is automatically incremented after every byte of instruction fetch.

8. I/O Ports:

- The 8051 has four numbers of 8-bit ports namely port-0, port- 1, port-2 and port-3.
- Each port has a latch and driver (or buffer).
- When external memory is employed the port-0 lines will function as multiplexed low byte address/data lines and port-2 lines will function as high byte address lines.
- Also the port pins P3.7 and P3.6 are used to output read and write control signals respectively.
- The port-1 is dedicated I/O port and does not have any alternate function.

9. Instruction Register (IR) & timing and control unit:

- The controller will fetch the instructions one by one, starting from the address stored in PC and store in Instruction Register, which decodes the instructions and give information to timing and control unit.
- Using the information supplied by the IR unit the control signals necessary for internal and external operations are generated by the timing and control unit.

10. Timer/Counter:

- The 8031/8051 has two 16-bit programmable timer/counter namely timer-1 and timer 0.
- In the counter mode of operation, they can count the number of high to low transitions of the signal applied to the timer pins.
- In timer mode of operation, they can be independently programmed to work in any one of the four operation modes. They are called mode-0, mode-1, mode-2 and mode-3.

11. Serial port:

- The 8031/8051 has a serial data communication circuit that uses pins RXD (P3.0) and TXD (P3.0) for connecting serial communication device.
- Special function registers related to serial port are SBUF, SCON and PCON.

12. Special Function Registers:

- Special function registers are registers with dedicated functions.

3.6 MEMORY ORGANIZATION

- The 8051 has Harvard architecture which uses two types of memory for Program and Data.
- Program Memory (ROM) is used for permanent saving program being executed, while Data Memory (RAM) is used for temporarily storing and keeping intermediate results and variables.

Internal RAM:

The 128 bytes internal RAM is organized into 3 distinct areas, as shown in fig 1.14:

1. **Register banks:**
   - 32 bytes from address 00h to 1Fh that make up 32 working registers organized as 4 memory banks of 8 registers each.
   - The 4 register banks are numbered 0 to 3 and are made up of 8 registers named R0 to R7. Each register can be addressed by name or by its RAM addresses. Thus R0 of bank3 is R0 (if bank3 is selected) or address 18h (where bank3 is selected).
   - Bits RS0 and RS1 in the PSW determine which bank of registers is currently in use at any time when program is running.
   - Register banks not selected can be used as general purpose RAM.
   - Bank0 is selected by default on reset.
2. **Bit addressable memory:**
   - A bit addressable area of 16 bytes occupies RAM byte addresses 20h to 2Fh, forming total of 128 bits.
   - An addressable bit may be specified by its bit address of 00h to 7Fh or 8 bits may form any byte address from 20h to 2Fh.For example bit address 4fh is also bit 7 of byte address 29h.

3. **A general purpose RAM:**

- A general purpose RAM area above the bit area from 30h to 7Fh, addressable as byte.

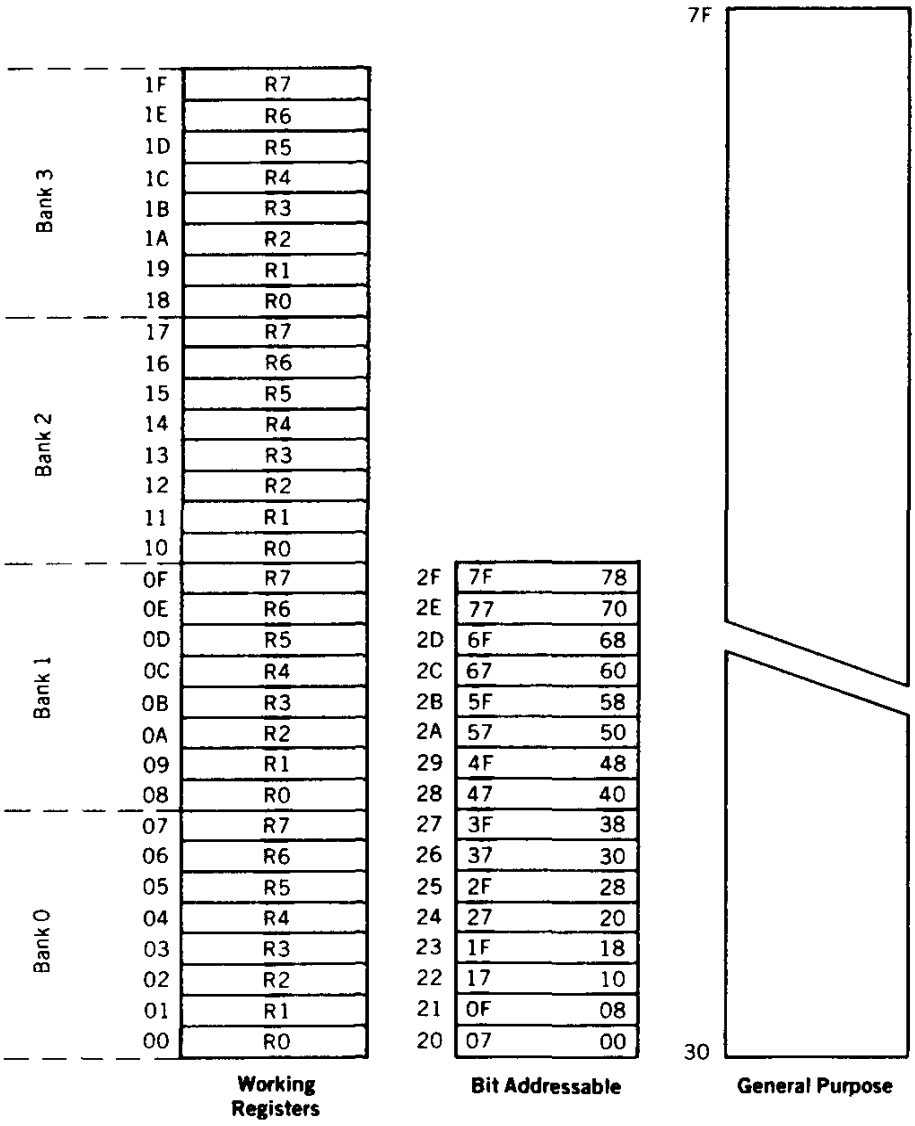


Fig. Internal RAM structure

Special Function Registers (SFR):

- Special function registers (SFR) are addressed using addresses from 80h to 0FFh.
- Some SFRs are also bit addressable as is the case for the bit area of RAM.
- Not all of the addresses from 80h to 0FFh are used for SFRs. Only the addressed ones can be used in programming SFRs and equivalent internal RAM addresses are shown in Figure below
- The set of Special Function Registers (SFRs) contain important registers such as Accumulator, Register B, and I/O Port latch registers, Stack pointer, Data Pointer, Processor Status Word (PSW) and various control registers.
- Some of these registers are bit addressable (they are marked with a * in the Figure below).

Special Function Registers and the addresses

ADDRESS	Special Function Registers							
0F8H								
0F0H	B*							
0E8H								
0E0H	ACC*							
0D8H								
0D0H	PSW*							
0C8H	(T2CON)*		(RCAP2L)	(RCAP2H)	(TL2)	(TH2)		
0C0H								
0B8H	IP*							
0B0H	P3*							
0A8H	IE*							
0A0H	P2*							
98H	SCON*	SBUF						
90H	P1*							
88H	TCON*	TMOD	TL0	TL1	TH0	TH1		
80H	P0* 80H	SP 81	DPL 82	DPH 83	84	85	86	PCON 87

Internal ROM:

- 8051 is organized so that data memory and program code memory can be two entirely different physical memory entities. Each has the same address ranges. The internal program ROM occupies code address space 0000h to 0FFFh.
- The PC is normally used to address program code bytes from address 0000h to FFFFh. Program addresses higher than 0FFFh which exceed the internal ROM capacity will cause the 8051 to automatically fetch code bytes from external memory.

External Memory Interfacing:

- The system designer is not limited by the amount of internal ROM and RAM available on chip.
- The designer can interface external program memory and data memory if the available internal memory is not enough.
- Program counter is used to address the external program memory and DPTR is used to address the external data memory.
- $\overline{\text{PSEN}}$ (Program store enable) pin is used as read signal for program memory.
- $\overline{\text{EA}}$ pin is used to enable external program memory. When $\overline{\text{EA}}$ = 0, then 8051 microcontroller access from external program memory (ROM) only.
- $\overline{\text{RD}}$ or $\overline{\text{WR}}$ (alternate function of P3.7 and P3.6) pins are used to access external data memory.

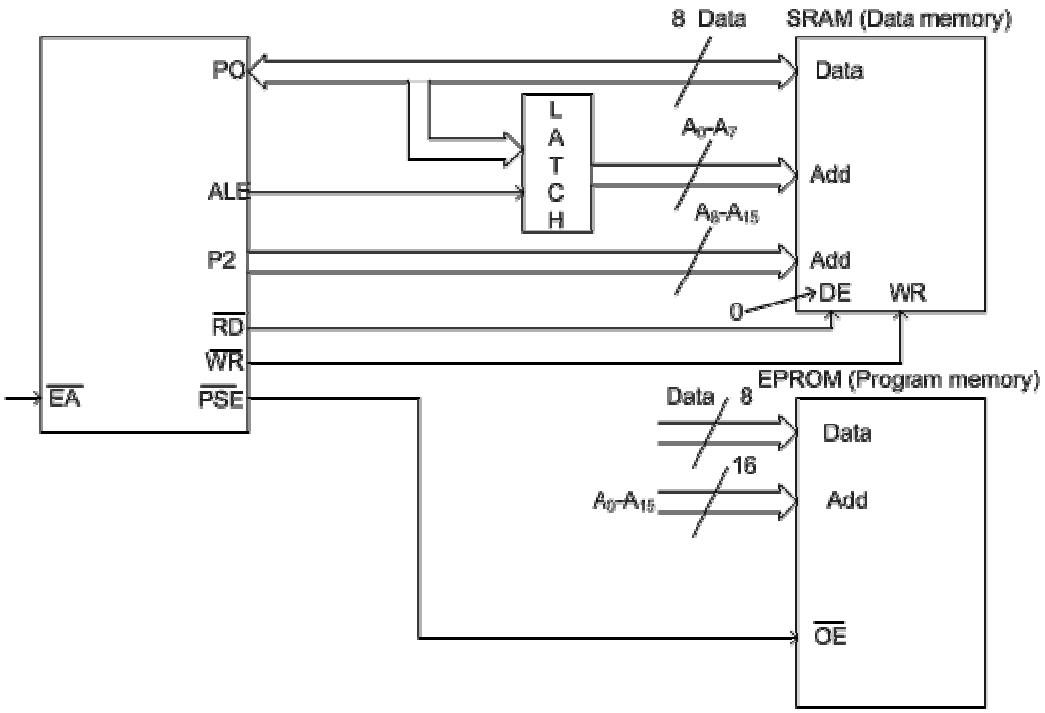


Diagram for Interfacing of External Memory

STACK IN 8051

- The stack is a section of RAM used by the CPU to store information temporarily.
- The register used to access the stack is called the SP (stack pointer) register.
- The stack pointer in the 8051 is only 8 bits wide, which means that it can take values of 00 to FFH.
- When the 8051 is powered up, the SP register contains value 07.
- The storing of a CPU register in the stack is called a PUSH, and pulling the contents off the stack back into a CPU register is called a POP.

Pushing onto the stack

- In the 8051 the stack pointer (SP) points to the last used location of the stack. When we push data onto the stack, the stack pointer (SP) is incremented by one first, then the data is moved to the stack..

Popping from the stack

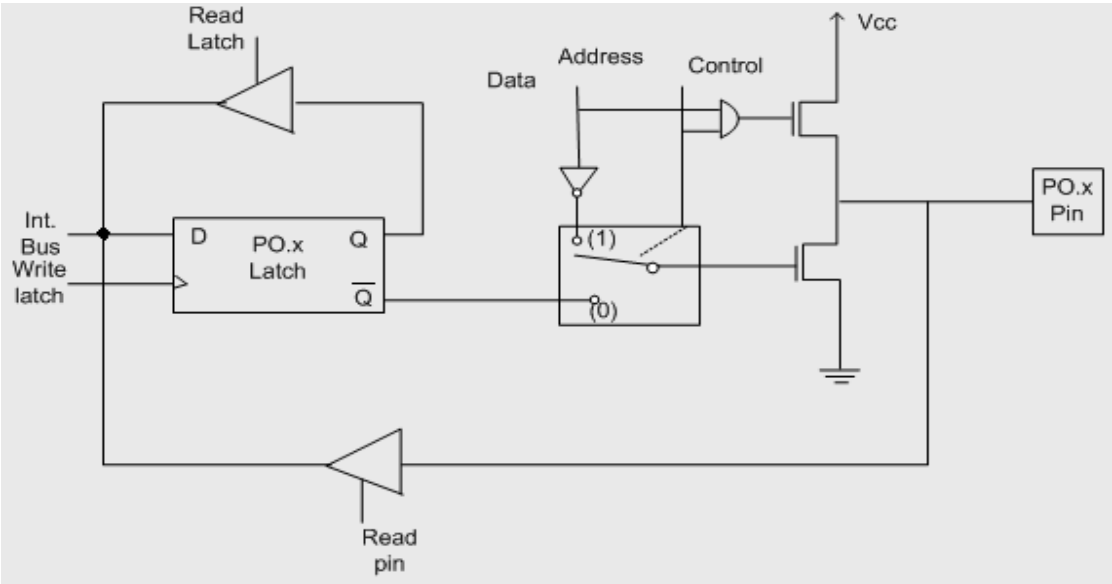
- Popping the contents of the stack back into a given register is the opposite process of pushing.
- With every pop, the top byte of the stack is copied to the register specified by the instruction and then stack pointer is decremented by one.

3.7 I/O PORTS

- 8051 has 32 I/O pins configured as four 8 bit parallel ports ($P_0 - P_3$).
- All 4 ports are bidirectional, can be configured as either input or output or both.
- All port pins are multi functional except pins of Port 1.
- Each port consists of latch, output driver and input buffer.

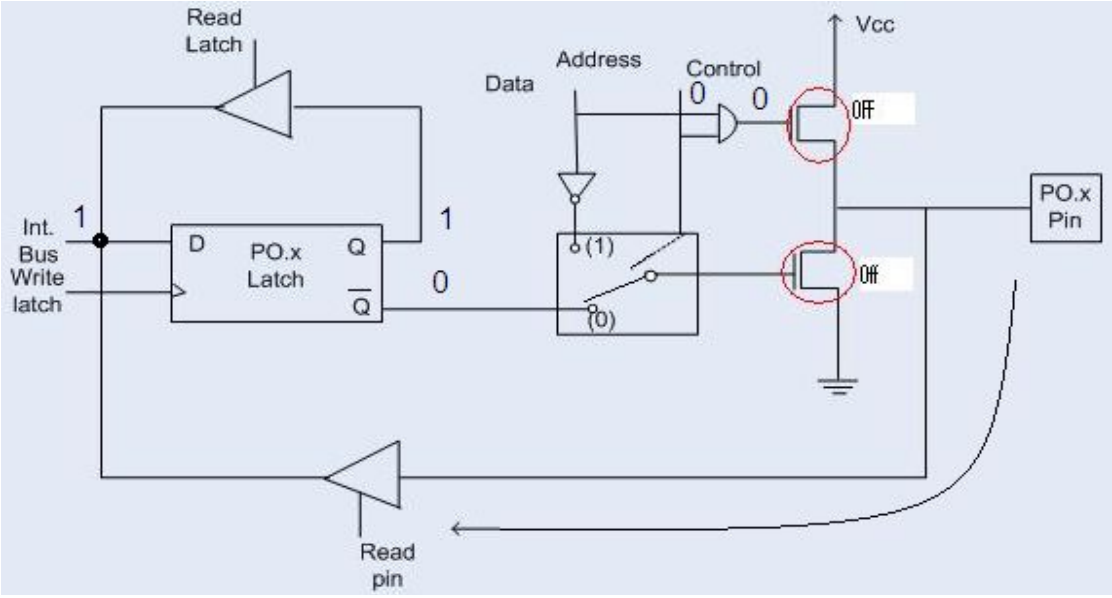
PORT0:

- Port -0 has 8 pins identified as P0.0-P0.7.
- The structure of a Port-0 pin is shown below.
- Port-0 can be configured as a normal bidirectional I/O port or it can be used for address/data interfacing for accessing external memory.
- When control is '1', the port is used for address/data interfacing. When the control is '0', the port can be used as a normal bidirectional I/O port.



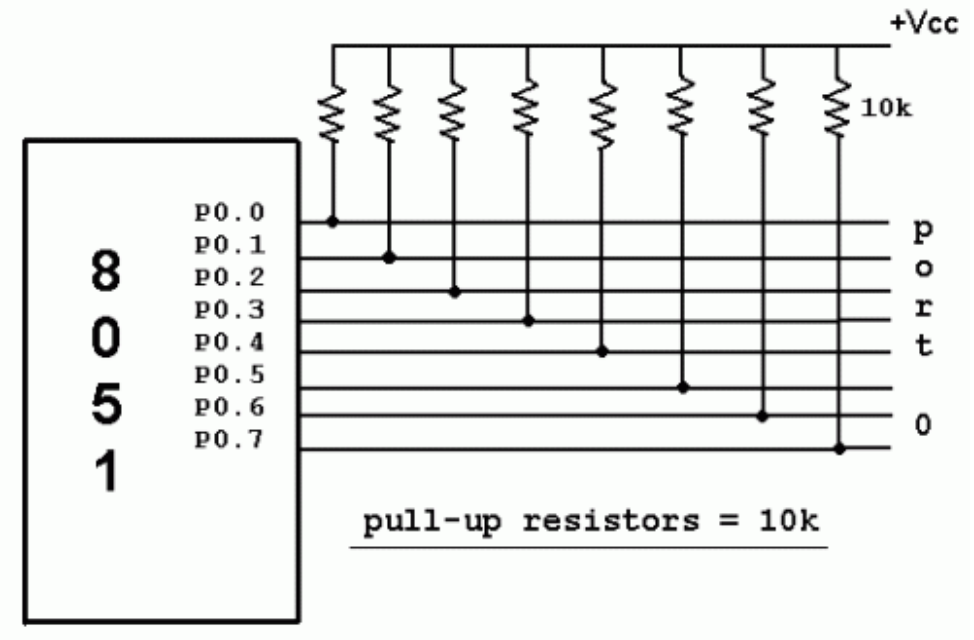
PORT 0 as an Input Port

Let us assume that control is '0'. When the port is used as an input port, '1' is written to the latch. In this situation both the output MOSFETs are 'off'. Hence the output pin has floats hence whatever data written on pin is directly read by read pin.

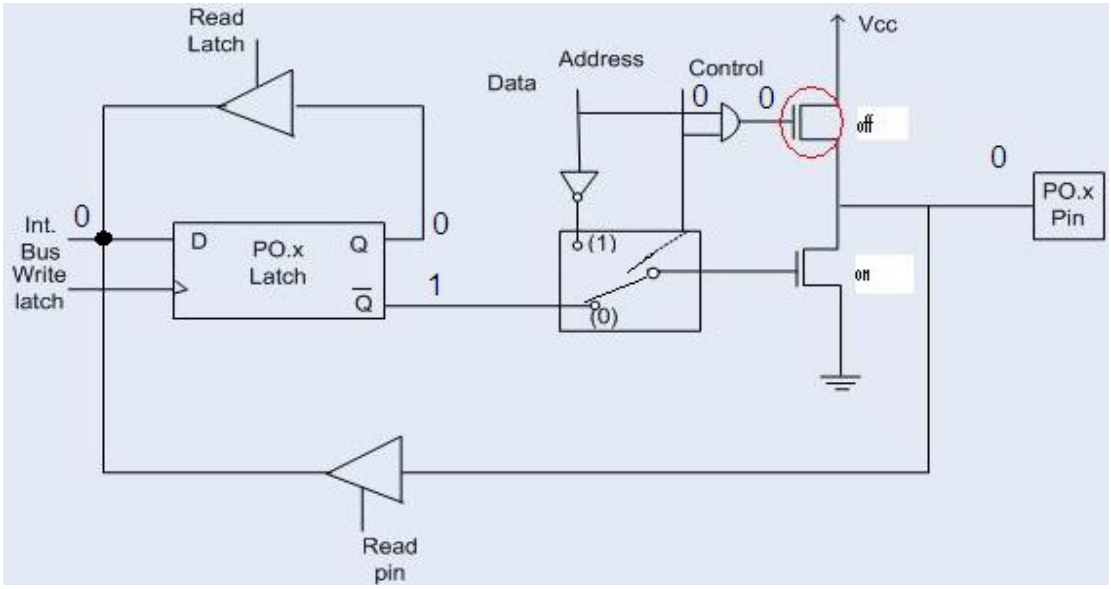


PORT 0 as an Output Port

Suppose we want to write 1 on pin of Port 0, a '1' written to the latch which turns 'off' the lower FET while due to '0' control signal upper FET also turns off as shown in fig. above. Here we wants logic '1' on pin but we getting floating value so to convert that floating value into logic '1' we need to connect the pull up resistor parallel to upper FET . This is the reason **why we needed to connect pull up resistor to port 0 when we want to initialize port 0 as an output port** .

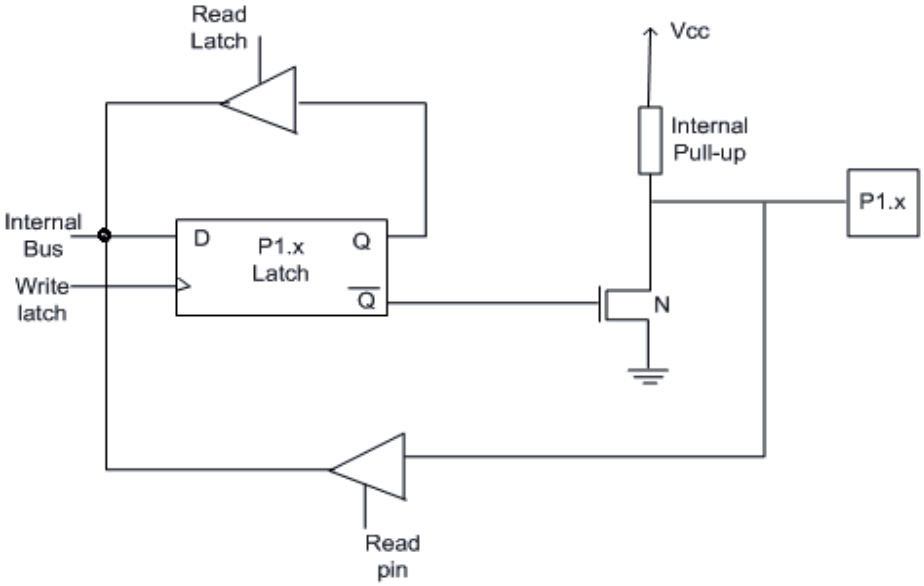


If we want to write '0' on pin of port 0 , when '0' is written to the latch, the pin is pulled down by the lower FET. Hence the output becomes zero.



PORT-1

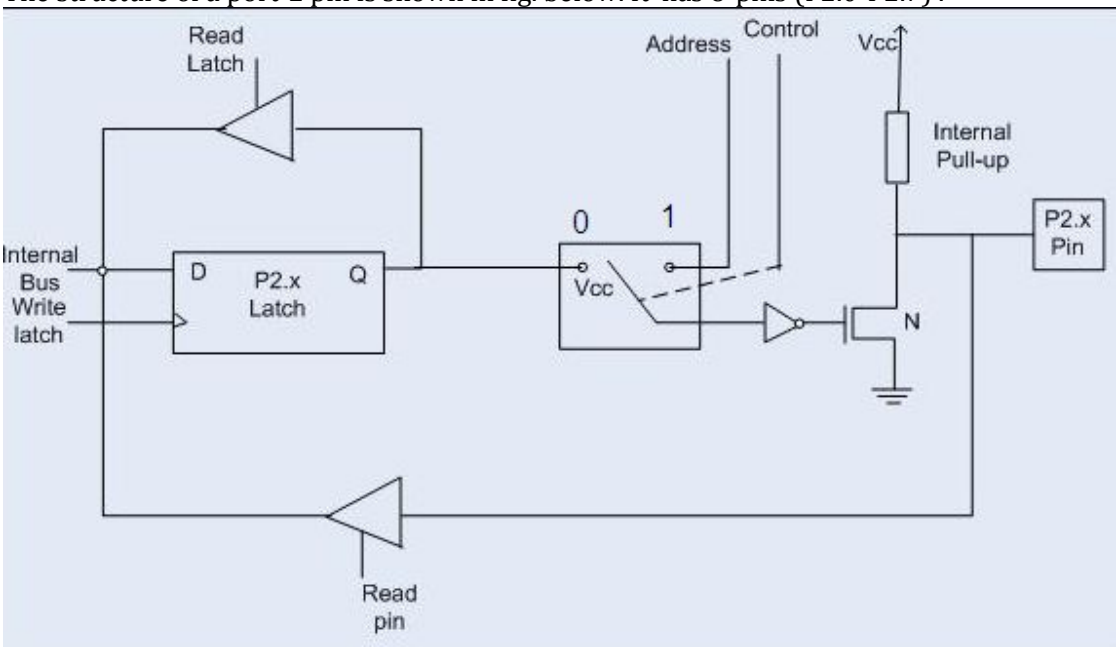
- Port-1 has 8 pins (P1.1-P1.7) .The structure of a port-1 pin is shown in fig



- Port-1 does not have any alternate function i.e. it is dedicated solely for I/O interfacing.
- When used as output port, the pin is pulled up or down through internal pull-up.
- To use port-1 as input port, '1' has to be written to the latch. In this input mode the bit written to the pin by the external device can be read the processor.

PORT-2

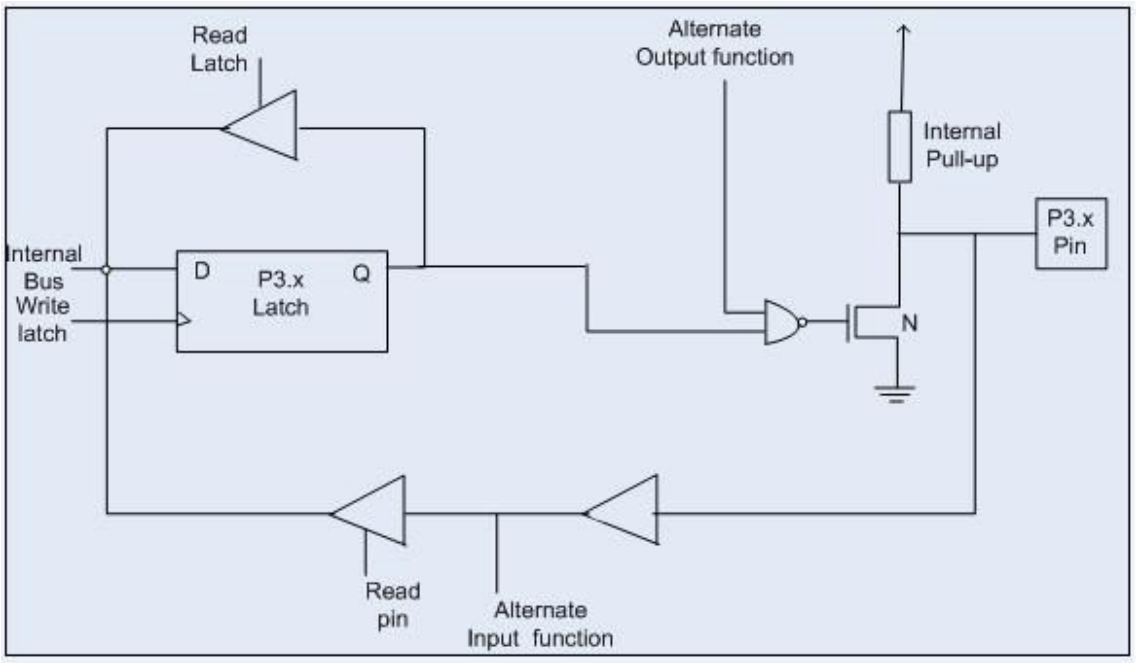
The structure of a port-2 pin is shown in fig. below. It has 8-pins (P2.0-P2.7) .



- Port-2 is used for higher external address byte or a normal input/output port.
- The I/O operation is similar to Port-1.
- Port-2 latch remains stable when Port-2 pin are used for external memory access.

PORT-3

- Port-3 (P3.0-P3.7) having alternate functions to each pin. The internal structure of a port-3 pin is shown in fig below.

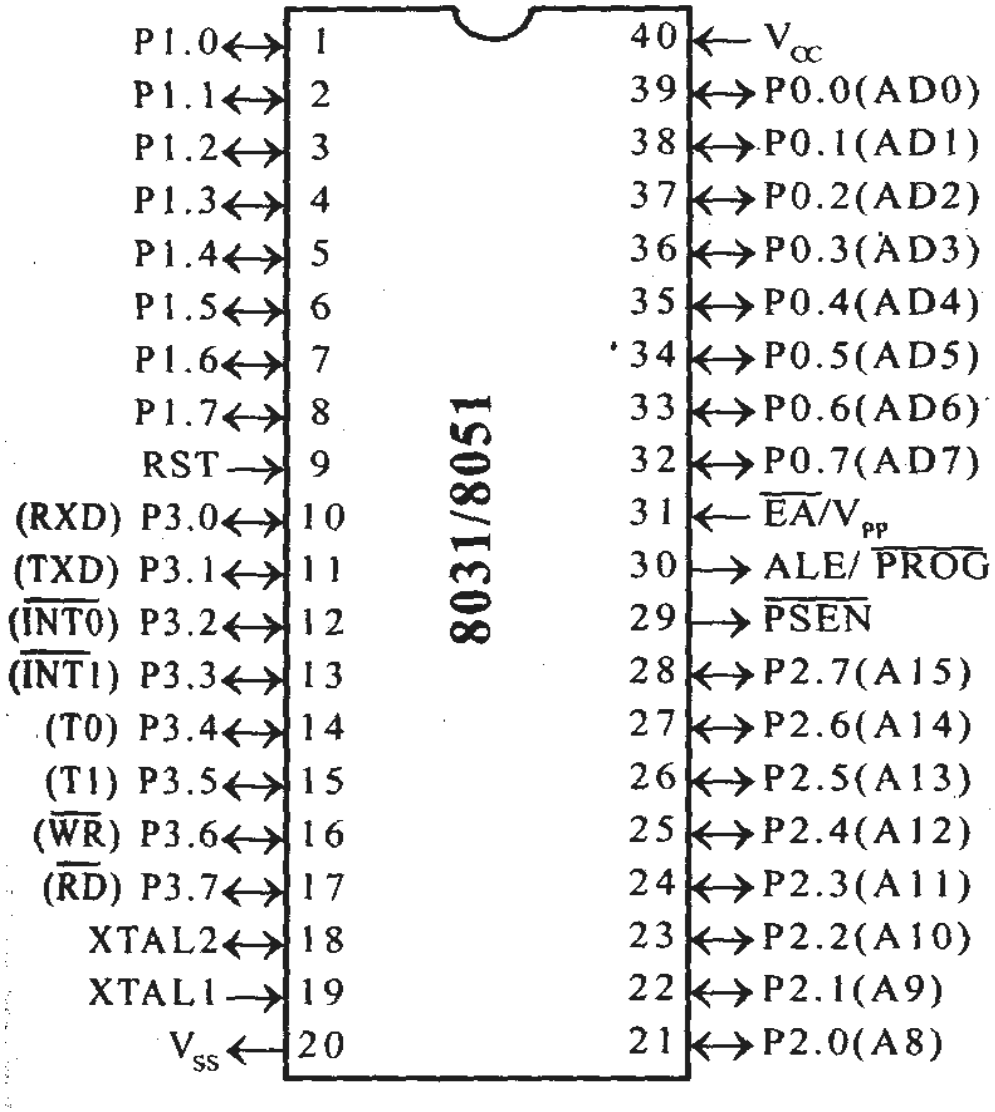


- Each pin of Port-3 can be individually programmed for I/O operation or for alternate function.

- The alternate function can be activated only if the corresponding latch has been written to '1'.
- To use the port as input port, '1' should be written to the latch.
- Alternate functions of Port-3 pins:

P3.0	RxD
P3.1	TxD
P3.2	$\overline{INT0}$
P3.3	$\overline{INT1}$
P3.4	T0
P3.5	T1
P3.6	$\overline{WR}$
P3.7	$\overline{RD}$

3.8 PIN DETAILS OF 8051



Ports: (pin 1 to 8, pin 10 to 17, pin 21 to 28 and pin 32 to 39)

- The 8031/8051 microcontroller has 32 I/O pins and they are organized as four numbers of 8-bit parallel port.
- The ports are denoted as port-0, port-1, port-2 and port-3. Each port can be used as either 8-bit parallel port or 8 numbers of 1-bit ports.
- Port-1 can be used only for I/O operation
- When external memory is employed, the port-0 function as multiplexed low byte address or data lines, and port-2 function as high byte address lines. Therefore for accessing external memory the microcontroller uses 16-bit address and access the memory in bytes.

Port pins	Alternate signal	Description
P0.7 - P0.0	AD7 - AD0	Multiplexed low byte address/data.
P2.7 - P2.0	A15 - A8	High byte address
P3.7	$\overline{RD}$	External memory read control signal
P3.6	$\overline{WR}$	External memory write control signal
P3.5	T1	External input to timer 1
P3.4	T0	External input to timer 0
P3.3	$\overline{INT1}$	External interrupt 1
P3.2	$\overline{INT0}$	External interrupt 0
P3.1	TxD	Serial data output
P3.0	RxD	Serial data input

Alternate functions of port pins

$\overline{PSEN}$

- The signal $\overline{PSEN}$ is used as read control/enable for program memory.

$\overline{RD}$ and $\overline{WR}$

- The port pin P3.7 function as read control and the port pin P3.6 function as write control for data memory.

ALE

- ALE is used to demultiplex the low byte address or data using an external latch.

$\overline{EA}$ /Vpp

- When the microcontroller access program from external memory, then this pin is low.
- When the microcontroller access program from internal memory, then this pin is high. At that time this pin is used to supply programming voltage to EPROM.

XTAL 1 AND XTAL2:

- The XTAL 1 and XTAL2 pins are provided for external quartz crystal connection, in order to generate the required clock for the microcontroller. The maximum frequency of quartz crystal that can be connected to 8031/8051 microcontroller is 12 MHz.

$\overline{RST}$:

- The $\overline{RST}$ signal is used to reset the microcontroller in order to bring the controller to a known state.