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VLSI CIRCUIT DESIGN

2nd Module

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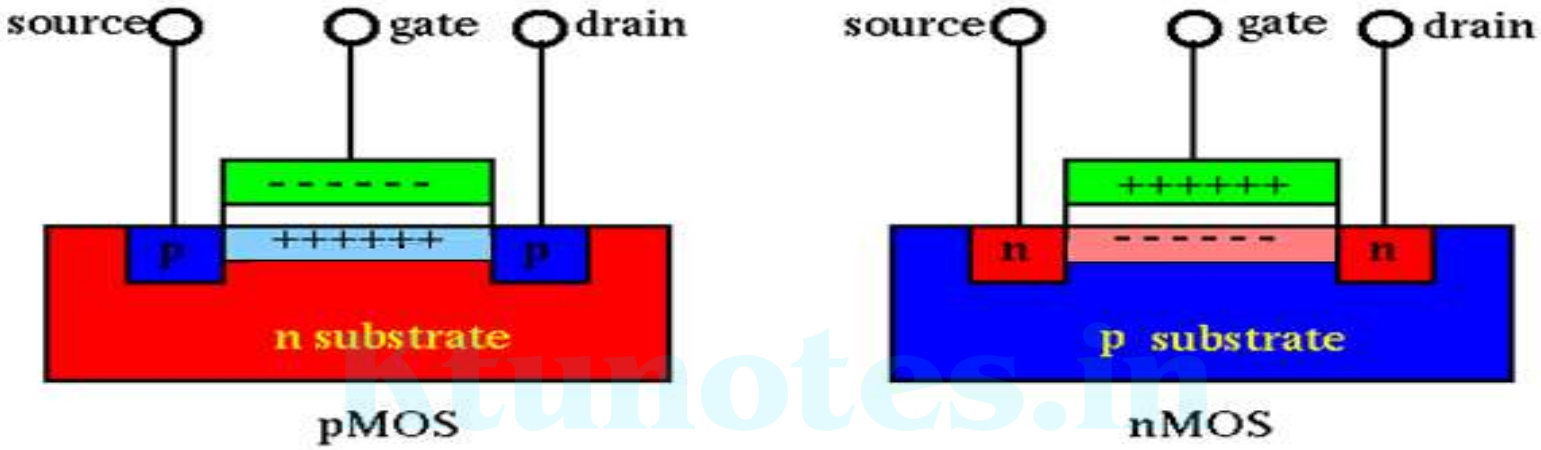
MOSFET
NMOS and PMOS



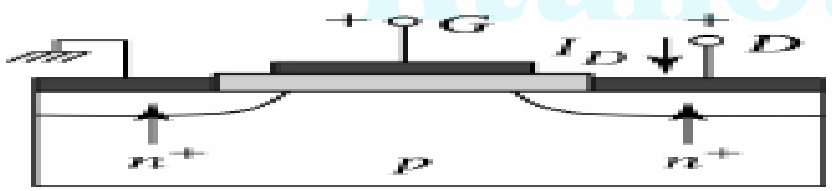
- NMOSFET: p-substrate (n-channel), n+ S & D
- PMOSFET: n-substrate (p-channel), p+ S & D

MOSFET Types

1).Enhancement –mode mosfet
2).Depletion –Mode Mosfet

1).Enhancement –mode mosfet

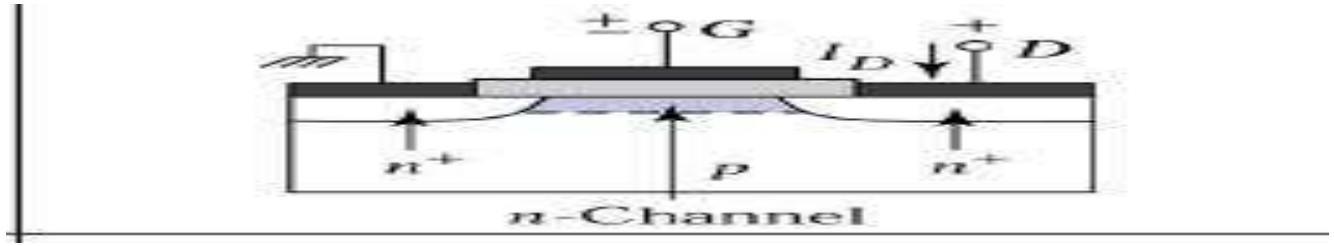
nMOS enhancement mode transistor



– Equivalent to a normally off switch
– We have to induce channel
– Commonly used

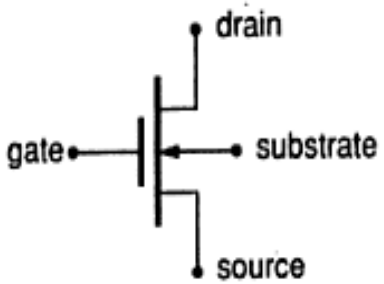
2.Depletion –mode mosfet

nMOS depletion mode transistor

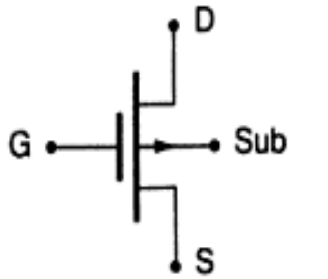


- Equivalent to a normally on switch
- By implanting suitable impurity in the region between source and drain during manufacture
- Channel is already present
- Inorder to control the current flow a negative voltage is applied at the gate

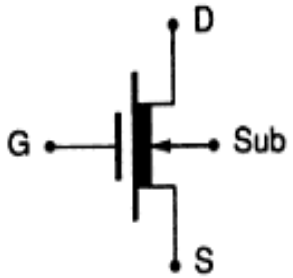
symbol



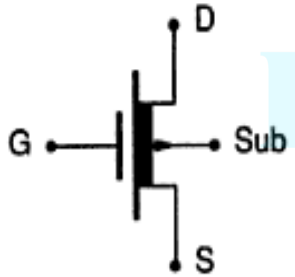
n-channel enhancement



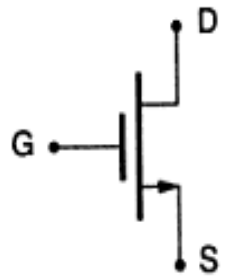
p-channel enhancement



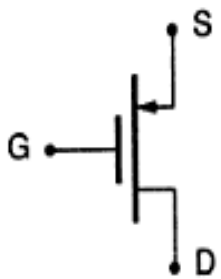
n-channel depletion



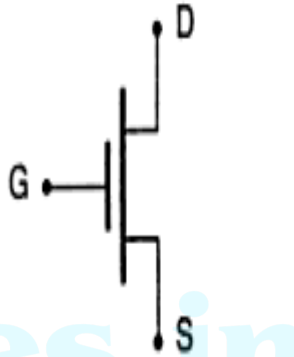
p-channel depletion



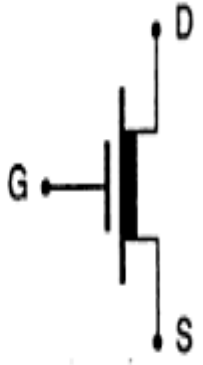
alternate n-channel notation



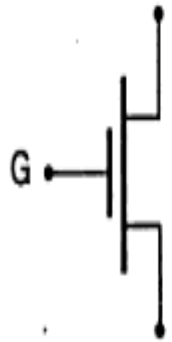
alternate p-channel notation



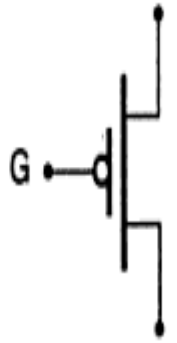
simplified enhancement



simplified depletion

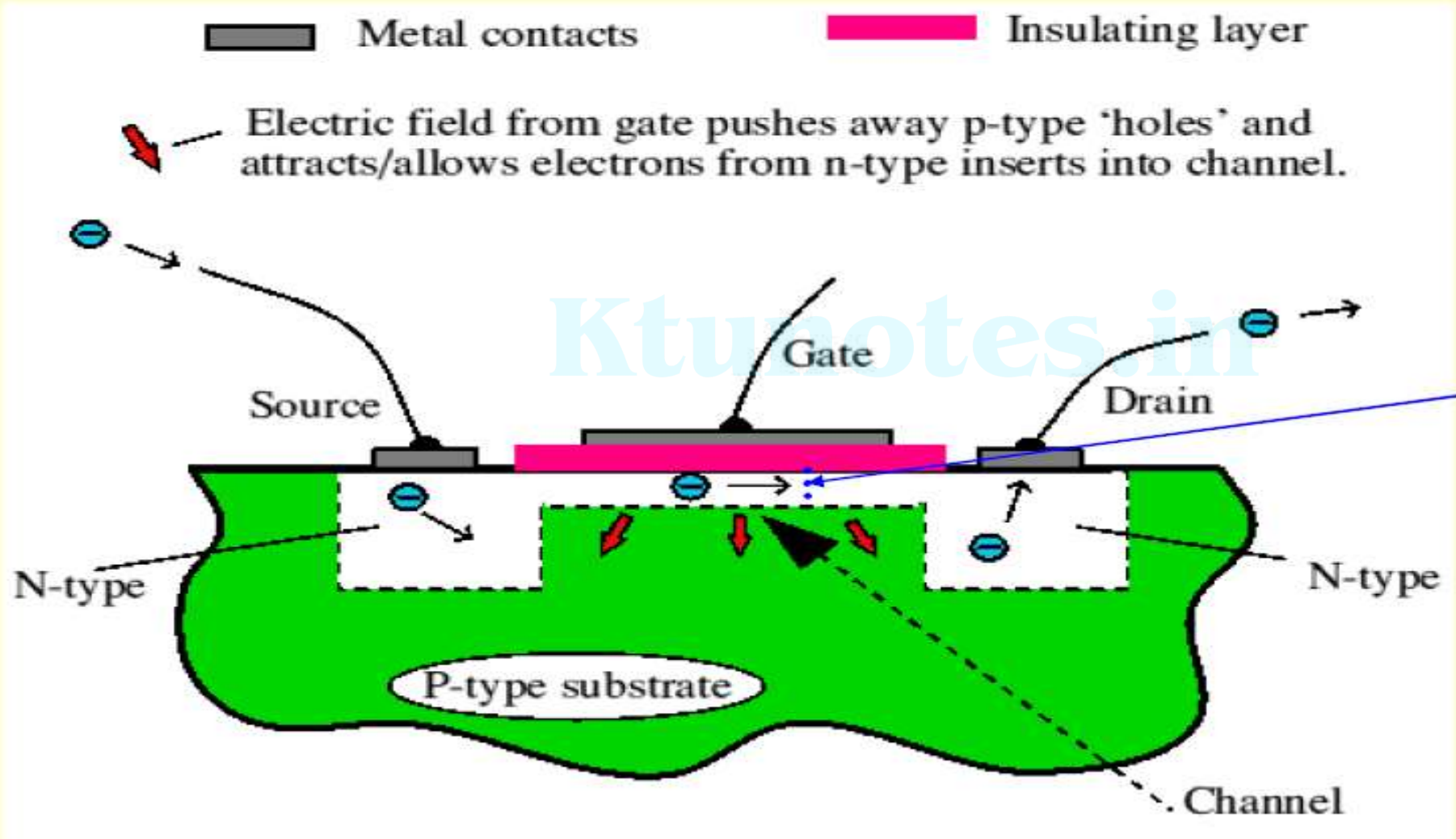


simplified n-channel



simplified p-channel

Basic MOSFET (n-channel) Enhancement mode



When VGS = 0, the n-channel is very thin and channel width enhances with

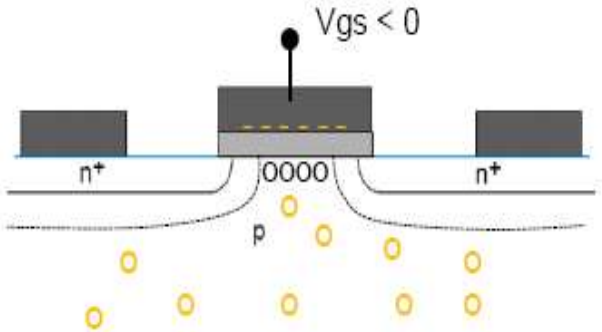
+ V_{GS}

- Channel width enhancement with +VGS
- The gate electrode is placed on top of a very thin insulating layer.
- There are a pair of small n-type regions just under the drain & source electrodes.
- If apply a +ve voltage to gate, will push away the ‘holes’ inside the p-type substrate and attracts the moveable electrons in the n-type regions under the source & drain electrodes

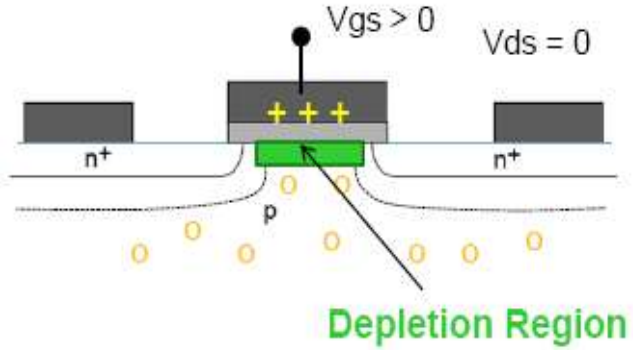
- Increasing the +ve gate voltage pushes the p-type holes further away and enlarges the thickness of the created channel.
- As a result increases the amount of current which can go from source to drain —this is why this kind of transistor is called an *enhancement mode MOSFET.*

N-MOS System under external Bias

- When Vg<0
  - Negative potential at the gate
  - Holes are attracted towards the surface
  - Electrons are repelled deep into the substrate
  - This is called as accumulation

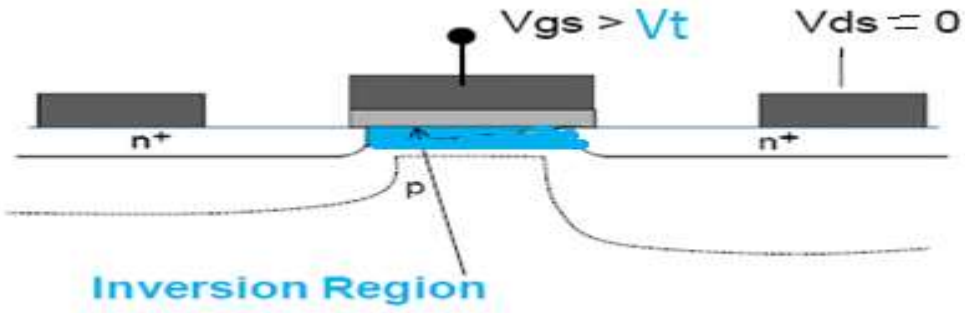


- When Vg>0
  - Slight positive potential at the gate
  - Holes are repelled into the substrate by leaving negatively charged fixed acceptor ions
  - Depletion region is created
  - No mobile charges at the si-sio2 interface
  - This is called as depletion



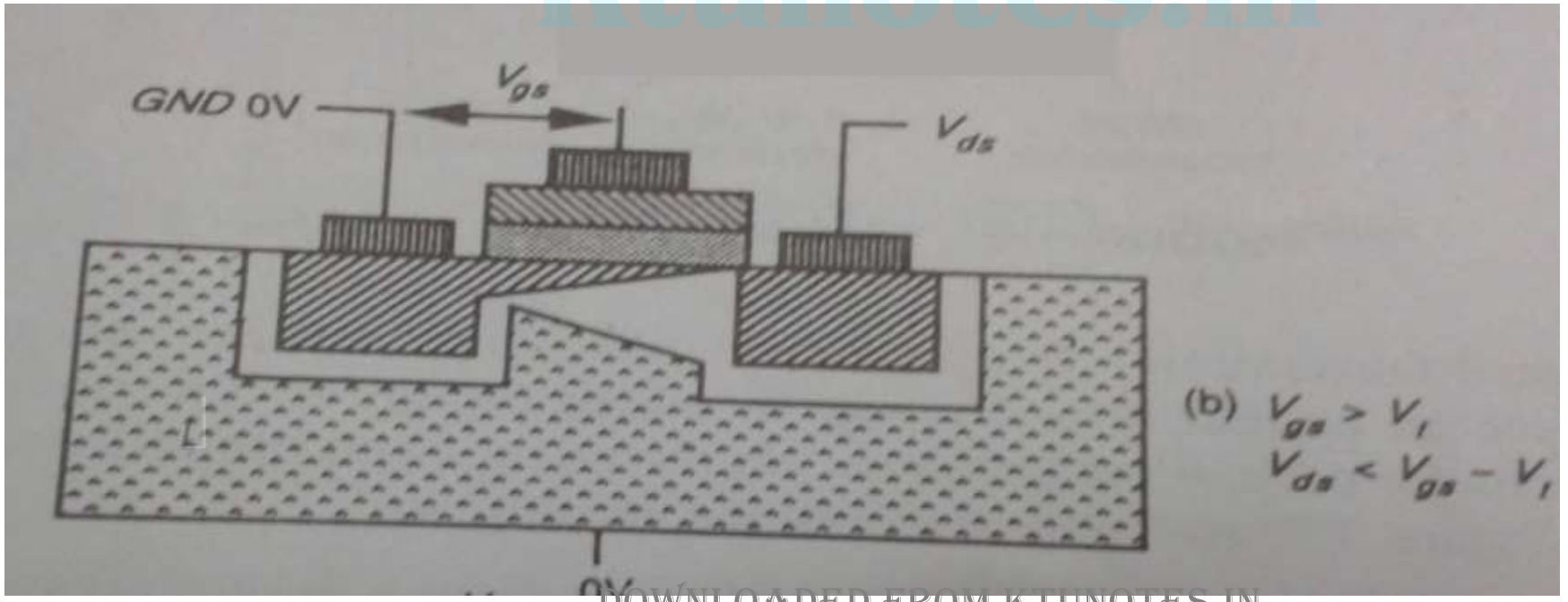
N-MOS System under external Bias

- When Vg>0
  - Here a large positive potential applied at the gate
  - Negative ions alone cannot compensate the positive charge on the Gate
  - So Electrons are attracted toward the surface from substrate and N+ regions
  - So here an inversion region(opposite to p-substrate) is formed. It is called as n-channel
  - This is called as Inversion
- This Gate Voltage is called as Threshold Voltage Vt

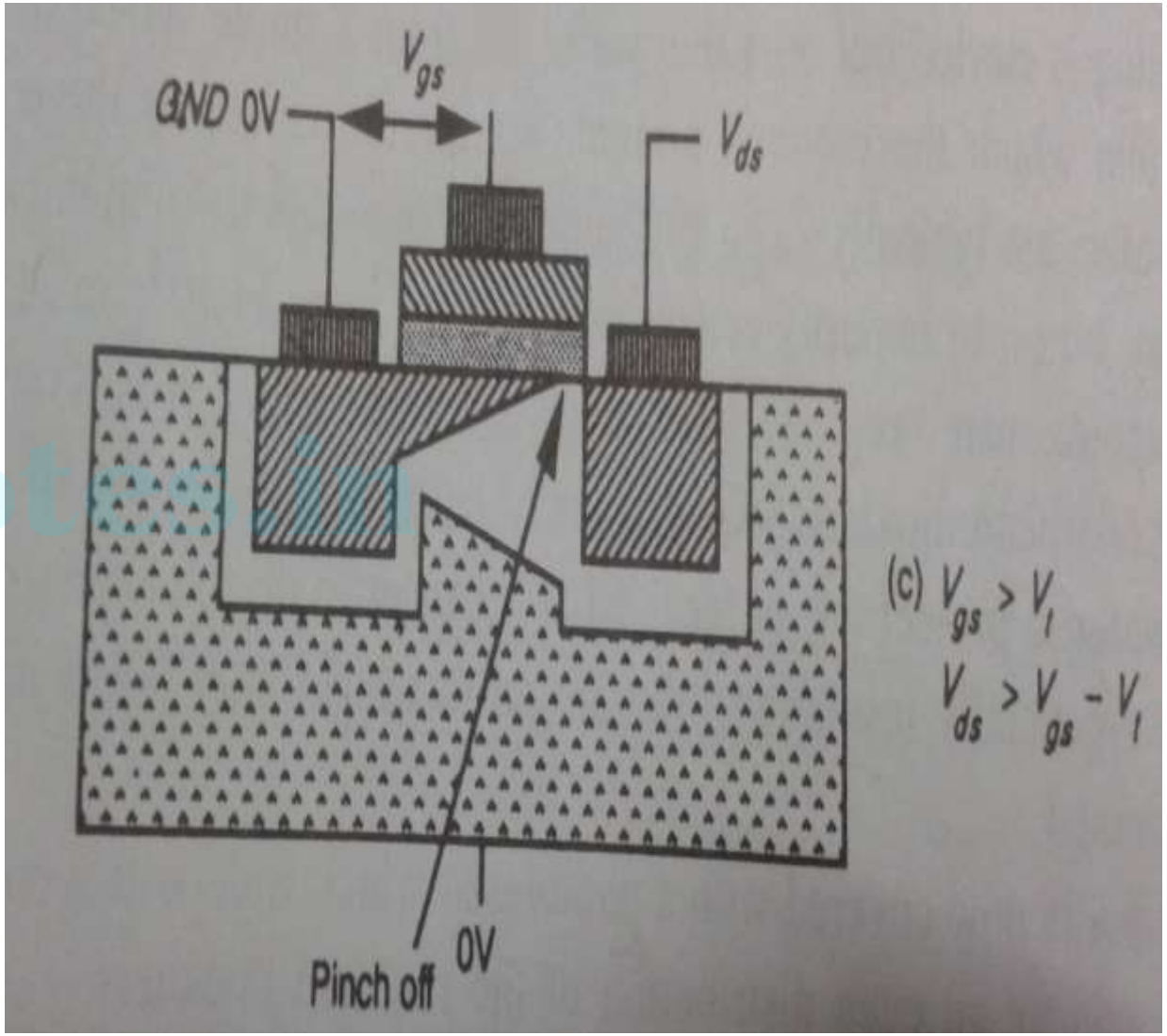


- Here channel established ,but no current flow between source and drain

- current flows in the channel by applying a voltage Vds between source and drain,this corresponds IR drop = Vds along the channel
- This results voltage between gate and channel varying with distance along the channel with the voltage being a maximum of Vgs at the source end
- since the effective gate voltage is Vg=Vgs-Vt , there will be voltage available to invert channel at drain end so long as Vgs-Vt>=Vds
- For all voltages Vds<Vgs-Vt, the device is in **non-saturated** region of operation



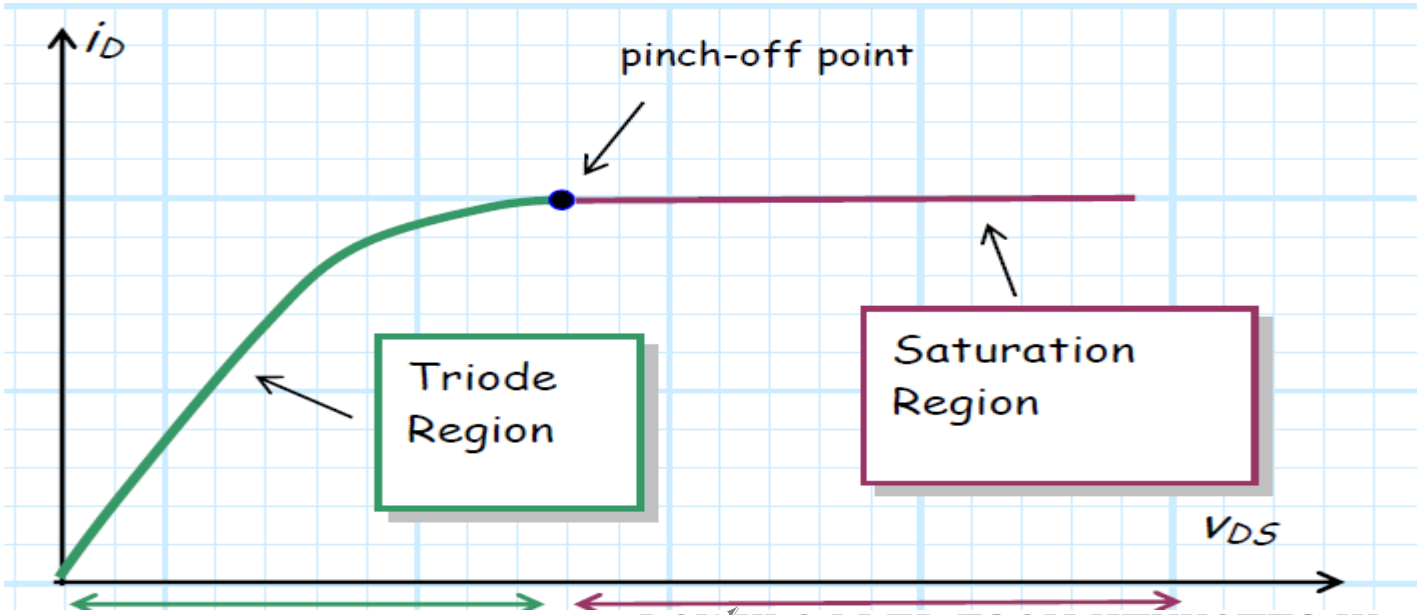
- Vds >=Vgs-Vt,in this case an IR drop =Vgs-Vt take place over less than the whole length of the channel
- over part of the channel, near the drain, there is insufficient electric field available to give rise to an inversion layer to create the channel.the channel is there for pinched off.
- Diffusion current complete the path from source to drain in this case, causing the channel to exhibit a high resistance and and behave as a constant current source
- This region is known as **saturation**



1**. Cutoff** – When Vgs-Vt <0 , no channel is induced (no inversion layer is created), and so Id=0. We call this mode **CUTOFF**.

2. **Triode** - When an induced channel is present (i.e., Vgs-Vt >0), but the value of Vds is not large enough to pinch-off this channel, the NMOS is said to be in **TRIODE** mode.

3. **Saturation** - When an induced channel is present (i.e.,Vgs-Vt >0), and the value of Vds is large enough to pinch off this channel, the NMOS is said to be in **SATURATION** mode.



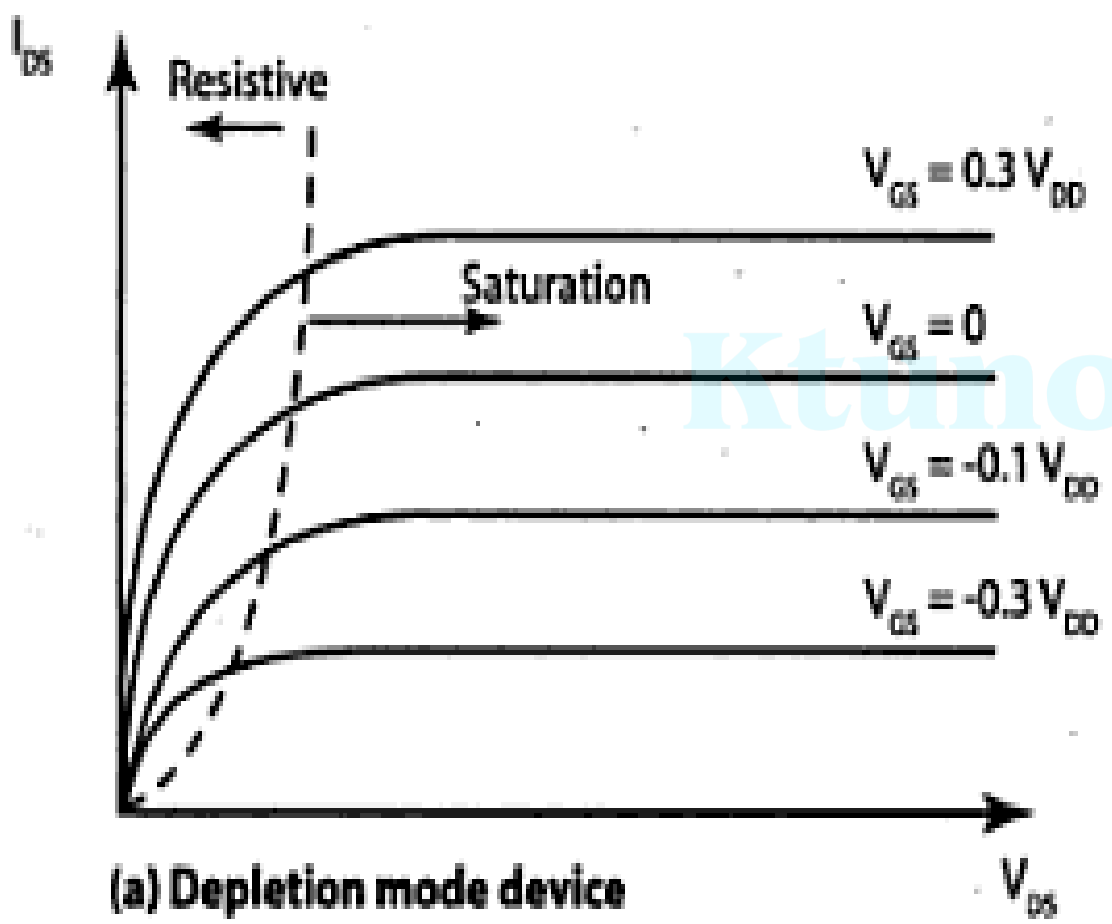
$$\therefore I_{DS} = K\frac{W}{L}\left\{(V_{GS} - V_t)V_{DS} - \frac{V_{DS}^2}{2}\right\}$$

Active region

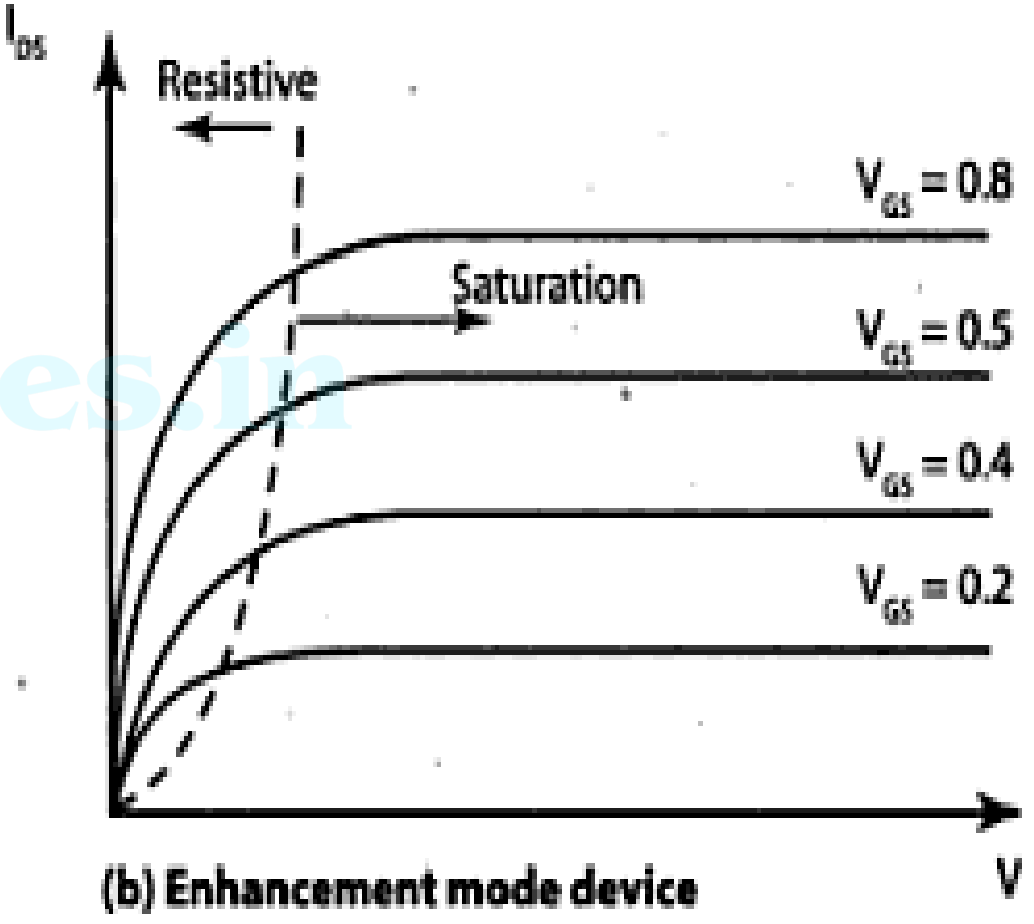
$$I_{DS} = K\frac{W}{L}\frac{(V_{GS} - V_t)^2}{2}$$

Saturated region

MOS Transistor Characteristics



(a) Depletion mode device



(b) Enhancement mode device

MOS Inverter : Static Characteristics

-

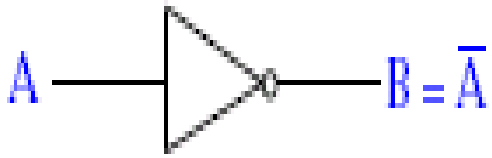
Introduction

- **Inverter is most fundamental logic gate that uses single input.**
- **The basic principles employed in design and analysis of MOS inverters can be directly applied on more complex logic circuits.**
- **Therefore inverter design forms basis for digital circuits.**
- **First we start with DC Characteristics.**

What do you understand by DC response of the circuit?

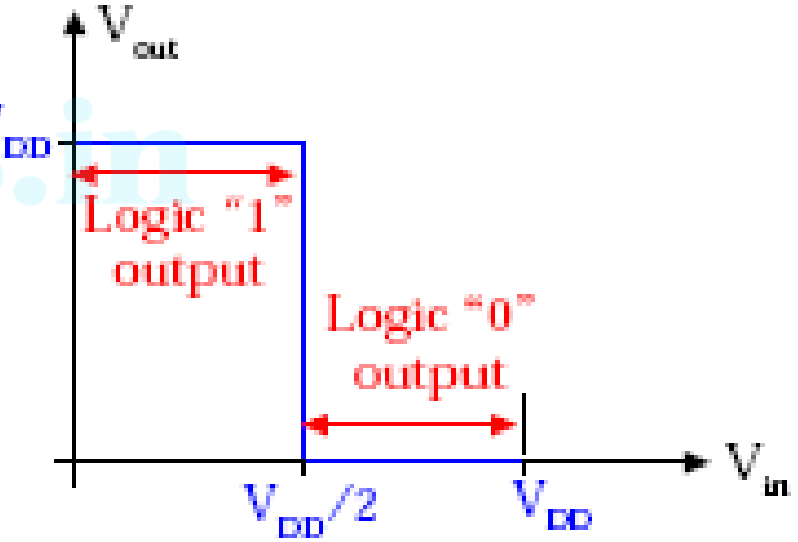
Introduction (contd.)

The DC response is Ultra Low Frequency response of the Circuit.
– When you are at a logic low or high before switching it is a DC condition.



A	B
0	1
1	0

Fig. 1



IDEAL INVERTER VOLTAGE TRANSFER CHARTERISTIC (VTC)

Fig. 2

- The logic symbol and the truth table of the ideal inverter are shown in Fig. 1.
- In MOS inverter circuits, both the input variable A and the output variable B are represented by node voltages, referenced to the ground potential.
- Using positive logic convention, the Boolean (or logic) value of "1" can be represented by a high voltage of VDD, and the Boolean (or logic) value of "0" can be represented by a low voltage of 0.
- The DC voltage transfer characteristic (VTC) of the ideal inverter circuit is shown in Fig. 2.
- The voltage Vth is called the inverter threshold voltage. Note that for any input voltage between 0 and Vth = VDD/2 , the output voltage is equal to VDD (logic"1").
- The output switches from VDD to 0 when the input is equal to Vth

- For any input voltage between Vth and, VDD the output voltage assumes a value of 0 (logic "0"). Thus, an input voltage 0 < Vin< Vth is interpreted by this ideal inverter as a logic "0," while an input voltage Vth < Vin < VDD is interpreted as a logic " 1."
- The DC characteristics of actual inverter circuits will obviously differ in various degrees from the ideal characteristic shown in Fig. 2.

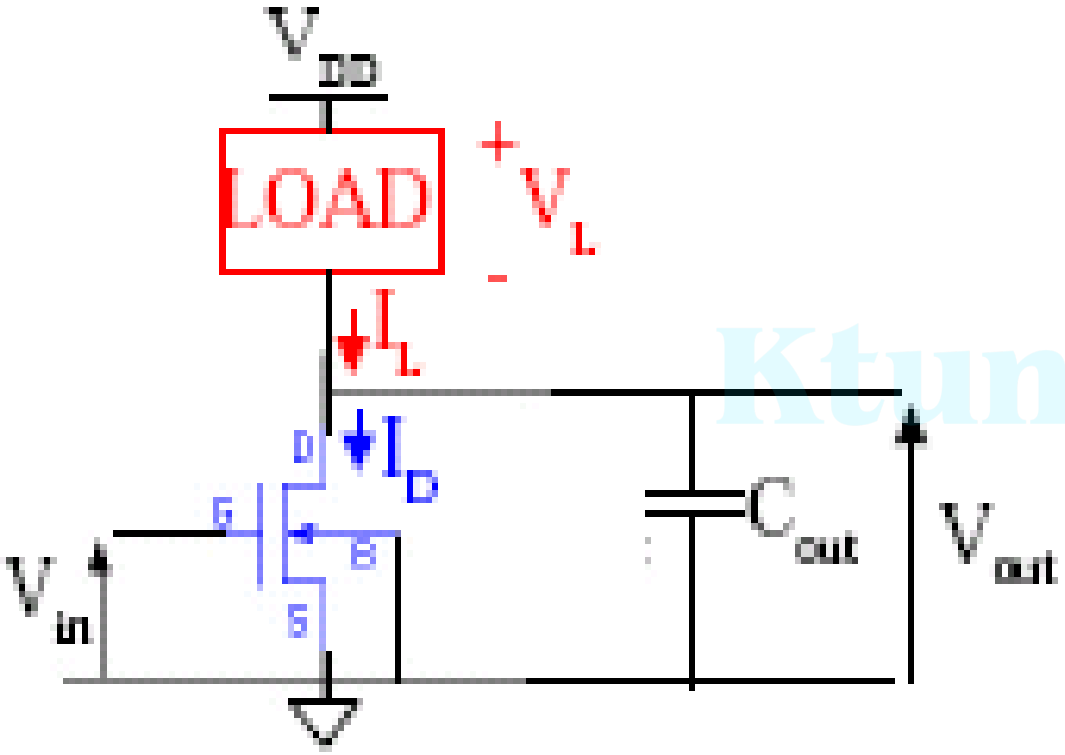


Fig. 3

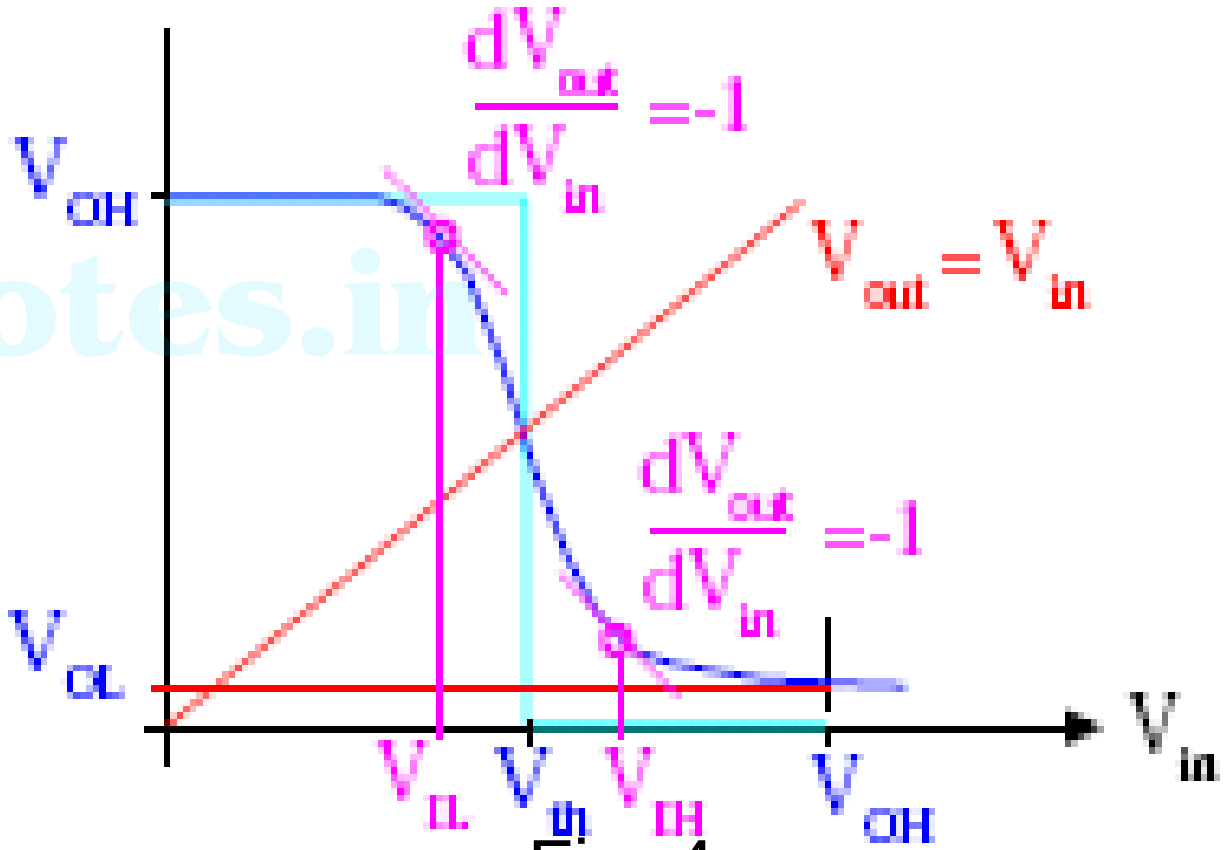


Fig. 4

- Figure 3 shows the generalized circuit structure of an nMOS inverter. The input voltage of the inverter circuit is also the gate-to-source voltage of the nMOS transistor (Vin = V_{GS}), while the output voltage of the circuit is equal to the drain-to-source voltage (Vout= V_{DS}).
- The source and the substrate terminals of the nMOS transistor, also called the driver transistor, are connected to ground potential; hence, the source-to-substrate voltage is V_{SB} = 0.
- In this generalized representation, the load device is represented as a two-terminal circuit element with terminal current IL and terminal voltage VL(IL).
- One terminal of the load device is connected to the drain of the n-channel MOSFET, while the other terminal is connected to VDD, the power supply voltage

- The output terminal of the inverter shown in Fig.3 is connected to the input of another MOS inverter.
- Consequently, the next circuit seen by the output node can be represented as a lumped capacitance, Cout.
- Since the DC gate current of an MOS transistor is negligible for all practical purposes, there will be no current flow into or out of the input and output terminals of the inverter in DC steady state.
- Applying Kirchhoff's Current Law (KCL) to this simple circuit, we see that the load current is always equal to the nMOS drain current.
- $I_D (V_{in}, V_{out}) = I_L (V_L)$ ..... (1)

- The voltage transfer characteristic describing V as a function of Vin under DC conditions can then be found by analytically solving (1) for various input voltage values.
- The typical VTC of a realistic nMOS inverter is shown in Fig. 4.
- Upon examination, we can identify a number of important properties of this DC transfer characteristic.
- For very low input voltage levels, the output voltage V is equal to the high value of VOH (output high voltage). In this case, the driver nMOS transistor is in cut-off, and hence, does not conduct any current.
- Consequently, the voltage drop across the load device is very small in magnitude, and the output voltage level is high.

- As the input voltage V increases, the driver transistor starts conducting a certain drain current, and the output voltage eventually starts to decrease.
- Notice that this drop in the output voltage level does not occur abruptly, such as the vertical drop assumed for the ideal inverter VTC, but rather gradually and with a finite slope.
- We identify two critical voltage points on this curve, where the slope of the Vt(Vin) characteristic becomes equal to -1, i.e.,

$$dVout/dVin = -1 \qquad \text{..... (2)}$$

- The smaller input voltage value satisfying this condition is called the input low voltage V_{IL} and the larger input voltage satisfying this condition is called the input high voltage V_{IH}.
- Both of these voltages play significant roles in determining the noise margins of the inverter circuit.
- As the input voltage is further increased, the output voltage continues to drop and reaches a value of V_{OL} (output low voltage) when the input voltage is equal to V_{OH}.
- The inverter threshold voltage Vth, which is considered as the transition voltage, is defined as the point where Vin = Vout on the VTC.

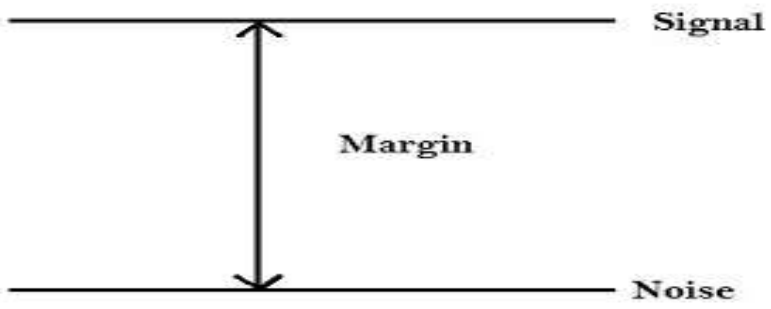
- There are five critical voltage points determine DC Characteristics and Noise margins :
  - V_{IL} : Maximum input voltage which can be interpreted as logic "0"
  - VIH : Minimum input voltage which can be interpreted as logic " 1"
  - VOL : Minimum output voltage when the output level is logic "0"
  - VOH : Maximum output voltage when the output level is logic " 1"

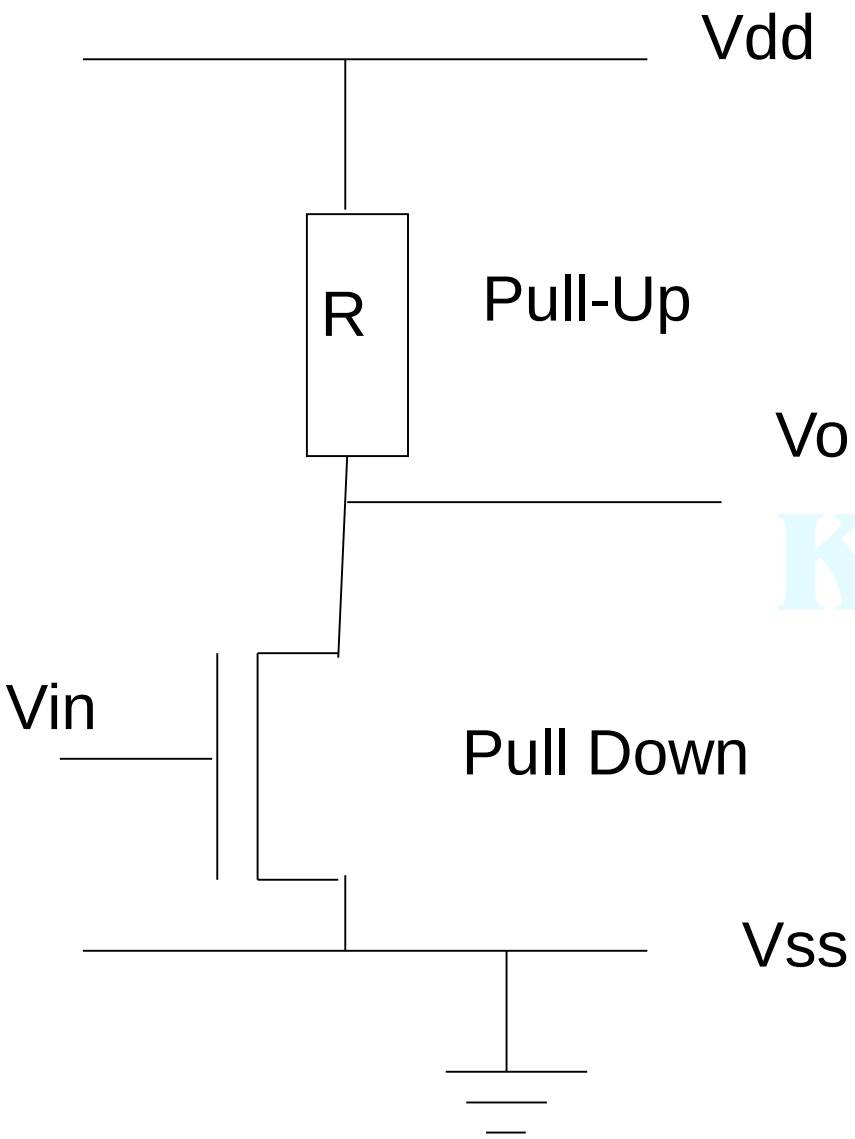
Noise Immunity and Noise Margin

•Noise margin is the amount of noise that a MOS circuit could withstand without compromising the operation of circuit.

• Noise margin does makes sure that any signal which is logic ‘1’ with finite noise added to it, is still recognized as logic ‘1’ and not logic ‘0’.

• It is basically the difference between signal value and the noise value. Refer to the diagram below.





Basic Inverter: Transistor with source connected to ground and a load resistor connected from the drain to the positive Supply rail

Output is taken from the drain and control input connected between gate and ground

Resistors are not easily formed in silicon - they occupy too much area

Transistors can be used as the pull-down device

Resistive-Load Inverter

The basic structure of the resistive-load inverter circuit is shown in Fig. An enhancement-type nMOS transistor acts as the driver device. The load consists of a simple linear resistor, RL. The power supply voltage of this circuit is VDD.

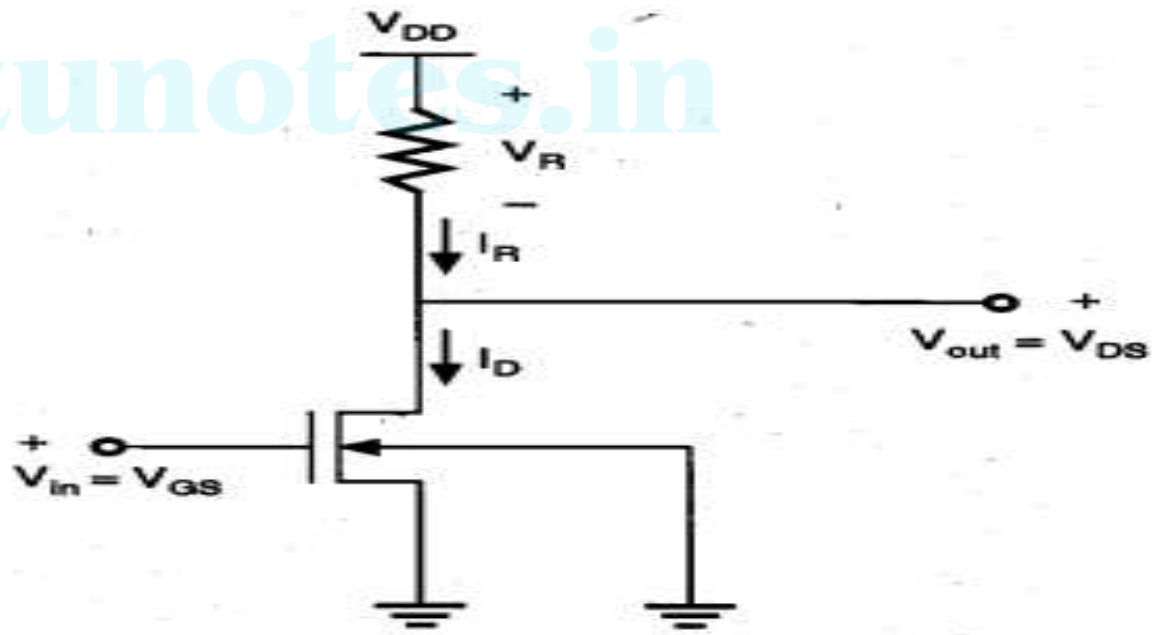


Figure **Resistive-load inverter circuit.**

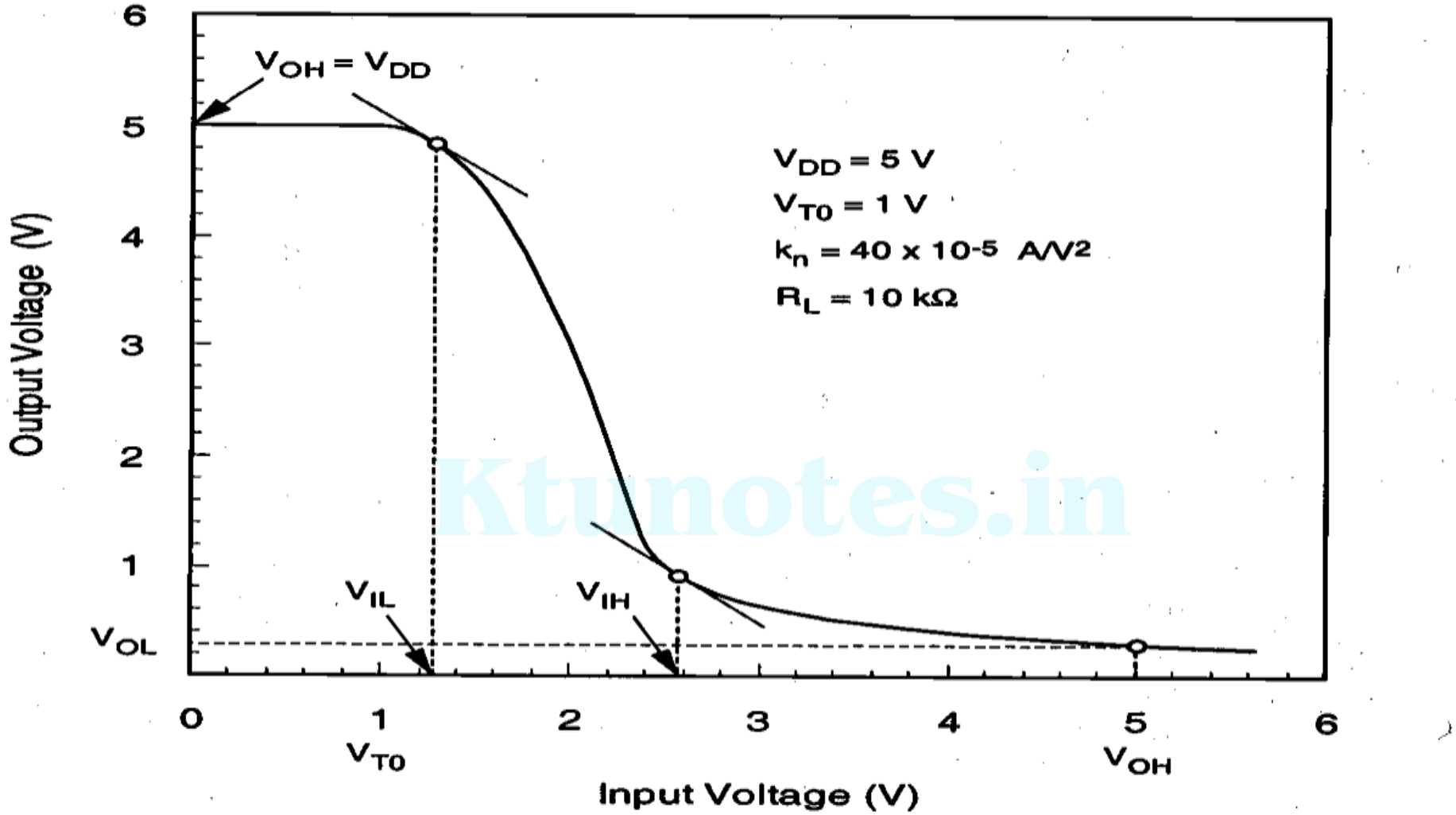
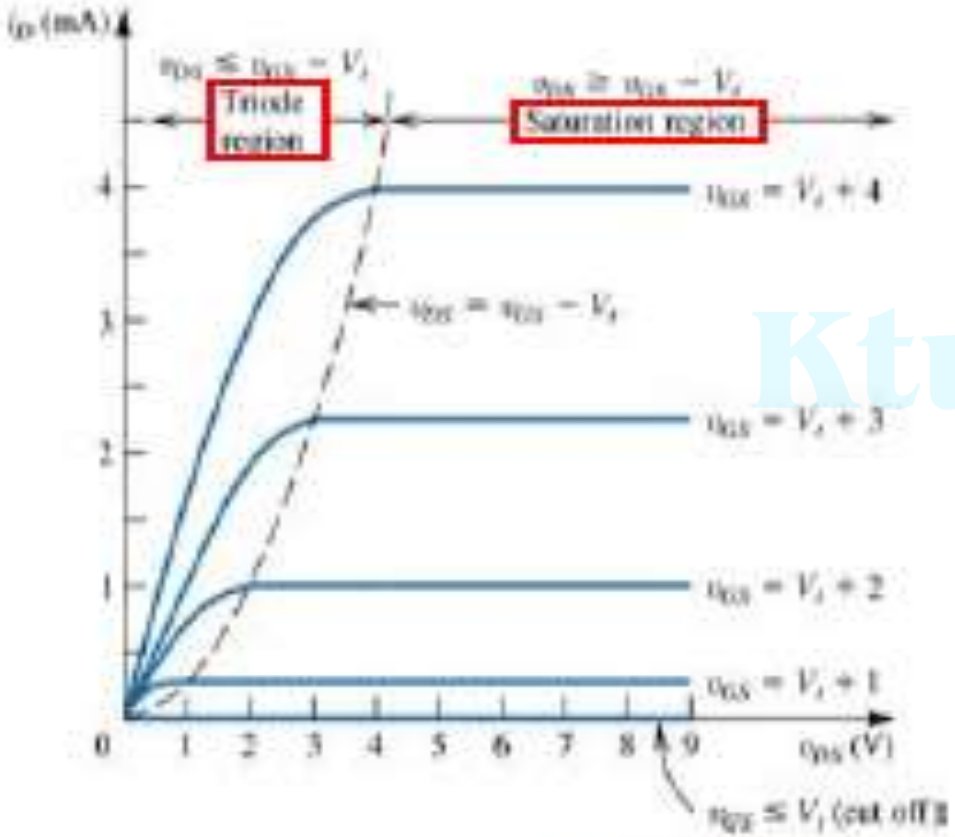
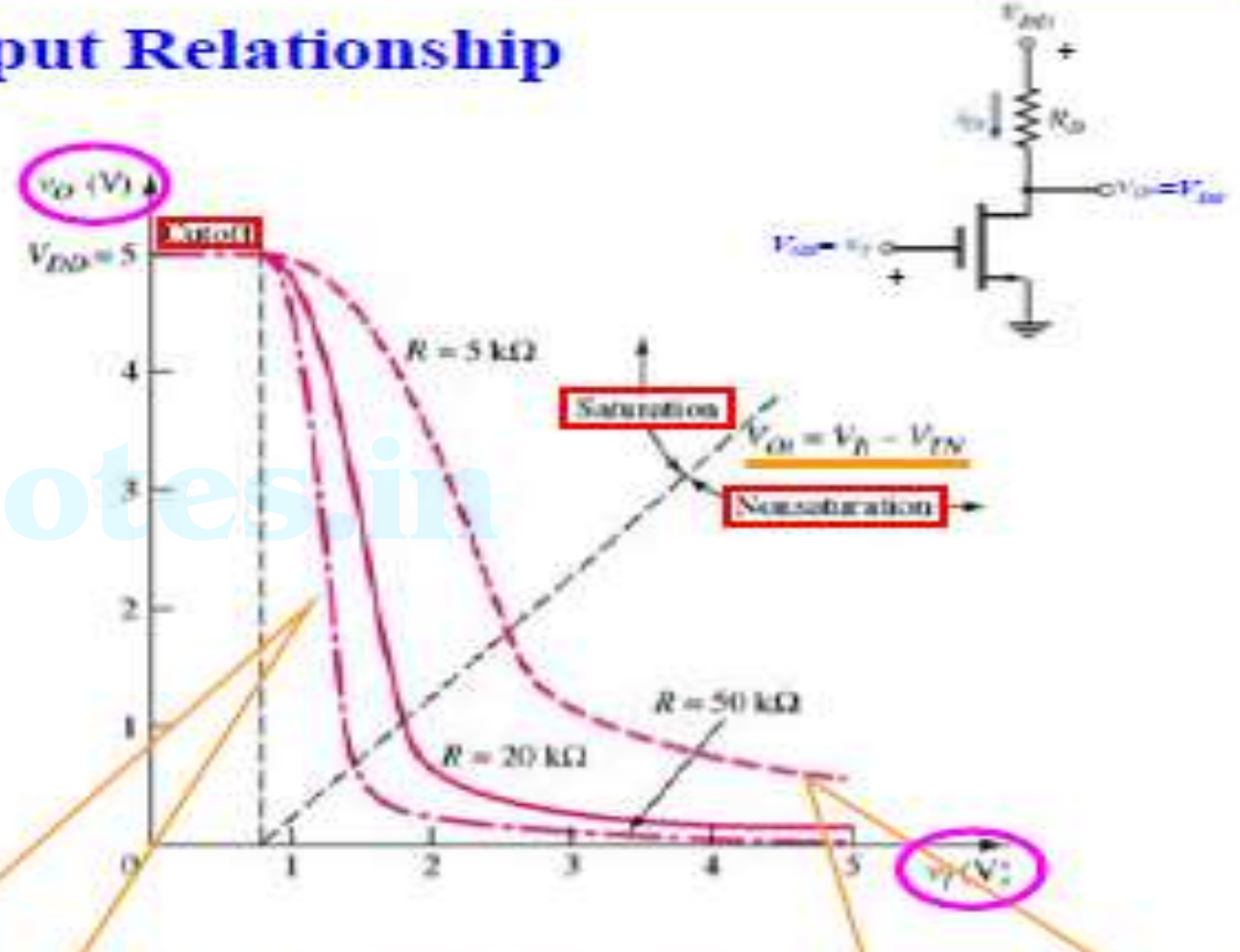


Figure 5.8. **Typical VTC of a resistive-load inverter circuit. Important design parameters of the circuit are shown in the inset.**

NMOS Inverter with Resister Load

Input-Output Relationship



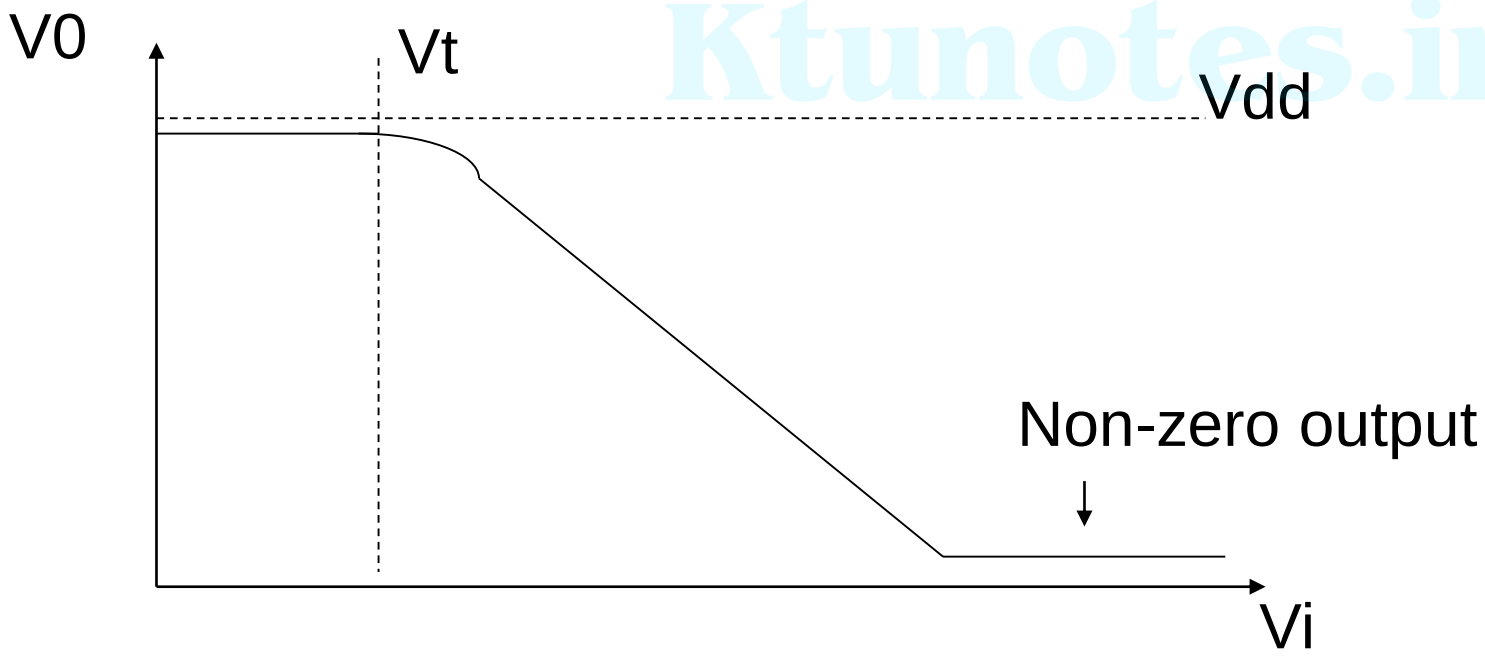


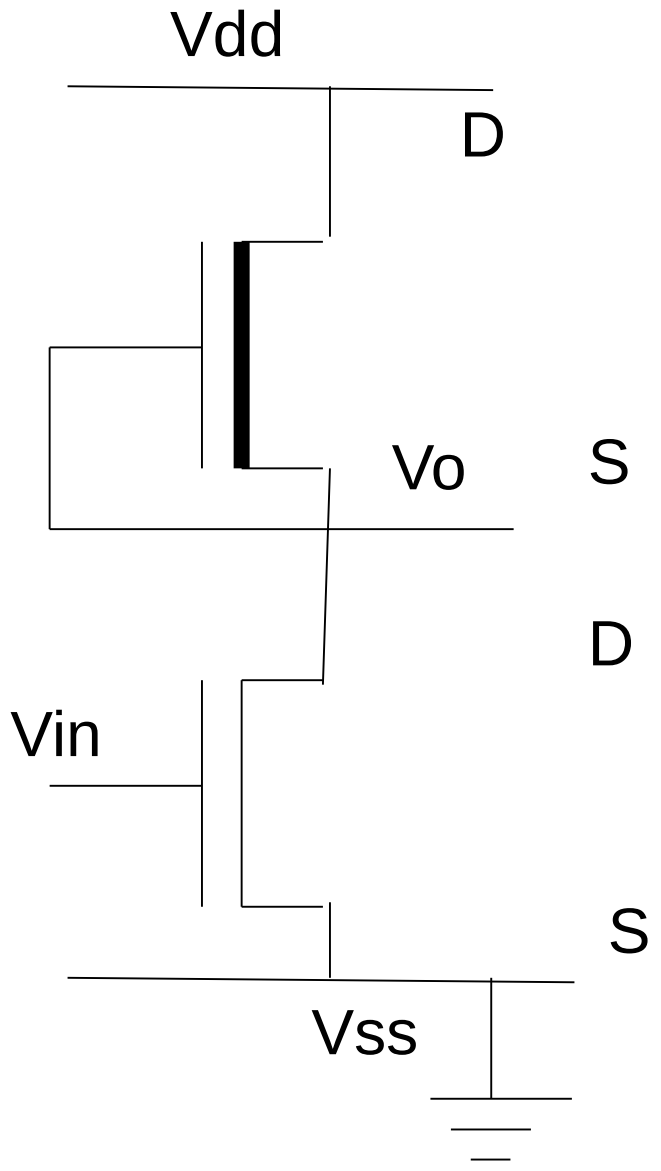
The sharpness of the transition region increases with increasing load resistance.

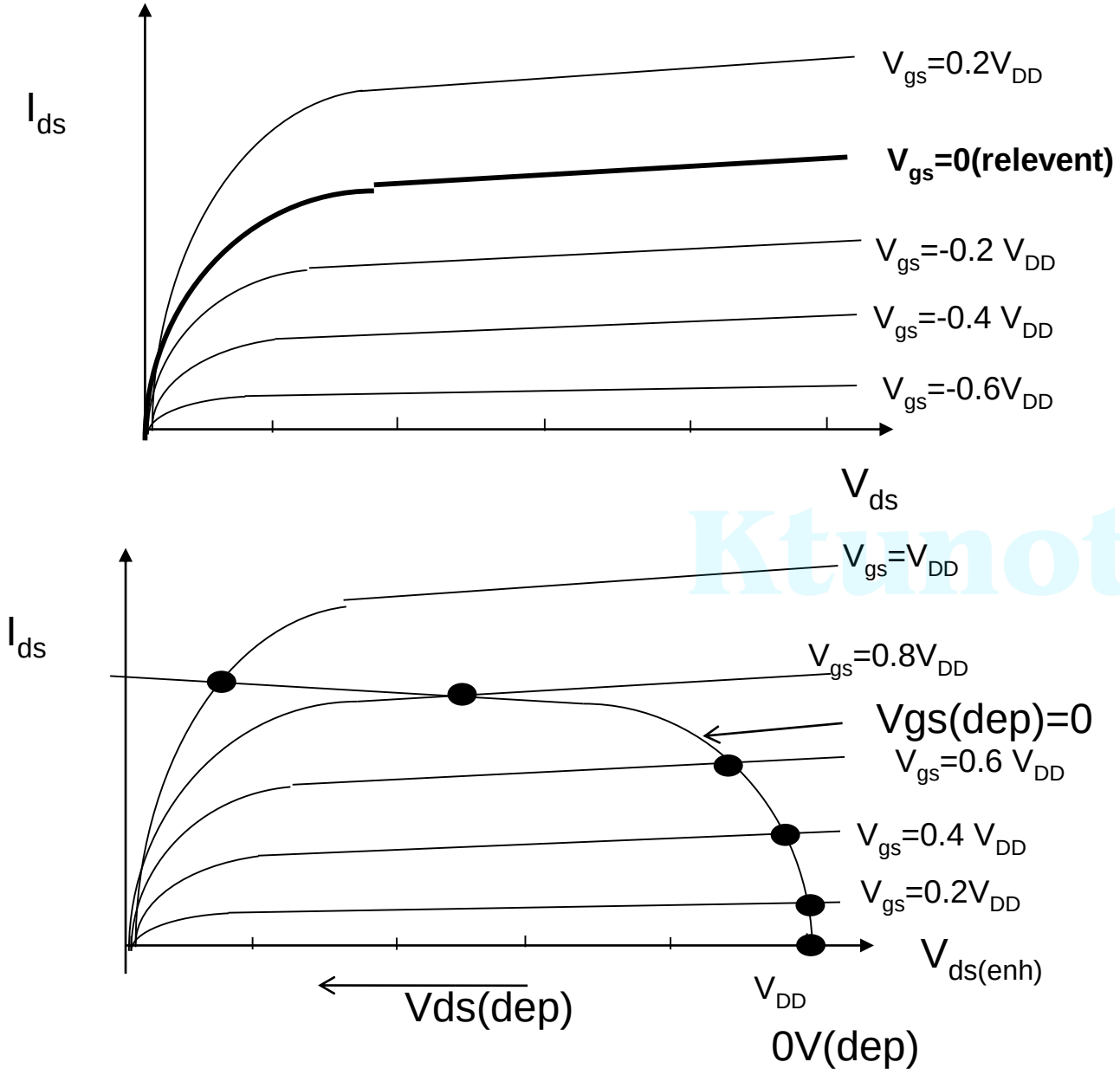
The minimum output voltage, or the logic 0 level, for a high input decreases with increasing load resistance.

2).NMOS Depletion Mode Transistor Pull - Up

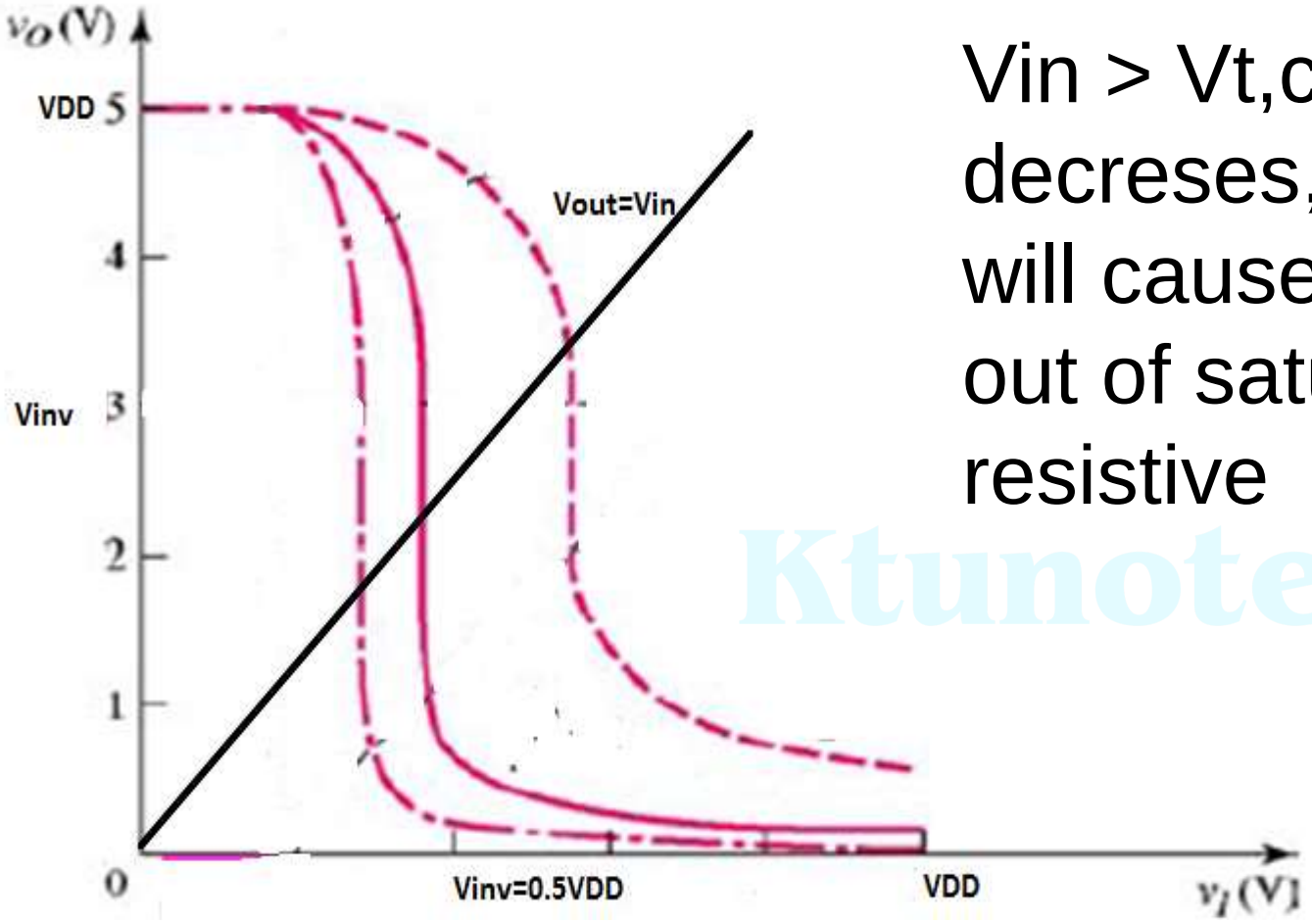
- Pull-Up is always on – Vgs = 0; depletion
- Pull-Down turns on when Vin > Vt
- With no current drawn from outputs, Ids for both transistors is equal





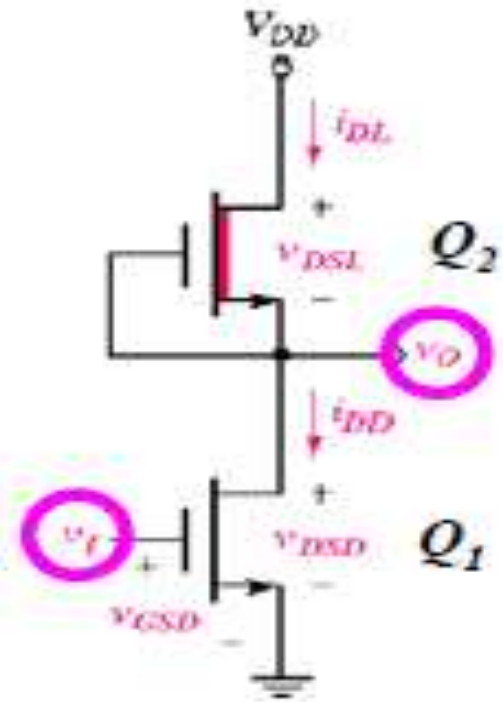


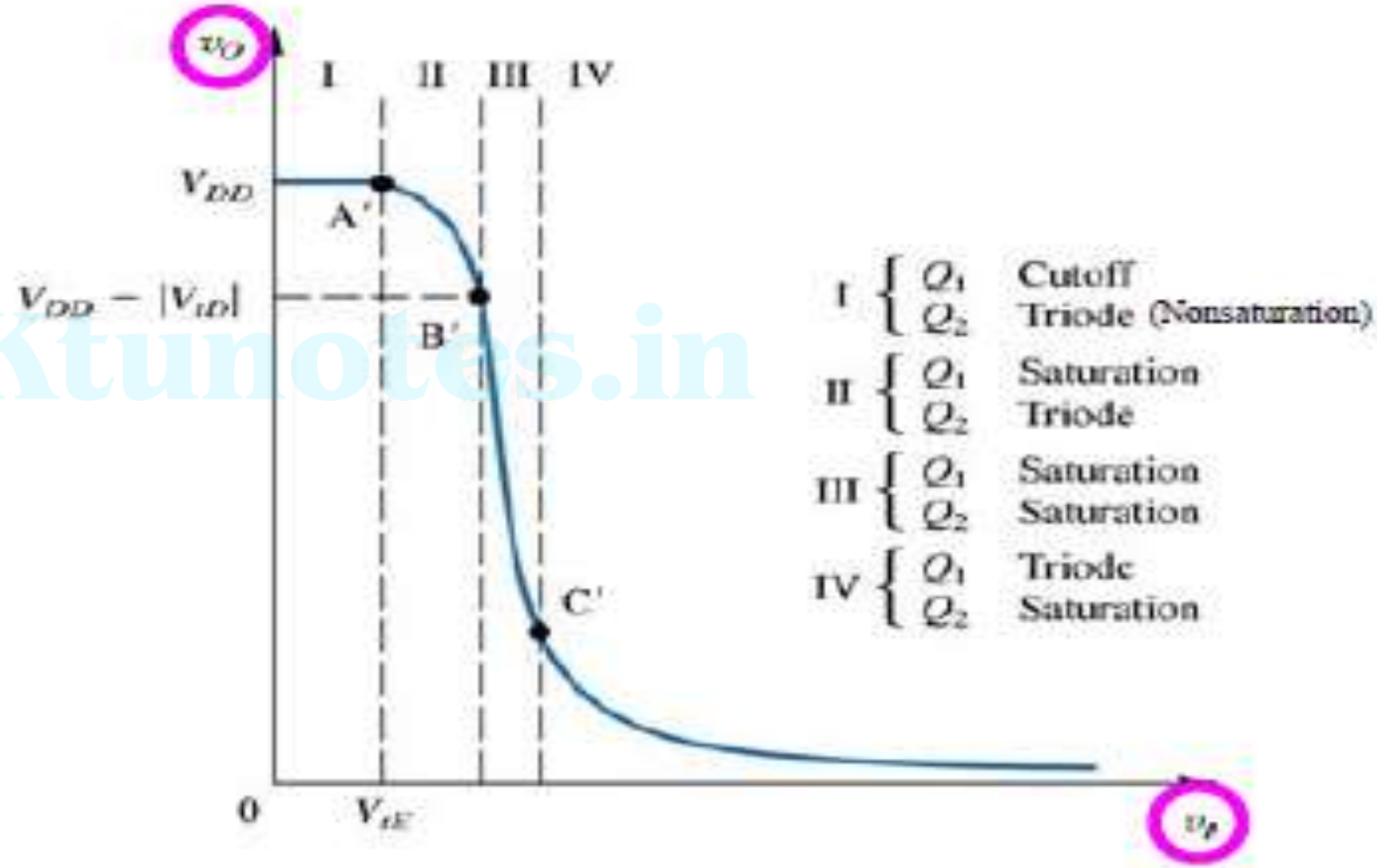
- To obtain inverter transfer characteristics,we superimpose vgs=0 depletion mode characteristicscurves on family of curves for enhancement mode device
- Maximum voltage corresponding to enhancement mode device corresponds to minimum voltage across the depletion mode transistor



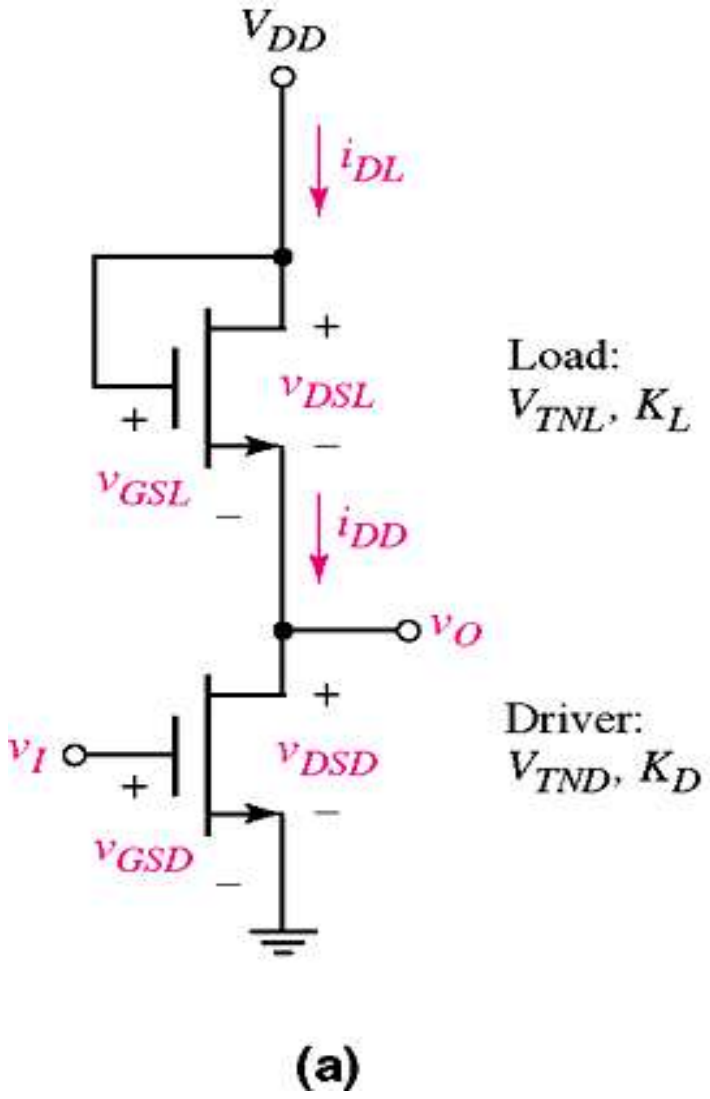
Vin > Vt,current begins to flow –Vout decreses,subsequant increse in Vin will cause the p.d transistor to come out of saturation and become resistive

Voltage transfer characteristics, NMOS inverter with depletion load,



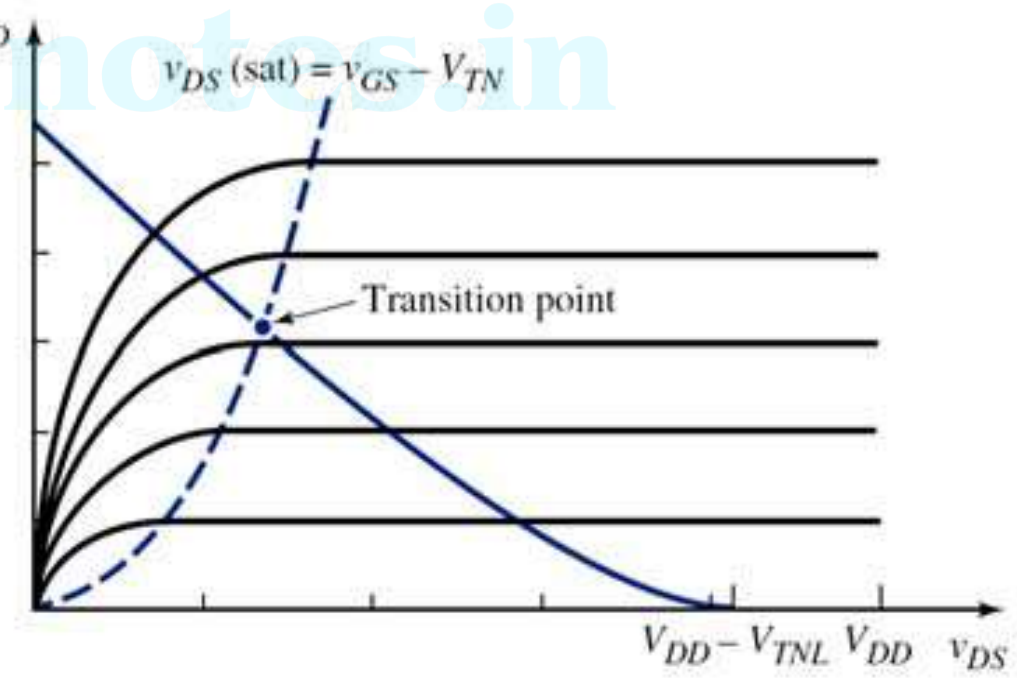


3).NMOS enhancement Mode Transistor Pull - Up

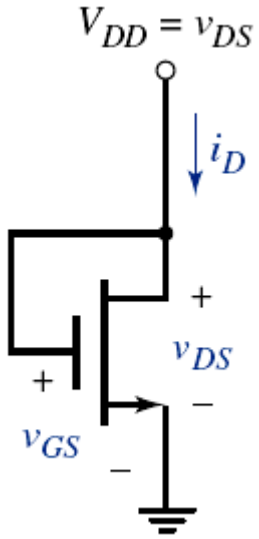


(a)

- This basic inverter consist of two enhancement-only NMOS transistors
- Much more practical than the resister loaded inverter



- An n-channel **enhancement-mode MOSFET with gate connected to the drain can** be used as a **load device**



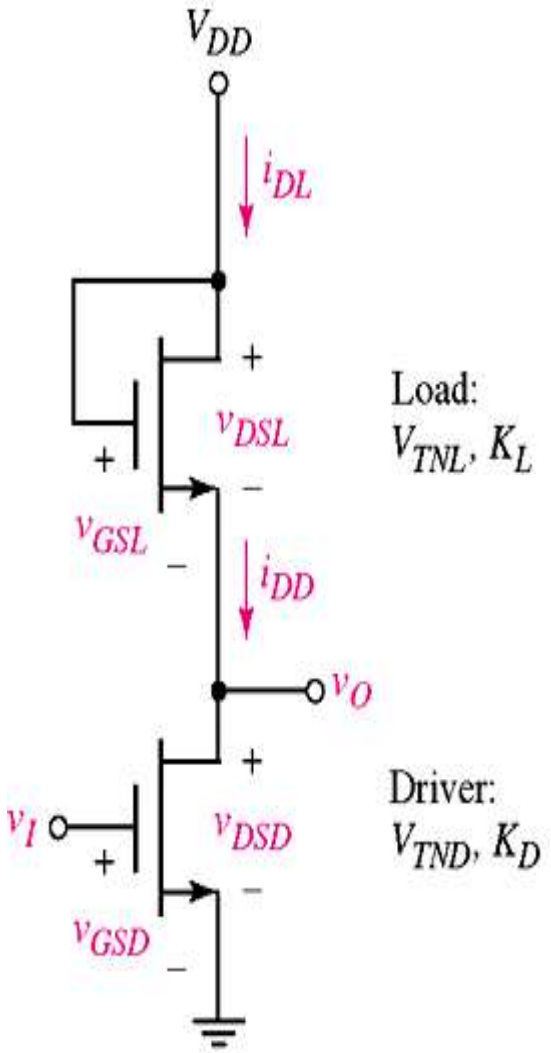
n-channel MOSFET connected as saturated load device

A transistor with this connection always operates in the saturation region when not in cutoff.

When ***vI < VTND*** driver is cut off and the drain currents are zero.

maximum output voltage $v_{O,\max} \equiv V_{OH} = V_{DD} - V_{TNL}$

For the enhancement-load NMOS inverter, the maximum output voltage, which is the logic 1 level, does not reach the full V_{DD} value.



(a)

When ***vI > VT*** driver transistor turns on and is biased in the saturation region.

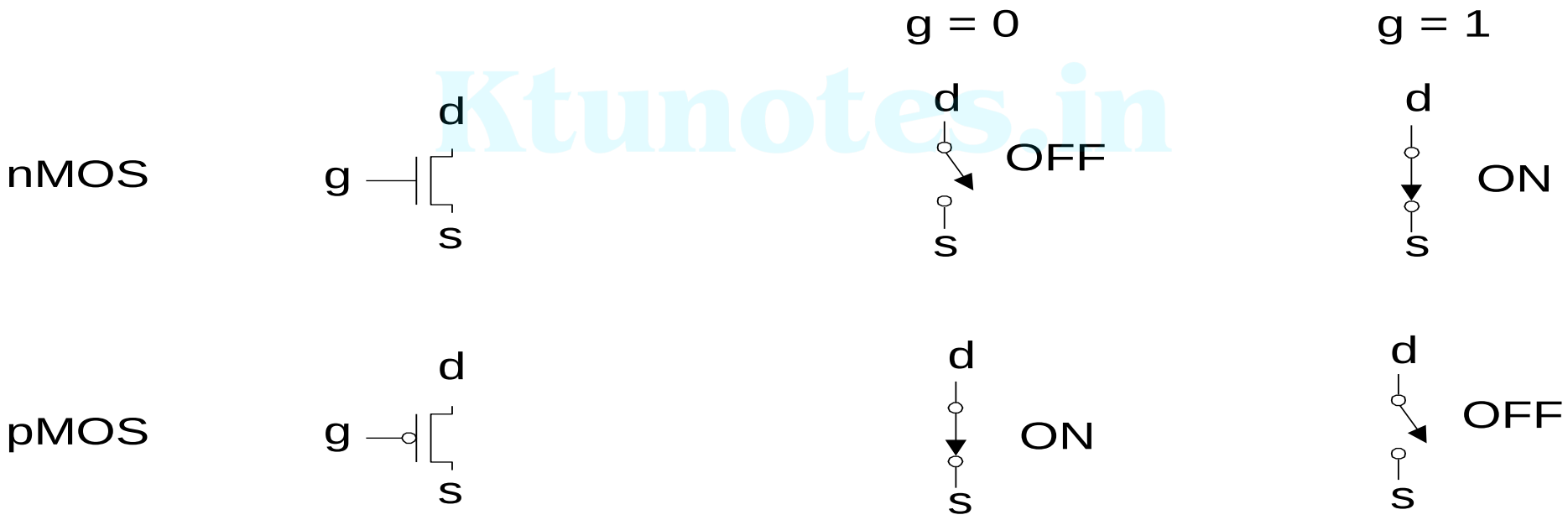
$i_{DD} = i_{DL}$ two drain currents are equal since the output will be connected to the gates of other MOS transistors.

As the input voltage increases, the driver Q-point moves up the load curve and the output voltage decreases linearly with v_I.

- When ***vI > Vt*** the driver transistor Q-point continues to move up the load curve and the driver becomes biased in the nonsaturation region.

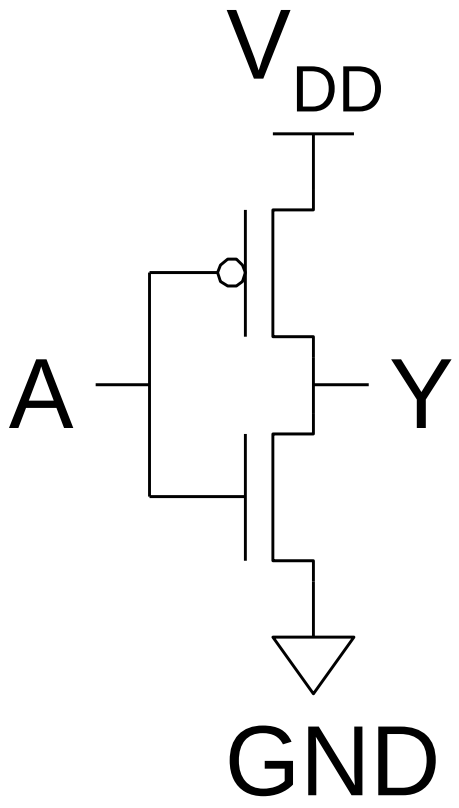
Transistors as Switches

- We can view MOS transistors as electrically controlled switches
- Voltage at gate controls path from source to drain



CMOS Inverter

- an enhancement-type nMOS transistor and an enhancement-type pMOS transistor, operating in complementary mode
- The circuit topology is complementary push-pull in the sense that for high input, the nMOS transistor drives (pulls down) the output node while the pMOS transistor acts as the load, and for low input the pMOS transistor drives (pulls up) the output node while the nMOS transistor acts asthe load.
- Consequently, both devices contribute equally to the circuit operation characteristics.



Advantages over other inverters

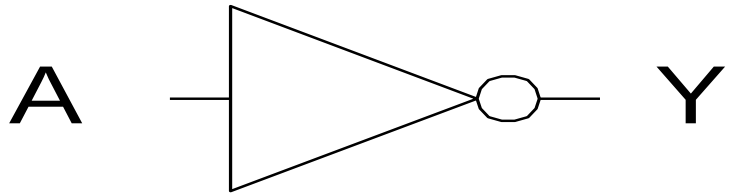
- steady state power dissipation of CMOS inverter circuit is negligible small
- VTC exhibits a full output voltage swing between 0V and VDD

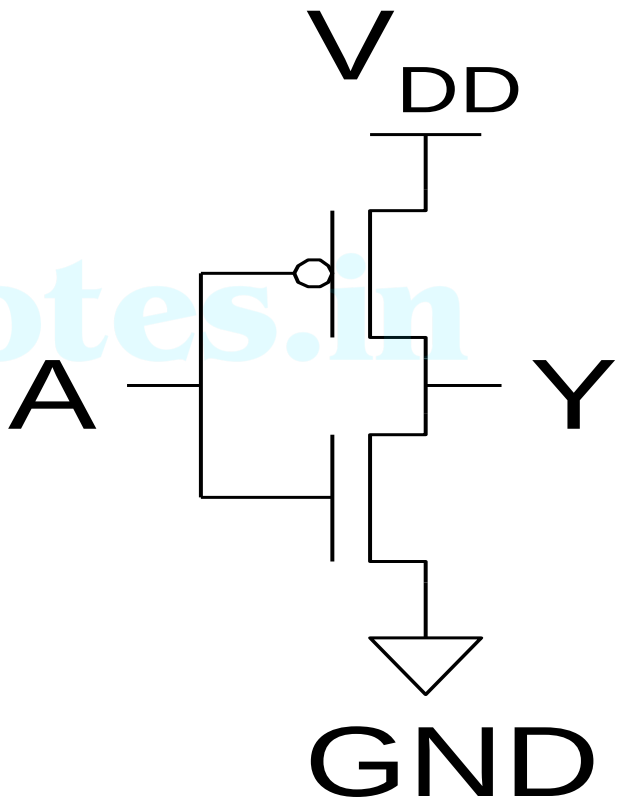
Limitations

- CMOS process is more complex than standard NMOS only process
- Due to parasitic effect chance of occurring latch up condition

CMOS Inverter

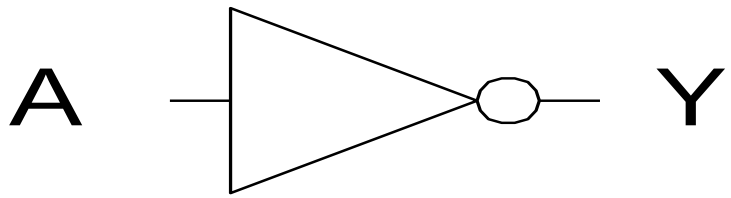
A	Y
0	
1	

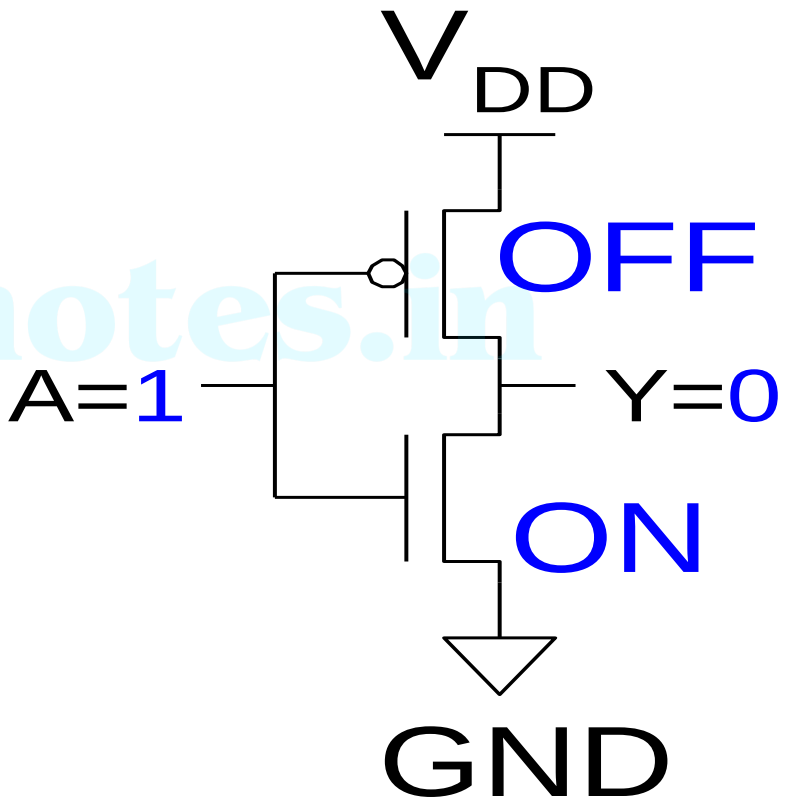




CMOS Inverter

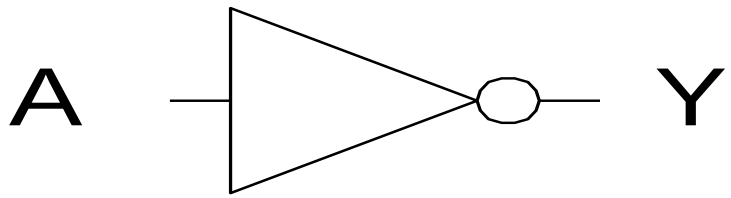
A	Y
0	
1	**0**

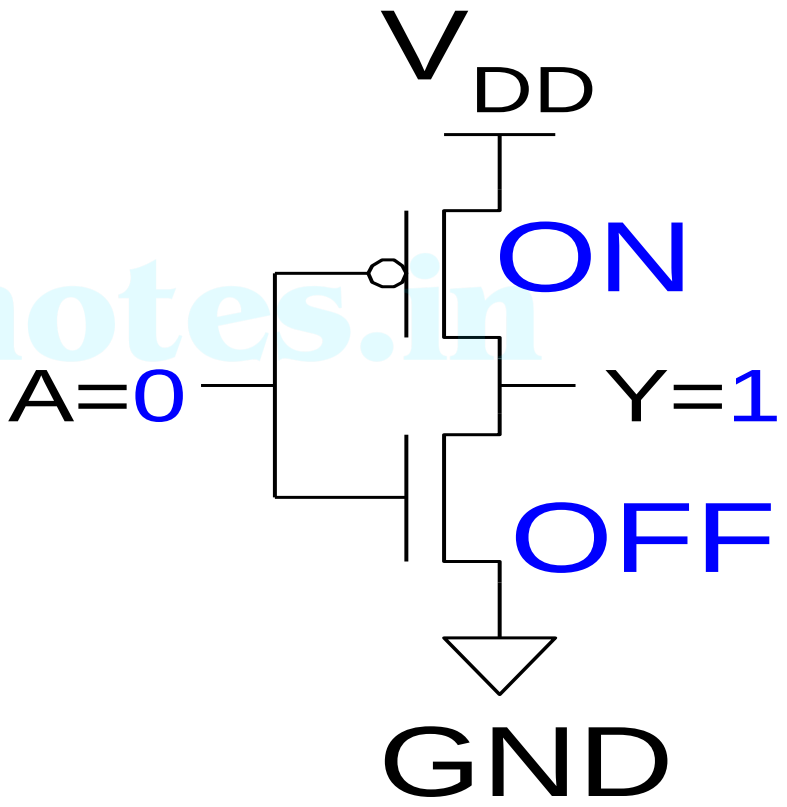




CMOS Inverter

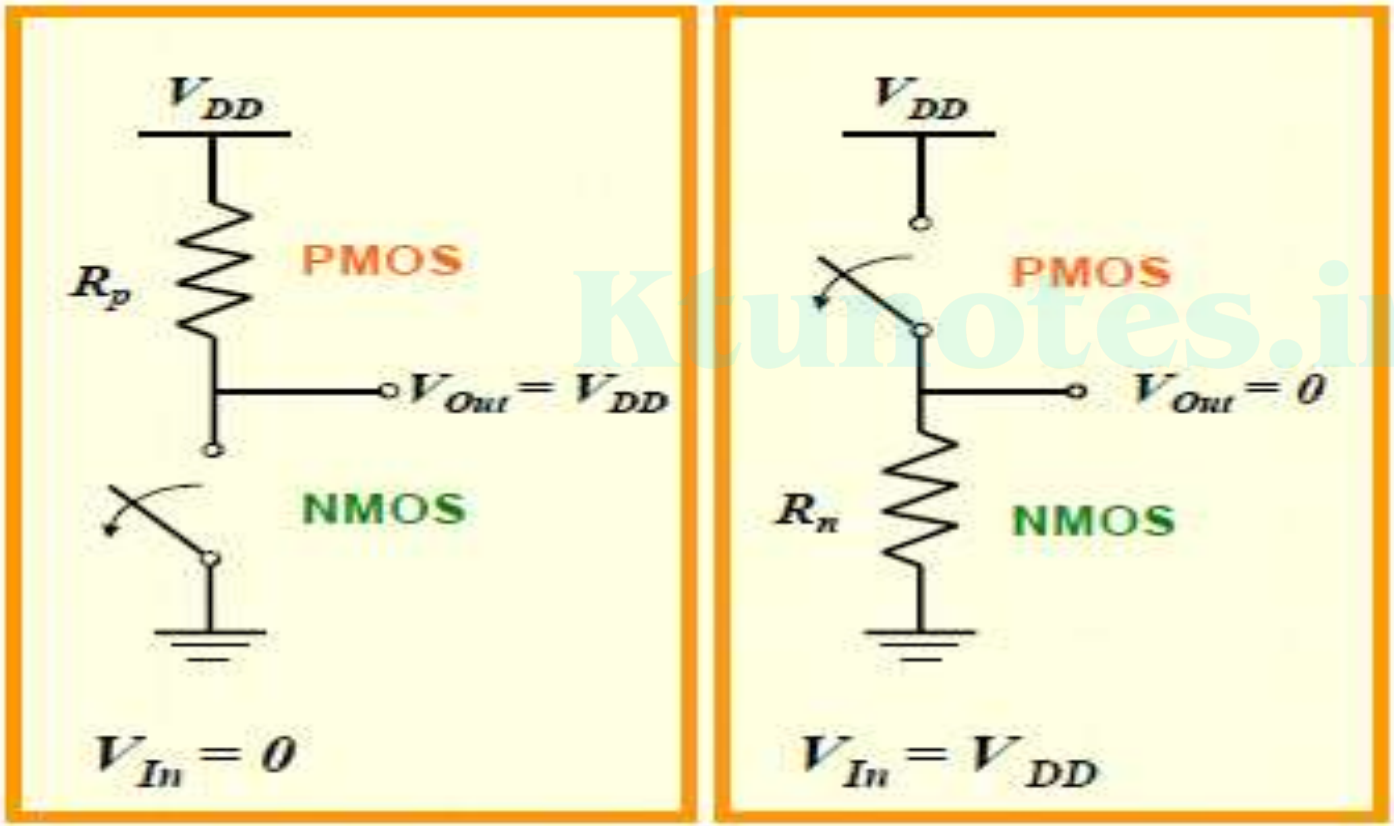
A	Y
0	**1**
1	0





CMOS Inverter

Steady State Response

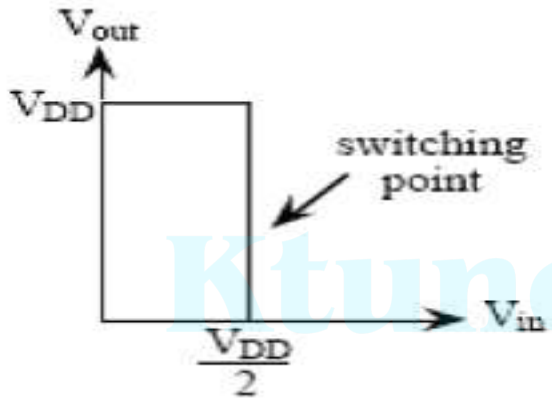


$$V_{OL} = 0$$

$$V_{OH} = V_{DD}$$

Inverter DC Characteristics

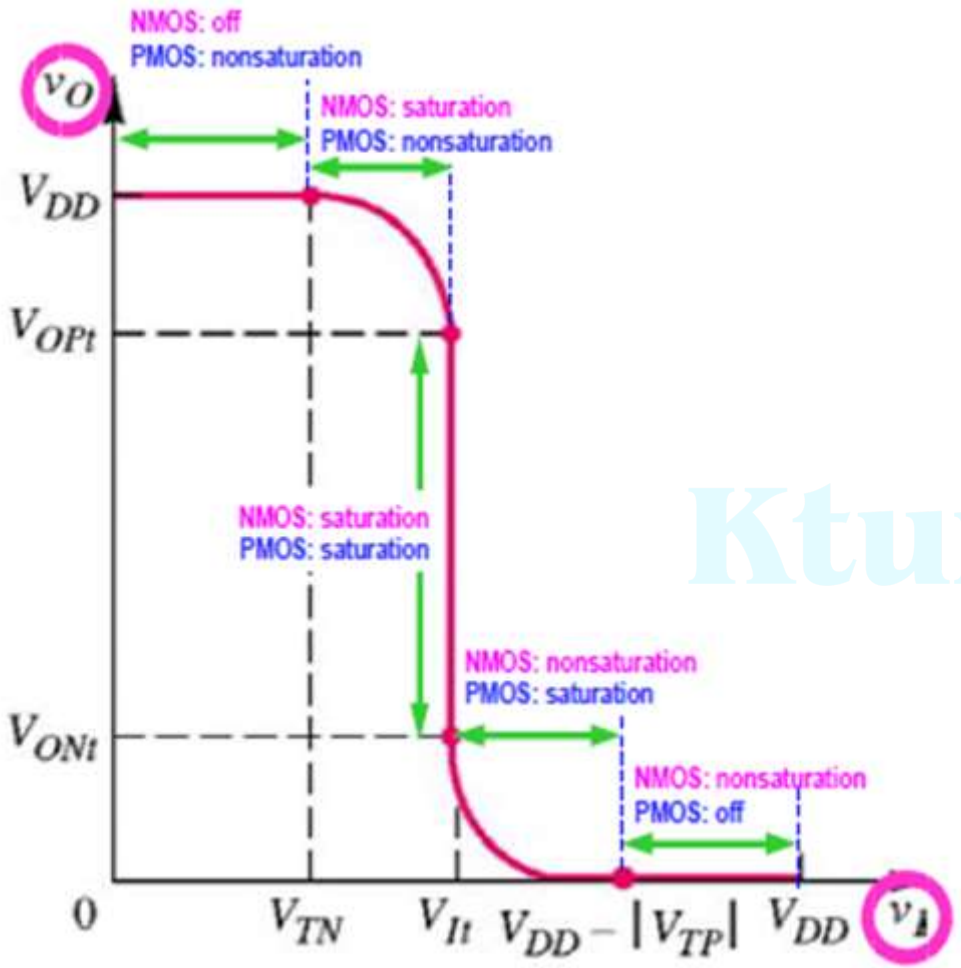
- Ideal characteristics of inverter

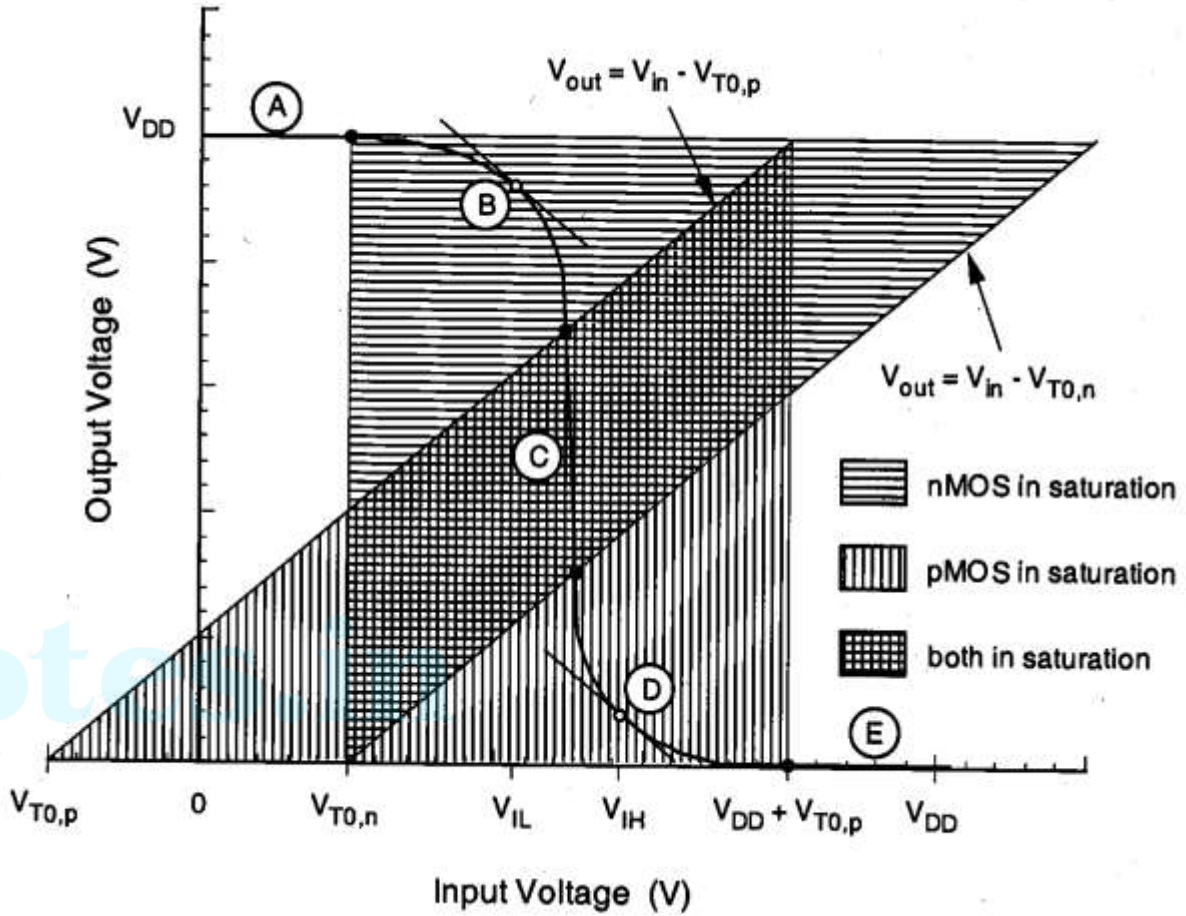


- The actual characteristics are drawn by plotting the values of output voltage for different values of the input voltage.

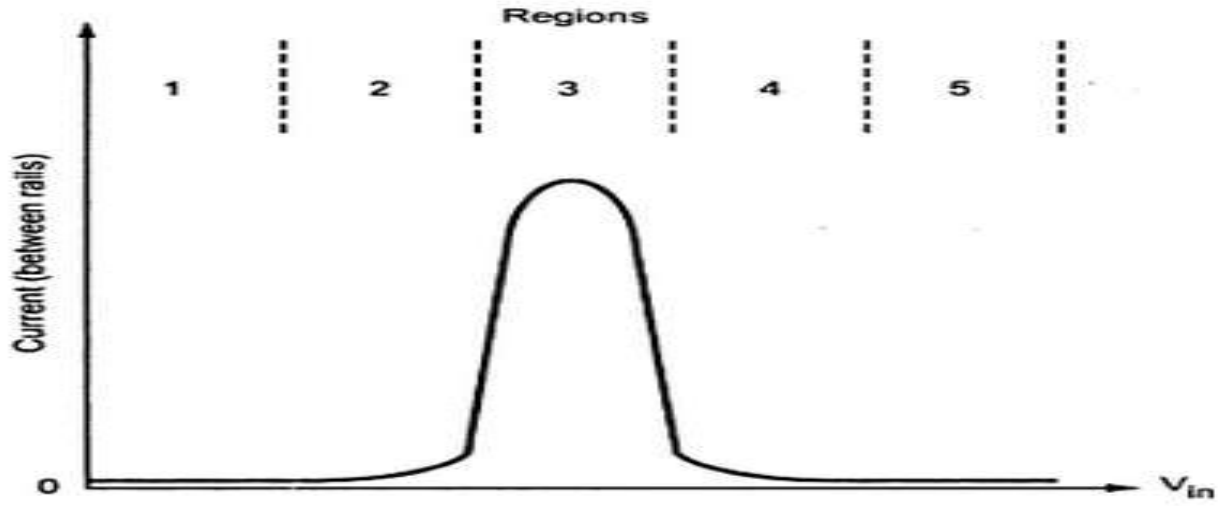
- Voltage Transfer Characteristic (VTC)
  - plot of Vout as a function of Vin
  - vary Vin from 0 to VDD
  - find Vout at each value of Vin

Complete voltage transfer characteristics





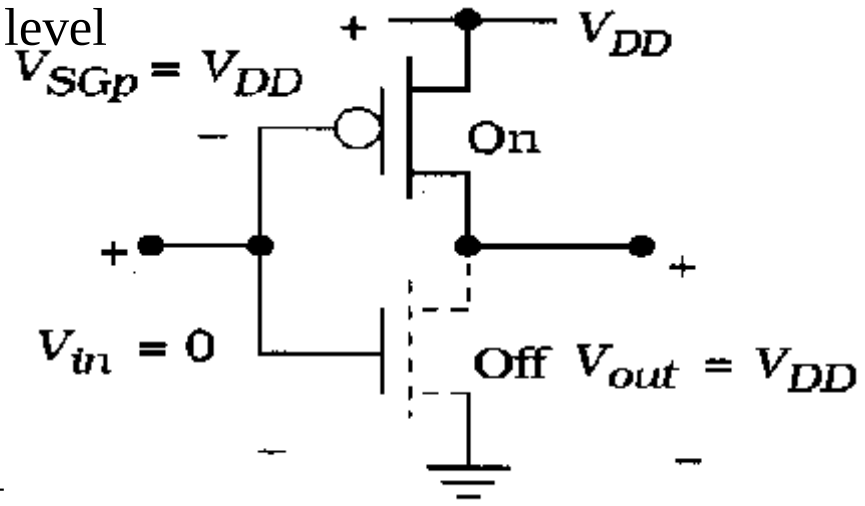
Region	V_{in}	V_{out}	nMOS	pMOS
A	$< V_{T0,n}$	V_{OH}	cut-off	linear
B	V_{IL}	high $\approx V_{OH}$	saturation	linear
C	V_{th}	V_{th}	saturation	saturation
D	V_{IH}	low $\approx V_{OL}$	linear	saturation
E	$> (V_{DD} + V_{T0,p})$	V_{OL}	linear	cut-off



(c) CMOS inverter current versus V_{in}

Region	nMOS	pMOS
A	Cutoff	Linear
B	Saturation	Linear
C	Saturation	Saturation
D	Linear	Saturation
E	Linear	Cutoff

Region 1 ->vin=logic 0 -> n transistor OFF &p transistor ON -> no current flow-> output is directly connected to VDD thorough p transistor. Output logic 1 level



Output High Voltage, V_{OH}

maximum output voltage

occurs when input is low (Vin = 0V)

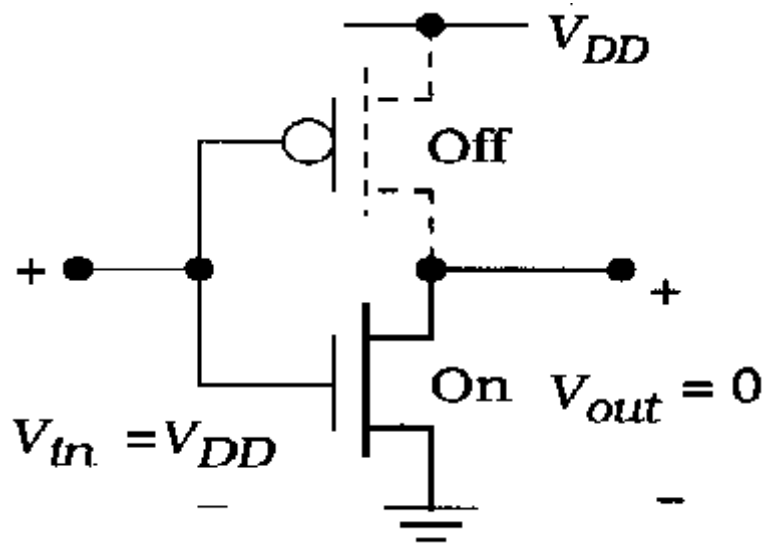
pMOS is ON, nMOS is OFF

pMOS pulls Vout to VDD

V_{OH} = VDD

Region 5 -> vin=logic 1 -> n transistor ON &p transistor OFF -> no current flow-> output logic 0 level

Region 1 & 5 static conditions



Output Low Voltage, V_{OL}

minimum output voltage

occurs when input is high (Vin = VDD)

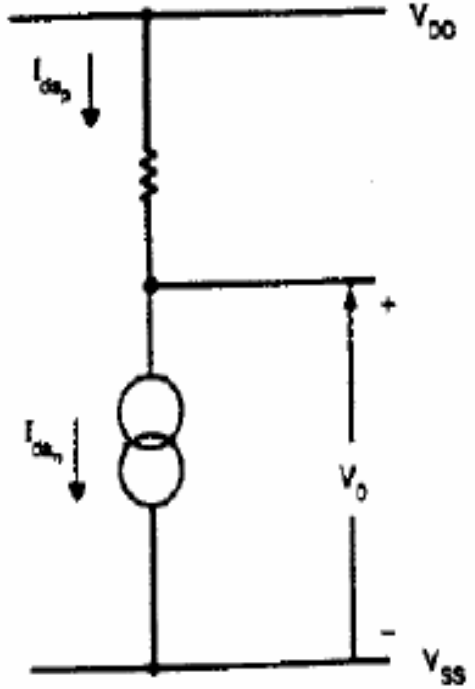
pMOS is OFF, nMOS is ON

nMOS pulls Vout to Ground

V_{OL} = 0 V

- **Region 2->** Vin> Vt of n transistor->n transistor conducts and has a large voltage between source and drain -> n transistor saturation ,p transistor also conducting but with only a small voltage across it. it operated unsaturated region ->circuit draws a small current from VDD supply to vss
- ***Calculation of VIL***

  By definition, the slope of the VTC is equal to (-1), i.e., *dV0/dVin* ***= -1 when the input*** voltage is *V = VIL. Note that in this case, the nMOS transistor operates in saturation while* the pMOS transistor operates in the linear region. From ***IDn= ID p we obtain the following*** current equation:



$$\frac{k_n}{2}\cdot\left(V_{GS,n}-V_{T0,n}\right)^2=\frac{k_p}{2}\cdot\left[2\cdot\left(V_{GS,p}-V_{T0,p}\right)\cdot V_{DS,p}-{V_{DS,p}}^2\right]$$

and also,

$$V_{GS,n}=V_{in}$$
$$V_{DS,n}=V_{out}$$
$$V_{GS,p}=-\left(V_{DD}-V_{in}\right)$$
$$V_{DS,p}=-\left(V_{DD}-V_{out}\right)$$

this expression can be rewritten as

$$\frac{k_n}{2}\cdot\left(V_{in}-V_{T0,n}\right)^2=\frac{k_p}{2}\cdot\left[2\cdot\left(V_{in}-V_{DD}-V_{T0,p}\right)\right.$$
$$\left.\cdot\left(V_{out}-V_{DD}\right)-\left(V_{out}-V_{DD}\right)^2\right]$$

To satisfy the derivative condition at *VIL we differentiate both sides of above equation with respect* to *Vin.*

$$k_n\cdot\left(V_{in}-V_{T0,n}\right)=k_p\cdot\left[\left(V_{in}-V_{DD}-V_{T0,p}\right)\cdot\left(\frac{dV_{out}}{dV_{in}}\right)+\left(V_{out}-V_{DD}\right)\right.$$
$$\left.-\left(V_{out}-V_{DD}\right)\cdot\left(\frac{dV_{out}}{dV_{in}}\right)\right]$$

Substituting *Vin = VIL and (dVoutldVin) = -1 in the above eqn, we obtain*

$$k_n\cdot\left(V_{IL}-V_{T0,n}\right)=k_p\cdot\left(2V_{out}-V_{IL}+V_{T0,p}-V_{DD}\right)$$

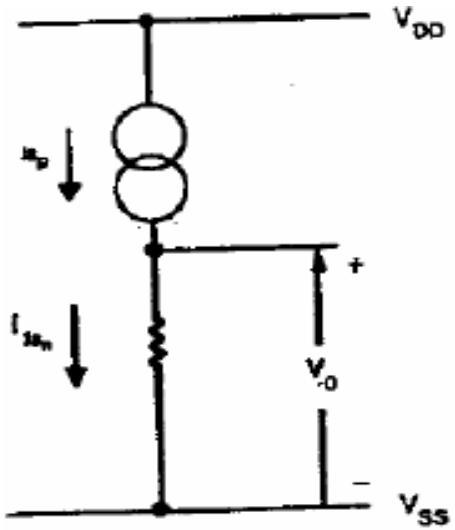
- The critical voltage *VIL can now be found as a function of the output voltage Vout, as* follows:

$$V_{IL} = \frac{2\,V_{out} + V_{T0,p} - V_{DD} + k_R\,V_{T0,n}}{1 + k_R}$$

where k_R is defined as

$$k_R = \frac{k_n}{k_p}$$

- **Region 4** -> n transistor non-saturation ,p transistor saturation -> draws small current



- ***Calculation of VIH***

When the input voltage is equal to *VIH,*

the nMOS transistor operates in the linear region,

and the pMOS transistor operates in saturation. Applying KCL to the output node, we obtain

$$\frac{k_n}{2}\cdot\left[2\cdot\left(V_{GS,n}-V_{T0,n}\right)\cdot V_{DS,n}-{V_{DS,n}}^2\right]=\frac{k_p}{2}\cdot\left(V_{GS,p}-V_{T0,p}\right)^2$$

$$V_{GS,n}=V_{in}$$
$$V_{DS,n}=V_{out}$$

and also,

$$V_{GS,p}=-\left(V_{DD}-V_{in}\right)$$
$$V_{DS,p}=-\left(V_{DD}-V_{out}\right)$$

this expression can be rewritten as

$$\frac{k_n}{2}\cdot\left[2\cdot\left(V_{in}-V_{T0,n}\right)\cdot V_{out}-{V_{out}}^2\right]=\frac{k_p}{2}\cdot\left(V_{in}-V_{DD}-V_{T0,p}\right)^2$$

Now, differentiate both sides of (5.64) with respect to V_{in}.

$$k_n\cdot\left[\left(V_{in}-V_{T0,n}\right)\cdot\left(\frac{dV_{out}}{dV_{in}}\right)+V_{out}-V_{out}\cdot\left(\frac{dV_{out}}{dV_{in}}\right)\right]$$
$$=k_p\cdot\left(V_{in}-V_{DD}-V_{T0,p}\right)$$

Substituting, *Vin = VIH and (dV0ut/ dVin) = -1 in the above eqn*

$$k_n \cdot \left(-V_{IH} + V_{T0,n} + 2V_{out}\right) = k_p \cdot \left(V_{IH} - V_{DD} - V_{T0,p}\right)$$

The critical voltage V_{IH} can now be found as a function of V_{out} as follows:

$$V_{IH} = \frac{V_{DD} + V_{T0,p} + k_R \cdot \left(2V_{out} + V_{T0,n}\right)}{1 + k_R}$$

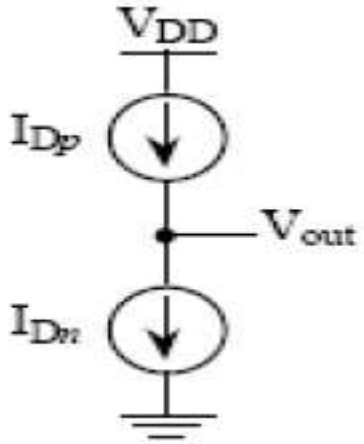
Region 3 -> most of energy consumed in switching from one state to other state attribute to large current flow in region 3->both transistors are in saturation-> here Idsp =-Idsn

Calculation of Vth

•The inverter threshold voltage is defined as *Vth = Vin= Vout*

Since the CMOS inverter exhibits large noise margins and a very sharp VTC transition, the inverter threshold voltage emerges as an important parameter characterizing the DC performance of the inverter.

For Vin = *Vout, both transistors are expected to be in saturation mode; hence, we* can write the following KCL equation.

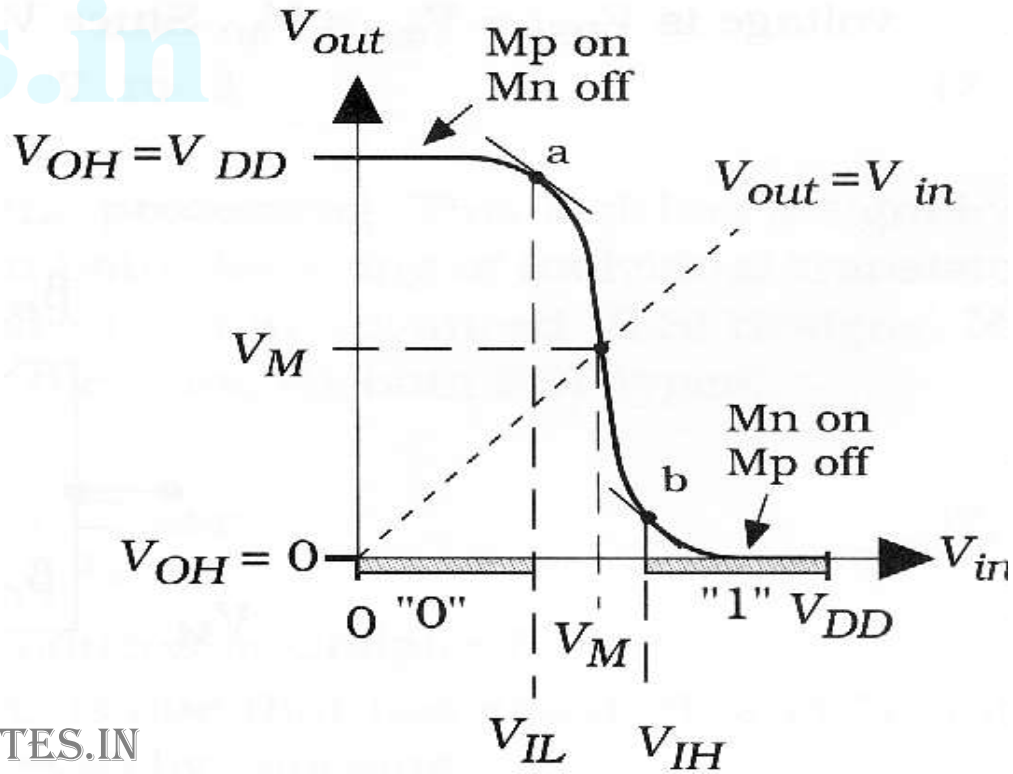


$$\frac{k_n}{2}\cdot\left(V_{GS,n}-V_{T0,n}\right)^2=\frac{k_p}{2}\cdot\left(V_{GS,p}-V_{T0,p}\right)^2$$

$$V_{GS,n}=V_{in}$$
$$V_{DS,n}=V_{out}$$

and also,

$$V_{GS,p}=-\left(V_{DD}-V_{in}\right)$$
$$V_{DS,p}=-\left(V_{DD}-V_{out}\right)$$



$$\frac{k_n}{2}\cdot\left(V_{in}-V_{T0,n}\right)^2=\frac{k_p}{2}\cdot\left(V_{in}-V_{DD}-V_{T0,p}\right)^2$$

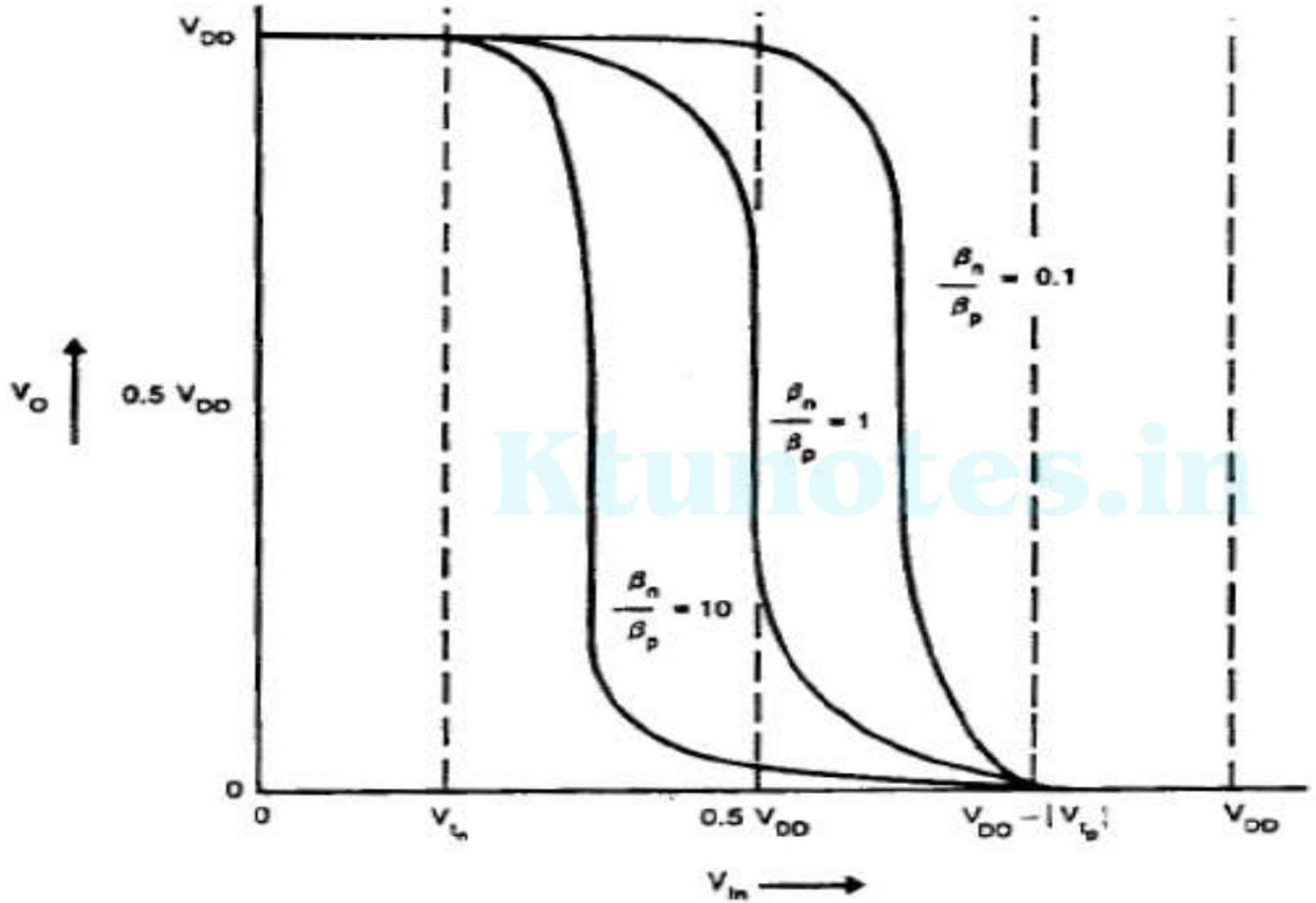
The correct solution for V_{in} for this equation is

$$V_{in}\cdot\left(1+\sqrt{\frac{k_p}{k_n}}\right)=V_{T0,n}+\sqrt{\frac{k_p}{k_n}}\cdot\left(V_{DD}+V_{T0,p}\right)$$

Finally, the inverter threshold (switching threshold) voltage V_{th} is found as

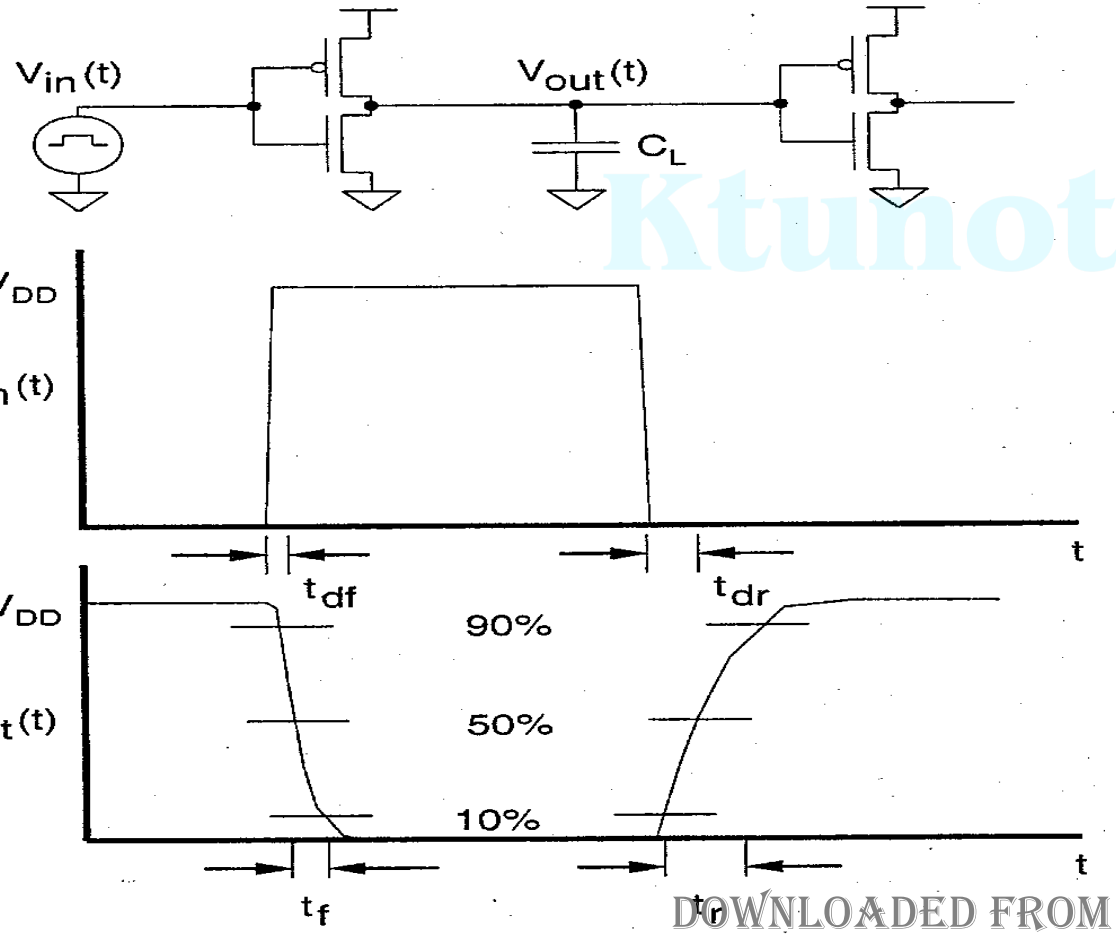
$$V_{th}=\frac{V_{T0,n}+\sqrt{\frac{1}{k_R}}\cdot\left(V_{DD}+V_{T0,p}\right)}{\left(1+\sqrt{\frac{1}{k_R}}\right)}$$

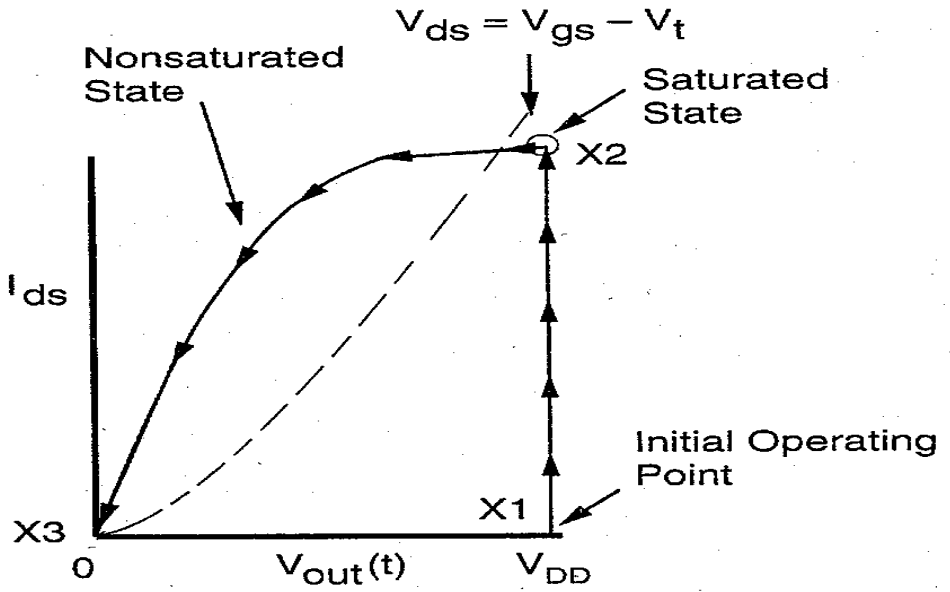
- Effect of βn/βp ratio change on the DC characteristics of CMOS inverter



Switching characteristics of CMOS inverter

- The switching speed of a CMOS gate is limited by the time taken to charge and discharge the load capacitance CL
- An input transition results in an output transition that either charges CL towards VDD or discharge CL towards Vss





- Rise time t_r = time taken for a waveform to rise from the 10% point to 90% of its steady state value.
- Fall time t_f = time taken for a waveform to fall from 90% to 10% of its steady state value.
- Delay time t_d = time difference between input transition(50%) and 50 % output level
- Falling delay t_{df} = delay time with output falling
- Rising delay t_{dr} = delay time with output rising

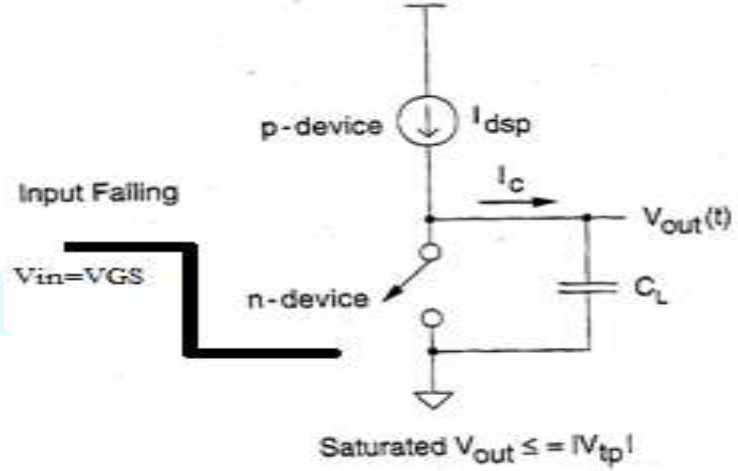
- CMOS Inverter can be viewed as a single transistor either charging the Cload or discharging the Cload
  - Vin is assumed to switch abruptly
  - If Vin switches high, the NMOS Tx discharges Cload while the PMOS Tx turns OFF
  - If Vin switches low, the PMOS Tx charges Cload while the NMOS Tx turns OFF
- Cload is comprised of
  - Cgate due to the gate capacitance of receiving circuits
  - Cwire of the interconnect metal
  - Cdiffusion of the inverter output junctions

Estimation of CMOS inverter delay

- CMOS inverter either charges or discharges a capacitive load CL

Rise time estimation

- assume that the p device stay in saturation for the entire charging period of the load capacitor CL.
- The circuit can modelled as



- Saturation current for p transistor is given by

$$I_{DSp} = \frac{K_p}{2}(V_{GS} - V_{Tp})^2$$

- This current charges CL and its magnitude is approximately constant
- Now

$$V_{out} = \frac{I_{DSp}t}{C_L}$$

Substituting for Idsp and rearranging

- We have

$$t = \frac{2C_L V_{out}}{K_p (V_{GS} - V_{Tp})^2}$$

- Assume that t=tr when vout=+VDD

Hence

$$\tau_r = \frac{2V_{DD}C_L}{K_p (V_{GS} - V_{Tp})^2}$$

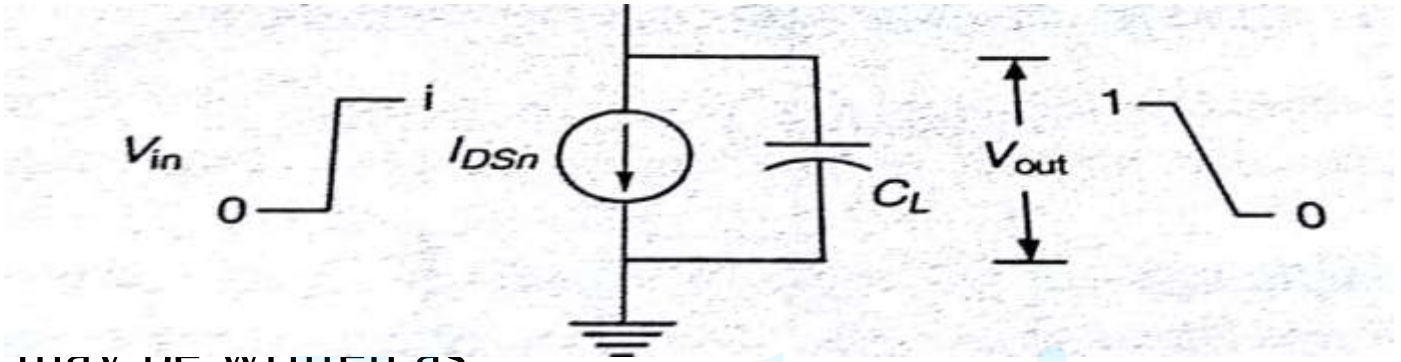
With $V_{Tp} = 0.2V_{DD}$,

$$\tau_r = \frac{3C_L}{K_p V_{DD}}$$

this is the rise time expression of cmos inverter

Fall time estimation

- By applying similar reasoning to the discharge of CL through the n transistor



- The fall time may be written as

$$\tau_f = \frac{3C_L}{K_n V_{DD}}$$

it can be deduced that

$$\frac{\tau_r}{\tau_f} = \frac{k_n}{k_p}$$

- From equations it is observed that rise time and fall time depends on load capacitance CL ,the supply voltage VDD and transconductance parameter k
- The delay is directly prepotional to CL.Thus to achive high speed circuits one has to minimize the load capacitance seen by the gate
- Delay is inversely proportional to supply voltage .,i.e as supply voltage raised delay time is reduced ,their by increasing the speed of gate inthat circuit
- Delay is inversely proportional to k of the driving transistor .the value of k depends on W/L of transistor

Power dissipation

- Two component that establish the amount of power dissipated in a CMOS circuit.

1. Static dissipation due to leakage current or other current drawn continuously from the power supply
2. Dynamics dissipation due to a) switching transient current
   b) charging and discharging of capacitor

1. Static dissipation
   - cmos gate one transistor always off corresponding to the input
   - No dc path from VDD to Vss,the resultant steady state current and hence power P is zero
   - But their is small static dissipation due to reverse bias leakage between diffusion regions conduction can contribute to the static dissipation.
   - In addition, subthreshold conduction can contribute to the static dissipation.

- The leakage current is described by diode equation

$$I = I_s \left(e^{\frac{qV}{kT}} - 1 \right)$$

Is=reverse saturation current

V=diode voltage

q=electron charge

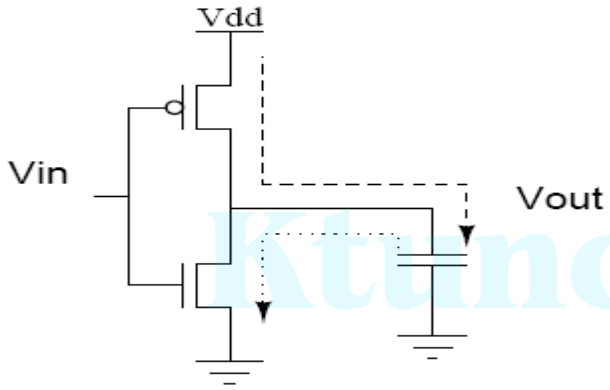
k= Boltzman's constant

T=temparature

- The static power dissipation is the product of device leakage current and the supply voltage
- At room temperature ,the leakage current is about 0.1nA to 0.5 nA per device
- Typical power dissipation due to leakage for an inverter operating at 5Vs between 1 and 2 nW

2 Dynamic dissipation

- During transition from either 0 to 1 or from 1 to 0 ,both n and p type transistors are ON for a short period of time
- Results short current pulse from VDD to VSS
- Current is also required to charge and discharge the output capacitive load



- Current pulse from vdd to vss results in a 'short circuit' dissipation that is independent of the input rise/fall time,load capaciance and the gate design
- The dynamic dissipation can be modelled by assuming that the rise and fall time of the step input is much less than the repetition period
- The average dynamic power Pd , dissipated during switching for a square wave input, vin, having a repetition frequency ,is given by

$$f_p = \frac{1}{t_p}$$

$$P_d = C_L V_{DD}^{\ 2} f_p$$

- Thus for a repetitive step input the average power that is dissipated is proportional to the energy required to charge and discharge the circuit capacitance
- The important factor to be noted here is that ,power to be proportional to switching frequency but independent of device parameters

Short circuit dissipation

Short circuit dissipation is given by

$$P_{SC} = I_{mean} V_{DD}$$

- where tp is the period of the waveform.
- It shows that the short-circuit current is dependent on β and the input waveform rise and fall times.
- Slow rise times on nodes can result in significant **(20%) short-circuit power** dissipation for loaded inverters.

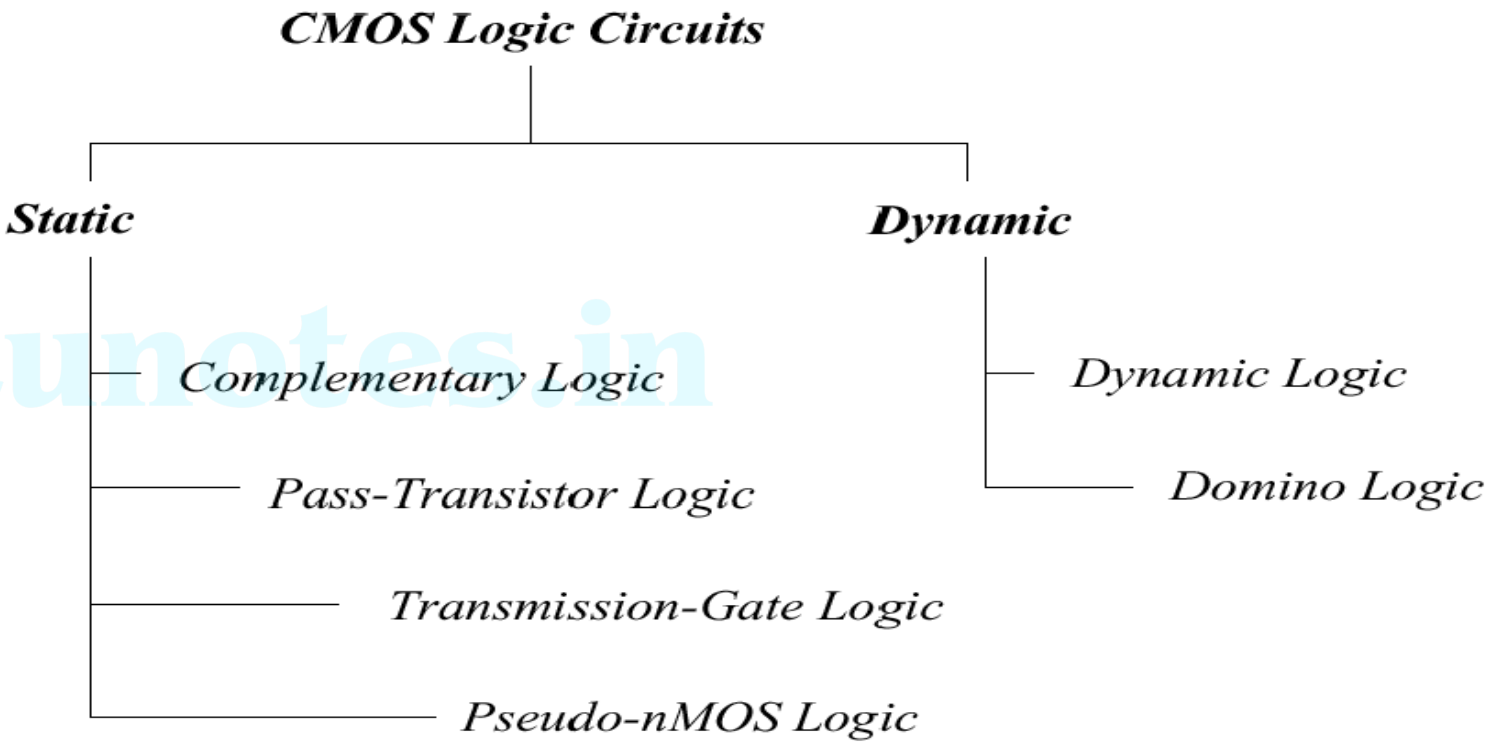
Total power dissipation

Total power dissipation can be obtained from the sum of three components, so

$$Ptotal = P_S + P_d + P_{SC}$$

CMOS Logic Structures

- Static logic circuits hold their output values indefinitely
- Dynamic logic circuits store the output in a capacitor, so it decays with time unless it is refreshed.
- We will look at a few of these structures



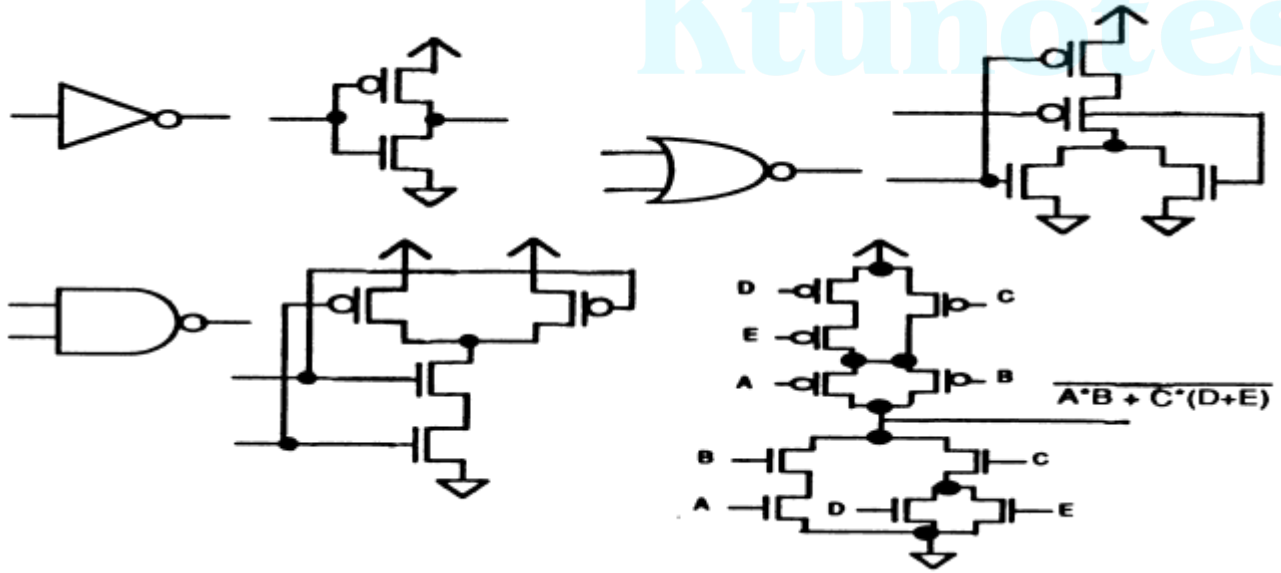
Different structures of CMOS logic circuits.

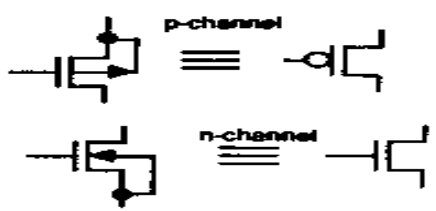
Static CMOS Circuit

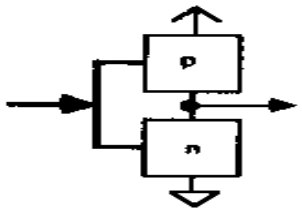
- At every point in time (except during the switching transients) each gate output is connected to either VDD or Vss via a low-resistive path.
- The outputs of the gates assume at all times the value of the Boolean function, implemented by the circuit (ignoring, once again, the transient effects during switching periods).
- This is in contrast to the dynamic circuit class, which relies on temporary storage of signal values on the capacitance of high impedance circuit nodes.

Static CMOS Circuit

- Basic CMOS combinational circuits consist of:
  - Complementary pull-up (p-type) and pull-down (n-type



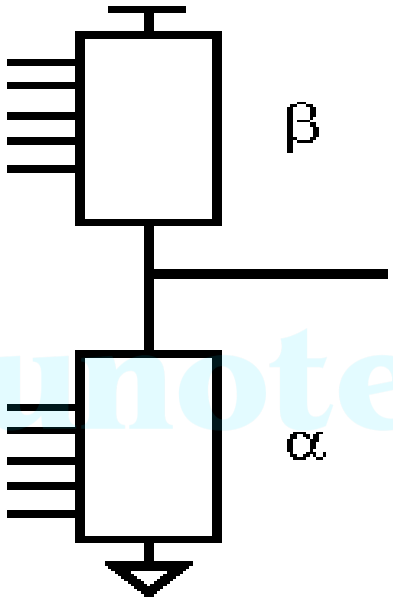




Static CMOS

To build a logic gate $\bar{f}(x_1, \ldots, x_n)$, need to build two switch networks:

The pullup network connects the output to Vdd when f is false.



pMOS only, since only passes 1

The pulldown network connects the output to Gnd when f is true.

nMOS only, since only passes 0

Pulldown

$$\alpha(x_1, \ldots, x_n) = f(x_1, \ldots, x_n)$$

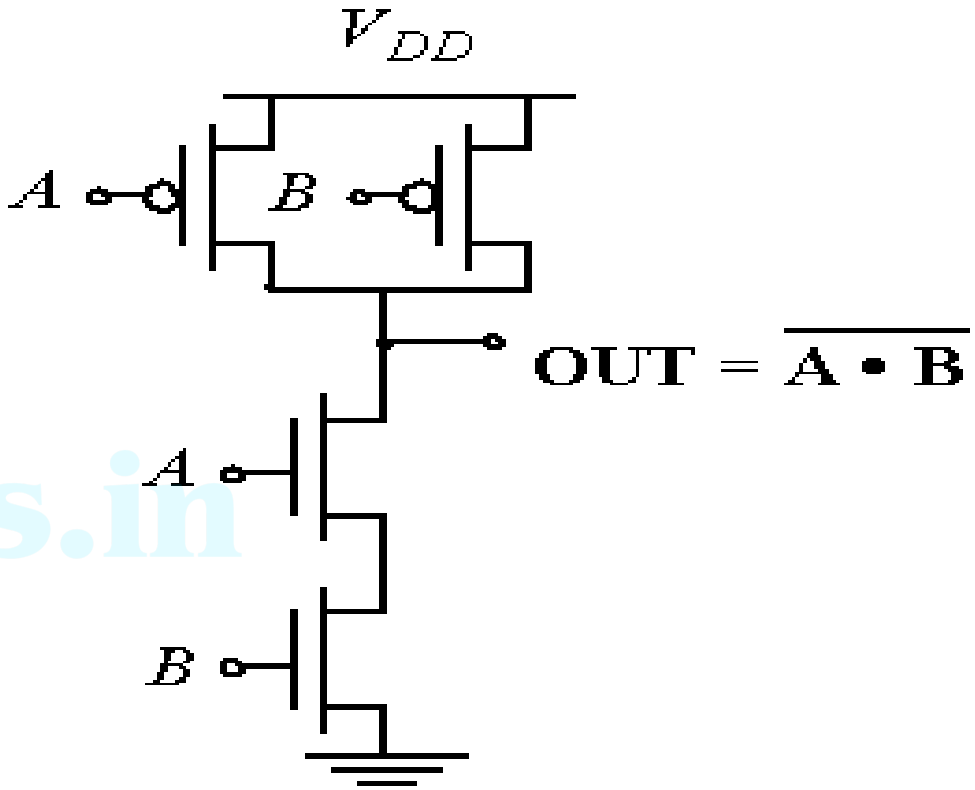
Pullup

$$\beta(\bar{x}_1, \ldots, \bar{x}_n) = \bar{f}(x_1, \ldots, x_n)$$ (since pMOS invert inputs)

Example Gate: NAND

A	B	Out
0	0	1
0	1	1
1	0	1
1	1	0

Truth Table of a 2 input NAND gate



PDN: G = A B $\Rightarrow$ Conduction to GND

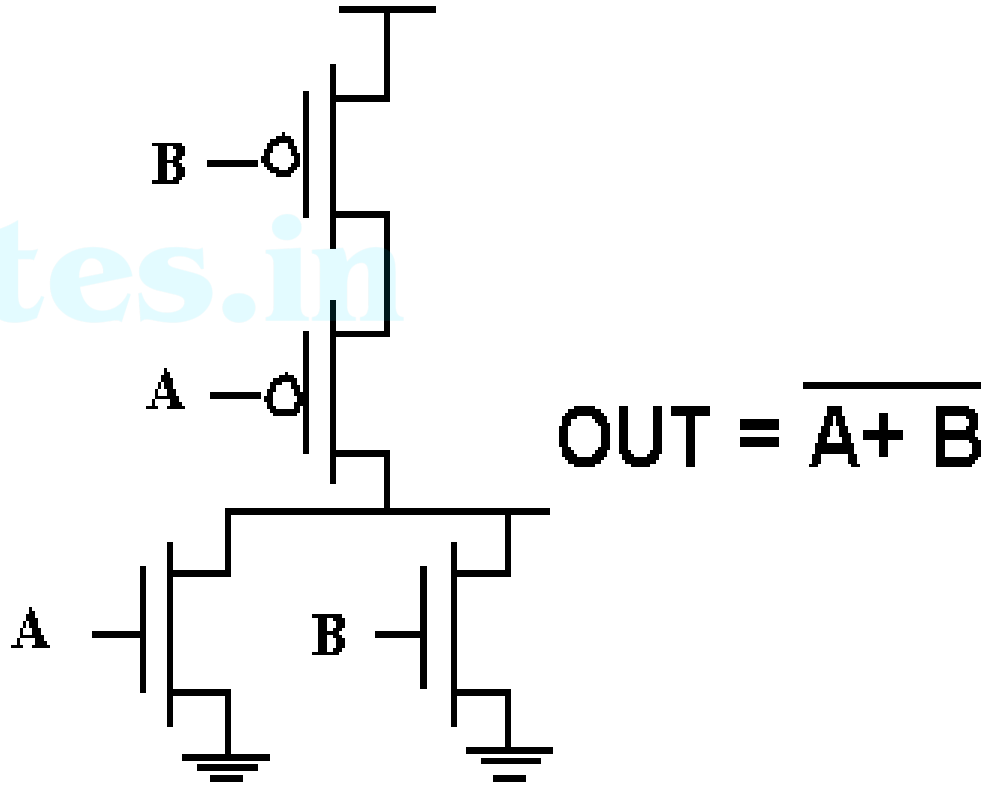
PUN: F= $\overline{A} + \overline{B} = \overline{AB} \Rightarrow$ Conduction to V_{DD}

$$\overline{G(In_1, In_2, In_3, \ldots)} \equiv F(\overline{In_1}, \overline{In_2}, \overline{In_3}, \ldots)$$

Example Gate: NOR

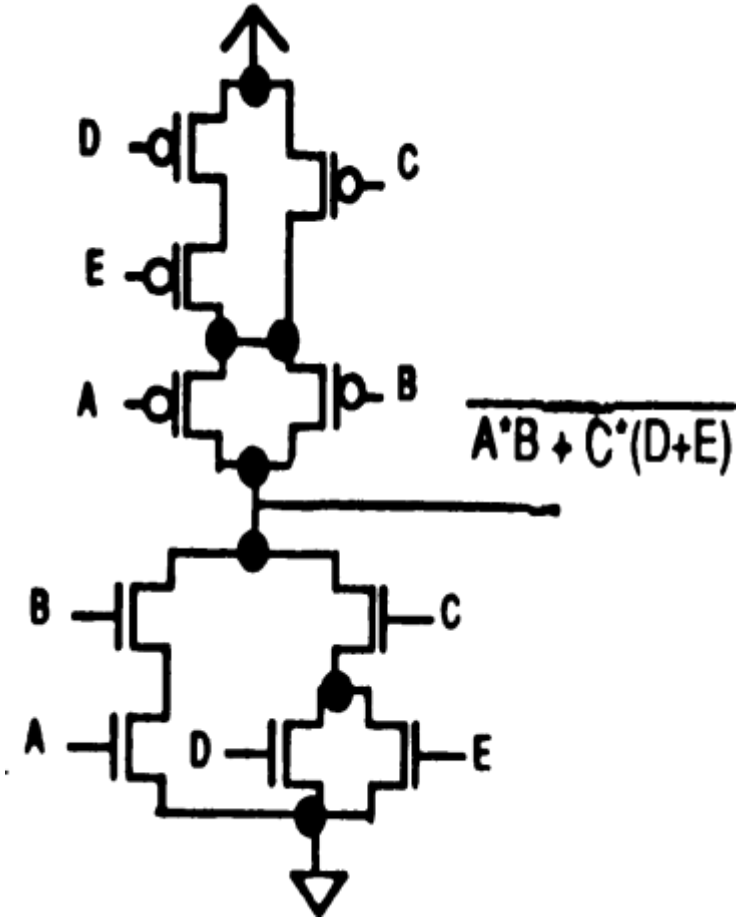
A	B	Out
0	0	1
0	1	0
1	0	0
1	1	0

Truth Table of a 2 input NOR gate

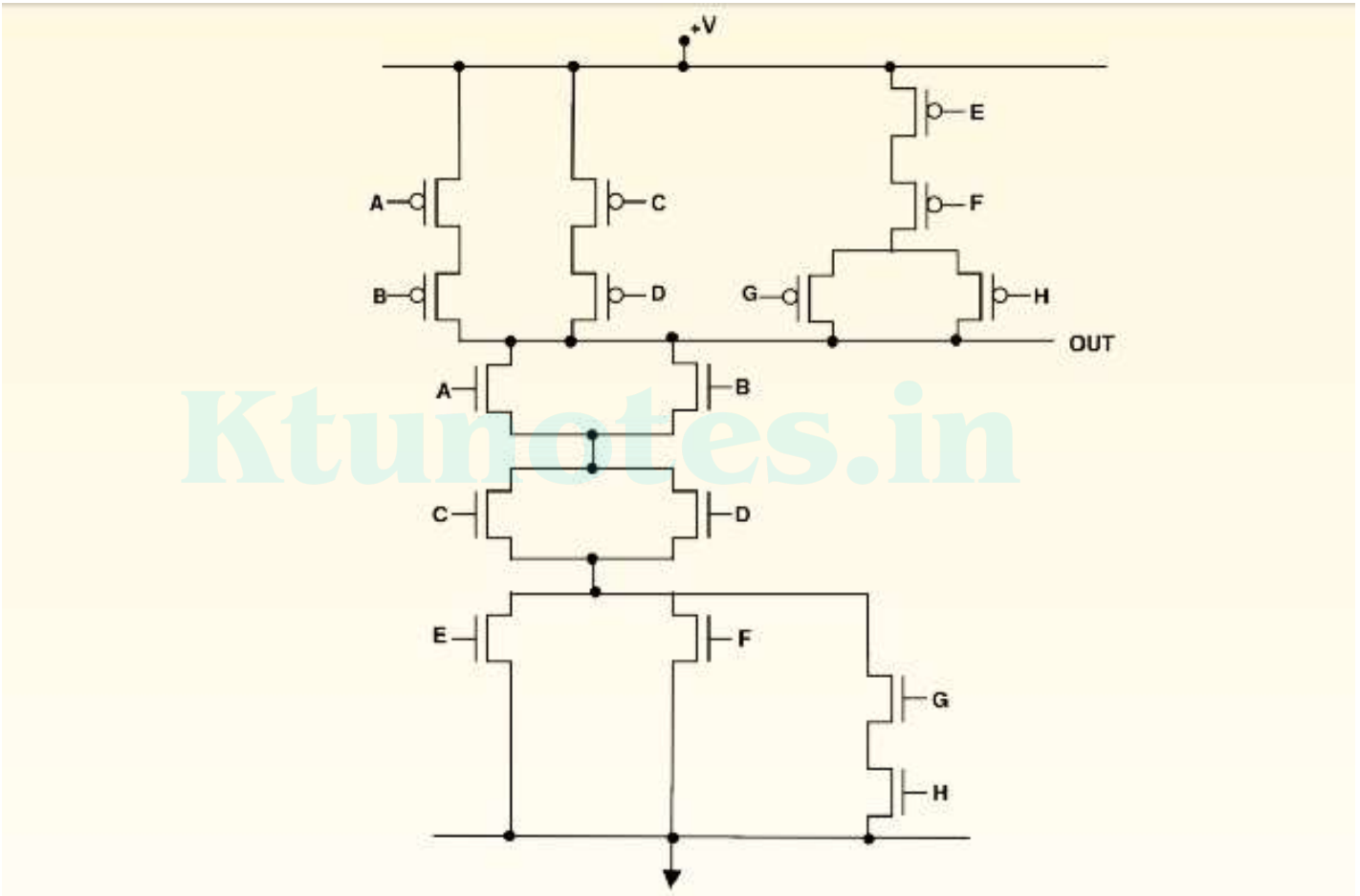


Complex Gate

- We can form complex combinational circuit function in a complementary tree. The procedure to construct a complementary tree is as follow:-
- Express the boolean expression in an inverted form
- For the n-transistor tree, working from the inner- most bracket to the outer-most term, connect the OR term transistors in parallel, and the AND term transistors in series
- For the p-transistor tree, working from the inner- most bracket to the outer-most term, connect the OR term transistors in series, and the AND term transistors in parallel

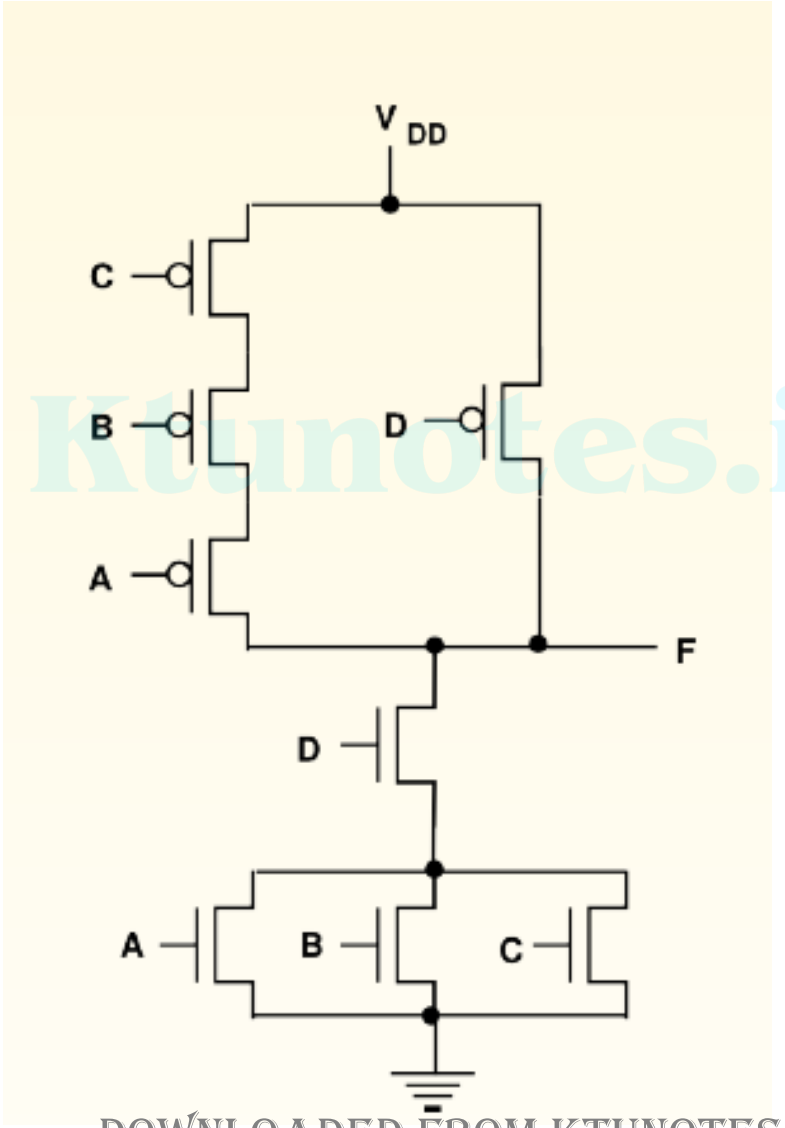


Example Gate: COMPLEX CMOS GATE



$$OUT = \overline{(A + B) \cdot (C + D) \cdot (E + F + (G \cdot H))}$$

Example Gate: COMPLEX CMOS GATE



$$F = \overline{(A + B + C) \cdot D)}$$

Properties of Complementary CMOS Gates

1)High noise margins

V_{OH} and V_{OL} are at V_{DD} and *GND* , respectively.

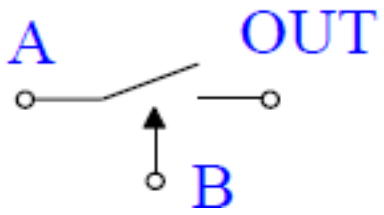
2)No static power consumption

There never exists a direct path betweenV_{DD} and V_{SS} (*GND*) in steady-state mode

3)Comparable rise and fall times:

(under the appropriate scaling conditions)

- Advanced logic function or switching scheme are implemented using the feature of transistor
- MOS to work as a simple switch
- It has the advantage of being simple and fast.
- Complex gates are implemented with the minimum number of transistors (the reduced parasitic capacitance results in fast circuits)



$$OUT = A \cdot B$$

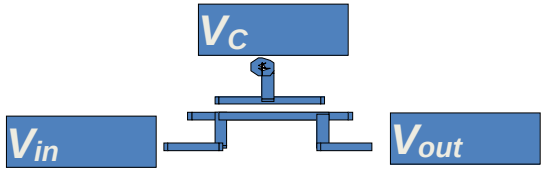
- The static and transient performance strongly depend upon the availability of an high quality switch with low parasitic resistance and capacitance

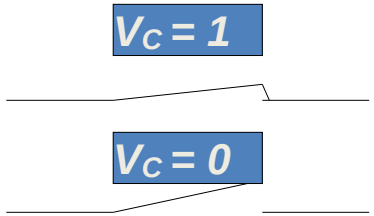
❑ A single transistor is used as switch: *Pass Transistor*

❑ N- and P-transistor are used: *Transmission Gate*

Pass Transistors

– The **pass transistor** is an **nFET** used as a switch-like element to connect logic and storage.





– Used in **NMOS**; sometimes used in **CMOS** to reduce cost.

– The voltage on the gate, V_C, determines whether the pass transistor is "open" or "closed" as a switch.

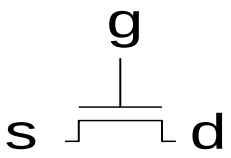
• If $V_C = H$, it is "closed" and connects V_{out} to V_{in}.

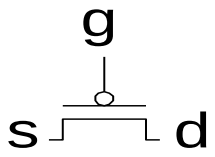
• If $V_C = L$, it is "open" and V_{out} is not connected to V_{in}.

– Consider $V_{in} = L$ and $V_{in} = H$ with $V_C = H$. With $V_{in} = L$, the pass transistor is much like a pull-down transistor in an inverter or **NAND** gate. So V_{out}, likewise, becomes L. But, for $V_{in} = H$, the output becomes the effective source of the **FET**. When $V_{GS} = V_{DD}-V_{OUT} = V_{Tn}$, the **nFET** cuts off. The **H** level is $V_{OUT} = V_{DD}-V_{Tn}$.

Pass Transistors

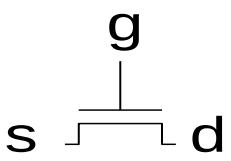
- Transistors can be used as switches

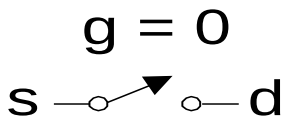


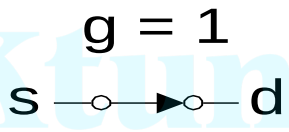


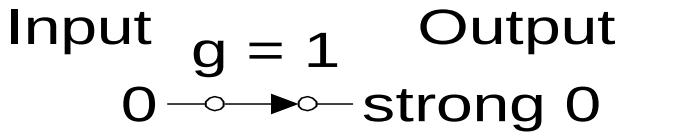
Pass Transistors

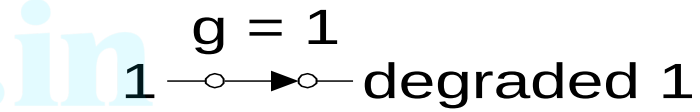
- Transistors can be used as switches

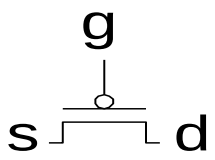


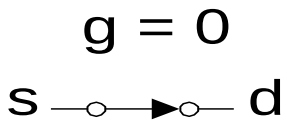


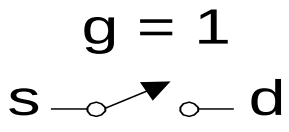


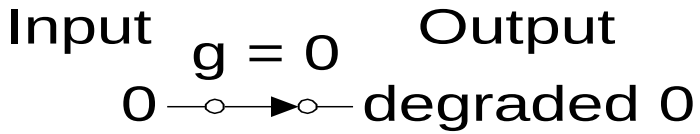




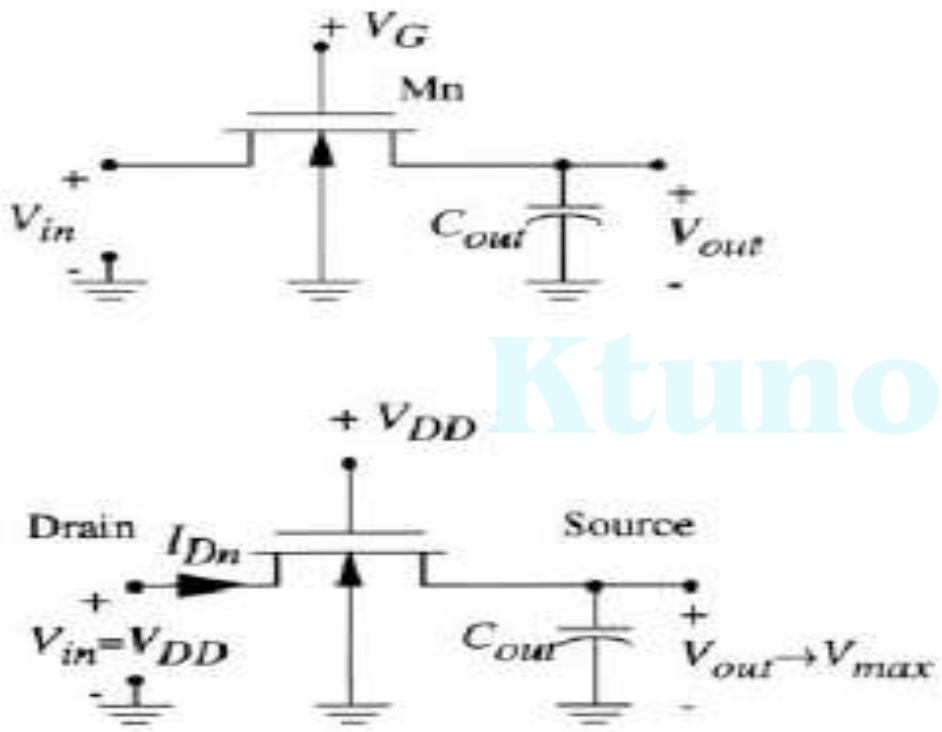




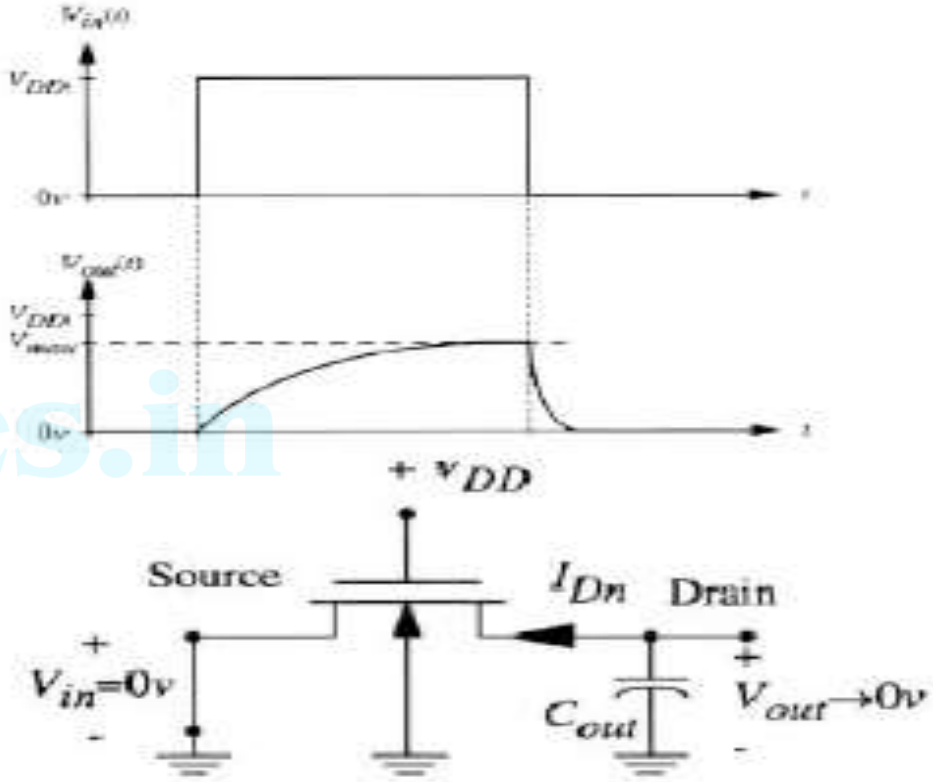




NMOS Pass Transistor



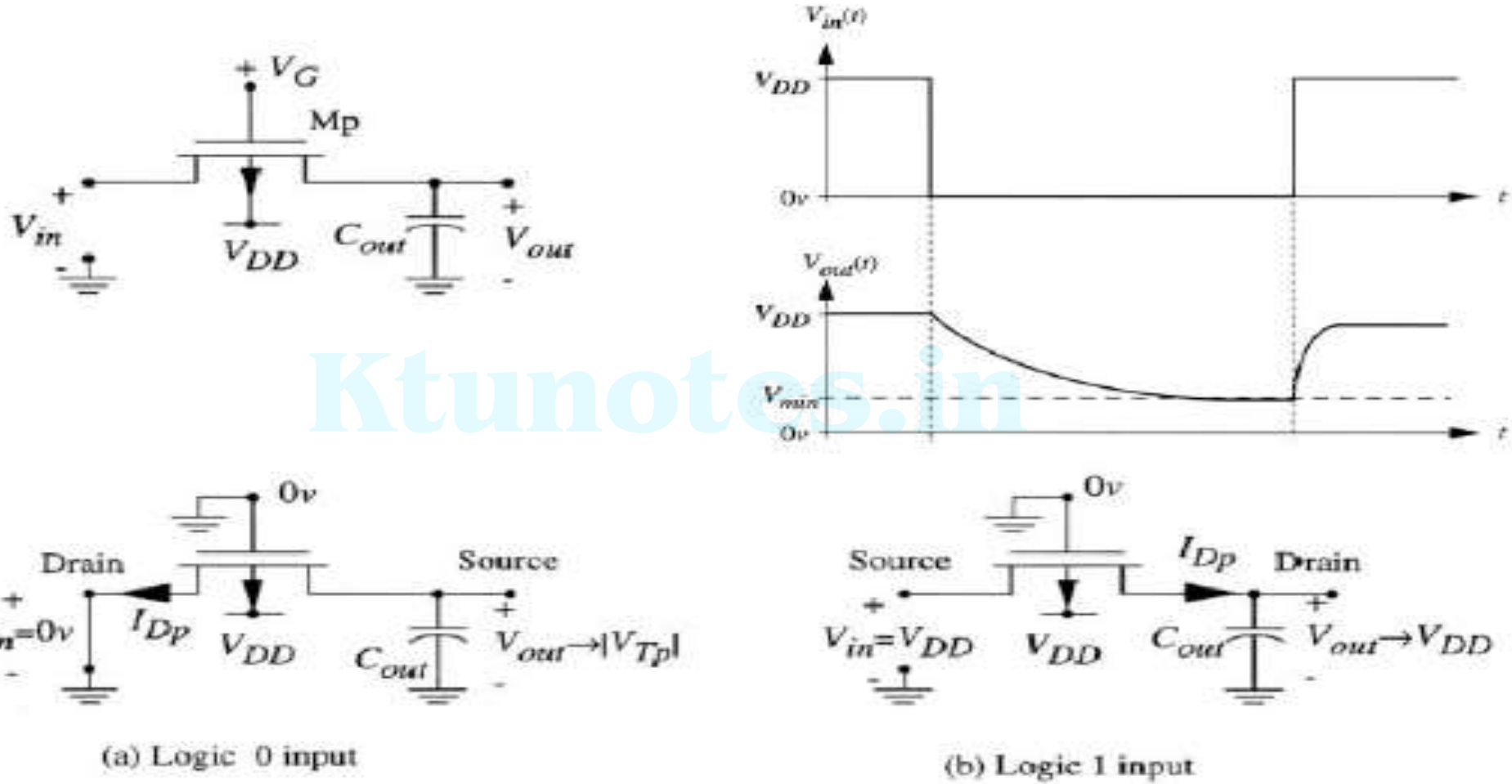
(a) Logic 1 input



(b) Logic 0 input

$$V_{max} = V_{DD} - V_{Tn}$$

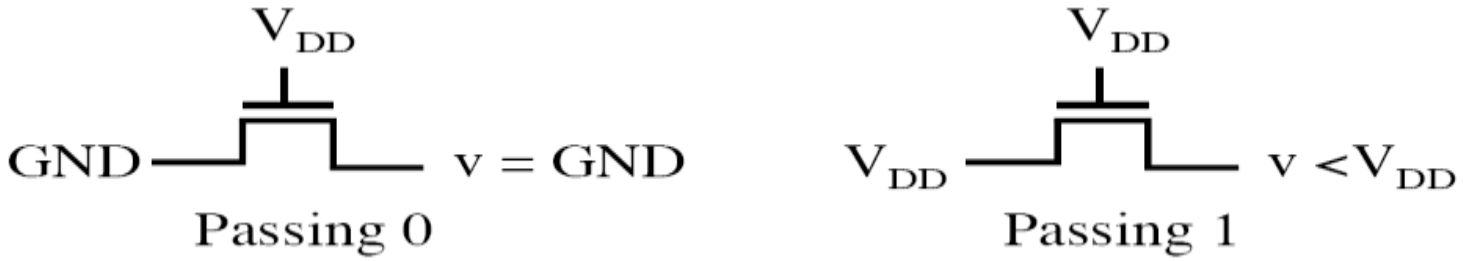
PMOS Pass Transistor



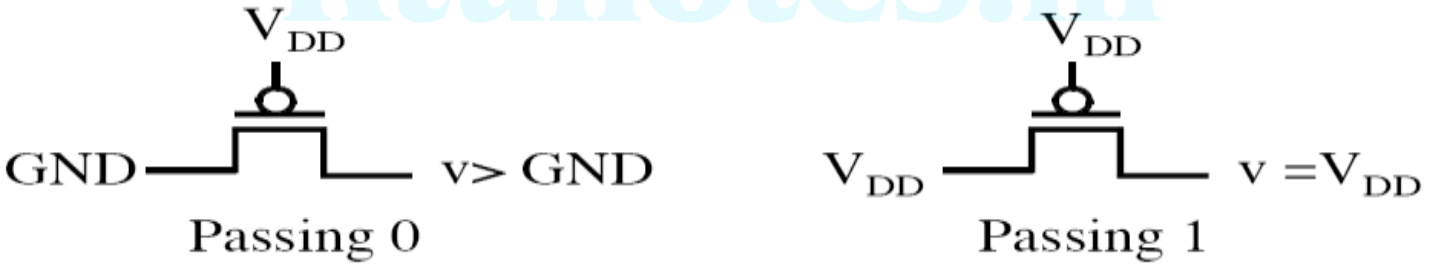
(a) Logic 0 input

(b) Logic 1 input

- N-Channel MOS Transistors pass a 0 better than a 1

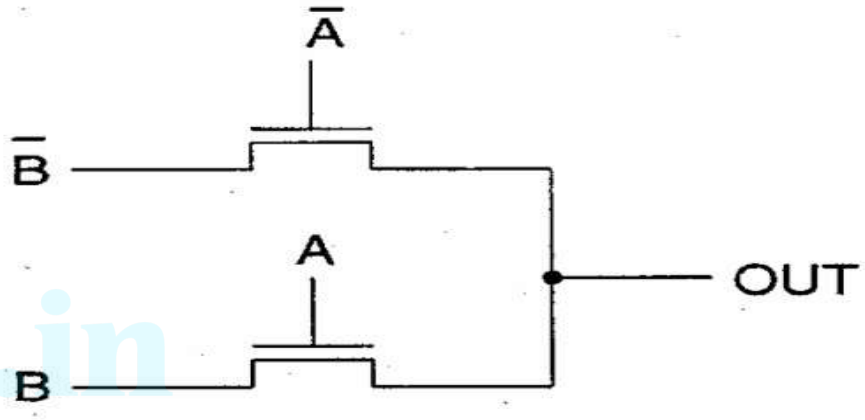


- P-Channel MOS Transistors pass a 1 better than a 0

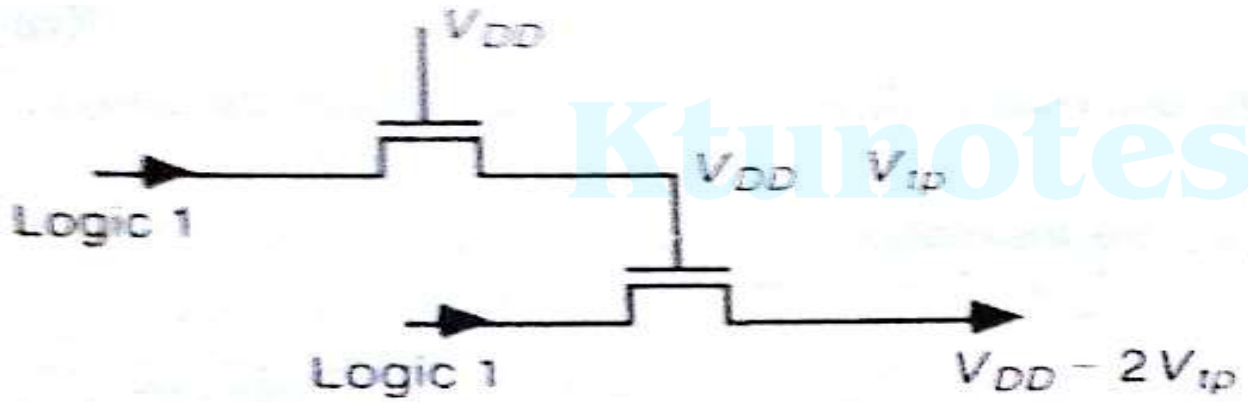


- This is the reason that N-Channel transistors are used in the pull-down network and P-Channel in the pull-up network of a CMOS gate. Otherwise the noise margin would be significantly reduced.

- This figure shows a simple XNOR implementation using pass transistors:
- If A is high, B is passed through the gate to the output
- If A is low, B’ is passed through the gate to the output



- No pass transistor gate may be driven through one or more pass transistors



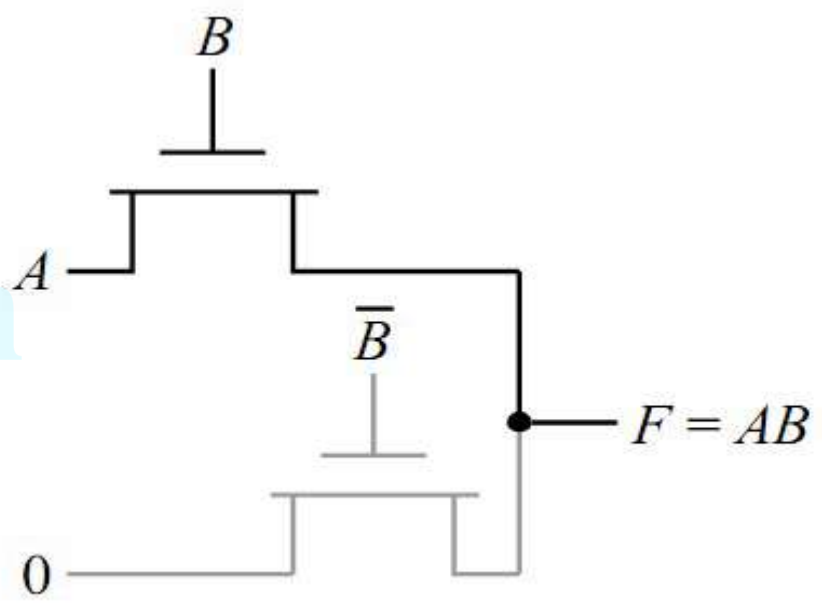
Loss of logic level 1 if the gate of a pass transistor is driven from another pass transistor.

•Logic levels propagated through pass transistors are degraded by threshold voltage effects.

•Signal out of pass transistor T1 doesnot reach a full logic 1 -> voltage one trasistor threshold below a true logic1 ,this degraded voltage would not permit the output of T2 to reach acceptable logic 1 level

Advantages of pass transistor logic

- Fewer devices to implement the logical functions as compared to CMOS
- Example AND gate.
- When B is “1”, top device turns on and copies the input A to output F.
- When B is low, bottom device turns on and passes a “0”.



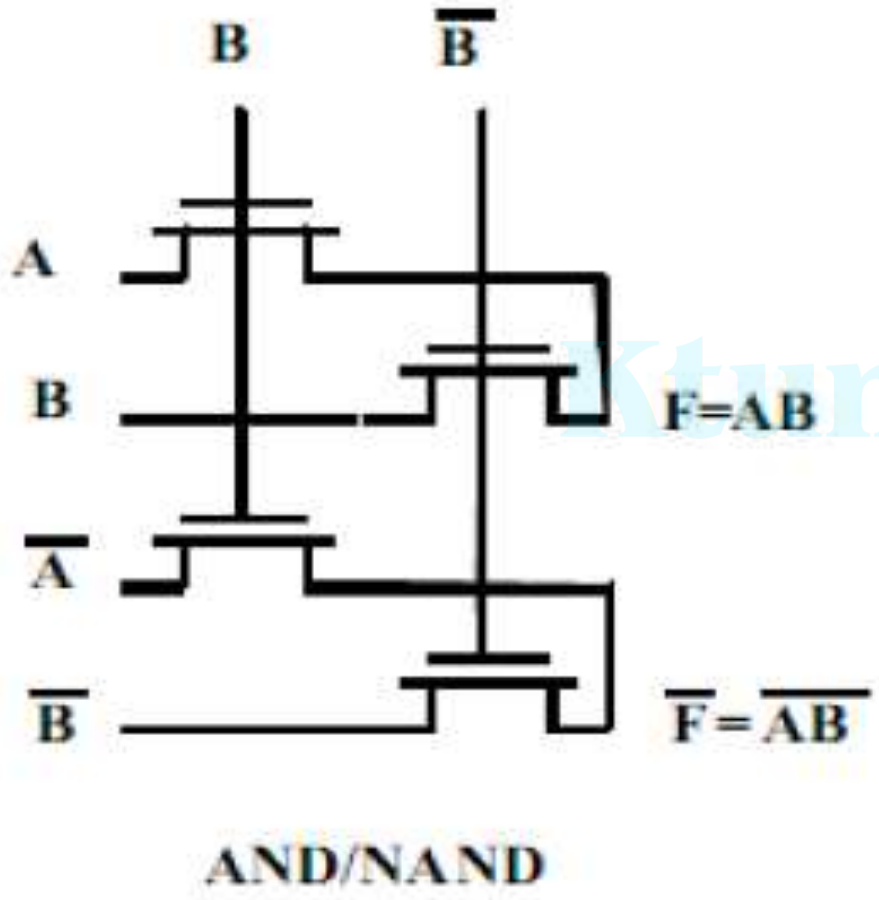
TRANSMISSION GATES

- ❑ NMOS pass transistor passes a ***strong*** 0 and a ***weak*** 1.
- ❑ PMOS pass transistor passes a ***strong*** 1 and a ***weak*** 0.
- ❑ Combine the two to make a CMOS pass gate which will pass a ***strong*** 0 and a ***strong*** 1.
- Pass transistors produce degraded outputs
- *Transmission gates* pass both 0 and 1 well

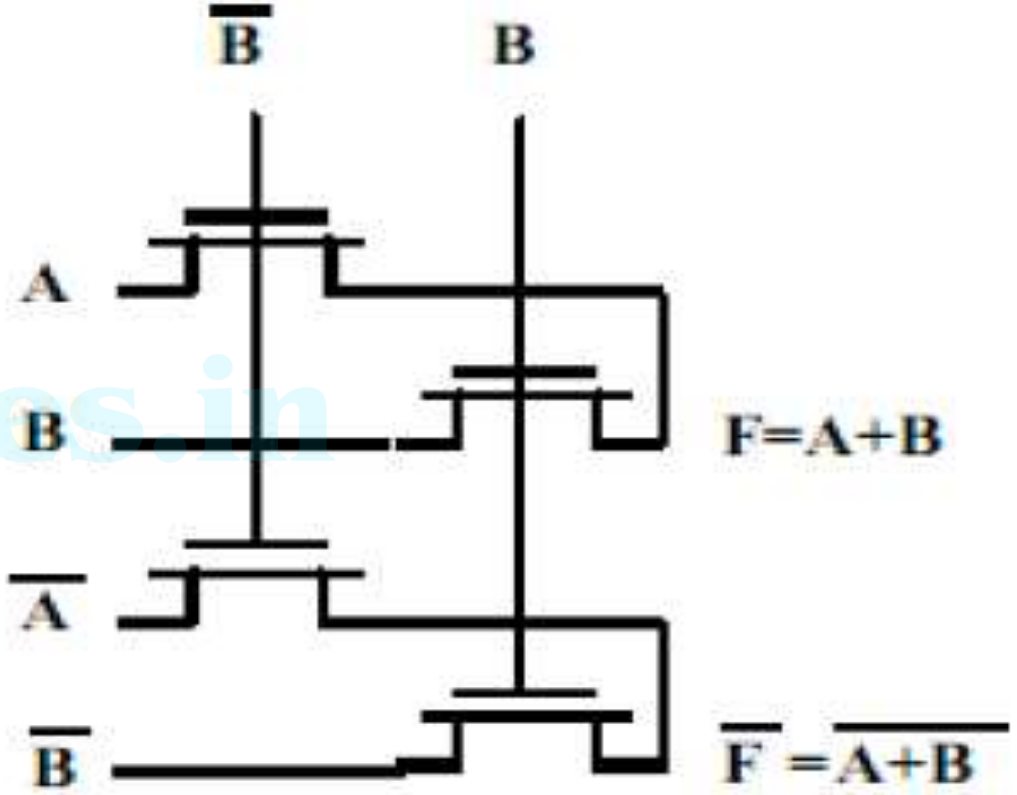
Complementary Pass Transistor Logic

- Some logical circuits using PTL

To accept and produce true and complementary inputs and outputs.

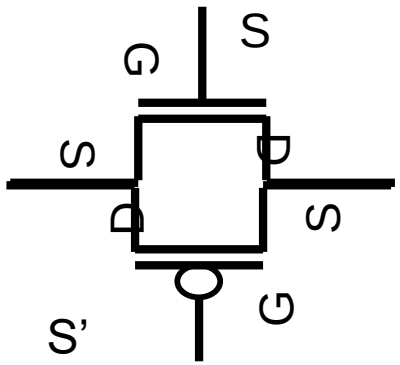


AND/NAND

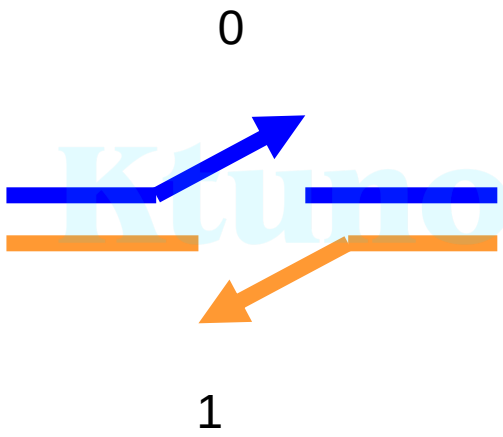


OR/NOR

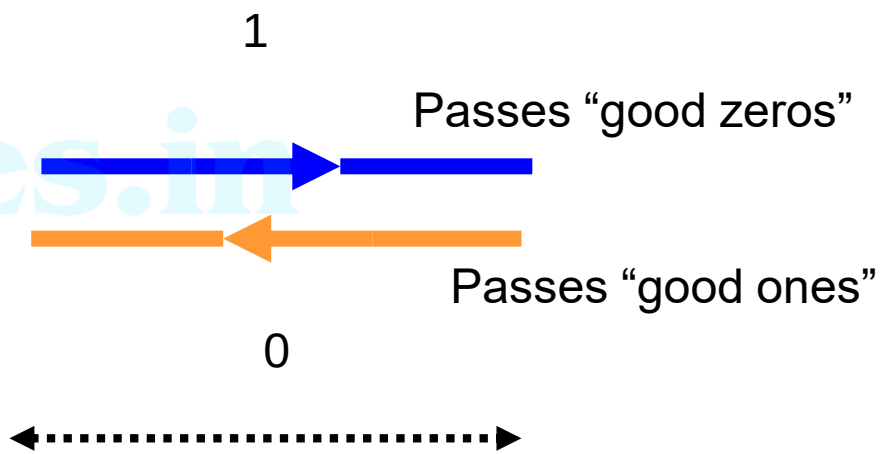
N Switch



P Switch



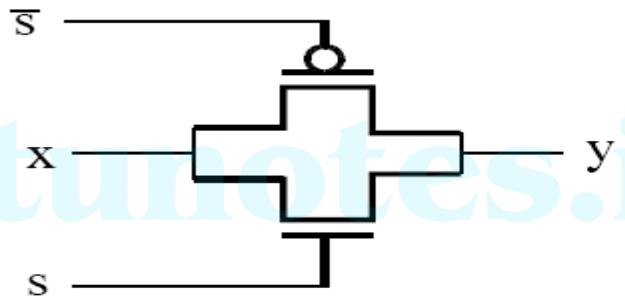
Open Circuit, High Z



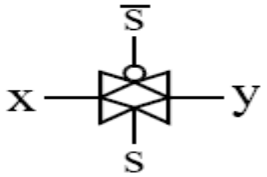
Bi-directional Switch

Transmission Gates

- A *transmission gate* is a essentially a switch that connects two points. In order to pass 0's and 1's equally well, a pair of transistors (one N-Channel and one P-Channel) are used as shown below:



Circuit



Symbol

When s = 1 the two transistors conduct and connect x and y

The top transistor passes x when it is 1 and the bottom transistor passes x when it is 0

When s = 0 the two transistor are cut off disconnecting x and y

Transmission Gates

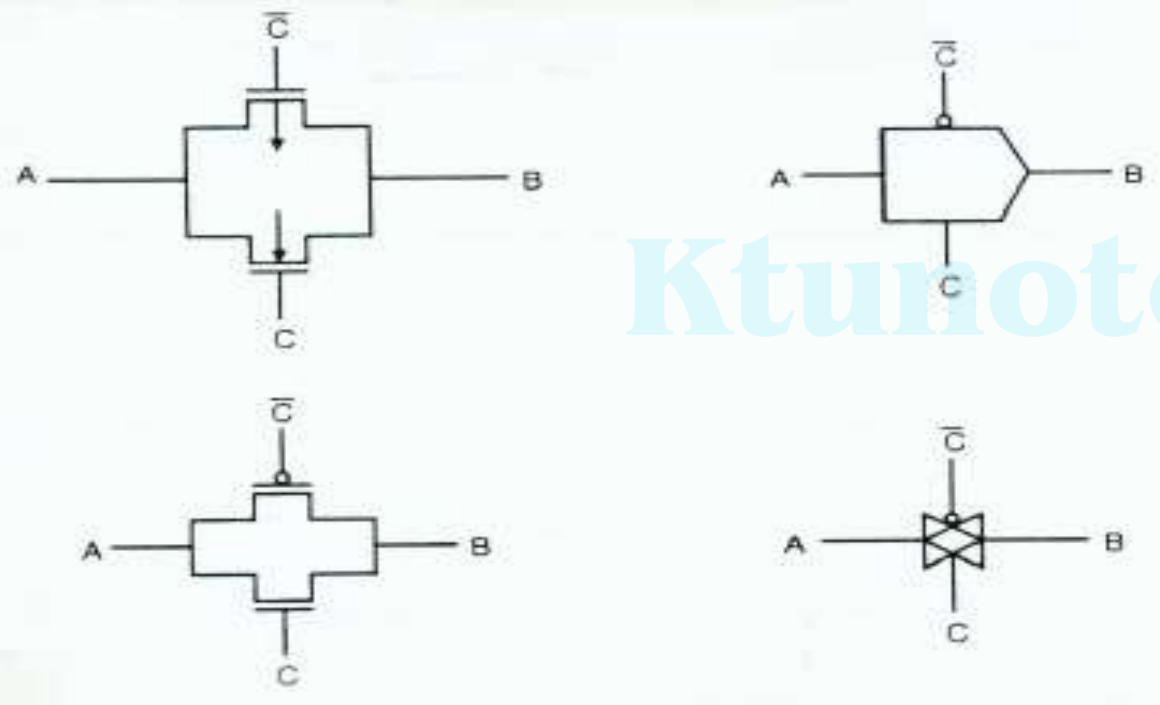
– **Operation**

- **S** is logic high ⇒ Both transistors are turned on and provide a low-resistance current path between nodes ***X*** and ***Y***.
- **S** is logic low ⇒ Both transistors will be off, and the path between nodes ***X*** and ***Y*** will be open circuit. This condition is called the *high-impedance state*.

– With the parallel **pFET** added, it can transfer a full V_{DD} from ***X*** to ***Y*** (or ***Y*** to ***X***). It can also charge driven capacitance faster.

– The substrates of **NMOS** and **PMOS** are connected to ***ground*** and V_{DD}, respectively. Therefore, the substrate-bias effect must be taken into account.

Analysis of CMOS TG



$A : Input$

$B : Output$

$C : Control\ Signal$

$$C = \begin{cases} 0,\ Z\ (high\ impedance) \\ 1,\ B = A \end{cases}$$

Transmission Gate Circuits

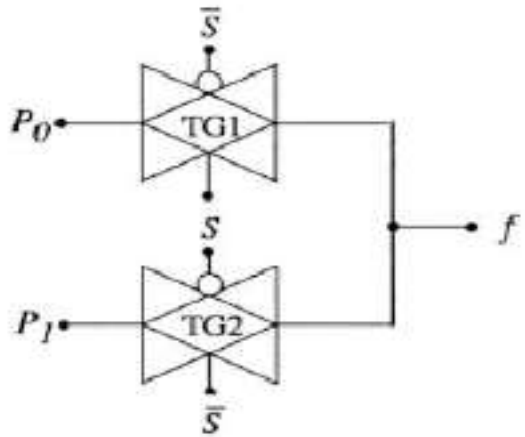
- A CMOS TG is created by connecting an nFET and pFET in parallel
  - Bi-directional
  - Transmit the entire voltage range [0, V_{DD}]

$$y = x \cdot s \quad iff \quad s = 1$$

$$y = x \cdot \bar{s} \quad iff \quad \bar{s} = 1$$

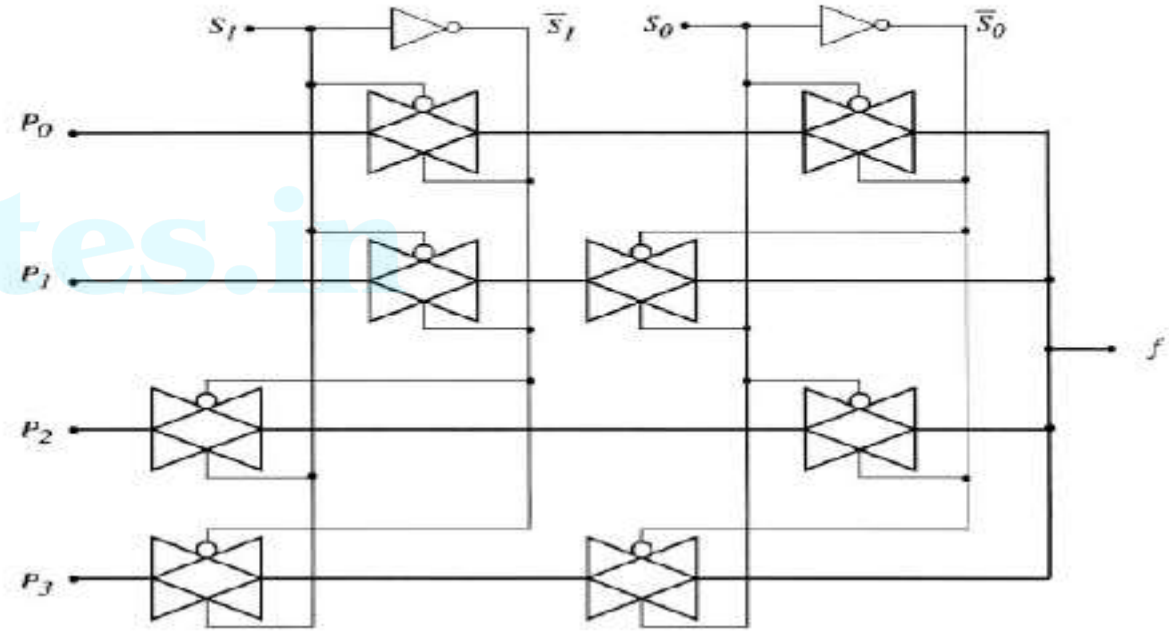
Figure Transmission gate (TG)

TG 2:1 Multiplexor

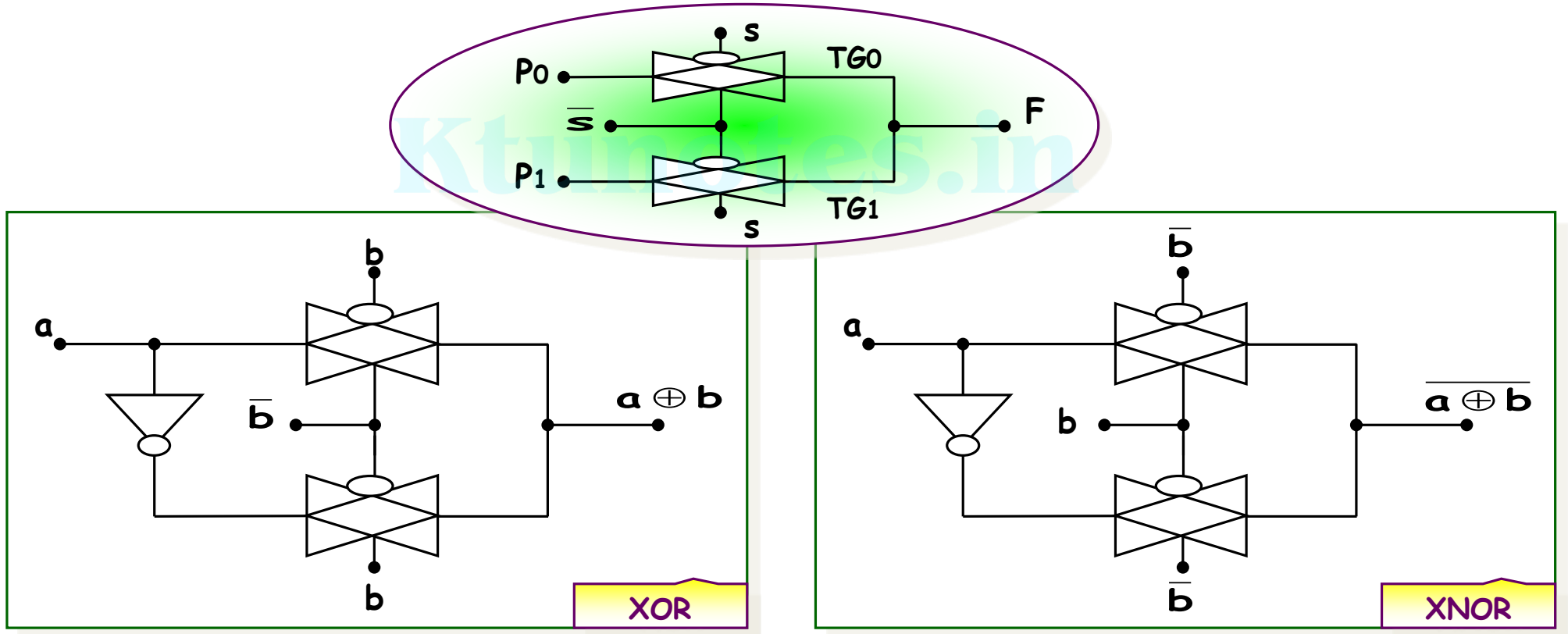


$$f = P_0 . S + P_1 . \bar{S}$$

TG 4:1 Multiplexor



- The 2:1 MUX can be modified to produced other useful function, such as XOR & XNOR circuits.



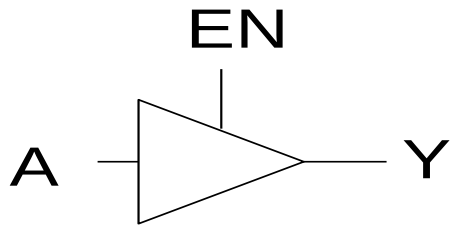
$f = A.\bar{B} + \bar{A}.B$

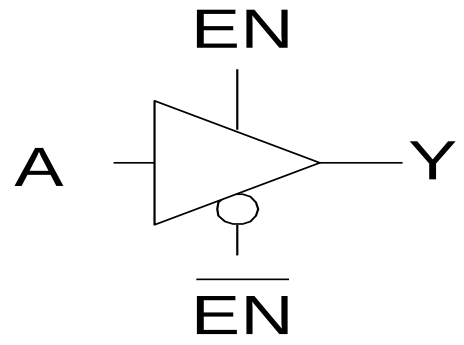
$f = A.B + \bar{A}.\bar{B}$

Tristates

- *Tristate buffer* produces Z when not enabled

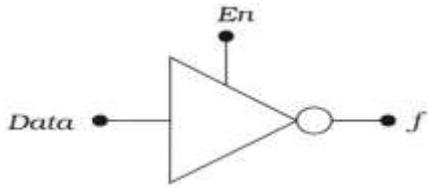
EN	A	Y
0	0	
0	1	
1	0	
1	1	





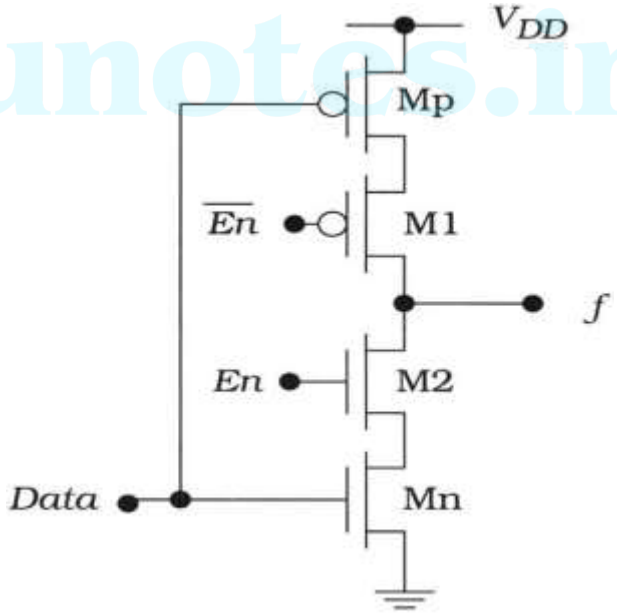
- Transmission gate acts as tristate buffer

- A tri-state circuit produces the usual 0 and 1 voltages, but also has a third high impedance Z (or Hi-Z)
  - Useful for isolating circuits from common bus lines
  - In Hi-Z case, the output capacitance can hold a voltage even though n hardwire connection exists
- A non-inverting circuit (a buffer) can be obtained by adding a regular static inverter to the input



En	f
0	Z
1	$\overline{Data}$

(a) Symbol and operation

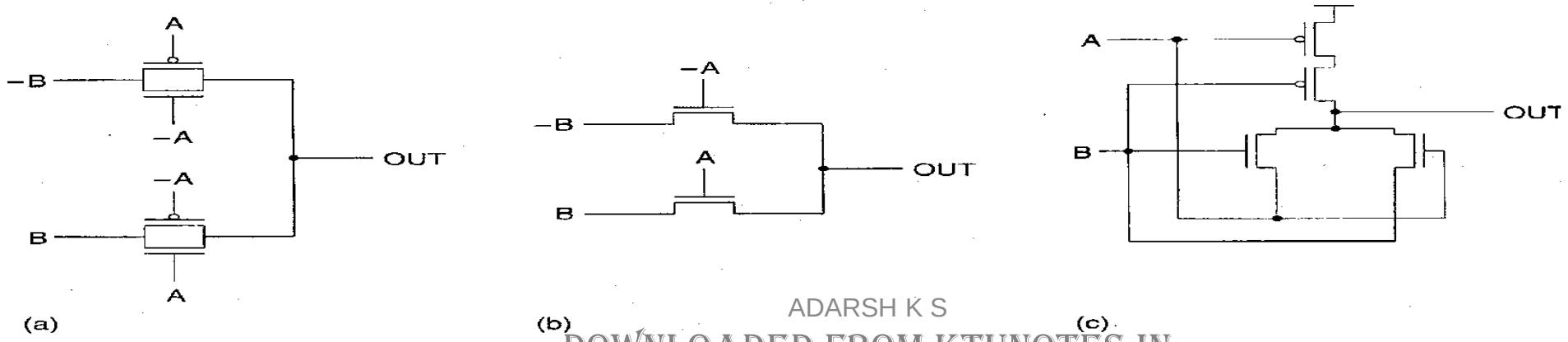


(b) CMOS circuit

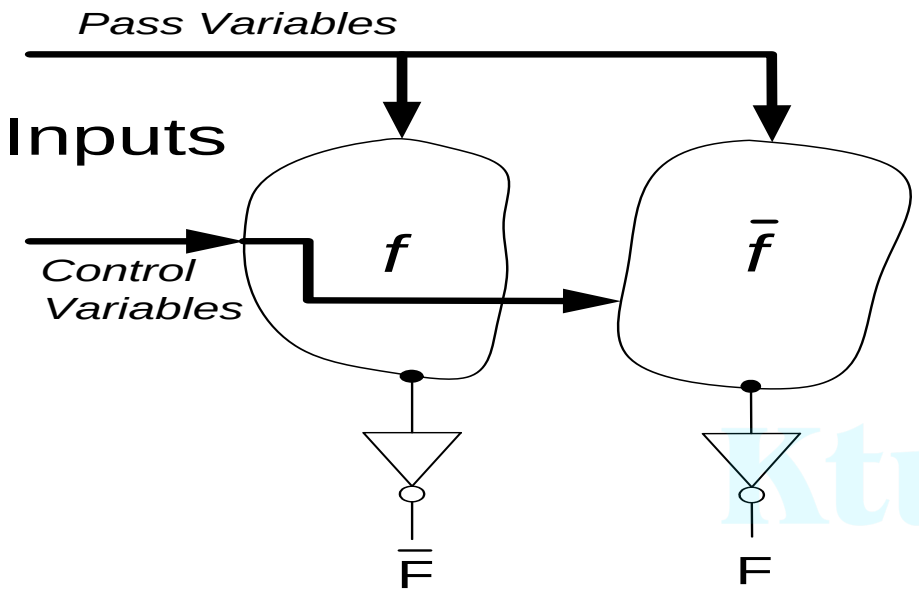
Complementary Pass-Transistor Logic (CPL)

The term "complementary pass transistor logic" to indicate a style of implementing logic gates that uses transmission gates composed of both NMOS and PMOS pass transistors

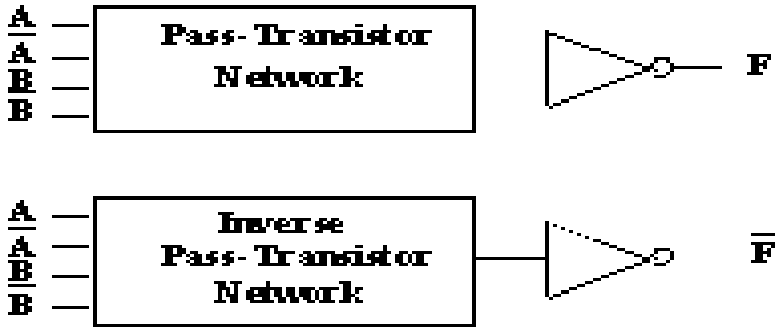
- Utilizes CMOS transmission gate (or just the single polarity version of TG) to perform logic
  - Logical inputs may be applied to both the device gates as well as device source/drain regions
  - Only a limited number of Pass Gates may be ganged in series before a clocked Pull-up (or pull-down) stage is required
- (a) and (b) show simple XNOR implementation:
  - If A is high, B is passed through the gate to the output
  - If A is low, -B is passed through the gate to the output
- (c) shows XNOR circuit including a cross-coupled input with P pull-up devices which does not require inverted inputs

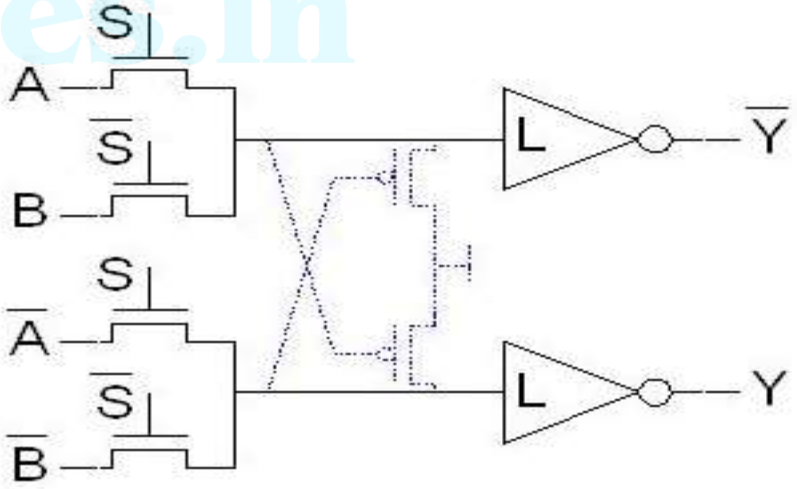


Complementary Pass-Transistor Logic (CPL)

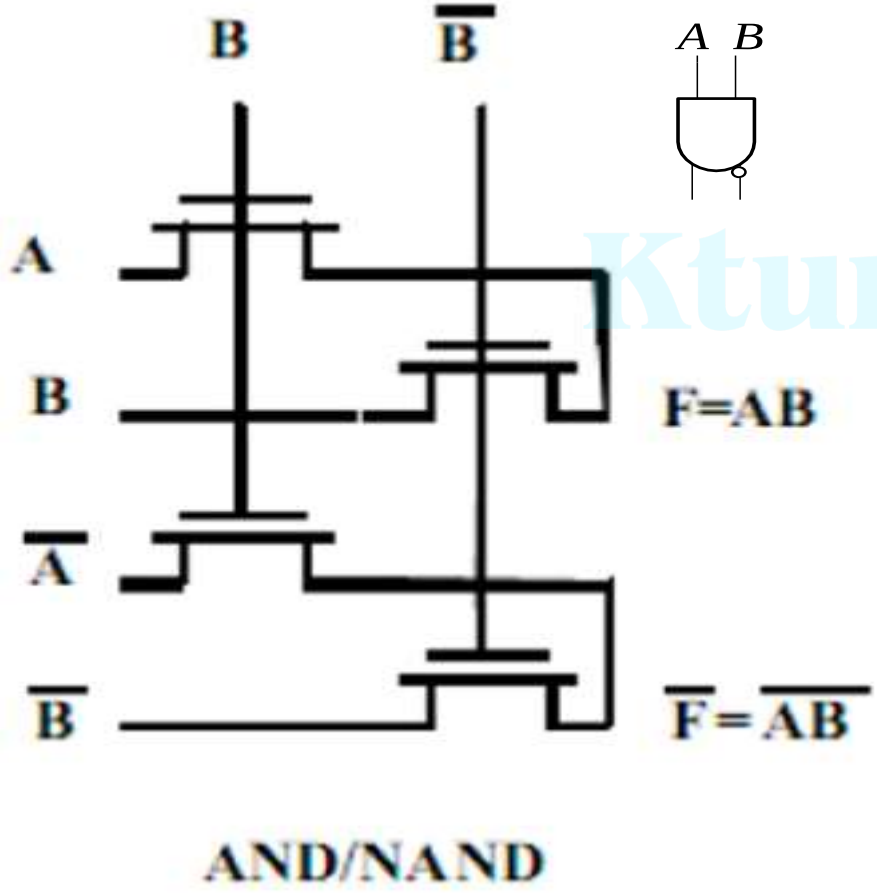


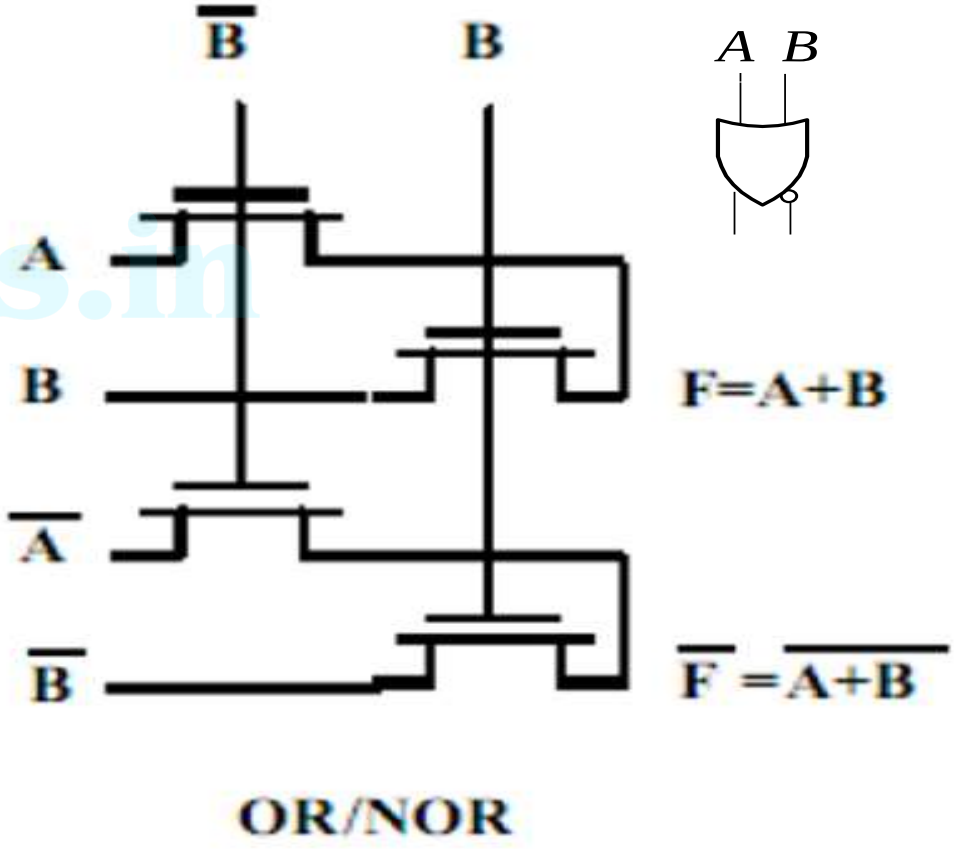
- **C**omplementary **P**ass-transistor **L**ogic
  - Dual-rail form of pass transistor logic
  - Avoids need for ratioed feedback
  - Optional cross-coupling for rail-to-rail swing

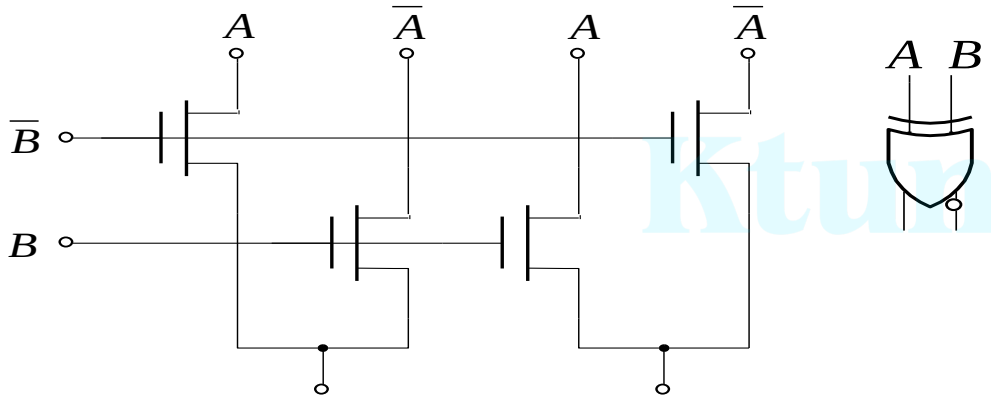




Basic logic functions in CPL







XOR/XNOR