GOVT. COLLEGE OF ENGINEERING KANNUR

Department of Electronics and Communication Engineering

Third Semester First Series Examination November- 2022 (2019 Scheme)

Course code: ECT203

Course Name: LOGIC CIRCUIT DESIGN

Max. Marks: 50   Duration: 90 Minutes

PART A

Answer all questions. Each question Carries 3 marks

1. Express $(6820)_{10}$ in NBCD, XS3 and 2421 codes.   (3 Marks)

2. Find x if $(211)_x=(152)_8$.   (3 Marks)

3. Express the switching function $f(A,B,C)=(A+B'+C)(A'+B'+C)(A+B'+C')$ (3 Marks)
   in Canonical SOP and Canonical POS notations.

4. State the principle of duality? Write the dual of the Boolean identity $X(Y+Z)=XY+XZ$ (3 Marks)

5. Realize a two input X-NOR function using a 2:1 Mux.   (3 Marks)

PART B

6. Design a 4bit binary to gray code converter and implement the circuit using   (14 Mark)
   EX-OR gates.

OR

7. Design a 4 bit 84-2-1 to 8421 code converter and implement the circuit using 2 level AND-OR
   gates   (14 Marks)

8. a) Simplify the Boolean function $F(A,B,C,D,E)= \sum m(0,2,5,8,13,15,18,21,24,29,31)$ (7 Marks)
   Using Karnaugh map.

   b) Write the gate level Verilog code for the above simplified expression   (7 Marks)

OR

9. a) Simplify the Boolean function $F(A,B,C,D,E,F)=\sum m(6,9,13,18,19,25,27,29,41,45,57,61)$
   Using Karnaugh map.   (8 Marks)

   b) Write the gate level Verilog code for the above simplified expression.   (6 Marks)

10. Show that 2:1 Mux is a universal multiplexer   (7 Marks)

OR

11. Implement the Boolean function $F(A,B,C,D) =\sum m(1,3, 4,11, 12,13,14,15)$ using 4:1   (7 Marks)
    Mux using A and B as select lines.