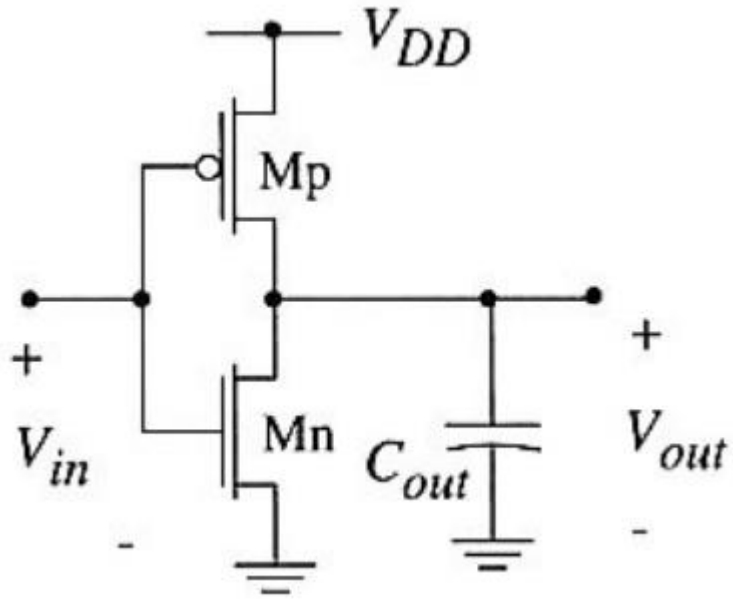
MODULE-2
1.CMOS Inverter Switching Characteristics
2.Power dissipation in CMOS

ECT304
VLSI CIRCUIT DESIGN

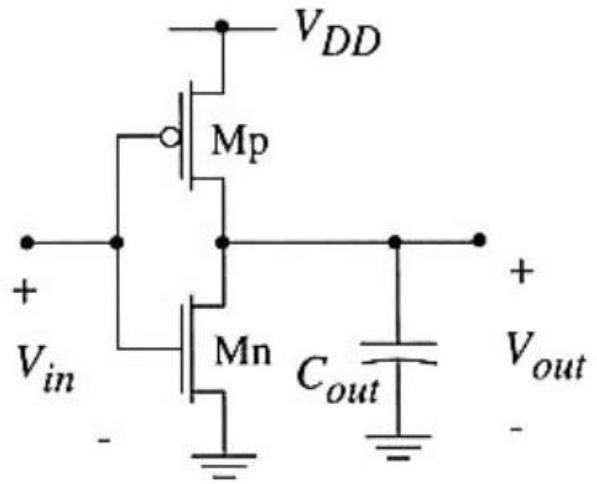
CMOS INVERTER SWITCHING CHARACTERISTICS

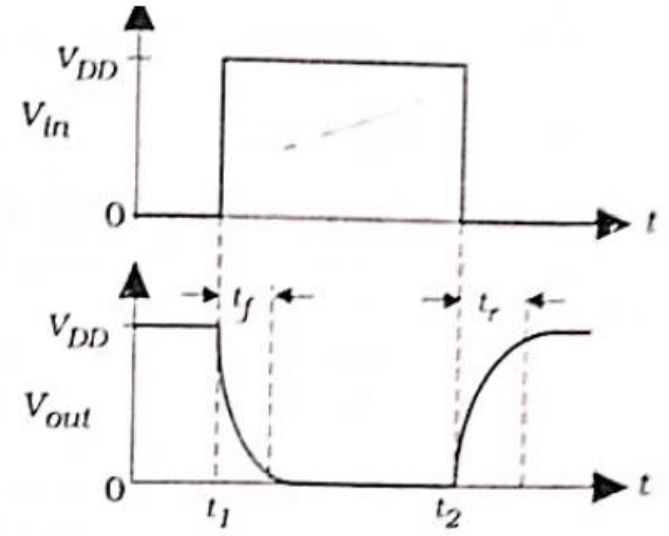
- Transient switching times are used to calculate data throughput rates and are also important in system timing.
- Switching times are determined by two circuit properties: Transistor current flow levels & parasitic capacitances.
- Both are set by the chip design parameters and are sensitive to transistor aspect ratios, layout geometry and logic routing.
- In this CMOS inverter PMOS is pull up device and NMOS is the pull down device.
- ***When the Input is High the NMOS will be ON and Capacitor Cout will discharge and Output will be Low.***
- ***When the Input is Low the PMOS will be ON and Capacitor Cout will charge and Output will be High.***



CMOS INVERTER SWITCHING CHARACTERISTICS

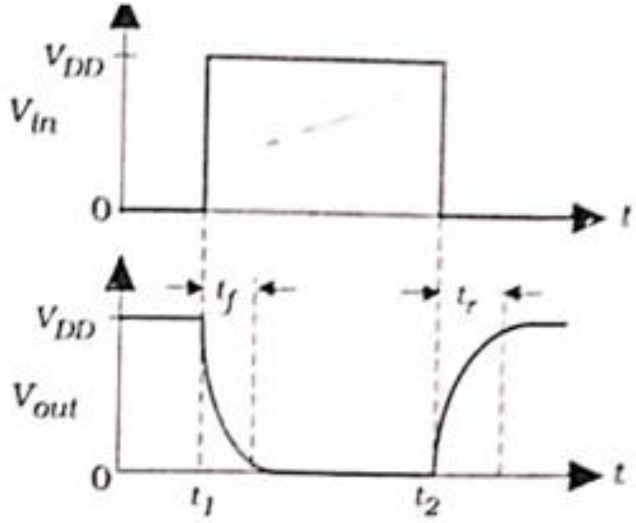
- High-speed digital system design is based on the ability to perform calculations very quickly.
- This requires that logic gates introduce a minimum amount of time delay when the inputs change.
- Designing fast logic circuits is one of the more challenging (but critical) aspects of VLSI physical design.
- An input voltage V(t) is applied to the inverter, resulting in an output voltage Vout(t).
- Assume that Vin(t) has step-like characteristics and makes an abrupt transition from 0 to 1 at time t1 and back to 1 to 0 at time t2.
- The output waveform reacts to the input, but output voltage cannot change instantaneously.

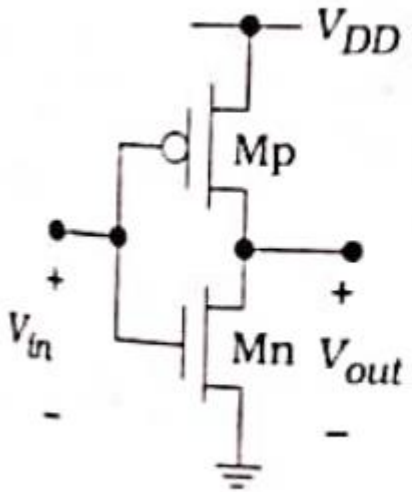


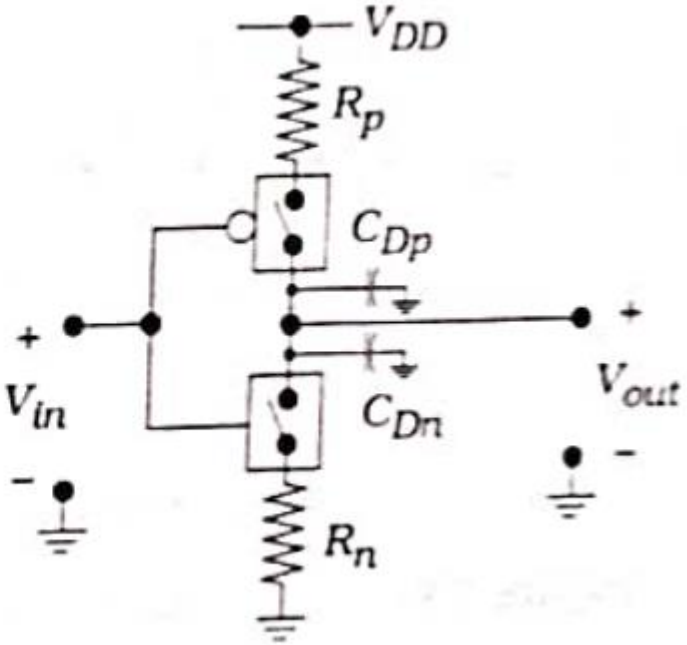


CMOS INVERTER SWITCHING CHARACTERISTICS

- The output 1 to 0 transition introduces a **Fall time delay**
- The output 0 to 1 transition introduces a **Rise time delay**
- The Rise time and Fall time delays are due to the **parasitic resistance and capacitances of the transistors.**

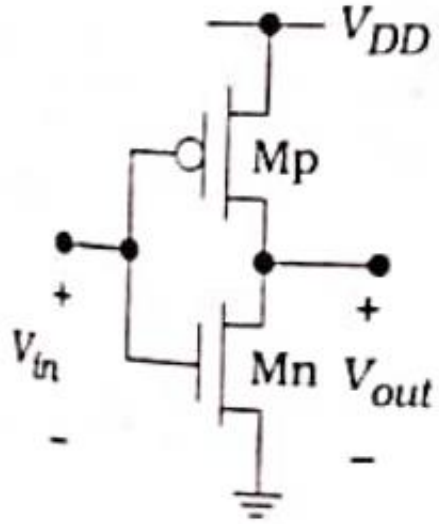


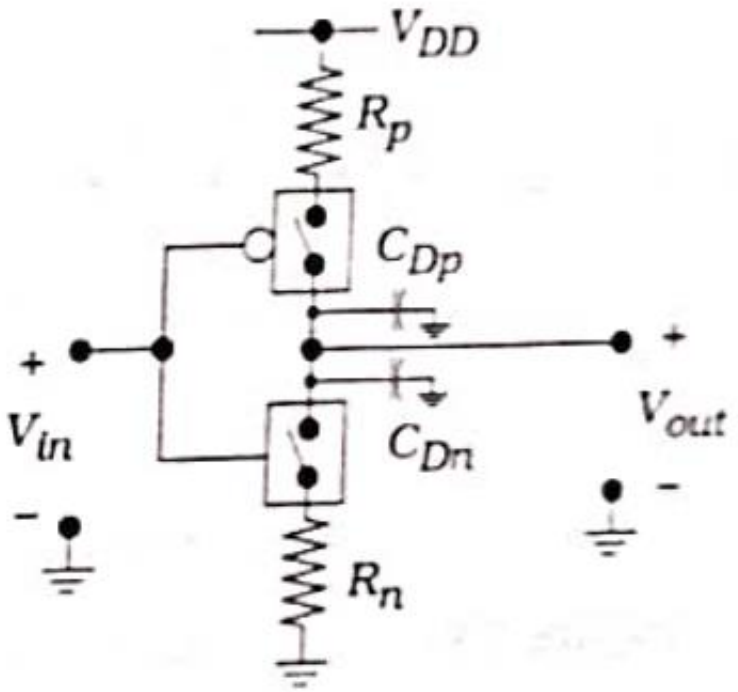




- The simplified RC model of the inverter circuit is shown with transistors replaced by switches.

CMOS INVERTER SWITCHING CHARACTERISTICS



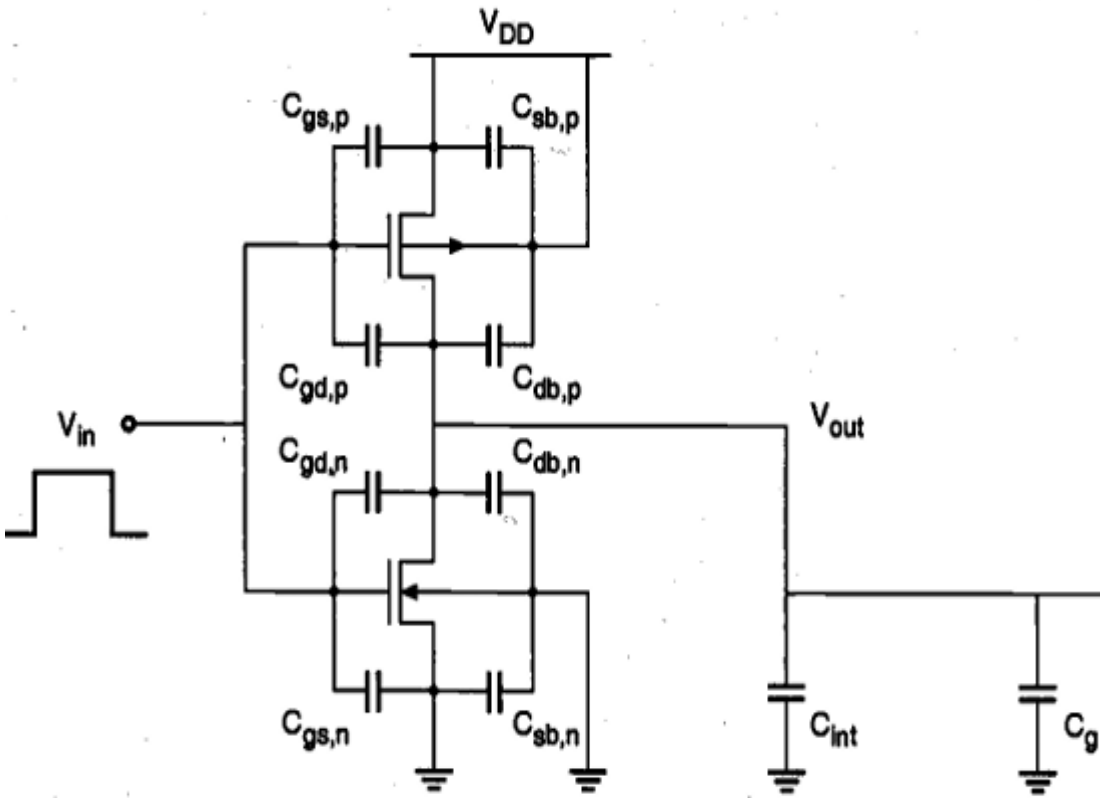


- The parasitic resistance Rn an Rp is given by

$$R_n = \frac{1}{\beta_n (V_{DD} - V_{Tn})}$$

$$R_p = \frac{1}{\beta_p (V_{DD} - |V_{Tp}|)}$$

CMOS INVERTER SWITCHING CHARACTERISTICS



Load Capacitance

$$C_{load} = C_{gd,n} + C_{gd,p} + C_{db,n} + C_{db,p} + C_{int} + C_g$$

- The capacitances C_{gd} and C_{gs} are primarily due to gate overlap with diffusion
- while C_{db} and C_{sb} are voltage-dependent junction capacitances
- The capacitance component C_g is due to the thin-oxide capacitance over the gate area.
- the lumped interconnect capacitance C_{int}, represents the parasitic capacitance contribution of the metal or polysilicon connection between the two inverters.

CMOS INVERTER SWITCHING CHARACTERISTICS

FALL TIME (t_F)

- **Fall Time:** Time interval from where output drops from **$0.9V_{DD}$ to $0.1V_{DD}$**
- Initial Condition, **$V_{out} = V_{DD}$**
- When input is switched **PMOS – OFF & NMOS – ON**
- Capacitor discharges to 0 through Rn.
- Current is leaving the capacitor, so

  $i = -C_{out}\,(dv_{out}/dt)$

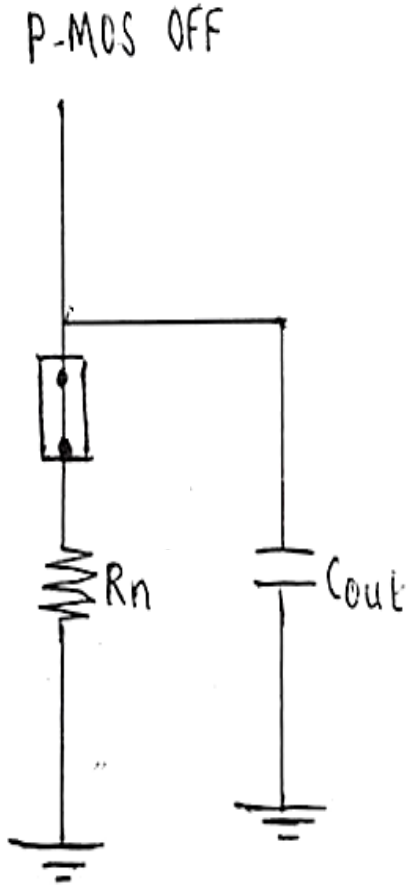
- Solving the initial condition

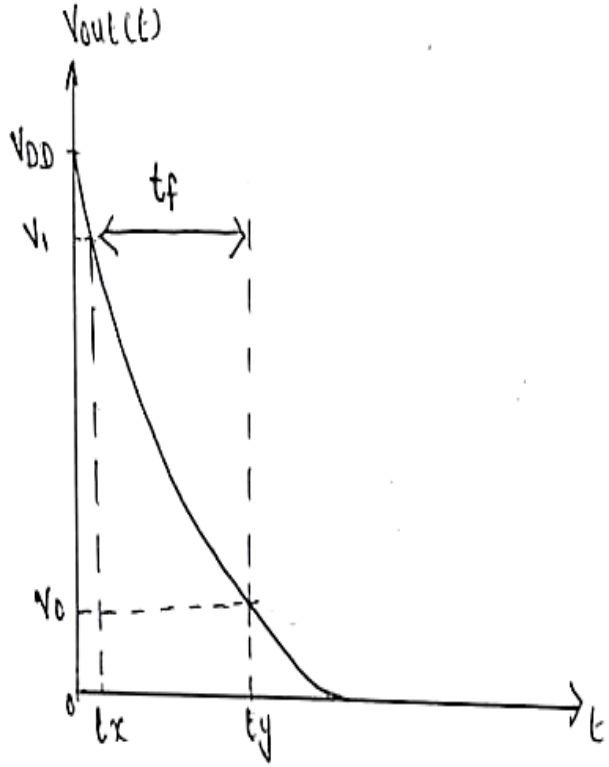
  $\tau_n = R_n C_{out}$

  $V_{out}(t) = V_{DD}.e^{-t/\tau_n}$

  $e^{-t/\tau_n} = V_{out}/V_{DD}$

  $T = \tau_n \ln(V_{DD}/V_{out})$





CMOS INVERTER SWITCHING CHARACTERISTICS

FALL TIME (t_F)

- **Fall Time:** Time interval from where output drops from **$0.9V_{DD}$ to $0.1V_{DD}$**

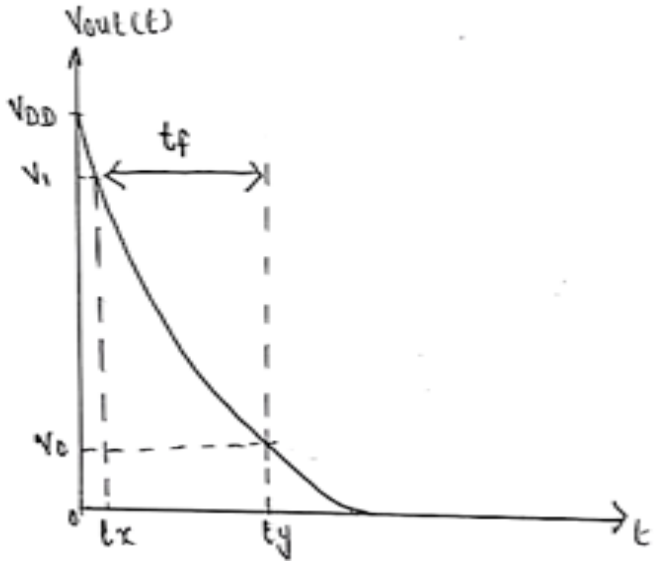
$$T = \tau_n \ln(VDD/Vout)$$

$$Tf = ty - tx$$

$$= \tau_n \ln(VDD/0.1VDD) - \tau_n \ln(VDD/0.9VDD)$$

$$= \tau_n \ln(9)$$

$$Tf = 2.2\ \tau_n$$

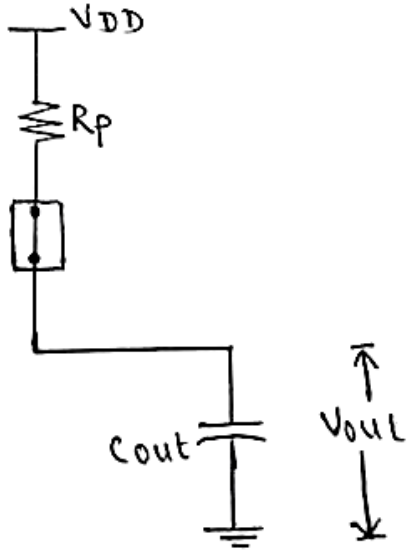


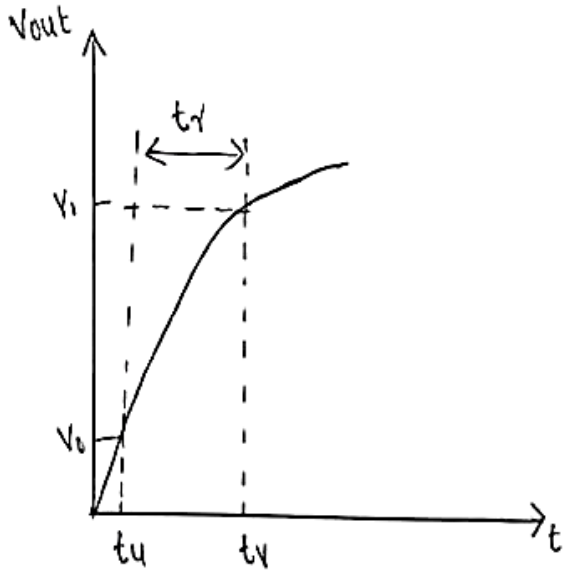
CMOS INVERTER SWITCHING CHARACTERISTICS

RISE TIME (t_R)

- **Rise Time:** Time interval where output increase from **$0.1V_{DD}$ to $0.9V_{DD}$**
- Initial Condition, **$V_{out} = 0$**
- When input is switched **PMOS – ON & NMOS – OFF**
- Capacitor charged to V_{DD} through Rp.
- Charging current, so

  i= Cout (dvout/dt)





- Solving the initial condition

  $\tau p = RpCout.$

$$Vout(t) = VDD[1 - e^{-t/\tau p}]$$

$$e^{-t/\tau p} = (VDD - Vout)/VDD$$

$$T = \tau p \ \ln. VDD/(VDD - Vout)$$

CMOS INVERTER SWITCHING CHARACTERISTICS

RISE TIME (t_R)

- **Rise Time:** Time interval where output increase from $\mathbf{0.1V_{DD}}$ **to** $\mathbf{0.9V_{DD}}$

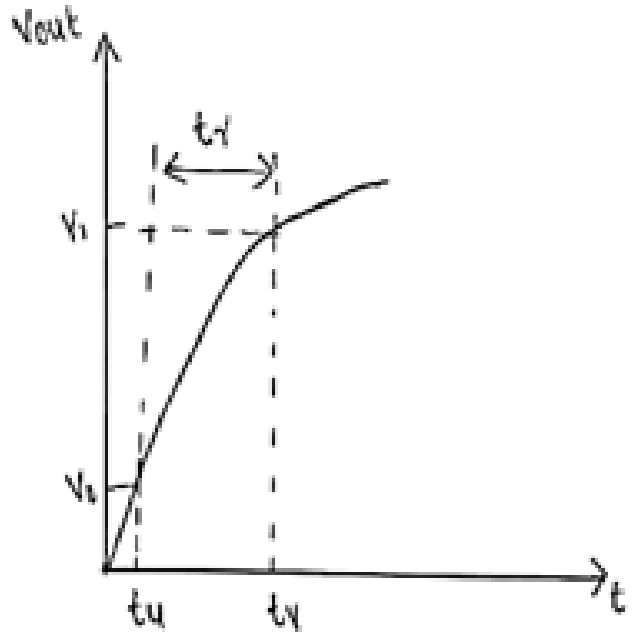
$$T = \tau_p \ln.[VDD/(VDD - Vout)]$$

$$Tr = tv - tu$$

$$= \tau_p \ln(VDD/VDD-0.9VDD) - \tau_p \ln(VDD/VDD-0.1VDD)$$

$$= \tau_p \ln(9)$$

$$\boxed{Tr = 2.2\ \tau_p}$$



CMOS INVERTER SWITCHING CHARACTERISTICS

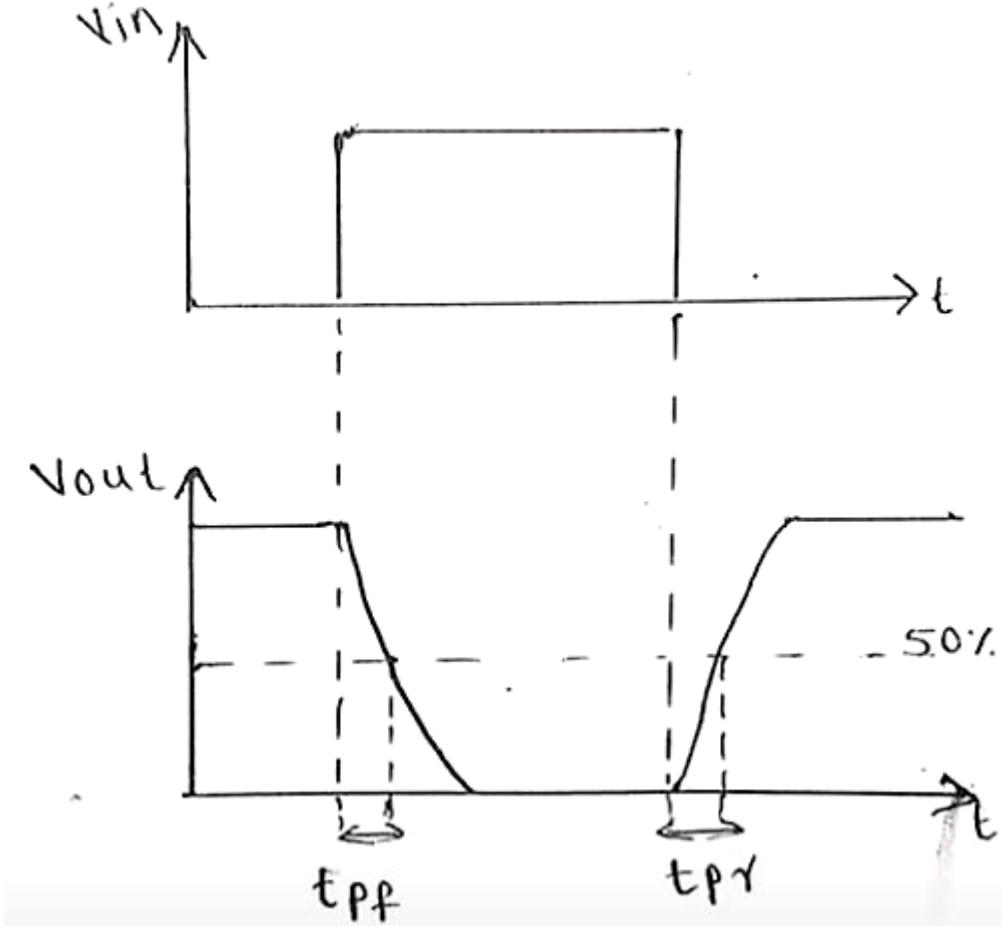
PROPAGATION DELAY (t_P)

- It is used to estimate delay time from input to output.
- It is given by $Tp = (tpf + tpr)/2$
- T_{pf} – time interval for the output to fall from maximum level to 50% of voltage **(V_{DD} to 0.5 V_{DD})**
- T_{pr}- time interval for the output to rise from minimum level to 50% of voltage **(0 to 0.5 V_{DD})**

$$Tpf = \ln 2\ \tau n$$

$$Tpr = \ln 2\ \tau p$$

$$Tp = 0.35(\tau n + \tau p)$$

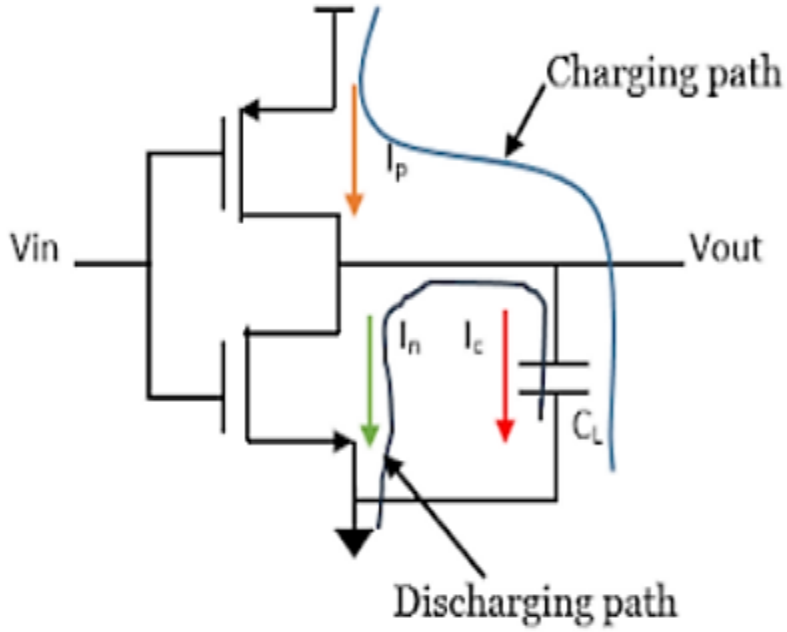


SOURCES OF POWER DISSIPATION IN CMOS

- Power dissipation in CMOS comes from two components.
- **Dynamic dissipation due to**
  - **Charging and discharging load capacitance** as gate switches.
  - **Short circuit current** while both PMOS & NMOS are partially ON.

$$P_{dynamic} = P_{switching} + P_{short\ circuit}$$

- **Static dissipation due to**
  - Sub threshold leakage through OFF transistors
  - Gate leakage through the gate dielectric
  - Junction leakage from source/drain diffusions.



DYNAMIC POWER DISSIPATION

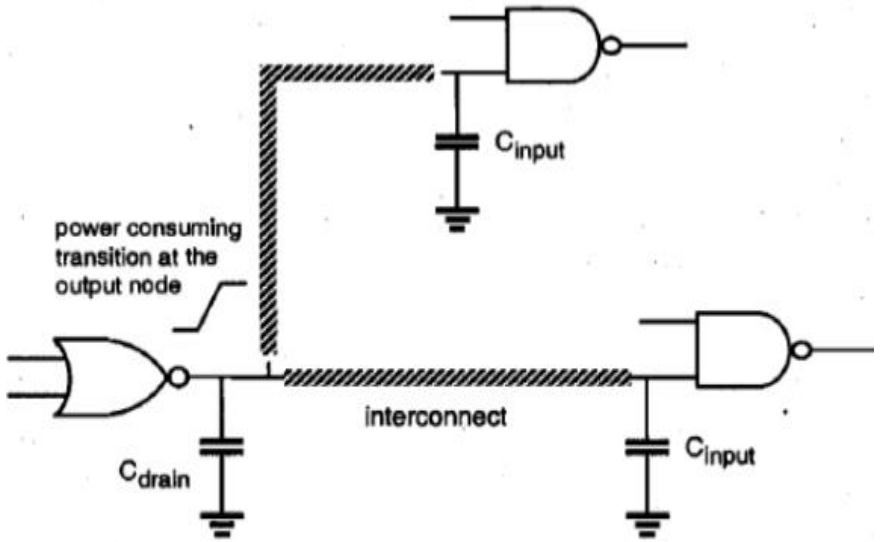
• SWITCHING POWER DISSIPATION

- Switching Power Dissipation represents the **power dissipation during a switching event.**
- Switching power dissipation means the **power dissipation due to charging and discharging of load capacitor** due to the transition of input from 1 to 0 or 0 to 1 state.
- consider the circuit given in Fig. Here, a two- input NOR gate drives two NAND gates, through interconnection lines. The total capacitive load at the output of the NOR gate consists of

  (1) The output capacitance of the gate itself

  (2) The total interconnect capacitance, and

  (3) The input capacitances of the driven gates.



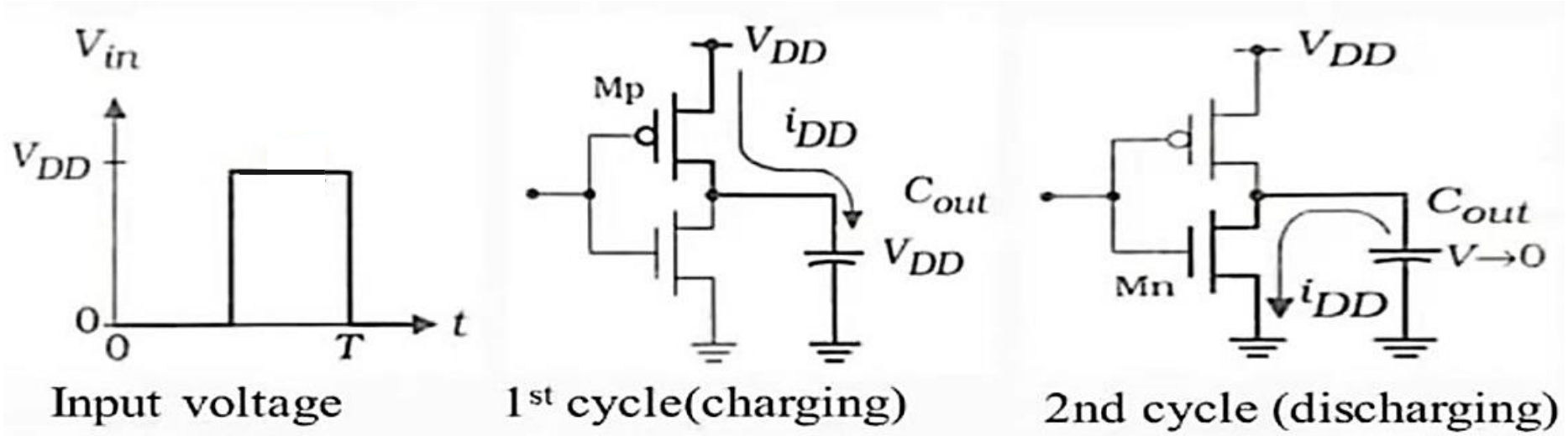
A NOR gate driving two NAND gates through interconnection lines.

DYNAMIC POWER DISSIPATION

- **SWITCHING POWER DISSIPATION**
- **Output capacitance:**
- Consists mainly of the junction parasitic capacitances, which are due to the drain diffusion regions of the MOS transistors in the circuit.
- The size of the total drain diffusion area determines the amount of parasitic capacitance.
- **Total interconnect capacitance:**
- The interconnect lines between the gates contribute to the total interconnect capacitance.
- In sub-micron technologies, the interconnect capacitance can become the dominant component, compared to the transistor-related capacitances.
- **Input capacitances:**
- Due to gate oxide capacitances of the transistors connected to the input terminal.
- The amount of the gate oxide capacitance is determined primarily by the gate area of each transistor.

DYNAMIC POWER DISSIPATION

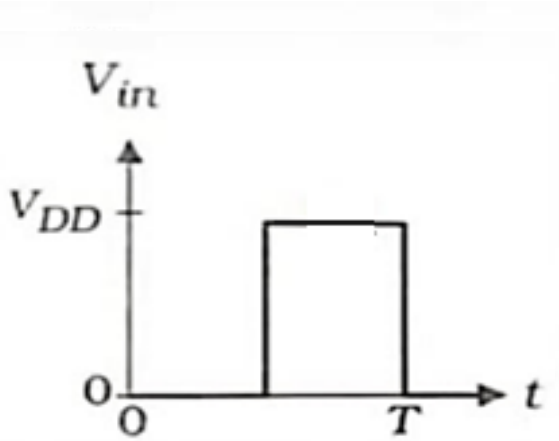
- **SWITCHING POWER DISSIPATION CALCULATION**



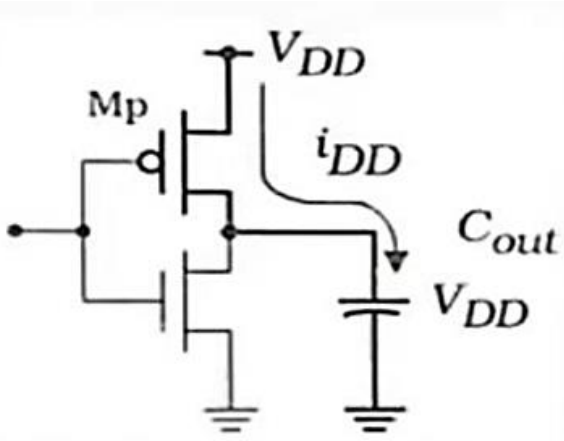
- To find the **dynamic power dissipation** we use a square wave input **vin(t)**. The period of the wave form is **T**
- In 1st half cycle ➔ Vin=0
- **NMOS is OFF, PMOS is ON,** current **I_{DD} flows through PMOS and Cout charges to a voltage of Vout=V_{DD}**

DYNAMIC POWER DISSIPATION

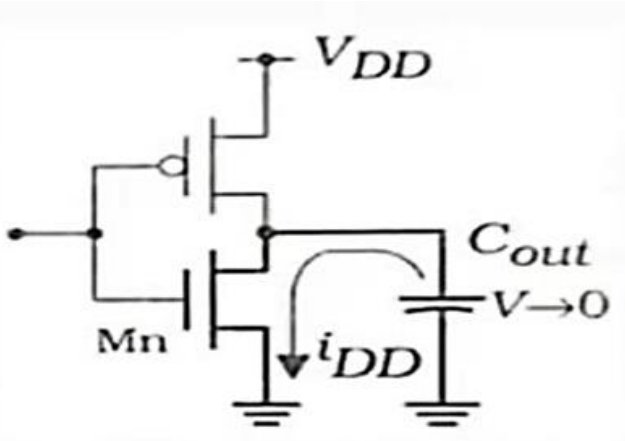
- **SWITCHING POWER DISSIPATION CALCULATION**



Input voltage



1st cycle(charging)



2nd cycle (discharging)

- In **2nd half cycle** ➔ The **input voltage is high and capacitor Cout discharges and Vout becomes zero.**
- The dynamic power pdyn arises from the observation that a complete cycle create a path for the current to flow from the power supply to ground.
- The charging event makes Cout with a output voltage of V_{DD}

DYNAMIC POWER DISSIPATION

• SWITCHING POWER DISSIPATION CALCULATION

- The stored charge in a capacitor is given by $Q_e = Co_{ut}.VDD$
- When the capacitor discharges the same amount of charge is lost.
- The average power dissipated over a single cycle with period T

$$P_{avg} = \frac{1}{T}\int_0^T i_{DD}(t).VDD\,dt$$

$$V = \frac{1}{C}\int i\,dt$$

$$\int i\,dt = C\,V$$

$$\int_0^T i_{DD}(t).\,dt = C_{out}.VDD$$

$$P_{avg} = \frac{1}{T}C_{out}.VDD.V_{DD}$$

DYNAMIC POWER DISSIPATION

- **SWITCHING POWER DISSIPATION CALCULATION**

$$P_{avg} = \frac{1}{T} C_{out}.VDD.V_{DD}$$

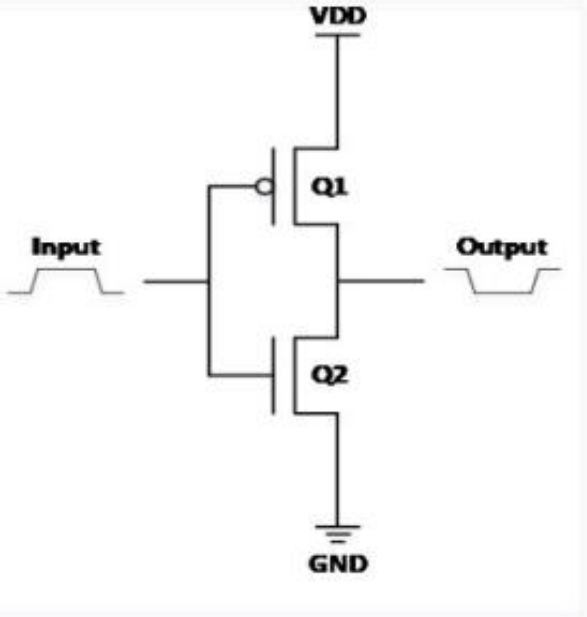
$$P_{avg} = \frac{C_{out}.VDD^2}{T} = C_{out}.VDD^2.f$$

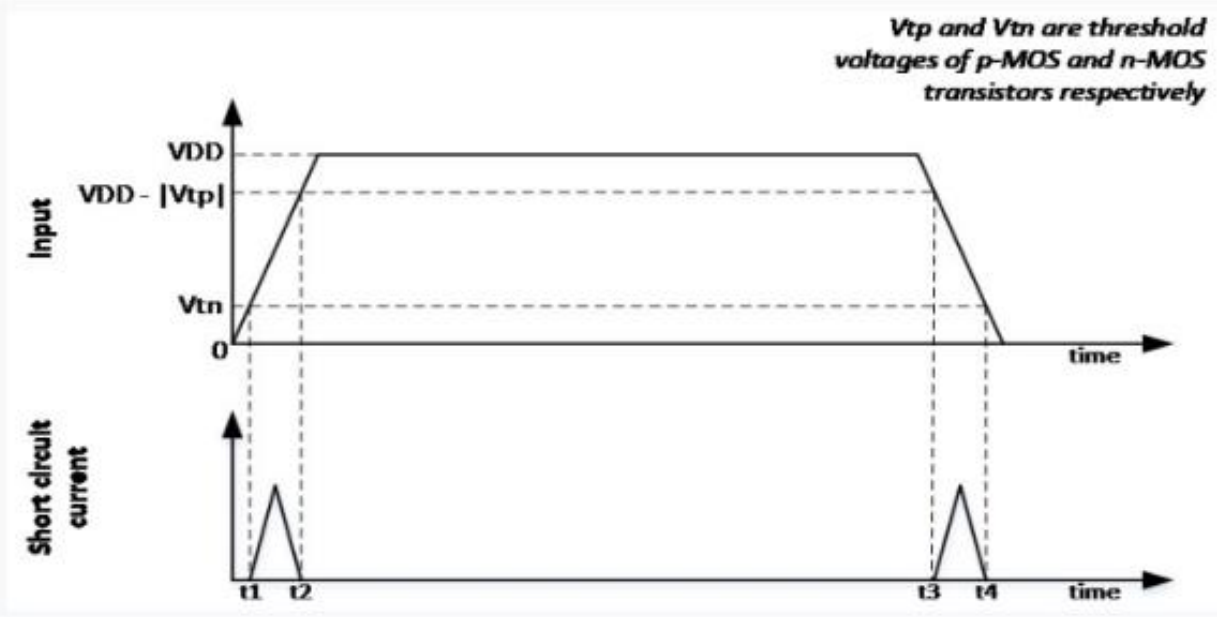
Switching power dissipation depends on **Output load capacitance**, **switching frequency** and **square of supply voltage**

DYNAMIC POWER DISSIPATION

• SHORT CIRCUIT POWER DISSIPATION

- As the input changes slowly, there will be certain duration of time for which some of the transistor(s) in the pull-up network and pull-down network are turned 'ON' simultaneously**, forming a short-circuit path from V_{DD} to GND**
- This is called **Short Circuit power dissipation.**





STATIC POWER DISSIPATION

- **Power dissipation** in CMOS **when there is no input transition.**
- The nMOS and pMOS transistors used in a CMOS logic gate generally have nonzero reverse leakage and sub threshold currents.
- In a CMOS VLSI chip containing a very large number of transistors, these currents can contribute to the overall power dissipation even when the transistors are not undergoing any switching event.
- **Static power dissipation is CMOS inverter is comparatively less than when compared with NMOS inverter.**
- The magnitude of the leakage currents is determined mainly by the processing parameters.
- Two main leakage current components found in a MOSFET are

    (1) Reverse diode leakage current

    (2) Sub threshold leakage current