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VLSI CIRCUIT DESIGN

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Why VLSI?

- Integration improves the design
 - Lower parasitics = higher speed
 - Lower power consumption
 - Physically smaller
- Integration reduces manufacturing cost -
(almost) no manual assembly

Levels of Integration

Tech	No. of Tran.
• SSI	< 10
• MSI	< 100
• LSI	1000-10000
• VLSI	10000-1000000
• ULSI	1000000-100000000
• Today	More than that

VLSI Applications

- VLSI is an implementation technology for electronic circuitry - analogue or digital
- It is concerned with forming a pattern of interconnected switches and gates on the surface of a crystal of semiconductor
- Microprocessors
 - personal computers
 - microcontrollers
- Memory - DRAM / SRAM
- Special Purpose Processors - ASICS (CD players, DSP applications)
- Optical Switches
- Has made highly sophisticated control systems mass-producible and therefore cheap

Moore's Law

- Gordon Moore: co-founder of Intel
- Moor's first law:-Predicted that the number of transistors per chip would grow exponentially (double every 18 months)
- Exponential improvement in technology is a natural trend:
 - e.g. Steam Engines - Dynamo – Automobile
- Moor's second law:-Cost of semiconductor plant doubles every four year

Why silicon ?

- Silicon is the most abundant material on the earths crust
- Inexpensive
- Ideal band energy gap
- Easier processing
- Excellent quality of SiO₂
- Ideal physical and chemical properties
- Lower defect
- Excellent Si-SiO₂ interface...etc

Clean room in National Semiconductor



Steps for Wafer fabrication



Step1: Metallurgical grade Si from SiO₂ (quartzite)

- Silicon wafers are obtained from quartzite
- Quartzite is heated with coke, charcoal, etc in an electric arc furnace to give 98% pure Si
- $\text{SiO}_2 \text{ (s)} + 2\text{C} \text{ (s)} \rightarrow \text{Si (l)} + 2\text{CO}$
- 6 to 8hr process
- 1700 oC



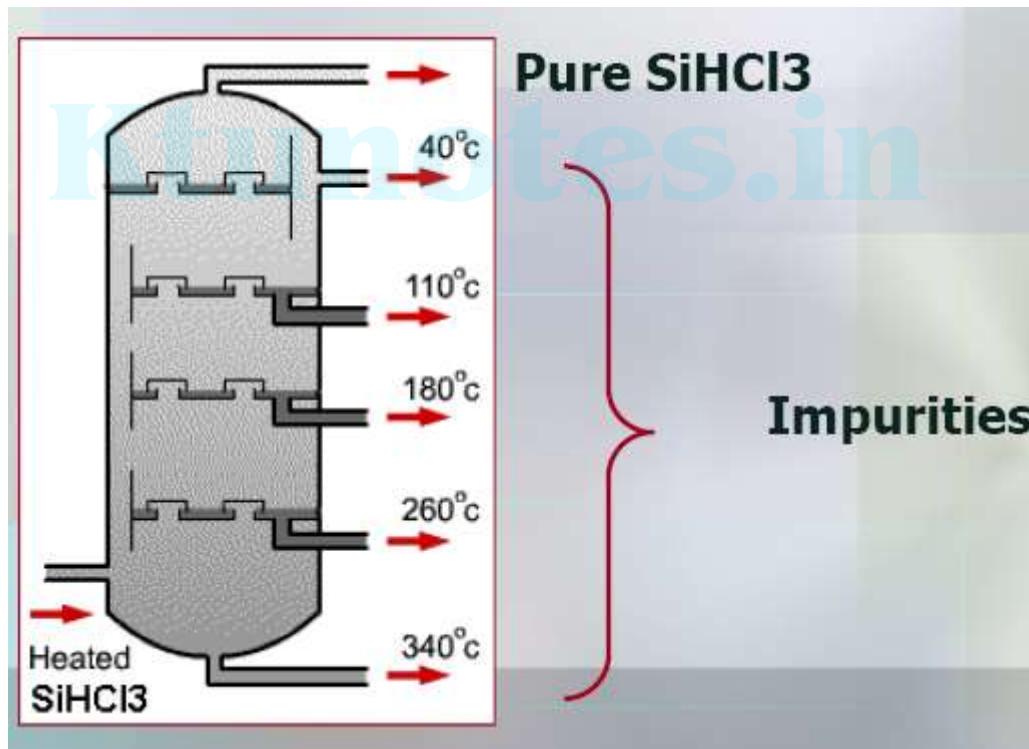
- Liquid crystal solidified to obtain Metallurgical grade Si (MGS)
- High purity of around 98%

Step 2 :Electronic Grade Si

- The impurities present in MGS are iron, Al and C
- MGS further purified to obtain EGS –used in IC
- EGS-poly crystalline material and is highly pure
- Pulverized Si is treated with anhydrous HCl at 300°C to form tri-chloro Silane (SiHCl_3)



- Fractional distillation of SiHCl₃ to remove unwanted impurities



- Reduction of SiHCl₃ in Hydrogen to form Electronic Grade Si (EGS)



- Polycrystalline Si obtained

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- **Polycrystalline materials** are solids that are composed of many crystallites of varying size and orientation

Step 3:Forming single crystal Si cube

- ❑ EGS is polycrystalline material
- ❑ In crystal growth EGS are converted to pure and defect free crystal
- ❑ In single crystal regularity is maintained throughout entire volume
 - ❖ Two silicon crystal orientation for manufacturing IC s ,ie (111) and (100)

(111) plane

- ❑ silicon have the largest number of atoms per cm²,

(100) plane

- ❑ The lowest number of atoms per cm²
- ❑ (111) oxidize faster than (100) ,oxidation rate is proportional to number of silicon atoms available for reaction
- ❑ (111) surface have higher density of electrical defects
- ❑ (100) has superior electrical properties of si/sio₂ interface dominant in manufacturing today
- ❑ Earlier many bipolar technology used(111) crystals

Notes....

EGS is Raw material for preparation single crystalline si

Crystal -regular array of identical units over long range

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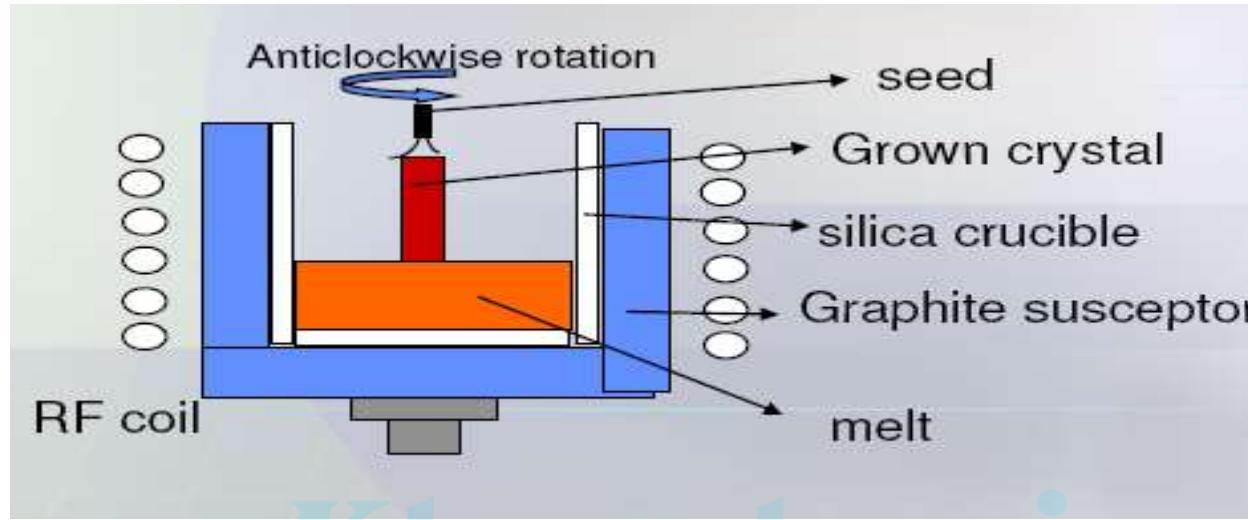
Crystal Growth

- ❑ The polycrystalline si rods(EGS) converted in to even proper and defect free crystals
- ❑ Two main crystal growth technique
 - ✓ **Czochralski technique(CZ)**
 - ✓ **Float zone technique(FZ)**
- ❑ In both the cases single crystal is obtained from by controlled re crystallization of silicon from the liquid-solid silicon system
- ❑ (ie).solidification of si atom takes place from a liquid phase at solid liquid interface

Czochralski Process

- ❑ Involves solidification of atom from liquid phase at the interface
- ❑ Involves solidification of a crystal from melt

The apparatus used for CZ crystal growth known as ‘puller’



❑It will hold 60 kg of si

Four main parts

- 1).Furnace 2).crystal pulling mechanism 3).Ambient control 4).control system

Furnace include fused silica crucible ,graphite susceptor , a rotation mechanism ,heating element and power supply

1).Furnace

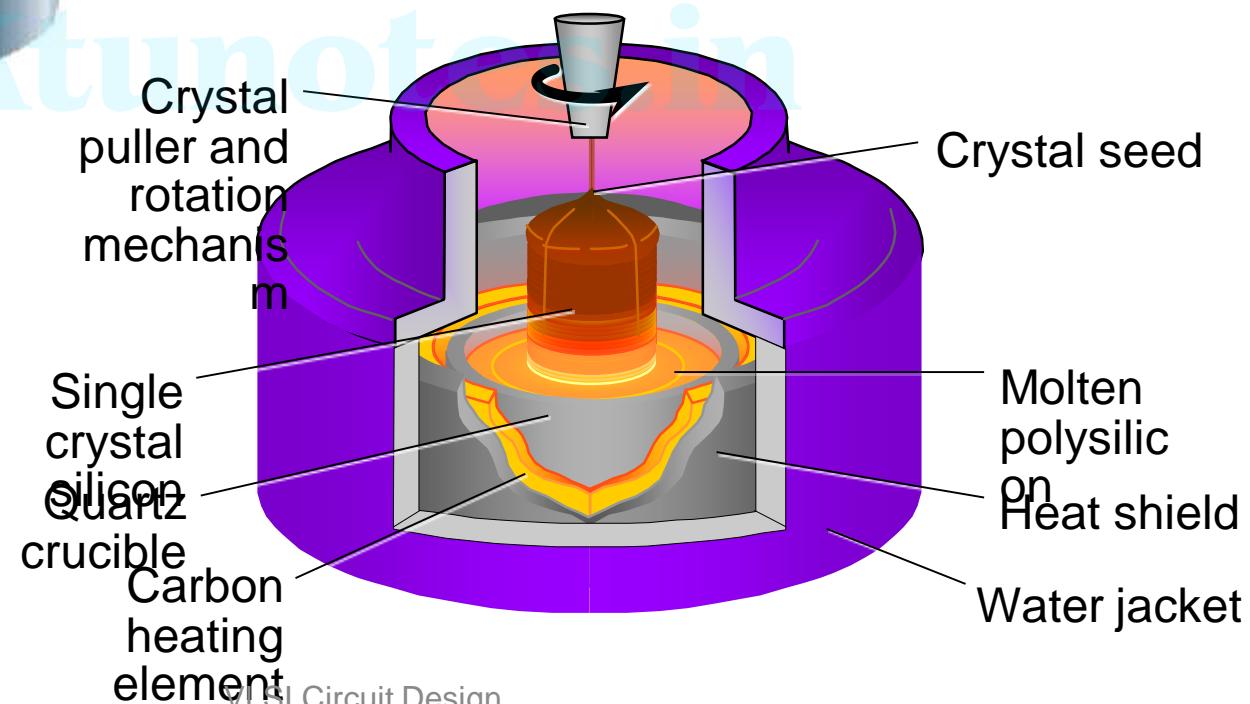
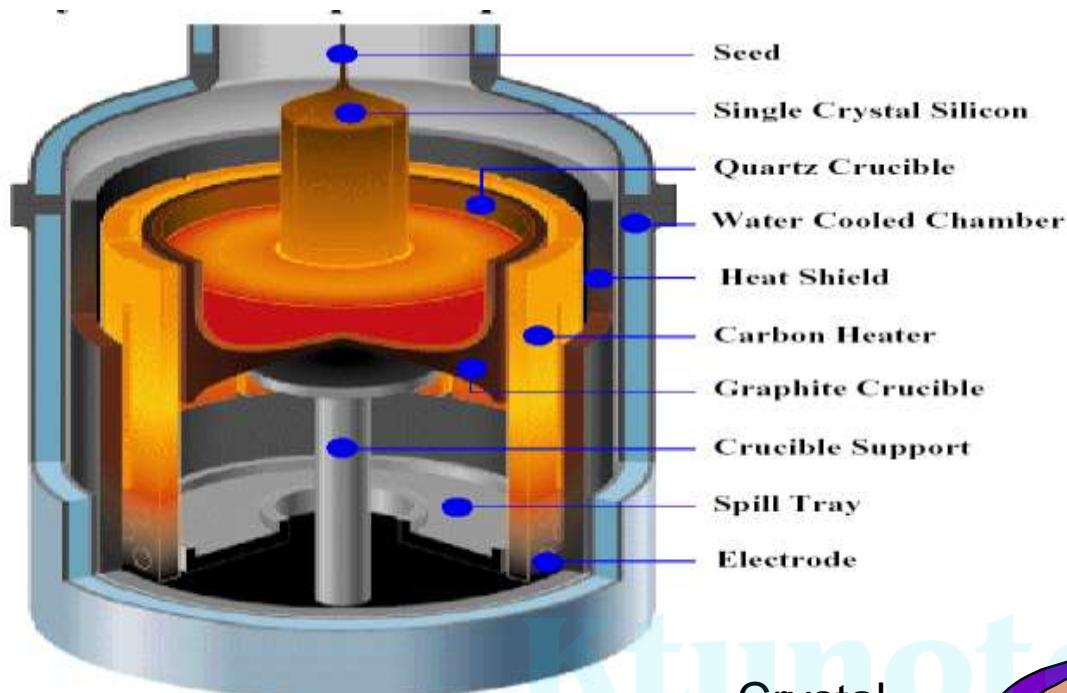
✓ Include fused silica crucible ,graphite susceptor , a rotation mechanism ,heating element and power supply

✓ Melt is contained in crucible . Unreactive with molten silicon

✓ Melting point of crucible should be very high for thermal stability and hardness

•Susceptor is used to support the silica crucible

•Graphite used highly pure to prevent contamination of crystal from impurities.



- Susceptor is placed on a pedestal whose shaft is connected to a motor that provide rotation
- To melt charge radio frequency heating(for small melt) or resistance heating (for large melt) is used.
- Graphite heater connected to a dc power supply

2).Crystal pulling mechanism

- Control the pull rate and crystal rotation so it should have minimum vibration and great precision
- Maintain the proper orientation perpendicular to the melt surface

3.Ambient control

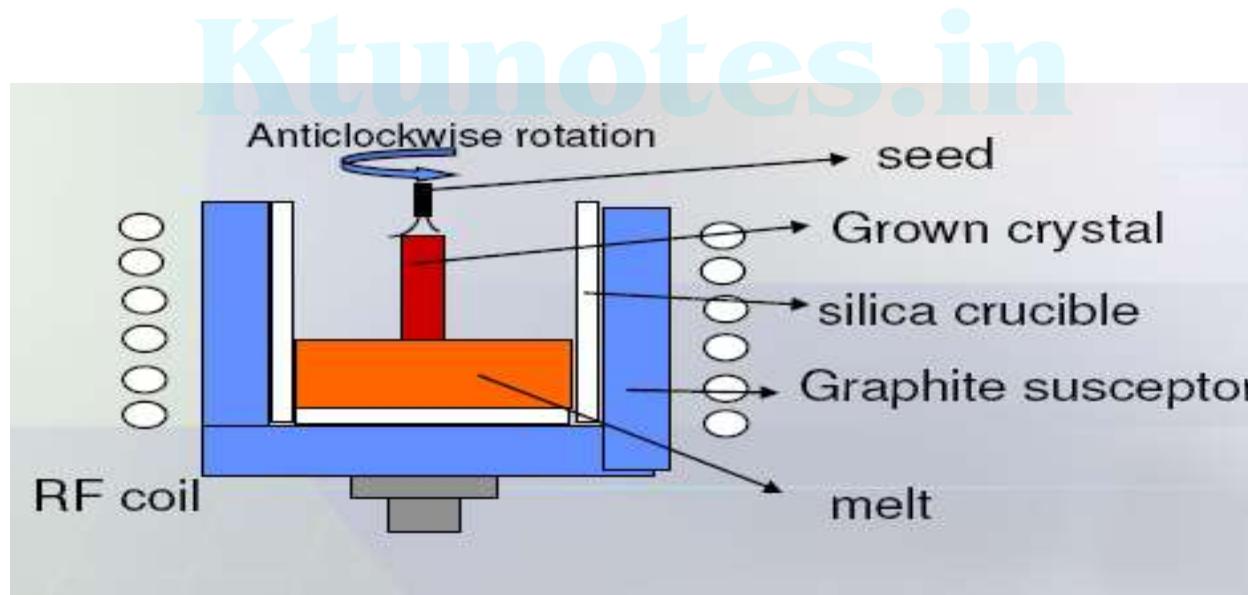
Inert gas source, a flow control and exhaust system

4).control system

- Include control of process parameter like temperature, crystal diameter, pull rate ,rotation speed etc..
- Microprocessor based control and infrared sensor are used to judge any change

Working

- Poly crystalline si in crucible heated to melt.
- Seed crystal is placed over crucible. seed is dipped in to melt .
- Some part of seed melt and some touch liquid surface-pull up seed-freeze-solid liquid interface occur-single crystal formed (**ingot or silicon boule**)
- Boule of si can reach a diameter of over 300mm and are 1 to 2 m long



- In Growth process a known amount of dopant added in the melt to obtain desired doping concentration in the grown crystal.

(i.e) P type material - boron , N type material - phosphorous

- Two important parameters of CZ growth-

a).**pull rate**:-rate at which the seed rod is pulled upward as the Si freezes on it(ie. The amount of Si solidified on the seed is determined by pull rate)

b).**growth rate**:-is the instantaneous solidification rate.

Pull Rate:

$$V_g = \frac{K_s}{\Delta h_{fus} \cdot \rho_s} \left[\frac{-2}{3} \cdot AB^{-\frac{5}{3}} \right]$$

$$A = \sqrt{\frac{9}{5} \frac{\sigma \cdot \varepsilon}{R \cdot K_s}}$$

$$B = T_m^{-\frac{3}{2}}$$

V_g = Pull Rate

K_s = Thermal Conductivity

ΔH_{fus} = Enthalpy of Fusion

ρ_s = Solid Density

σ = Stefan Boltzmann Constant

ε = Emmisivity

R= Raidus

T_m = Melting Temperatrue

Wafer preparation

- Boule is first characterized for resistivity and crystal perfection

Grinding and slicing

- Seed and tail are cutoff and boule is mechanically trimmed to the proper diameter(diameter at this point slightly larger than the final diameter, for additional etching)
- For wafers 150mm and less ,flats are ground the entire length of boule to denote the crystal orientation and the dop

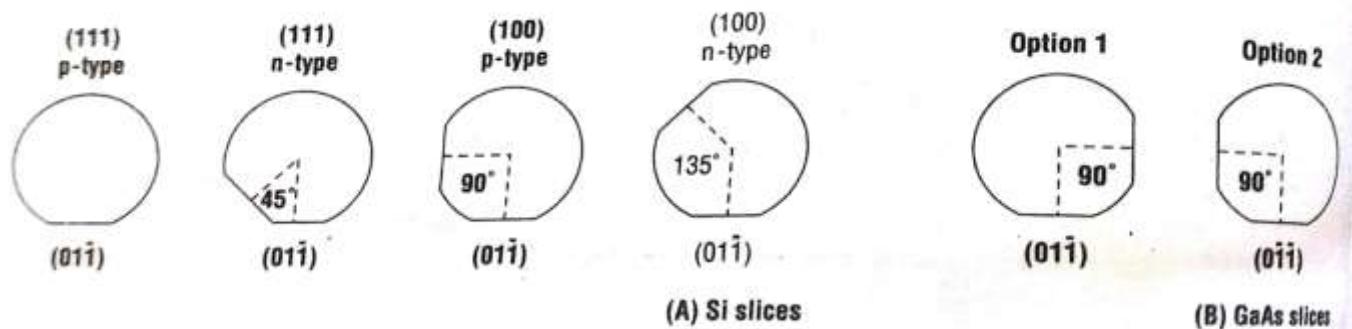


Figure 2.23 Standard flat orientations for different semiconductor wafers.

- After grinding the flats ,the wafer is dipped in a chemical etchant(normally HF-HNO₃) to remove the damage caused by the mechanical grinding **Ktunotes.in**
- After etching ,the boule is sliced in to wafers(critical step ,it will determine the wafer bow and flatness).typically, a wire impregnated with diamond particle is used
- The wafers may be then edge rounded in another mechanical grinding process(less

Lapping & etching

- Next Series of steps are performed to remove any residual mechanical damage
 - first the wafers are mechanically lapped in a slurry of alumina and glycerine, then etched as before to reduce the damage

Polishing & cleaning

- Finally ,one or both sides receive a polish in an electrochemical process involving a slurry of NaOH and very fine silica particles followed by a chemical bath.

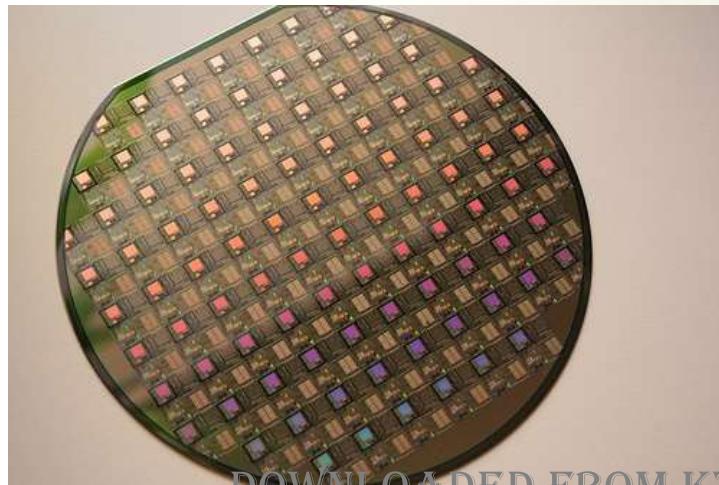
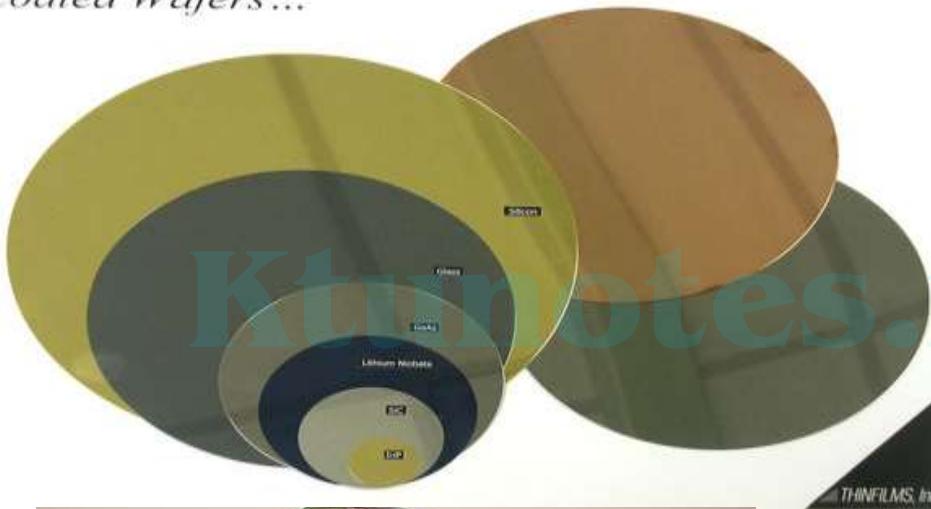
Typical specification for state of art of si wafer

Cleanliness(particle/cm ²)	<0.03
Oxygen concentration(cm-3)	specified +-3%
Carbon concentration(cm-3)	<1.5 *10 ¹⁷
Metal contaminants bulk(ppb)	<0.001
Grown in dislocation(cm-2)	<0.1
Oxidation induced stacking faults(cm-3)	<3
Diameter(mm)	>=150
Thickness(μm)	625 or 675
Bow(μm)	10
Global flatness(μm)	3
Cost(\$/cm ²)	0.2

Wafers

Dicing ->Lapping->etching ->polishing -> cleaning

Coated Wafers...



Example 1. A silicon ingot with 0.5×10^{16} boron atoms/cm³ is to be grown by CZ method. What should be the concentration of Boron in the melt to obtain the required doping concentration. The segregation coefficient of boron is 0.8.

Solution. Since the segregation coefficient K_0 is defined as

$$K_0 = \frac{C_s}{C_l},$$

where C_s is the concentration of the dopant in solid (ingot) and C_l is the concentration of dopant in liquid (melt)

∴

$$C_l = \frac{C_s}{K_0} = \frac{0.5 \times 10^{16}}{0.8} \text{ atoms/cm}^3$$

$$= 0.625 \times 10^{16} \text{ atoms/cm}^3$$

Example 2. Find the doping concentration of arsenic in silicon if the melt contains 10^{17} arsenic atoms/cm³ initially and the fraction solidified is 0.5. The segregation coefficient of arsenic is 0.3. Also find the initial concentration of dopant in silicon when the fraction solidified is 0.02 ?

Solution. The concentration of the dopant in solid is given by

$$C_s = K_0 C_0 \left[1 - \frac{M}{M_0} \right]^{K_0 - 1}$$

where C_0 is the initial concentration of dopant in melt. The ratio $\left(\frac{M}{M_0} \right)$ is known as the fraction solidified.

Substituting the values we have

$$\begin{aligned} C_s &= 0.3 \times 10^{17} [1 - 0.5]^{0.3 - 1} \\ &= 0.48 \times 10^{17} \text{ atoms/cm}^3 \end{aligned}$$

After obtaining the value of C_s for fraction solidified at 0.5 we find the value of C_s for fraction solidified at 0.02.

$$\begin{aligned} C_s &= 0.3 \times 10^{17} [1 - 0.02]^{0.3 - 1} \\ &= 0.304 \times 10^{17} \text{ atom/cm}^3 \end{aligned}$$

Example 3. The segregation coefficient of oxygen is 0.25. Find the concentration of oxygen in the silicon ingot at a fraction solidified of 0.3. The concentration of oxygen in the silicon at the top of the crystal is 12.5×10^{17} atoms/cm³ at fraction solidified of 0.1.

Solution. We have $C_s = K_0 \times C_0 \left(1 - \frac{M}{M_0}\right)^{K_0 - 1}$

The concentration of oxygen in the melt initially is obtained as

$$12.5 \times 10^{17} = 0.25 \times C_0 (1 - 0.1)^{0.25 - 1}$$

$$C_0 = 4.6 \times 10^{18} \text{ atom/cm}^3.$$

The expected value of C_s at a fraction solidified of 0.3 is

$$\begin{aligned} C_s &= 0.25 \times 4.6 \times 10^{18} (1 - 0.3)^{0.25 - 1} \\ &= 1.5 \times 10^{18} \text{ atoms/cm}^3. \end{aligned}$$

Example 4. A silicon ingot should contain 10^{17} phosphorus atoms/cm³ when grown by CZ method. What concentration of phosphorus atoms should be in melt to give the required concentration in the ingot ? If the initial load of silicon in the crucible is 60 kg. How many grams of phosphorus should be added ?

Solution. The initial concentration of phosphorus in the melt is

$$C_I = \frac{C_S}{K_0} = \frac{10^{17}}{0.35} = 2.85 \times 10^{17} \text{ atoms/cm}^3.$$

Since the density of silicon is 2.53 g/cm³ when in molten state, the volume of 60 kg silicon is $2.37 \times 10^4 \text{ cm}^3$.

Total number of phosphorus atoms in the melt is

$$2.85 \times 10^{17} \times 2.37 \times 10^4 = 6.77 \times 10^{21} \text{ atoms}$$

Now atomic weight of phosphorus is 30.97 g/mol. So the amount of phosphorus to be added is

$$= \frac{6.77 \times 10^{21} \times 30.97}{6.02 \times 10^{23}} = 0.35 \text{ gm.}$$

A silicon crystal is to be grown by Czochralski process and is to contain 5×10^{15} boron atoms/cm³. Given the segregation constant k_0 for Boron in silicon is 0.8. Atomic weight of boron equals 10.81g/mole, density of silicon 2.22g/cm³ and Avogadro number is 6.023×10^{23} atoms/mole. (a) Determine the initial concentration of Boron in the melt to produce the required doping density. (b) If the initial amount of silicon in the crucible is 20kg, how many grams of Boron should be added to obtain the same doping?

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Example 5. Show that to grow an oxide layer of thickness x , a thickness of $0.44x$ of silicon is consumed.

Solution. Volume of 1 mole of silicon = $\frac{\text{Molecular weight of silicon}}{\text{Density of silicon}}$
= $\frac{28.09 \text{ gm/mole}}{2.33 \text{ gm/cm}^3}$
= $12.06 \text{ cm}^3/\text{mole.}$

Volume of 1 mole of silicon dioxide = $\frac{\text{Molecular weight of silicon dioxide}}{\text{Density of silicon dioxide}}$
= $\frac{60.08 \text{ gm/mole}}{2.21 \text{ gm/cm}^3}$
= $27.18 \text{ cm}^3/\text{mole.}$

Now 1 mole silicon is changed into 1 mole silicon dioxide. Therefore we can write.

$$\text{Volume of 1 mole of silicon} = \text{volume of 1 mole of silicon dioxide}$$

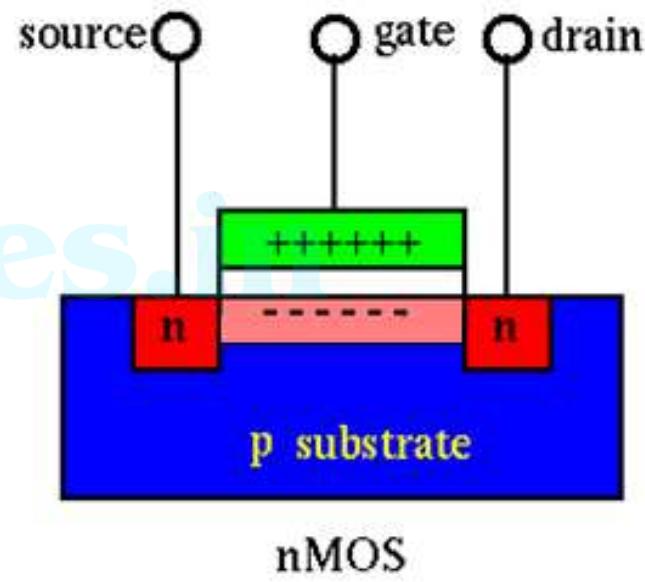
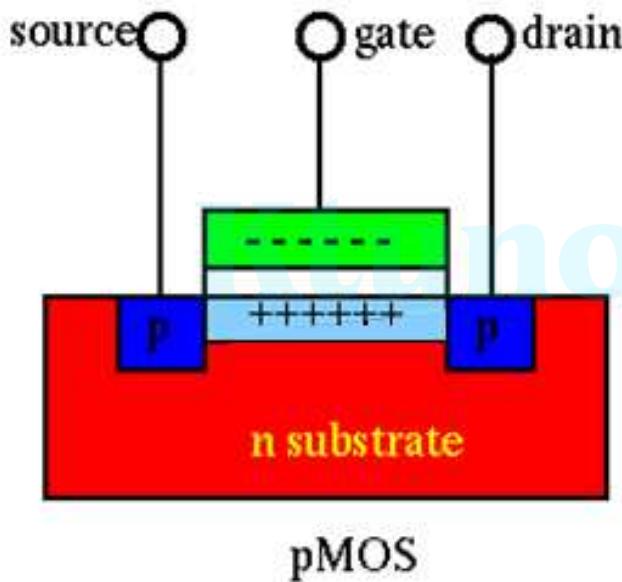
$$\frac{\text{Volume of 1 mole of silicon}}{\text{Volume of 1 mole of silicon dioxide}} = \frac{\text{thickness of Si} \times \text{Area}}{\text{thickness of } \text{SiO}_2 \times \text{area}}$$
$$\frac{12.06}{27.18} = \frac{\text{thickness of Si}}{\text{thickness of } \text{SiO}_2} = 0.44$$

So, the thickness of silicon consumed is equal to 0.44 times the thickness of oxide layer.

Determine the ratio of Silicon consumed to the thickness of grown SiO_2 layer over silicon wafer. If SiO_2 layer of $0.2 \mu\text{m}$ is to be grown, what would be the thickness of used up Silicon. Molecular weight of $\text{SiO}_2 = 60.08\text{g.mole}$, density of $\text{SiO}_2 = 2.2\text{g/cm}^3$, atomic weight of $\text{Si} = 20.09$ and density of $\text{Si} = 2.33\text{g/cm}^3$

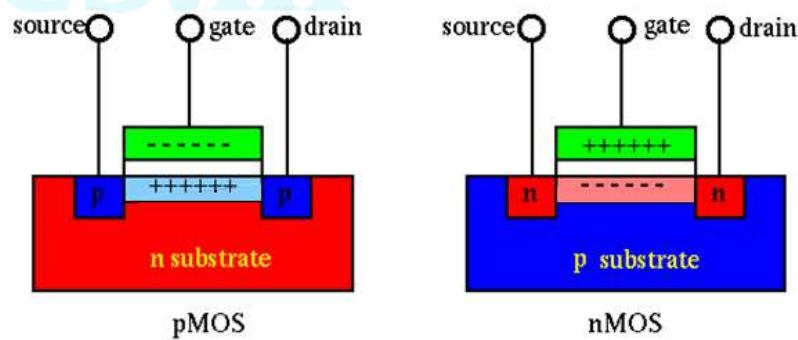
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MOSFET



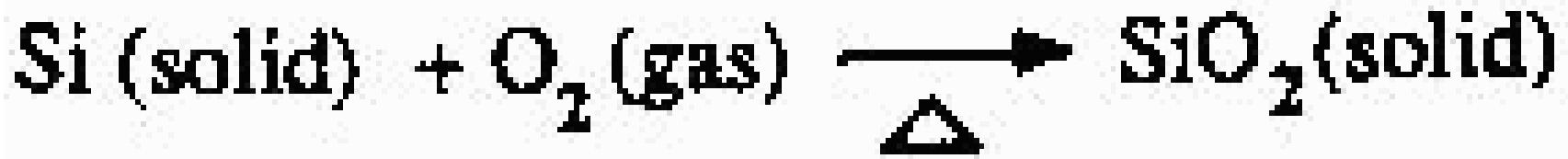
Steps of Silicon Device Manufacturing

- Oxidation
- Photolithography
- Etching
- Ion Implantation
- Diffusion
- Deposition



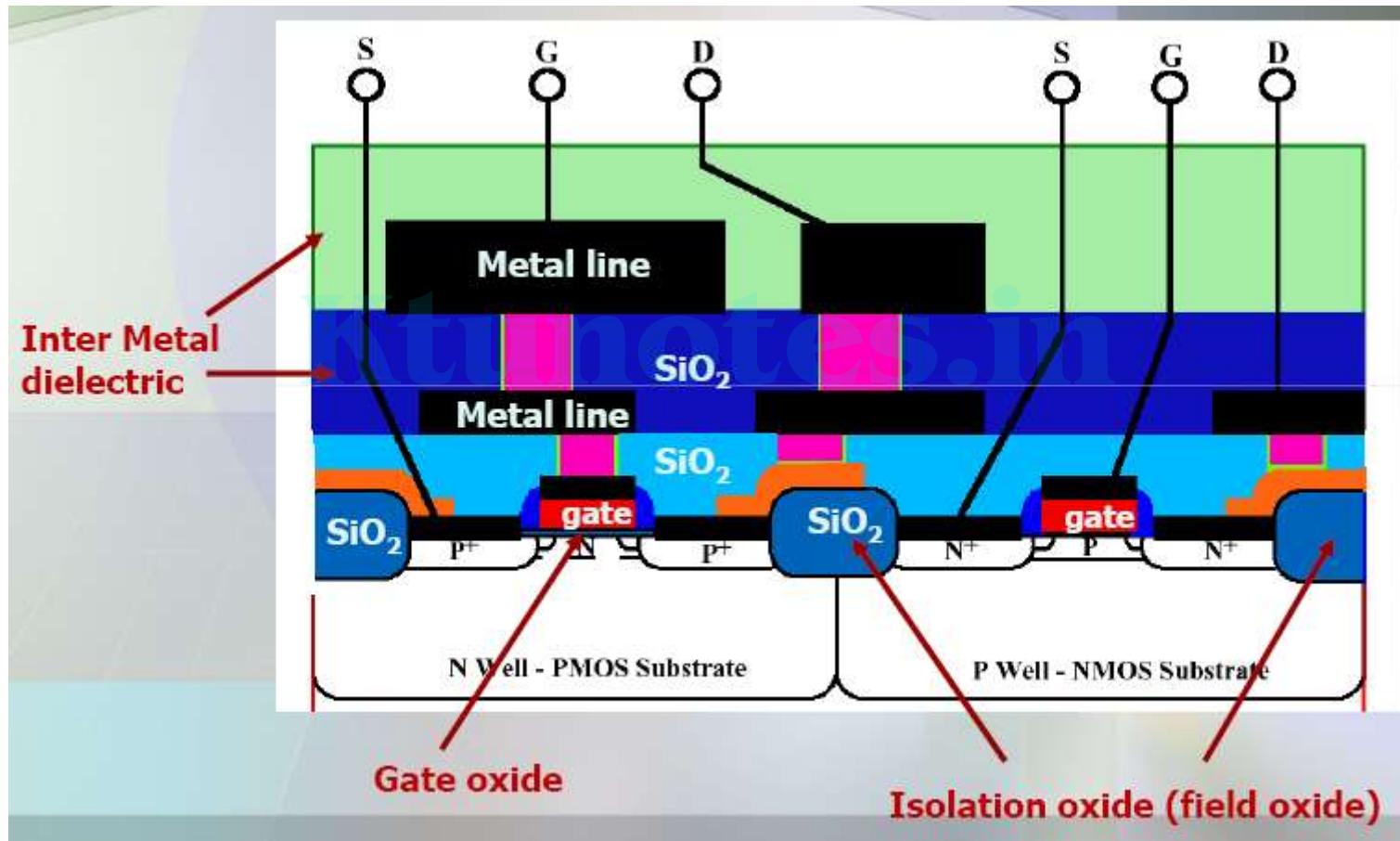
Oxidation

- Refers to reaction of forming SiO_2



In IC SiO_2 has the following uses

- Surface passivation
- Doping barrier
- Surface dielectric
- Device dielectric: Field oxide, Gate oxide



Surface passivation with silicon dioxide layers



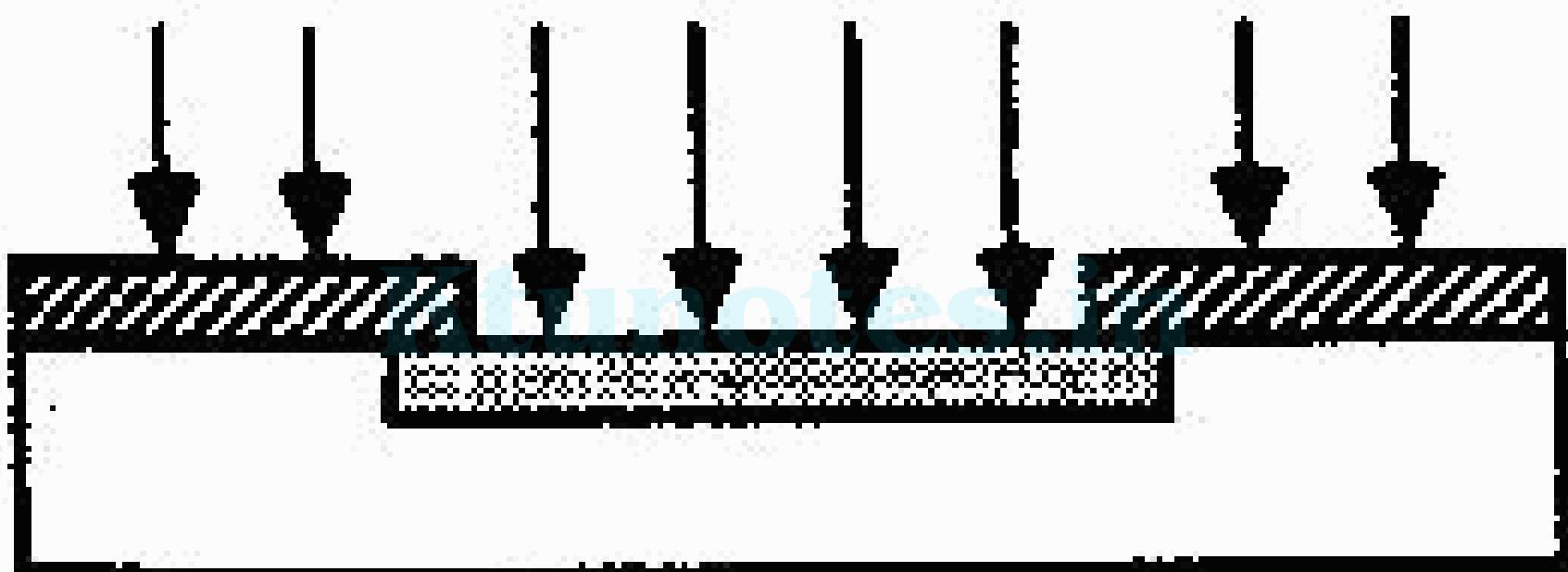
Silicon dioxide is very hard and dense can be used as passivation layer: Preventing dirt, scratches, chemical reactions.

Surface contaminants on the surface end up in the oxide during the oxide growth, can oxidize the surface and then remove the oxide to rid the surface of unwanted mobile ion contaminations

Surface
Passivation

Silicon dioxide layer as dopant barrier

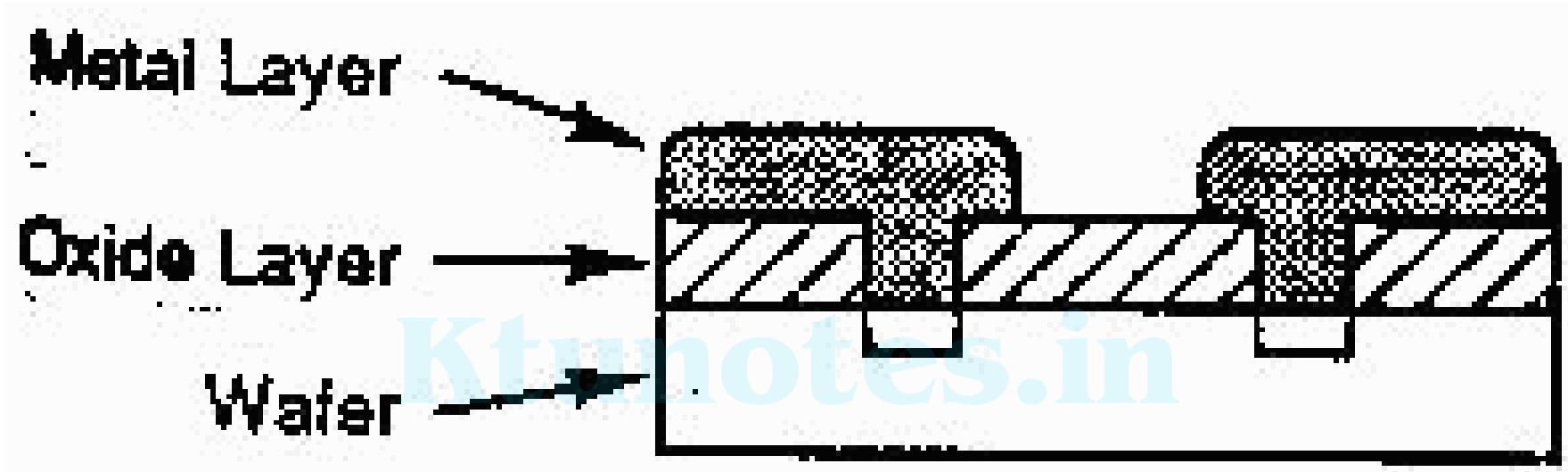
Dopants



Silicon dioxide layer can block the dopant form reaching the silicon surface.(very low hole density)

Silicon dioxide thermal expansion coefficient is similar to silicon, wafer will not warp during high temperature process

Dielectric use of silicon dioxide layer

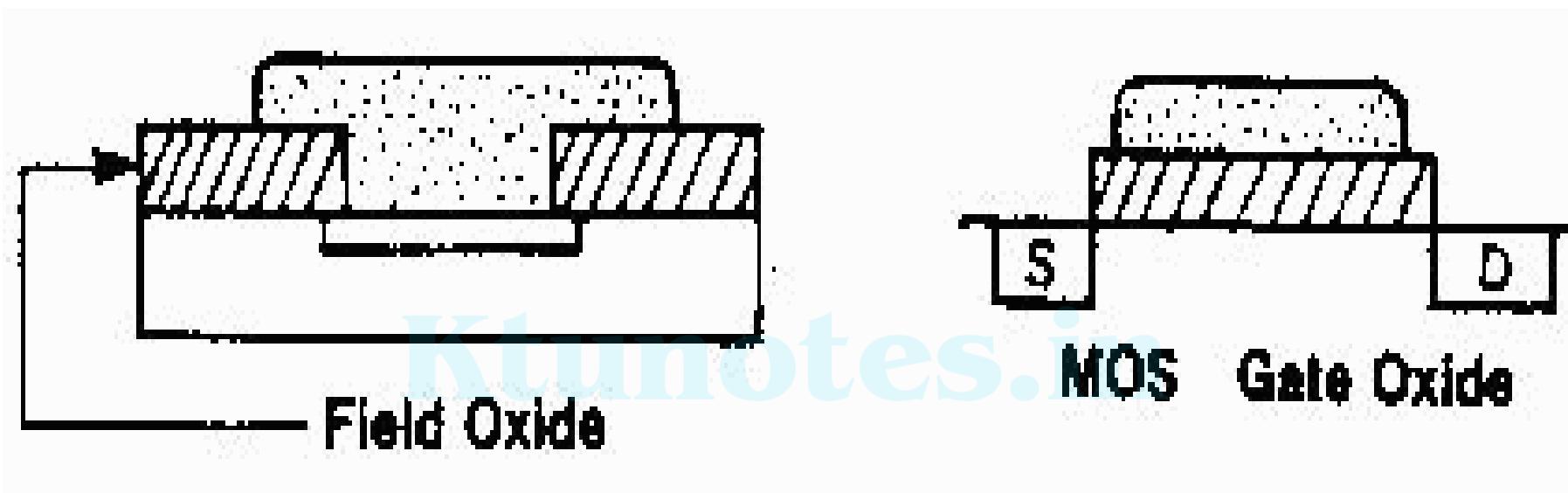


Silicon dioxide can be used as insulator between metal and silicon. However, it must be think enough not to induce charge induction in the silicon surface.

Induction:oxide between metal is thin that electrical charge in the metal line induces charges on the metal surface.

Field oxide: oxide that is thick enough not to induce the charge on the wafer surface

Silicon dioxide as field oxide and in MOS gate



Field oxide: oxide that is thick enough not to induce the charge on the wafer surface.

Gate oxide: oxide as dielectric With thickness thin enough to allow induction of a charge in the gate region under the oxide can be as thin as 35 to 80 Å range

Oxidation

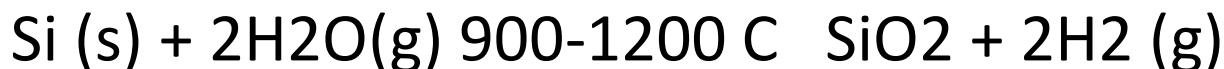
- Mainly two methods
 1. Thermal oxidation (wet and dry)
 2. Rapid Thermal Oxidation

1.Thermal Oxidation.

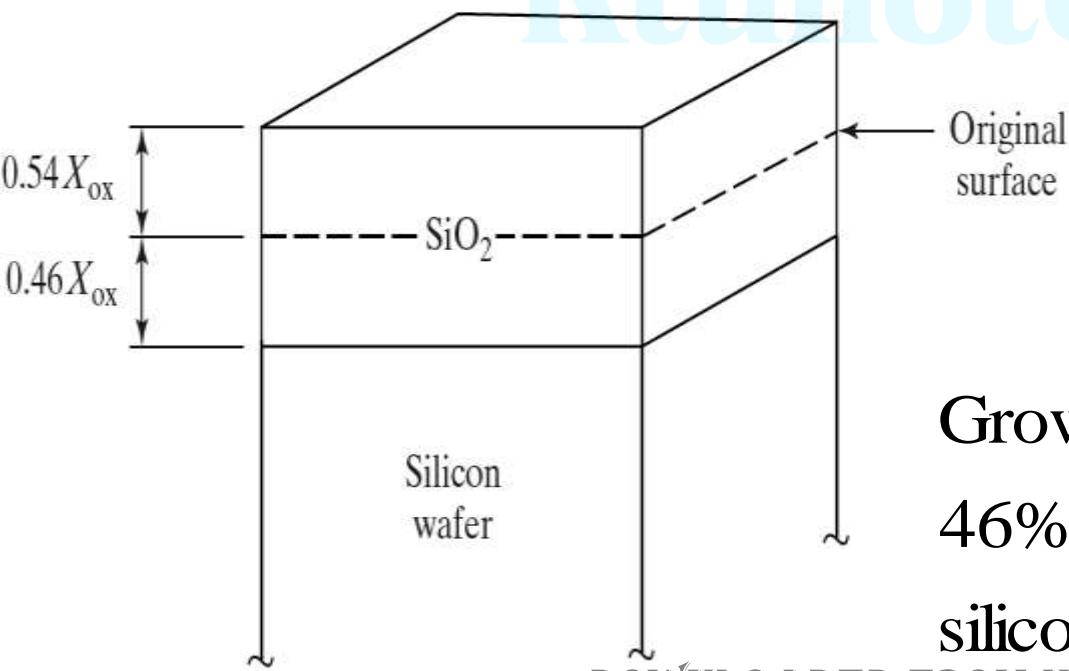
- Dry and wet oxidation need high temperature (900 - 1200°C) for growth, though the kinetics are different, which is why this process is called thermal oxidation
- Dry Oxidation



- Wet Oxidation

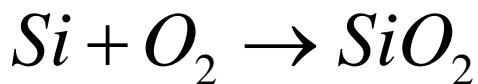


- Si is supplied by the underlying wafer
- Since the underlying Si is consumed, the Si/SiO₂ interface moves deeper into the wafer
- SiO₂ formation involves sharing of valence electron between si & oxygen.
- SiO₂ grows in both directions upward and downward



Growth Occurs 54% above and 46% below original surface as silicon is consumed

Dry oxidation

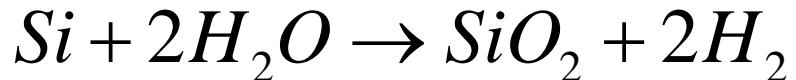


- Dense oxide formed (good quality, low diffusion)
- slow growth rate

- NEED TO KEEP WATER OUT OF THE SYSTEM

Dry oxide for gate ox

Wet oxidation



- Overall reaction
- Relatively porous oxide formed (lower quality, species diffuse faster)
 - Still good quality compared to electrochem oxidation
- faster growth rate
- Hydrogen oxygen ratio 2:1
- Thick field oxide

Wet oxide for masking

Oxide formation(growth mechanisms)

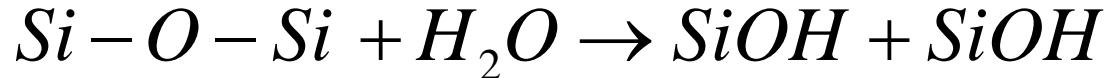
Wet oxidation



- An inert gas is bubbled through water at 95oC
- Direct oxidation result in forming an oxide layer having about 2.27 times the thickness of the consumed silicon
- To form the oxide the oxidising species must move through the growing oxide layer in order to reach the si surface

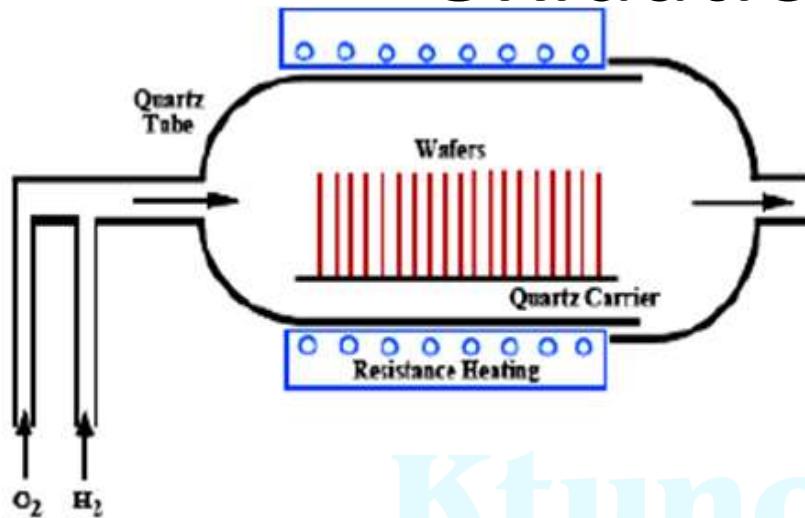
Detailed nature of reaction

- Water vapour react with bridging oxygen ions in the silica structure to form non-bridging hydroxyl groups



- At the oxide –silicon interface the hydroxyl groups react with the silicon lattice to form silicon polyhedra and hydrogen.
- Hydrogen leaves the oxide layer by rapid diffusion.some of the hydrogen reacts with bridging oxygen ions in the silica to form hydroxyl groups.
- Which weakens the silica structure.

Oxidation system

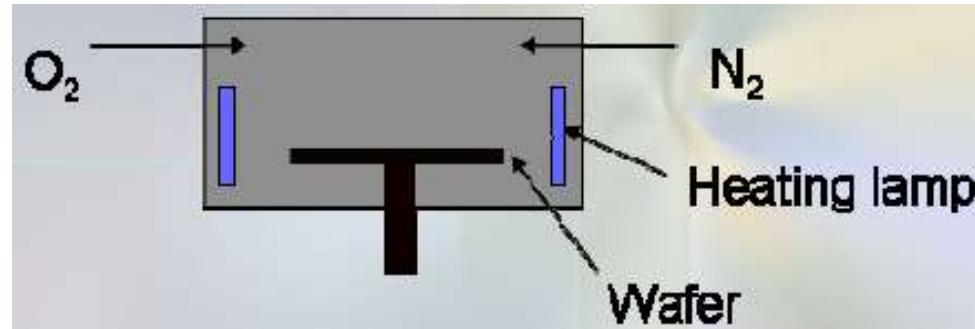


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- Wafer placed in quartz carrier
- Wafers are exposed to a source of either pure dry oxygen or pure water vapour
- Furnace temperature is maintained in between 900 to 1200 oC and gas flow rate maintained at 1cm/s

Rapid Thermal Oxidation

- Heat wafer rapidly to high temperatures and keep at high temperatures for a very short period of time (< 2minutes) in oxidizing ambient (O_2 , NO , N_2O , etc)
- Ramp rates are very high Room Temp to 900-1000C in < 2 minute
- Typically these furnaces can process only one wafer at a time and are used for high quality ultra thin oxides



Example 6. What is the thickness of the oxide grown by wet oxidation at a temperature of 1200°C at $\tau = 0$ where $A = 0.05 \mu\text{m}$ and $B = 0.720 \mu\text{m}^2/\text{h}$.

Solution. The oxide thickness is given by

$$\frac{d_0}{A/2} = \left[1 + \frac{t + \tau}{A^2/4B} \right]^{1/2} - 1$$

$$\frac{d_0}{.05/2} = \left[1 + \frac{t}{(.05)^2/4 \times 0.720} \right]^{1/2} - 1$$

So we have

If $t = 0.01 \text{ h}$ then

$$d_0 = 0.006 \mu\text{m}.$$

If $t = 100 \text{ h}$ then

$$d_0 = 0.846 \mu\text{m}$$

which shows that the thickness of oxide increases with time.

Example 7. Calculate the oxide thickness when it is grown by wet oxidation and when it is grown by dry oxidation at a temperature of 1000°C. Assume for wet oxidation $A = 0.226 \mu\text{m}$, $B = 0.287 \mu\text{m}^2/\text{h}$, $\tau = 0$ and for dry oxidation $A = 0.165 \mu\text{m}$, $B = 0.047 \mu\text{m}^2/\text{h}$, $\tau = 0.37 \text{ h}$

Solution. For wet oxidation

$$\frac{d_0}{0.226/2} = \left[1 + \frac{t}{(0.226)^2/4 \times 0.287} \right]^{1/2} - 1$$

At $t = 0.01 \text{ h}$ $d_0 = 0.012 \mu\text{m}$

At $t = 100 \text{ h}$ $d_0 = 5.27 \mu\text{m}$

For dry oxidation

$$\frac{d_0}{0.165/2} = \left[1 + \frac{t + 0.37}{(0.165)^2/4 \times 0.0117} \right]^{1/2} - 1$$

At $t = 0.01 \text{ h}$ $d_0 = 0.02 \mu\text{m}$

At $t = 100 \text{ h}$ $d_0 = 1 \mu\text{m}$

Example 8. Compare the oxide thickness grown for short time and long time oxidation at a temperature of 1200°C by wet oxidation method. At 1200°C, $A = 0.05 \mu\text{m}$ and $B = 0.720 \mu\text{m}^2/\text{h}$, $\tau = 0$.

Solution. For short oxidation times

$$d_0 = \frac{B}{A} (t + \tau)$$
$$= 14.40 (t + 0)$$

At $t = 0.01 \text{ h}$ $d_0 = 14.40 \times 0.01 = 0.144 \mu\text{m}$

For long oxidation times

$$d_0 = \sqrt{Bt}$$
$$= \sqrt{0.720 t}$$

At $t = 100 \text{ h}$

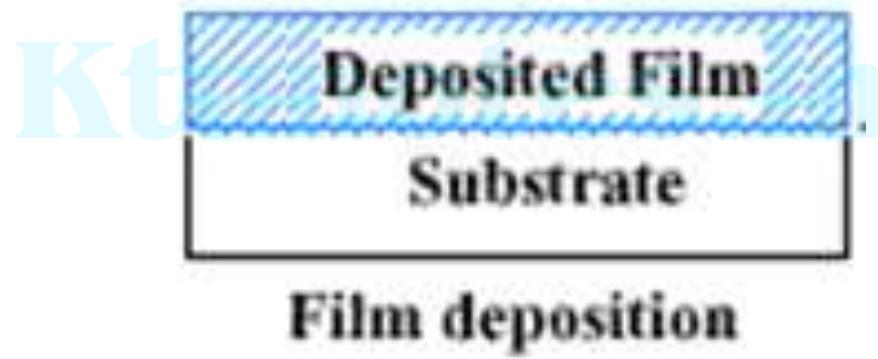
$$d_0 = 8.48 \mu\text{m.}$$

A SiO_2 layer is grown by wet oxidation at 1000°C for 40 minutes followed by dry oxidation for 1 hour at 1200°C . Determine the thickness of the oxide layer formed. For wet oxidation at 1000°C , $B=0.29$, $B/A=1.27$ and for dry oxidation at 1200°C , $B= 0.045$, $B/A= 1.120$, $\tau = 0.027$

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Up to Now....



Steps of Silicon Device Manufacturing

- Photolithography

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What is Lithography?

- Lithography is the process of transferring patterns of geometric shapes on a mask to a thin layer of radio sensitive material known as resist covering the whole surface of the semiconductor substrate.
- The patterns defines the regions of the integrated circuits that have to be fabricated.
- This include the implantation region ,contact region ,bonding pads etc..
- The resist patterns are the replicas of circuit elements
- Resist patterns are transferred into underlying layer
- After transferring patterns, etching is done to remove unmasked portion of the layers.

Lithography's Key Role in the Process

- With multiple etch, deposition, and doping processes taking place in the fabrication of a device, the lithography process is repeated many times.
- The precision and accuracy of lithography in the manufacturing process controls, to a first degree, the success in building a device.

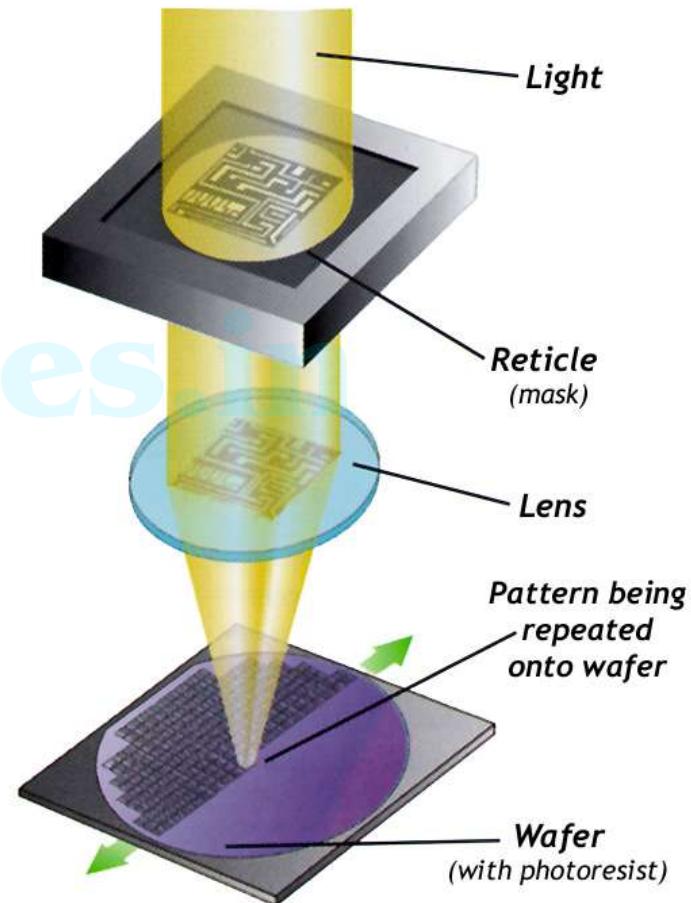
Photo Lithograph

- Literally means light-stone writing
- Use of light sensitive resist which deposited on SiO₂ surface
- The resist is then exposed through a mask developed to produce a pattern in the resist.
- Two step process
 - Transfer pattern from Mask on to PR covering the wafer
 - Transfer of pattern from PR to wafer by etching

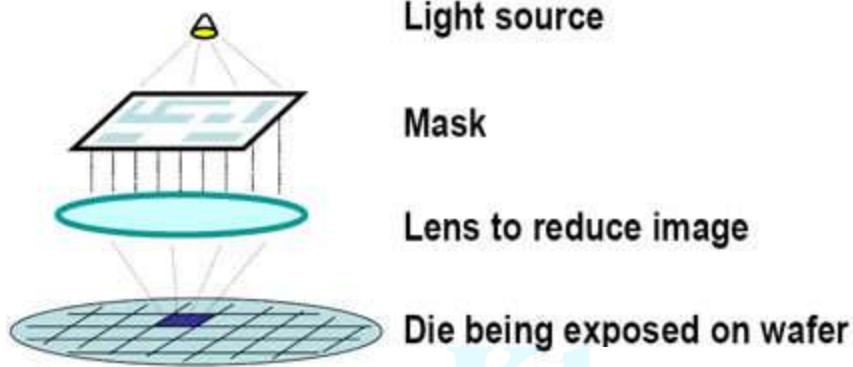


Overview of the Photolithography Process

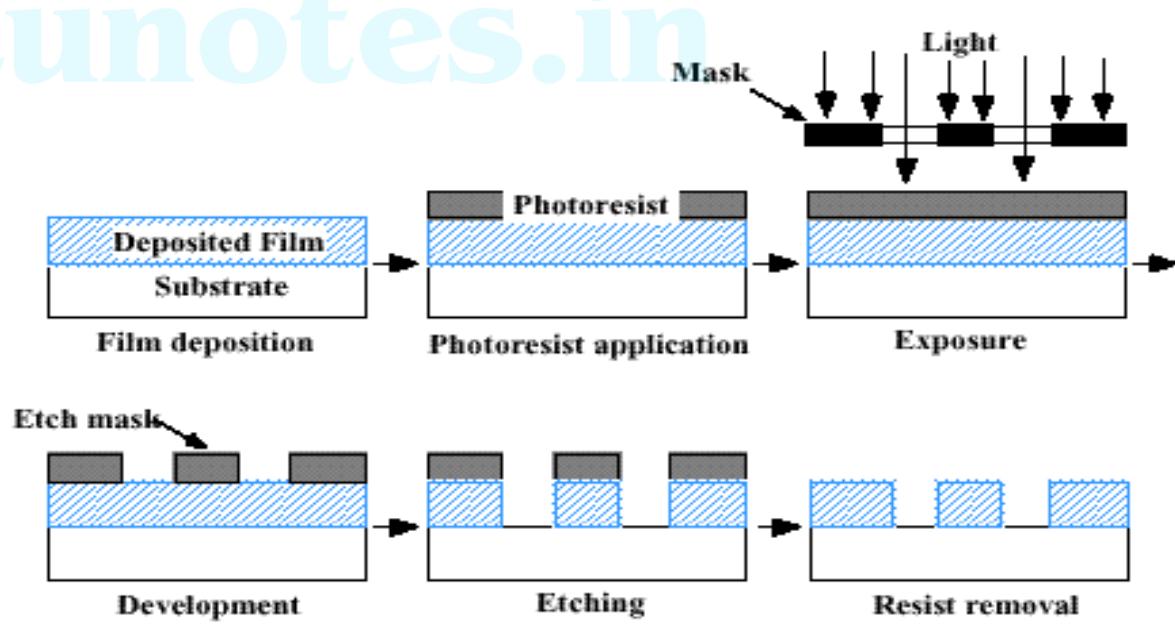
- Photolithography uses light energy passing through a patterned mask
- The light is focused onto the photosensitive surface
- Chemical changes in the surface coating occur
- Subsequent chemical development creates a temporary pattern on the surface.



Photolithography



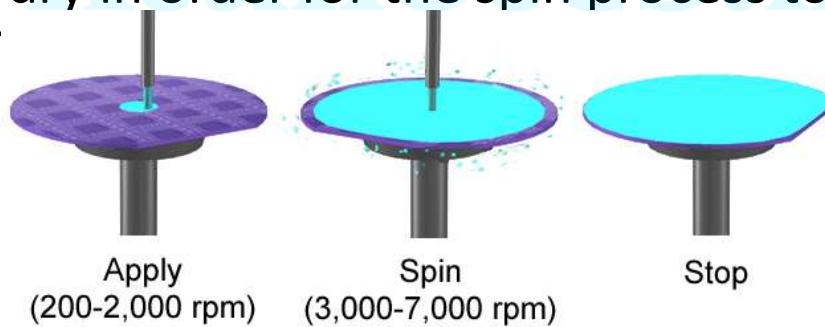
- ❑ During the developing ,the resist washes away in the regions where the diffusions are desired
- ❑ Resist then used as a mask to selectively etch the SiO₂ layer



Steps in the Lithography Process

1. Resist Coating

- Resist is a liquid emulsion .The Si substrate uniformly coated with resist by spin coating
- Photoresist is made up of chemical compounds whose properties are changed by exposure to radiant energy.
- The photoresist chemicals are in a liquid solution that is applied to a silicon wafer in a device called a spinner. The silicon wafer must be clean, flat, and dry in order for the spin process to create a flat, uniform coating of the resist.



2. Prebaking of photoresist

- Before alignment, baking the resist causes it to form a solid layer(Baking in an oven about 100°C)

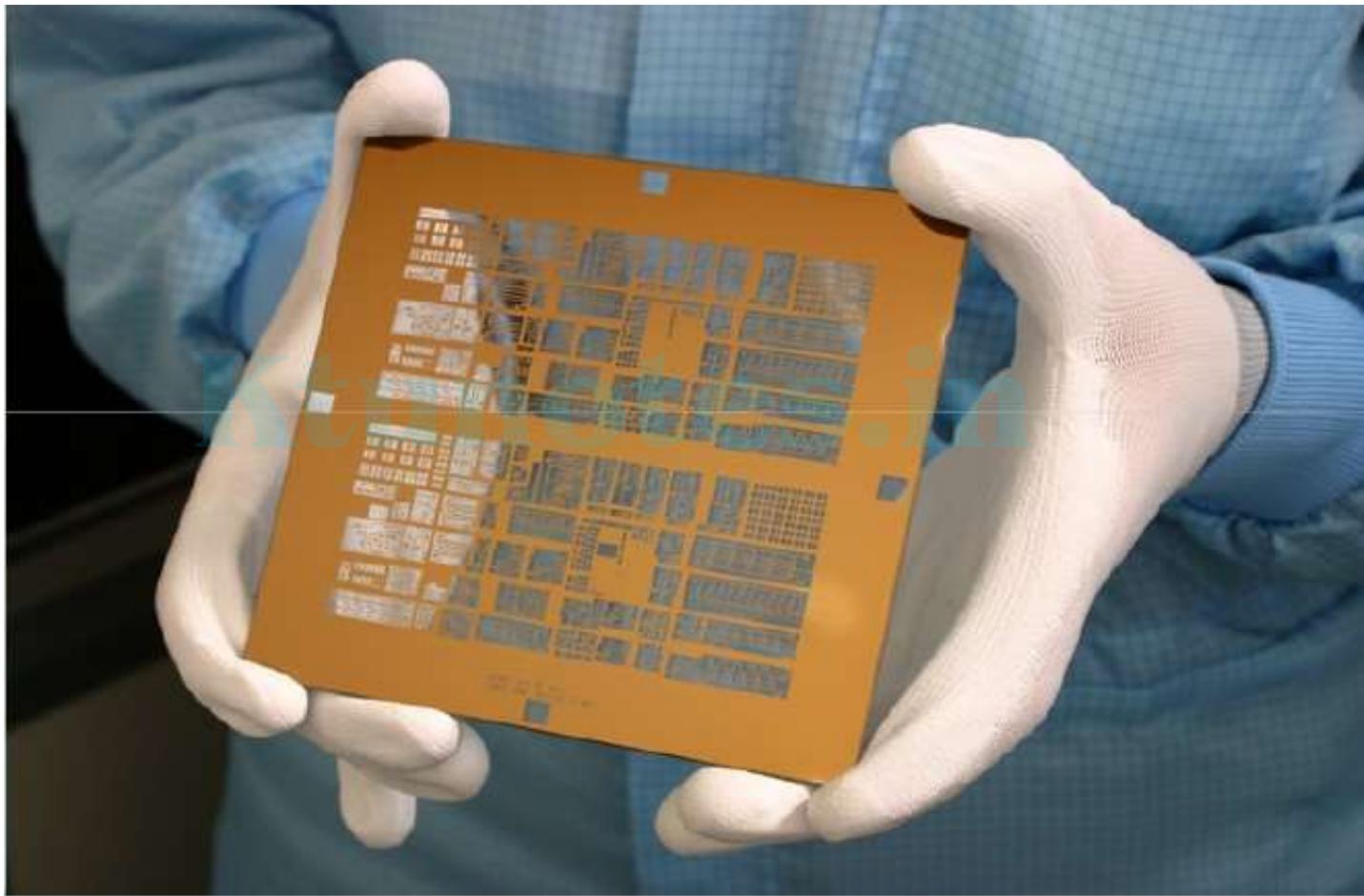
3. Exposure through Mask

- A photomask, typically made of quartz with a chrome plating, controls where the radiant energy will strike the photoresist.

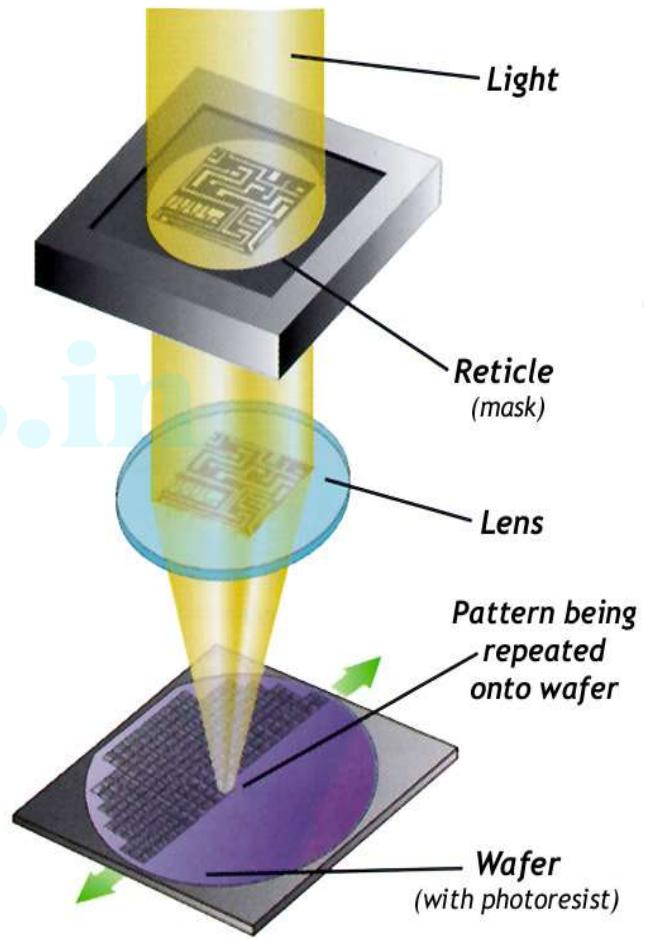
Mask

- Same size as finished chip or an integral factor (5x or 10x) of final chip
- During exposure, the image size is reduced.
- Typically 150mm square
- Made of fused silica (typically Quartz)
- Essential properties
 - High degree of optical transparency
 - Small thermal expansion coefficient
 - Flat and polished surface
 - Resistant to scratches
- Chromium is used as opaque layer
- Typically 15-20 masks are used in a process sequence

Mask



- The mask must be precisely aligned to the surface.
- The light source must provide even light to the entire area to be patterned, and the pattern must be in focus.
- There are several exposure methods possible.
 - Contact/proximity printing
 - Projection printing (shown here)
 - Projection scanning
- Contact printing puts the mask directly in contact with the coated surface.
- Projection printing moves the mask away from the surface and uses a condensing lens to focus the pattern



4.Resist development

- Resist undergoes certain chemical transformation in the selected region after development known as resist development

5.Post baking resist

- To increase the inertness of the resist on the substrate to subsequent steps

6.Selective removal of material

Some terms...

- **Resolution:**
 - Ability of PR to accurately transfer patterns on to film underneath
 - Is the minimum feature size that can be transferred with minimal tolerance
- **Registration:**
 - measure of how accurately patterns on successive masks can be aligned.
- **Throughput:**
 - Number of wafers processed per hour
 - For industry, this number has to be sufficiently high while maintaining good resolution and registration

Different types of Photolithography

- UV Lithography
 - UV(optical rays) are used
- X-Ray Lithography
 - X-Rays having shorter wavelength (0.4-4 nm)
 - So the resolution is high
 - Reduction of circuit dimension can be done
- Electron Beam Lithography
 - Since the electrons are very fast particles, no mask can be used here
 - Pattern is transferred by serial scanning
 - Very high resolution, expensive
- Ion Beam Lithography
 - Higher resolution
 - Ion Beams are used
 - Mask less lithography can be done
 - So it can be used for fabricating masks

Diffraction

- If the wavelength of light is much smaller than the aperture or slit width, a light wave simply travels onward in a straight line after passing through it
- when the wavelength exceeds the size of the slit, diffraction of the light occurs, causing the formation of a diffraction pattern

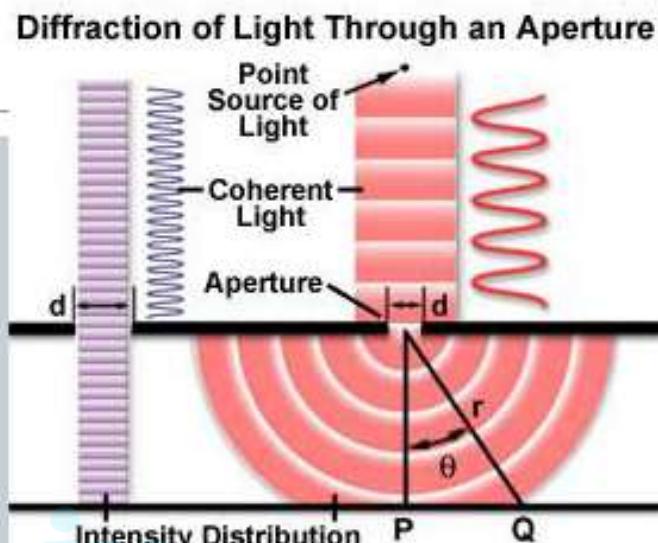


Figure 1
Intensity Distribution of Diffracted Light

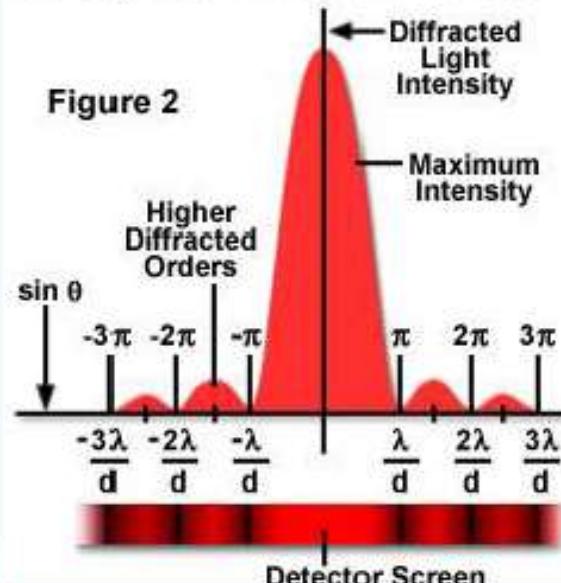


Figure 2

Diffraction

- Two types
- Fresnel Diffraction
 - Near field diffraction
 - Here the image plane is close to the aperture
 - The light travel directly from aperture to the plane where the image is formed.
- Fraunhofer Diffraction
 - Far field diffraction
 - Here the image is far from aperture
 - Lens is normally placed between the aperture and image plane to capture and focus the image

Basic Methods of wafer exposure

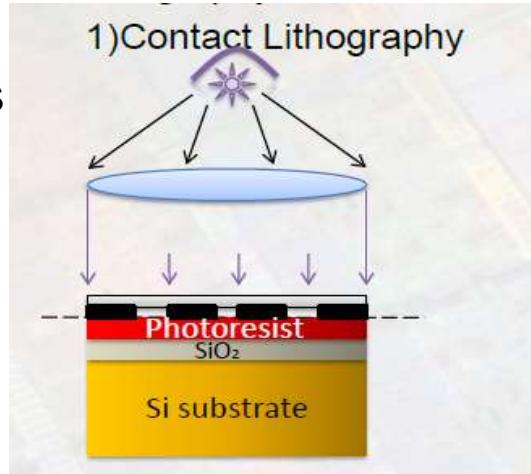
Three methods
1).contact printing
2).proximity
printing
3).projection printing

1. Contact and proximity systems(Fresnal diffraction)

- operate in near field
- No lens between mask and resist on the wafer

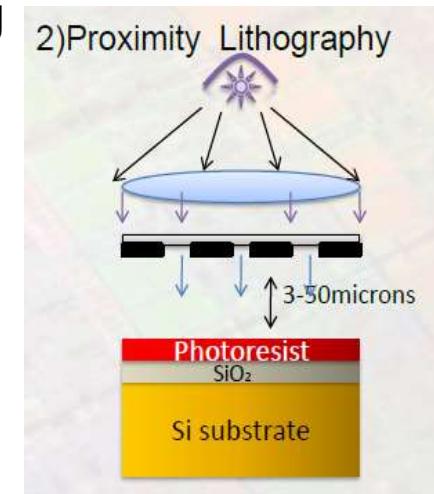
Contact printing

- Here the mask is in contact with the wafer



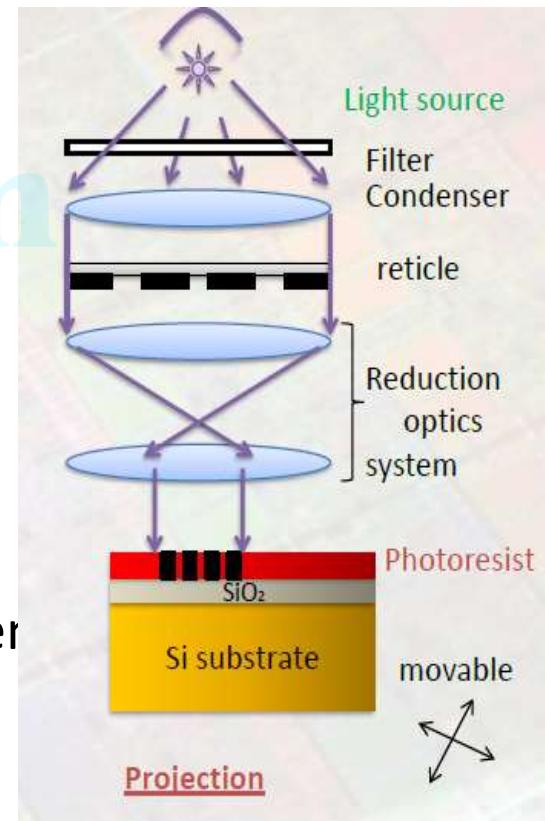
proximity printing

- Here mask is 5-25 micro meters away from wafer



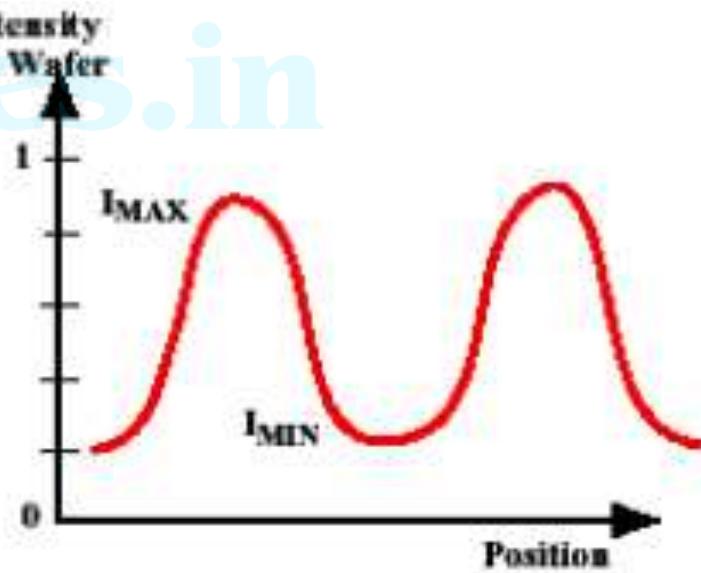
3. Projection printing(Fraunhofer diffraction)

- Developed to obtain high resolution of contact printing without any defects
- It uses a lens between mask and wafer and focus the aperture on the wafer
- Part of the light from the mask has been diffracted to large angle
- Try to reimagine the pattern on to the wafer one must , at minimum , collect that diffracted light.
- Numerical aperture (NA) of the system is defined as $NA = n \sin \alpha$
 α is one-half the angle of acceptance of objective lens & n is the refractive index of the media between objective and wafer , NA range from 0.16 to 0.8



- The **Modulation Transfer Function (MTF)** is used to approximate the position of best focus of a light in a photolithographic system
- Measure of the optical contrast in the areal image.
- Higher the MTF, better the optic contrast

$$MTF = \frac{I_{m\alpha} - I_{m\beta}}{I_{m\alpha} + I_{m\beta}}$$



- MTF less than about 0.5, the image can no longer be reproduced.

Photo Resist

- Is a radiation sensitive material which changes chemically on exposure to light
- Usually a carbon based organic molecule
- When the material absorbs the light, the energy from the photons generally breaks the covalent bonds. After this happens, the resist material chemically restructures itself in to a new form
- Two types of resist:
- **Positive**
 - Regions of resist exposed to light dissolve quickly in 'developer' Unexposed regions remain unchanged and are not removed by developer
- **Negative**
 - Regions exposed to light are hard to remove by developer. Unexposed regions are easily removed by developer
- Positive resists result in better resolution than negative resist

Electron Beam Lithography

Advantages:

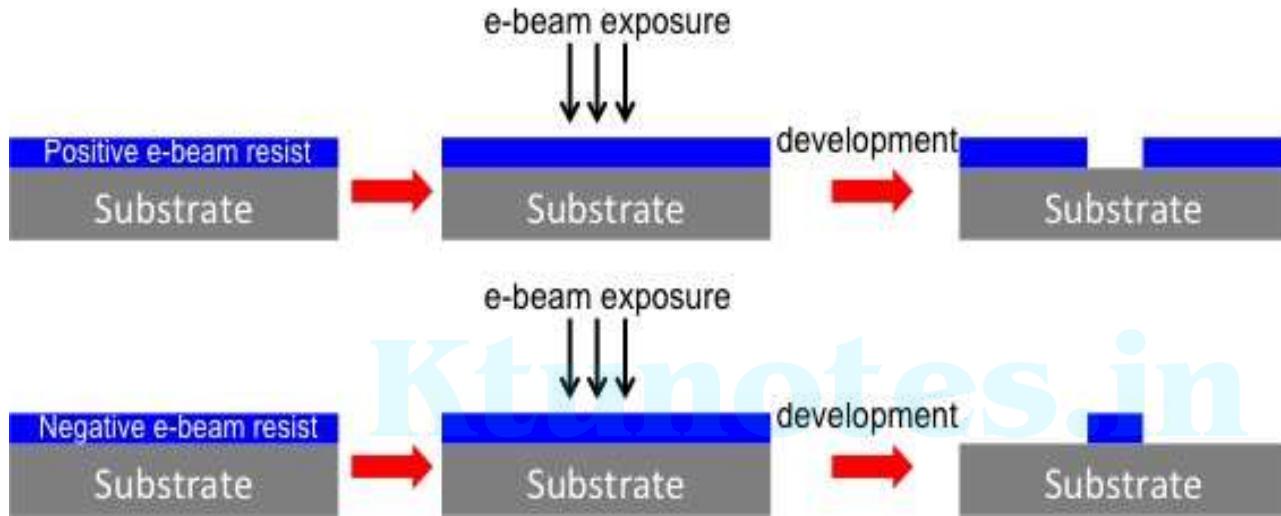
- Generation of submicron
- Resist geometries
- Greater depth of focus
- Direct patterning on a Semiconductor without Using a mask
- Currently EBL is the Technology of choice for Mask generation due to Its ability to accurately define small features.

Disadvantage:

- Low throughput
- high capital cost

1.Masks and resists

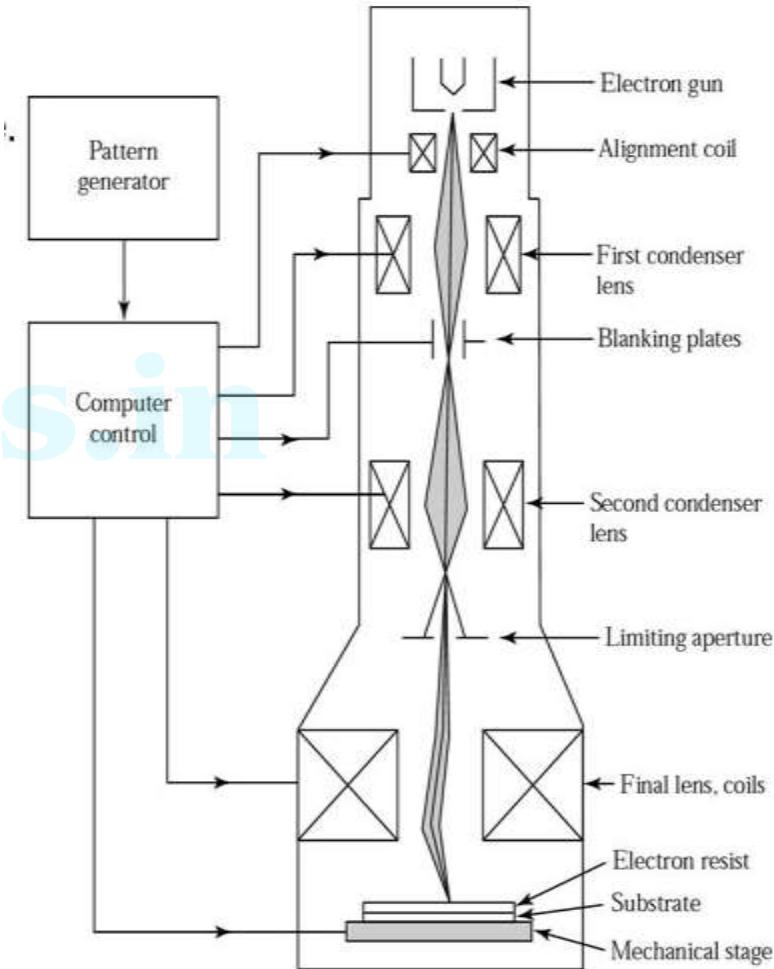
- The mask consists of a thin and low atomic number membrane and a high-atomic-number-metal-scattering element that is patterned
- Electron resists are polymers(same character as photoresist)
- Chemical or a physical change induced by radiation
- Electron exposure of resist occurs through bond breaking or the formation of bonds
- The electron beam exposes the resist where it strikes, i.e., the electrons break the molecules of the resist and so locally change its characteristics in such a way that subsequent development can either remove selectively the exposed part (positive resist) or remove the unexposed part (negative resist)



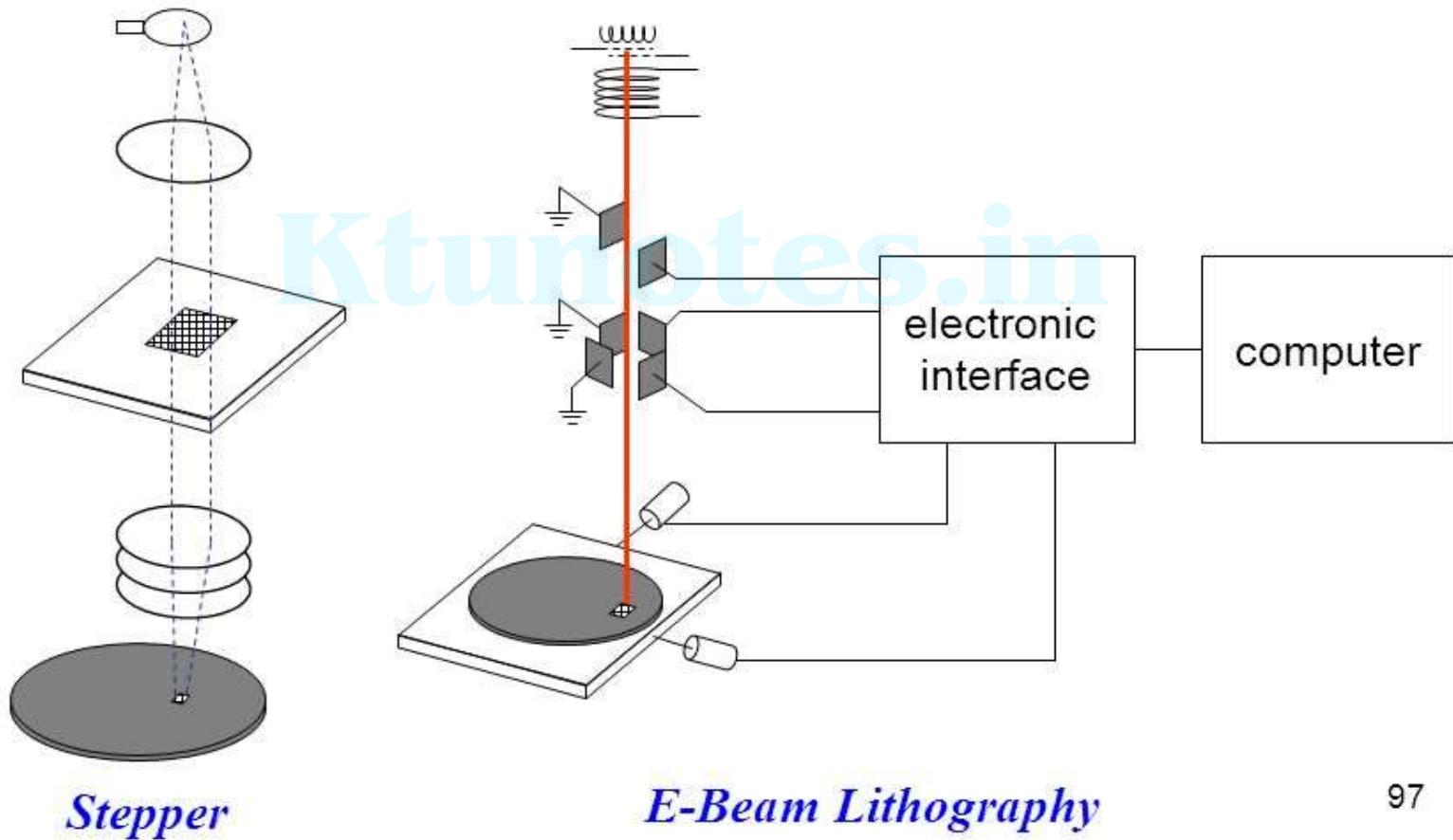
Exposure methods and printing techniques

Exposure System

- The electron gun is a device that can generate beam of electrons with a suitable current density
- A tungsten thermionic cathode can be used as electron gun
- Condenser lenses are used to focus the electron beam to a spot size of 0.01 to $0.1\mu\text{m}$ in diameter
- Beam blanking and beam deflection coils are computer controlled and operated at high speeds to direct the focussed electron beam to any location in the scan field on the substrate.

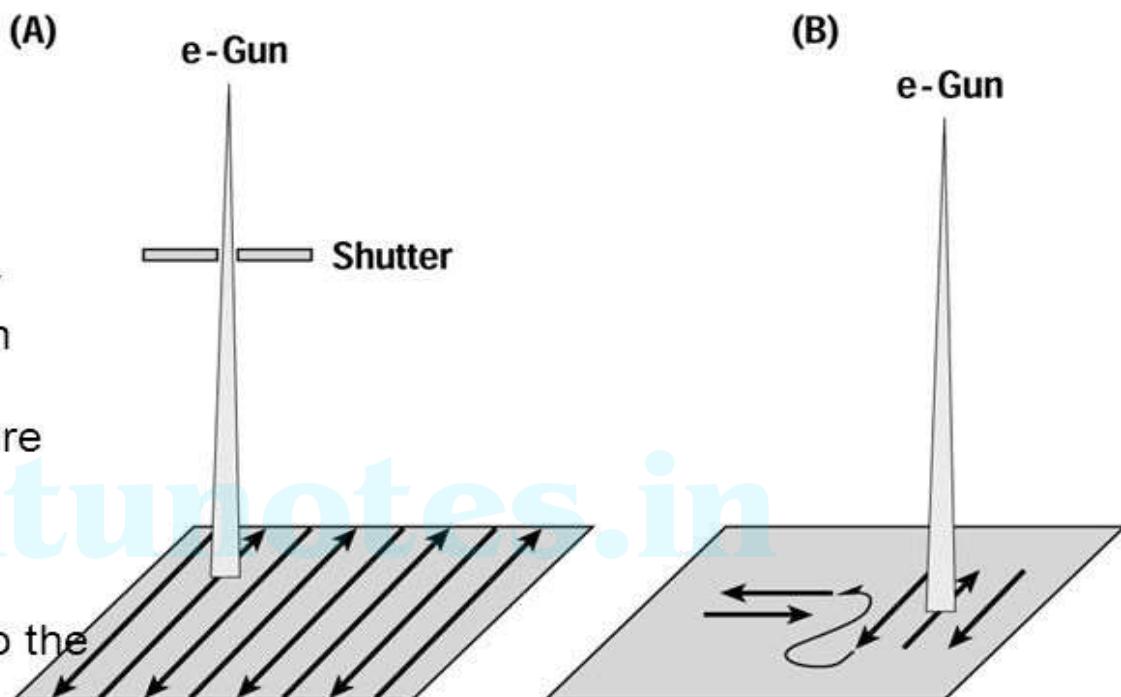


Wafer Exposure Systems



Two ways to scan the focussed electron beam

- Raster Scan
- Vector scan



In raster scan system

The beam scan sequentially over every possible location (pixel) on the mask and is turned off where no exposure is required.

In a vector scan system

The beam is directed only to the requested pattern features and jumps from features to features.

} A comparison of scanning methodologies:
raster scan (A) and vector scan (B).

Photolithographic Process

Photoresist

Si Substrate

SiO_2

Coating

Mask

Negative

Positive

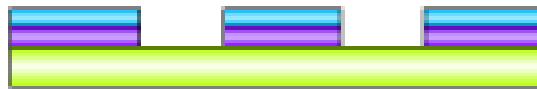
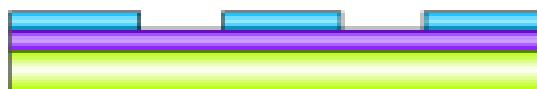
Exposure

Aqueous Base
Development

Transfer

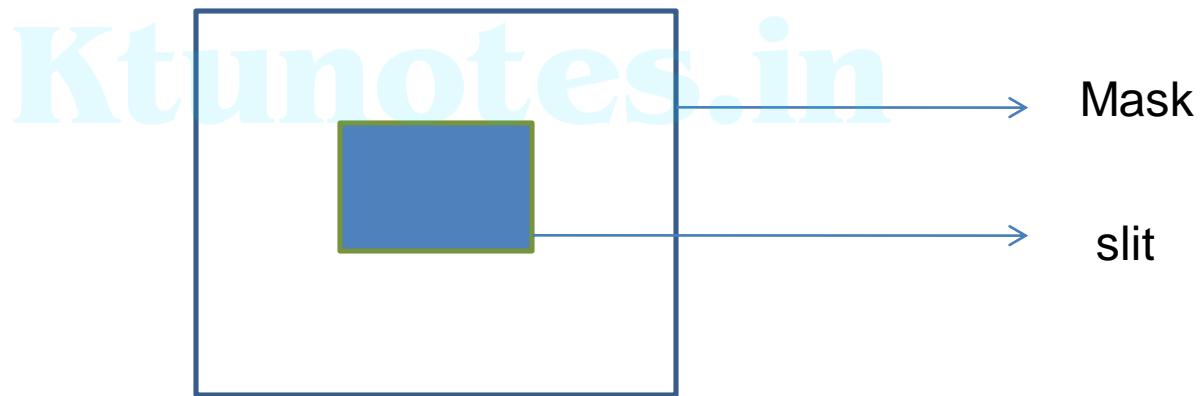
Strip

$h\nu$

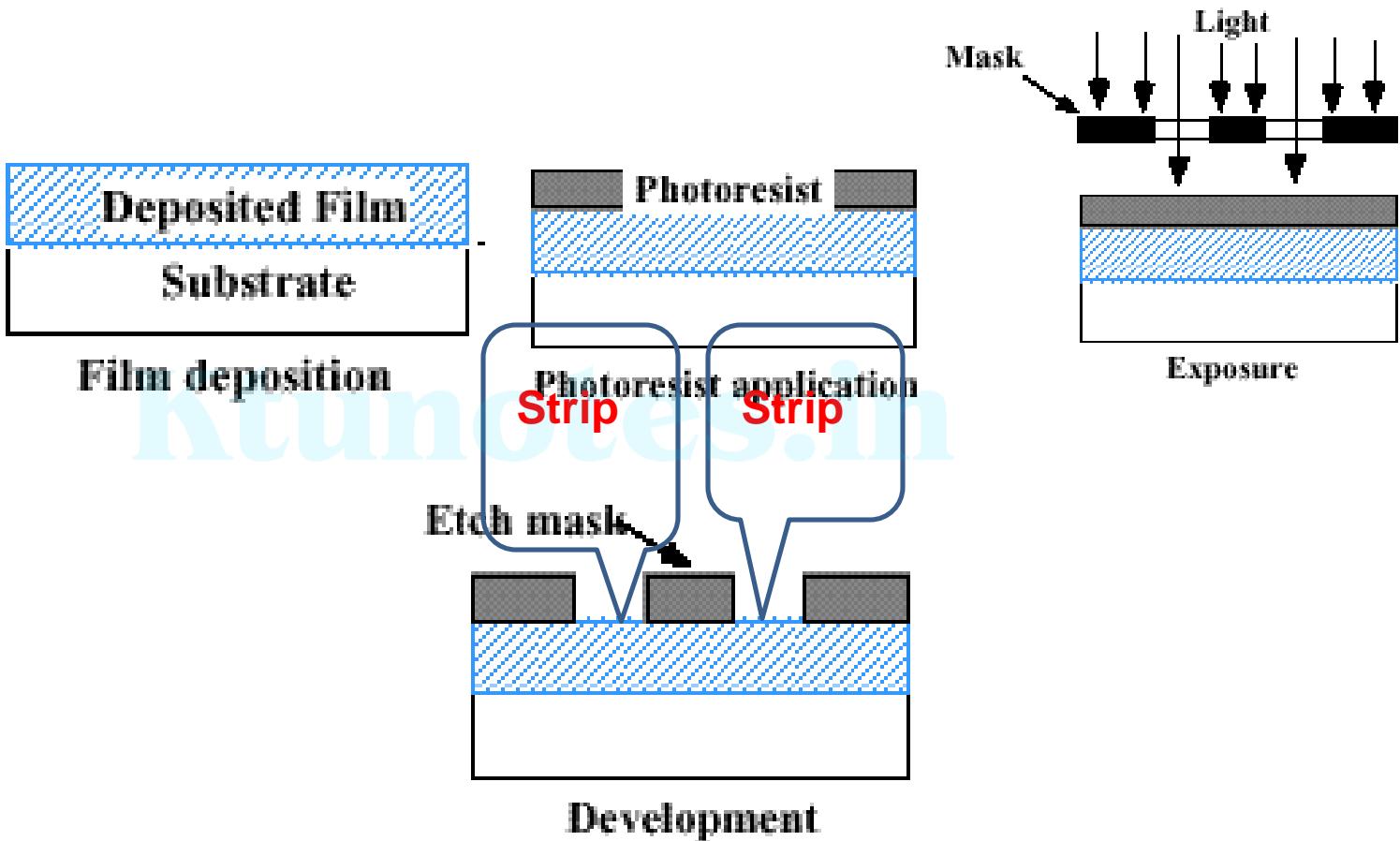


Question

- Please draw the Patterns after development of PR for +ve and -ve PR



Upto Now.....



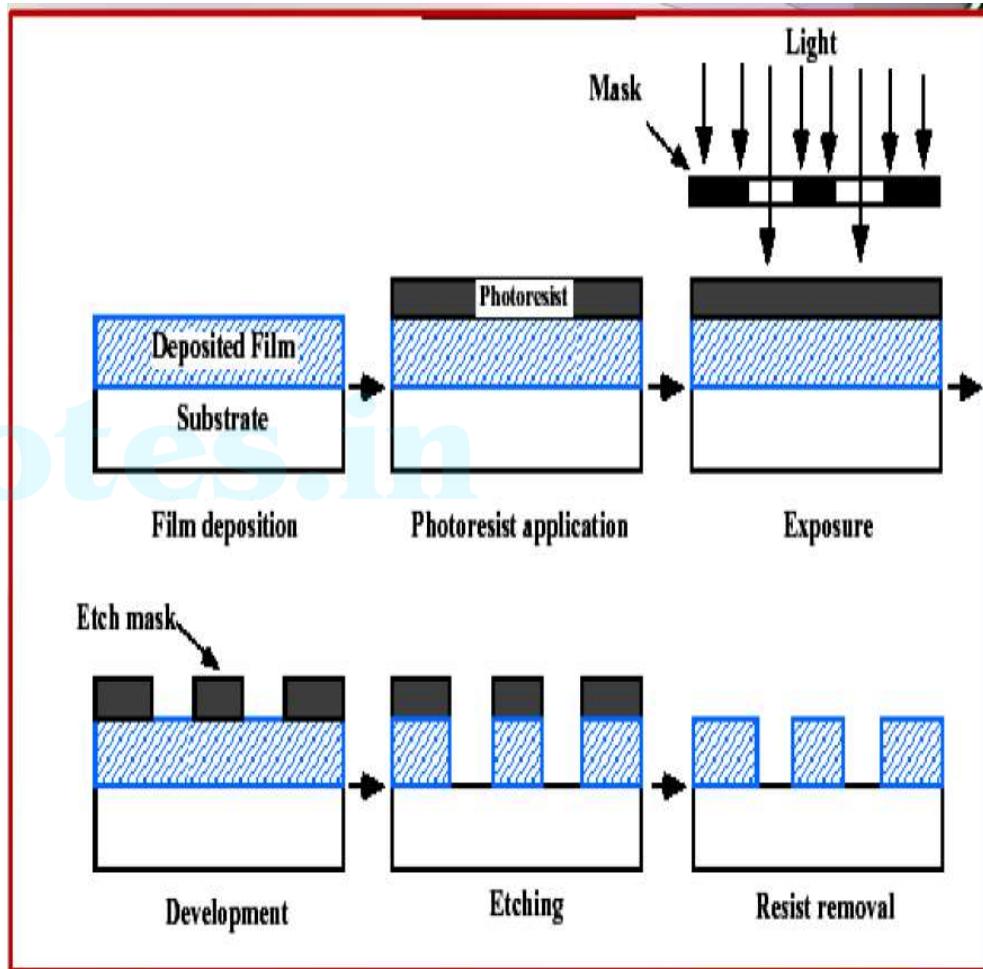
Steps of Silicon Device Manufacturing

- Oxidation
- Photolithography
- Etching
- Ion Implantation
- Diffusion
- Deposition

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Etching

- **Etching** is used in micro fabrication to selectively remove layers from the surface of a wafer during manufacturing
- Sometimes an oxide/nitride may be used as hard mask
- Multi-layer structures can be etched sequentially using same masking layer



Etching methods



- Etching Mechanisms
 - Physical removal of material (Ion milling)
 - Chemical reaction and removal (wet chemical etching)
 - Combination of both (plasma etching or dry etc)
- Etching environment: “wet” or “dry”
 - **Wet** etching uses liquid etchants with wafers immersed in etchant solution.
 - It is having chemical process only
 - **Dry** Etching uses gas phase etchants in plasma

Figures of merit

- Etch Rate (ER):
 - thickness removed per unit time
 - Dependent on etching process and film to be etched
 - Should not be too slow or too fast (poor control)
- Etch rate uniformity:
 - Depends on percentage of variation of etch rate

$$\text{Uniformity} = \left[\frac{\max ER - \min ER}{\max ER + \min ER} \right] * 100$$

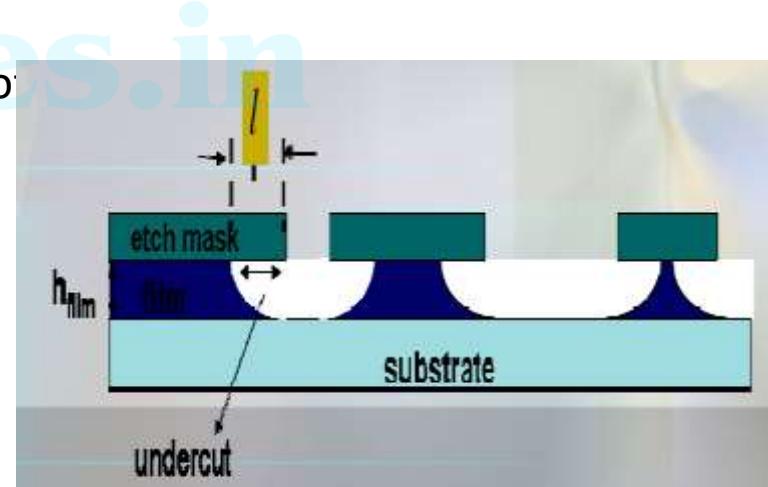
- Low value indicates etch rate is same across wafer

Figures of Merit

- Selectivity of Etch (S):
 - Ratio of etch rate of various materials
 - Sfm: Ratio of etch rate of **film** to etch rate of **hard mask/ photo resist**
 - Sfs: Ratio of etch rate of **film** to etch rate of **substrate beneath it**
 - High selectivity desired
 - Low selectivity results in etching of

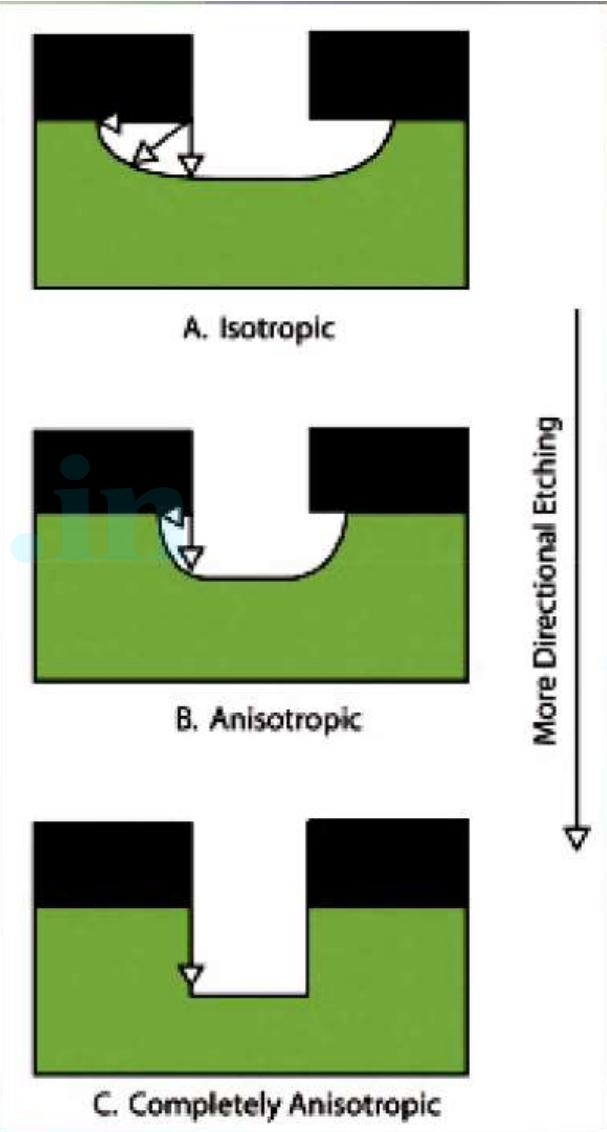
- Degree of Anisotropy (Af)

$$A_f = 1 - \frac{\text{Lateral ER}}{\text{Vertical ER}} = 1 - \frac{l}{h}$$



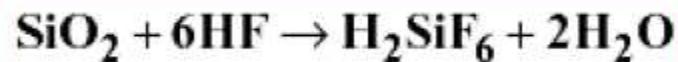
- ‘l’ represents lateral undercut while ‘h’ represents film height

- **Etch Directionality:** Measure of relative etch rates in different directions usually vertical vs. lateral
- **Isotropic Etching:** Etch rates are same in all directions. It is usually related to chemical processes
- **Anisotropic Etching:** Highly directional etching with different etch rates in different directions. Anisotropic etching is the preferred process

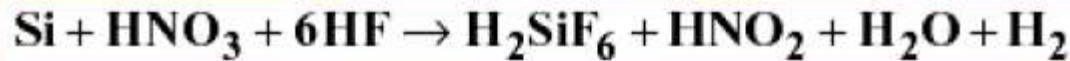


Wet etching

- The first etchants used in IC industry were wet etchants
- By immersing the wafers into baths of liquid chemicals
- Wet etches were developed for all steps in fabrication process
- A common wet etch for SiO₂ is HF, the overall reaction is

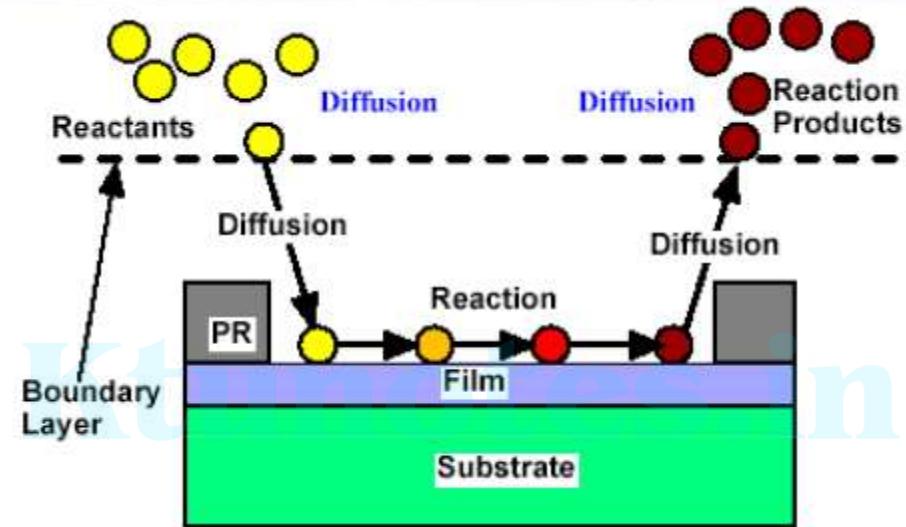


- Etching of SiO₂ by aqueous HF:
- Wet etchants work by chemically reacting with the film to form water soluble byproducts or gas
- In some cases etching occurs by first oxidizing the surface of the film or material and then dissolving the oxide
- For eg: Etching of Si by nitric acid (HNO₃) and HF, the overall reaction is



- Buffering agents are added to the etch solution to keep the etchants at maximum strength over use and time

Wet etching mechanism



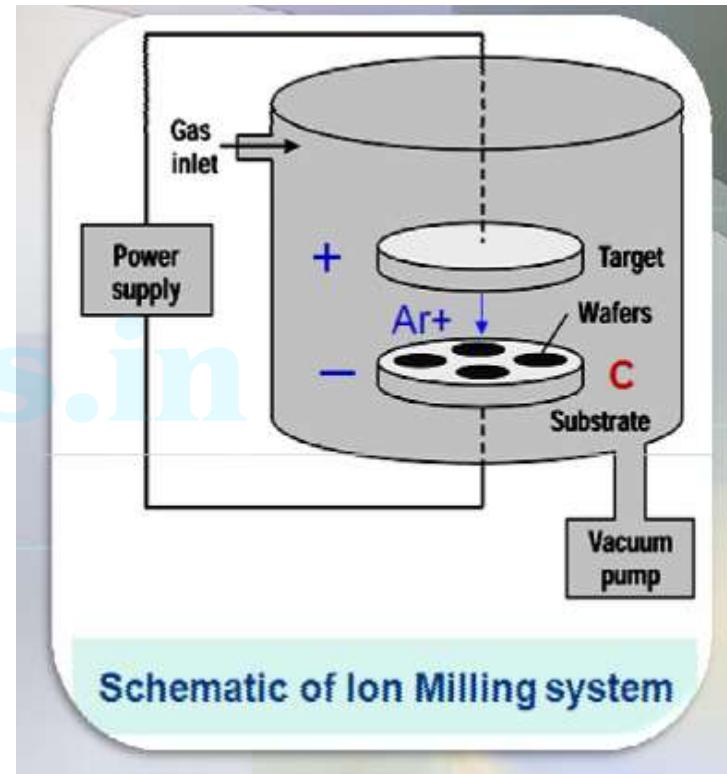
- Diffusion of reaction species through boundary layer on to wafer surface
- Reaction with desired film to form etch products
- Removal of etched products via diffusion through boundary layer to bulk liquid
- Slowest one is the rate limiting step

Wet etching challenges

- Mask or PR dimensions erode during etch
 - Need to account for mask erosion
- Formation of bubbles inhibit etching process
 - Stirring and heating help overcome this and minimize boundary layer
- Etch rate is very temperature sensitive, and hence difficult to achieve uniformity across the wafer
- High Selectivity and Low Degree of Anisotropy

Ion Milling(physical etching)

- Use of an energetic beam of inert atoms in a very low pressure chamber
- Etching by **physical action**
- Here wafers are placed in one electrode
- Here ionic species such as Ar⁺ accelerated to the wafer surface
- Argon ions strike the wafer instead of the target. This causes removal of material from wafer depending on incident ion energy
- Low pressure needed to maintain plasma (10^{-3} Torr).
- Magnetic field can be used to increase ion density



Ion Milling

- Kauffman source (thermal) is used for generating Ar⁺ ions.
- Consist of electron filament heated using the supply V_f.
- Electrons from filament collide with Ar⁺ atoms to ionize them
- Low pressure needed to maintain plasma (10⁻³ Torr).
- A grid held at a voltage V_g accelerate the ejected ions towards the target.
- Positive ions are collected through the negatively biased perforated shield on to wafer
- Magnetic field can be used to increase ion density

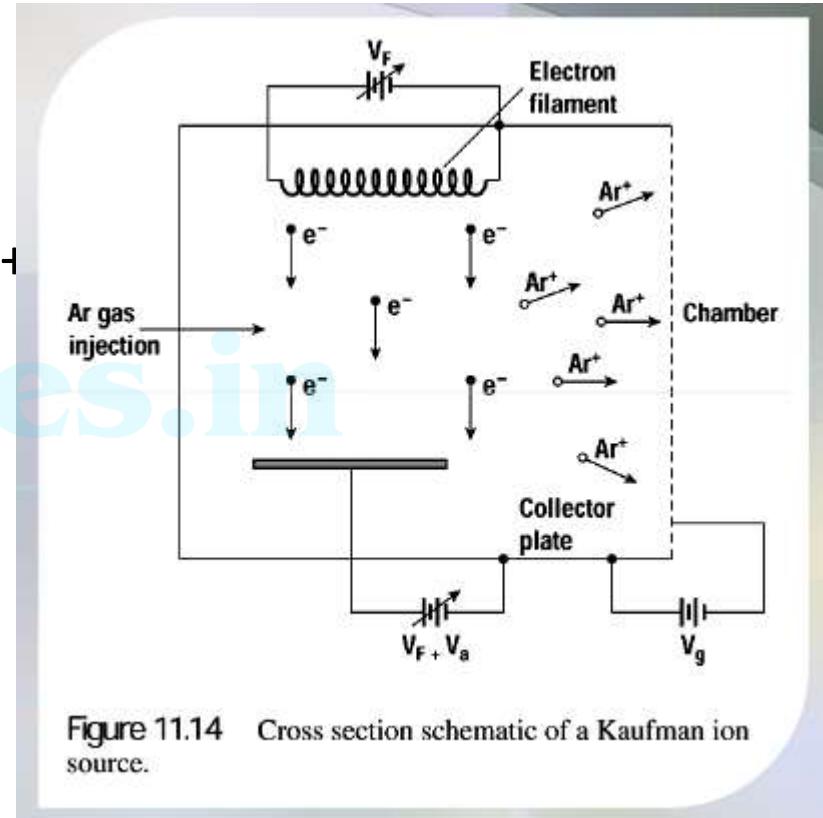
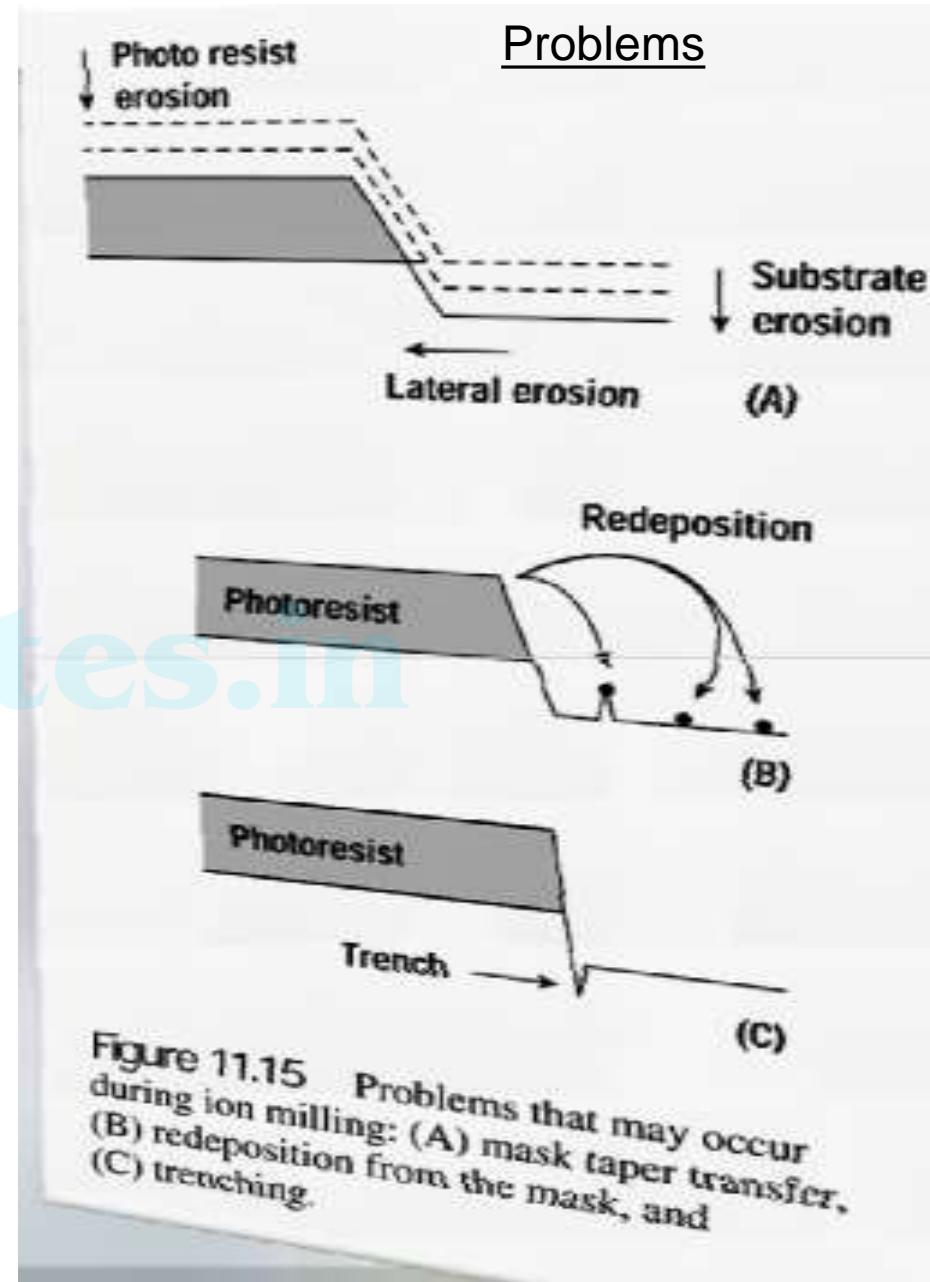


Figure 11.14 Cross section schematic of a Kaufman ion source.

Ion Milling

advantages

- Very good anisotropy: etching mostly in vertical direction
- Can be used for etching wide variety of films (dielectrics, metals, etc.)
- Poor selectivity: will easily etch the substrate below and photoresist
- Low throughput (one wafer at a time)
- To increase selectivity of ion milling, some reactive species need to be introduced



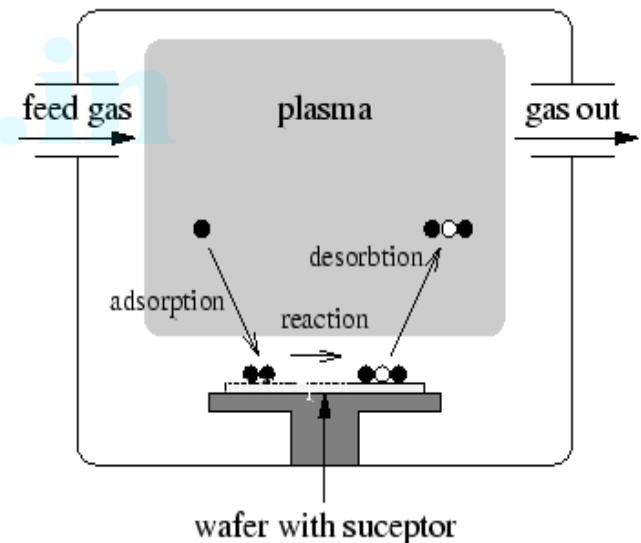
Notes....

- ❑ Since this process erode the mask, any taper in the masking layer will transferred to the pattern
- After etch is done and photoresist mask has been removed the resultant pattern broadened and appear similar to undercut
- Since the erode material from the target is not volatile some of it redeposit on the surface of wafer
- Some milling cross section shown an enhanced

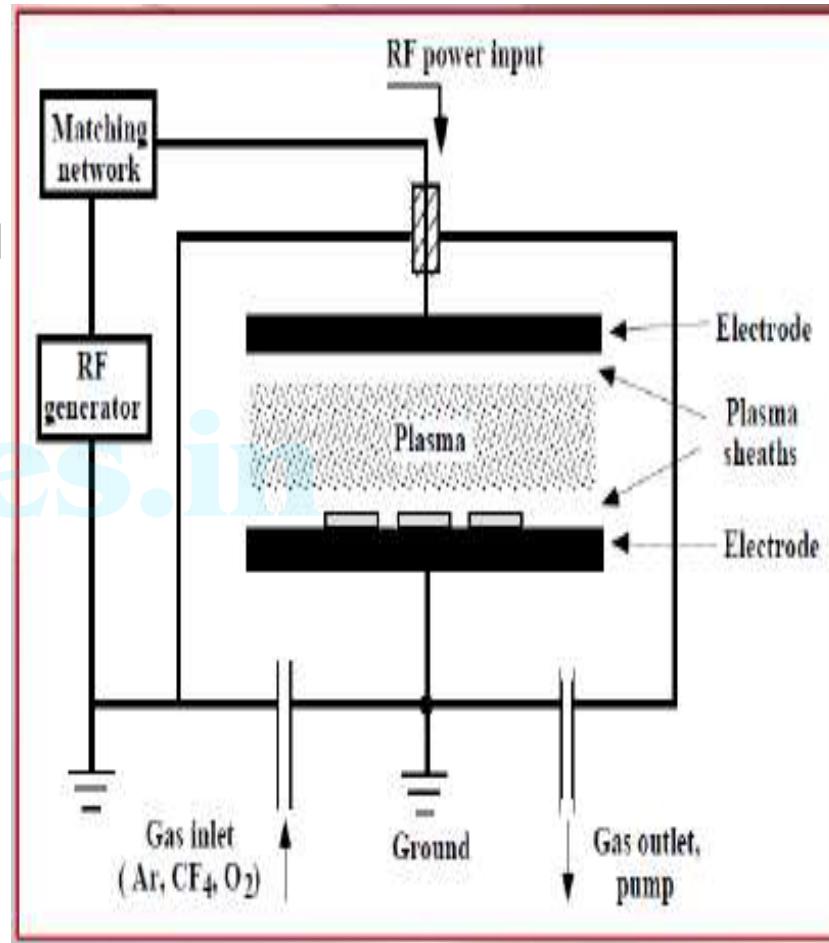
Plasma Etching

- Chemical + physical process
- Etch rate is faster
- Plasma
- **plasma** is a state of matter similar to gas in which a certain portion of the particles are ionized
- Plasma systems ionize a variety of source gases in a vacuum system by using RF generator
- The frequency of operation of the RF

- Four step process
 - Formation of active gas species
 - Transport of the active species to the surface
 - Reaction at the surface
 - Pump out the reaction products

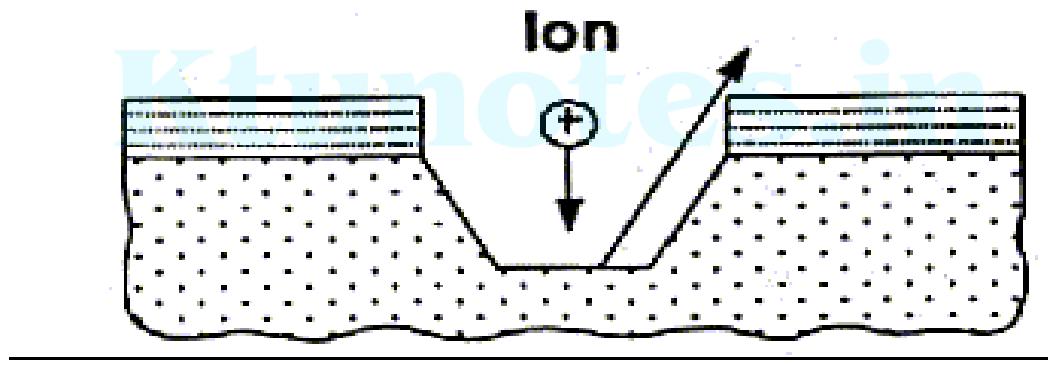


- Here low pressure gas is used in chamber(1mtorr-1torr)
- By applying the high electric field across two electrodes, some of the gas atoms are ionized ,producing positive ions and free electrons and creating plasma
- A voltage bias develop between plasma and the electrodes due to difference in mobility of electrons and ions
- plasma being biased positively w.r.t the electrodes
- The high energy electrons in plasma can cause Variety of reaction to occur with reactant gases



➤ Results plasma contains free electrons, ionized molecules, neutral molecules ,ionized fragments of broken up molecules and free radicals

- Two types of species 1).reactive neutral chemical specious(chemical etching) 2).ions (physical etching)
- Sputter Etching(physical etching)

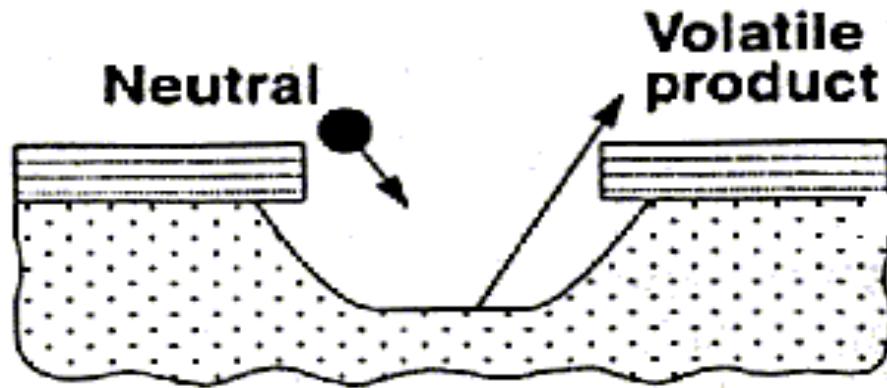


- Ions created by the plasma and propelled by the sheath potentials to knock loose particles
- Pressure has to be low

Chemical Etching

- Plasma generates neutral species
- Neutral species spontaneously react with substrate material

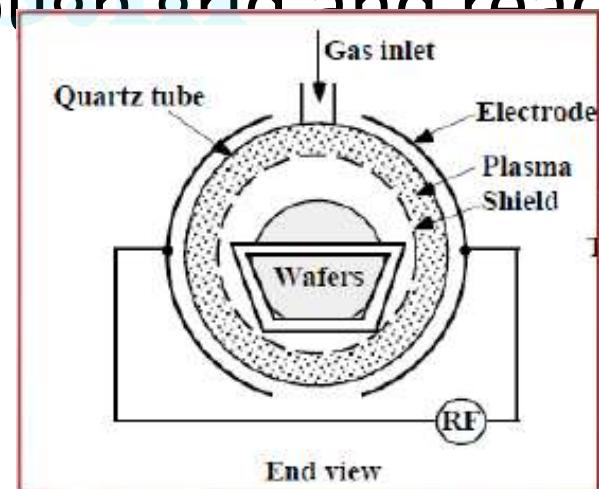
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- Reactive species diffuses through to the wafer, gets adsorbed, and reacts with exposed film.
- Reaction product is desorbed, and diffuses away from wafer
- Neutral species form the chemical component while the ions form the physical component of etch
- As RF power is increased, plasma density increases, and hence plasma voltage also increases thereby increasing ion velocity

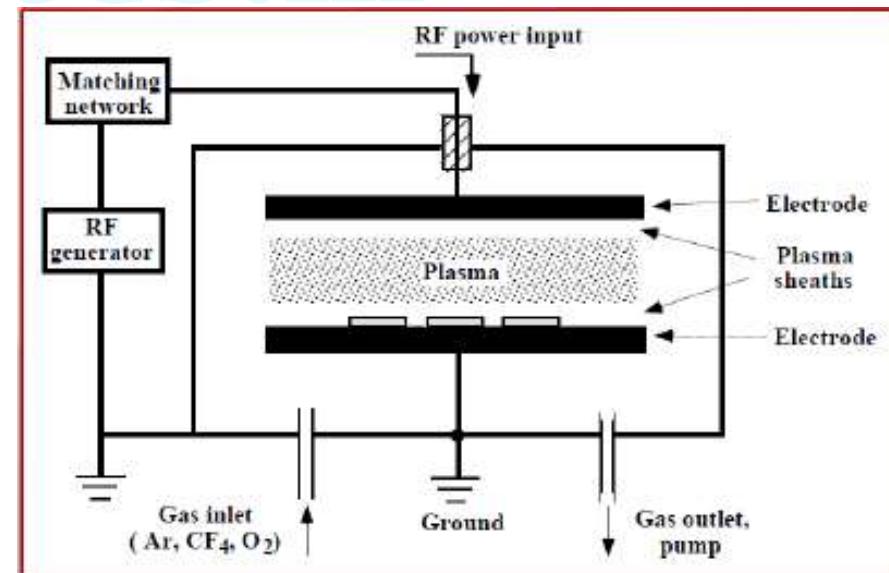
Plasma Etching configuration

- **Barrel Etchers**
- Wafers are kept isolated from electrodes and plasma by means of a metal grid shield
- reactive species diffuse through grid and react with wafers
- purely chemical etch



Plasma Etching configuration

- **Parallel plate plasma etcher**
- The electrode on which the wafer is sitting is connected to ground along with the walls of the chamber
- increases effective area of bottom electrode with respect to top electrode
- Voltage drop of plasma is lower with respect to bottom electrode
- moderate ion velocity
strong chemical component
- Reactive ion etching(RIE)



Sidewall passivation

- Higher anisotropy in plasma etching achieved by **sidewall passivation**
- Neutral atoms (non volatile flourocarbon) stick to sidewall as etching occurs – this prevents undercutting and improves anisotropy
- The non-volatile species also deposit on the horizontal etch surface, but can be removed by increasing physical bombardment of ions

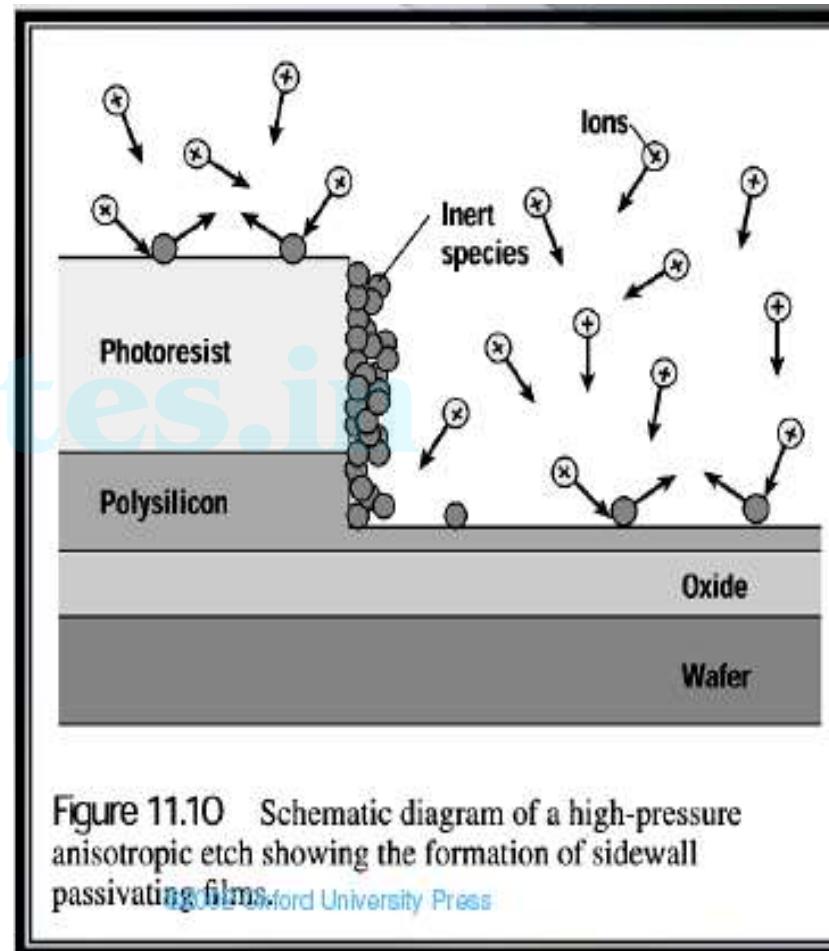
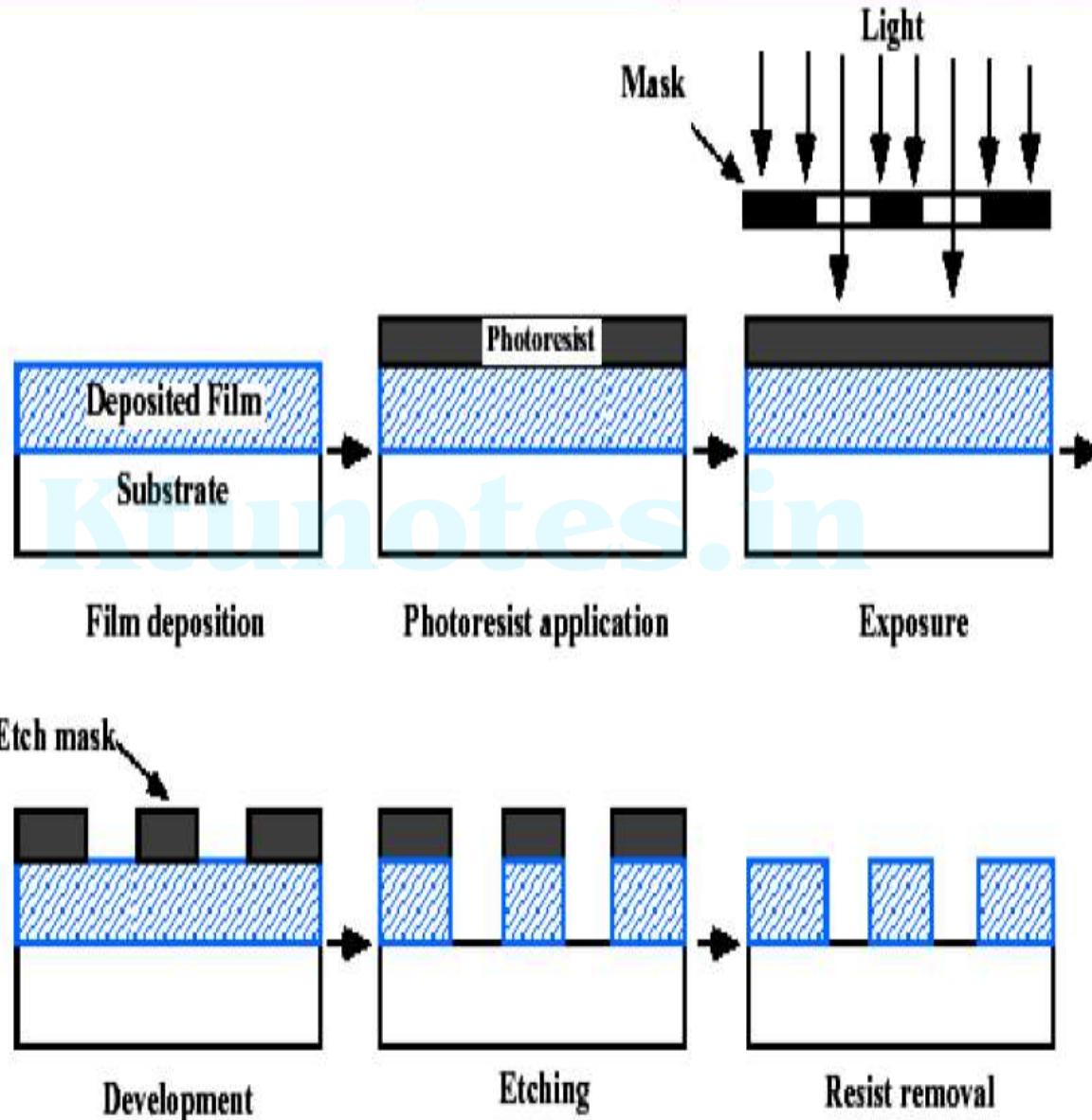


Figure 11.10 Schematic diagram of a high-pressure anisotropic etch showing the formation of sidewall passivating films
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Steps of Silicon Device Manufacturing

- Oxidation
- Photolithography
- Etching
- Ion Implantation
- Diffusion
- Deposition

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Doping Silicon

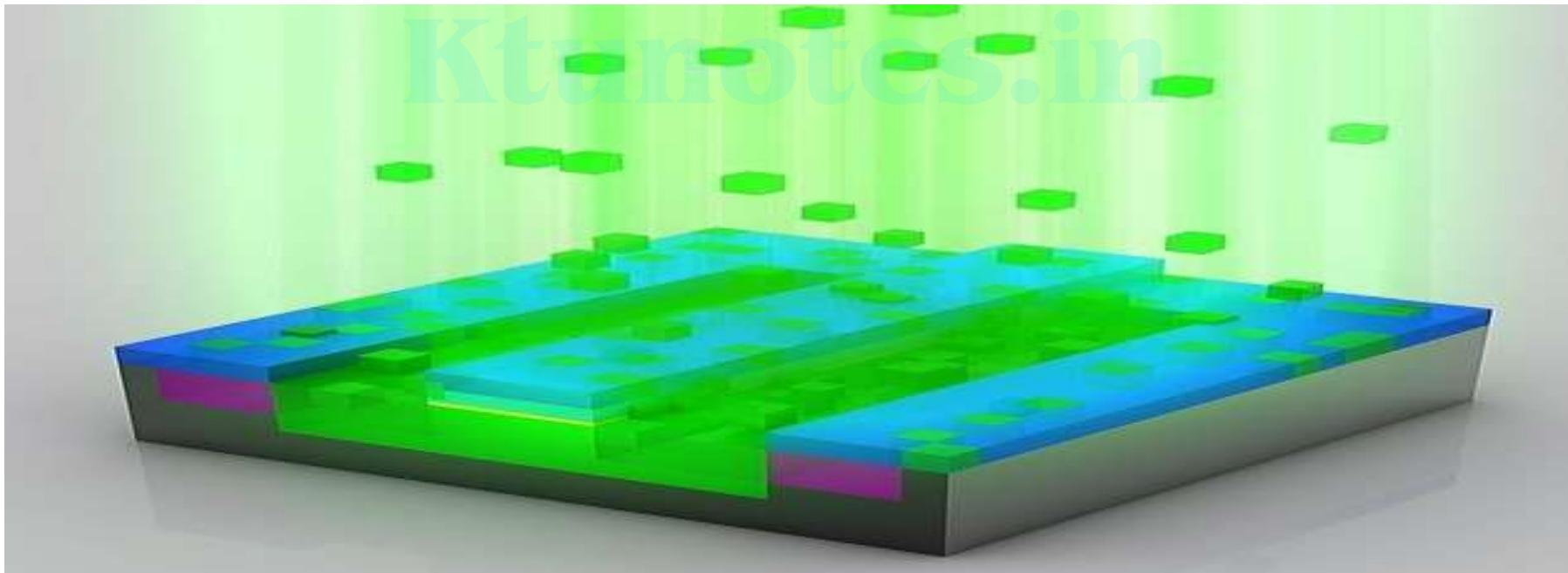
Doping by Diffusion and Implantation

Diffusion :

The spread of particles through random motion from regions of higher concentration to regions of lower concentration

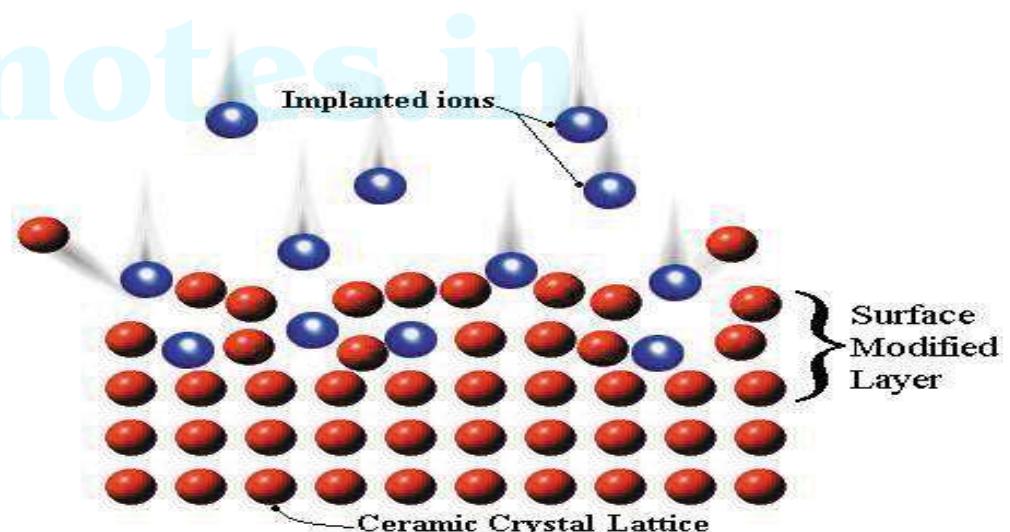
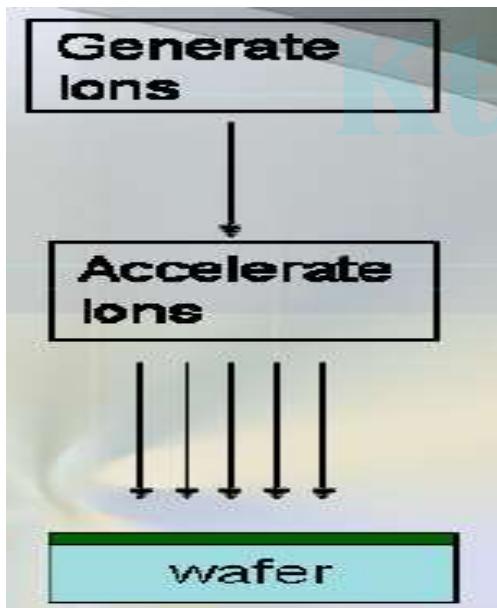
Ion implantation

Bombarding the substrate with ions accelerated to high velocities



Ion Implantation

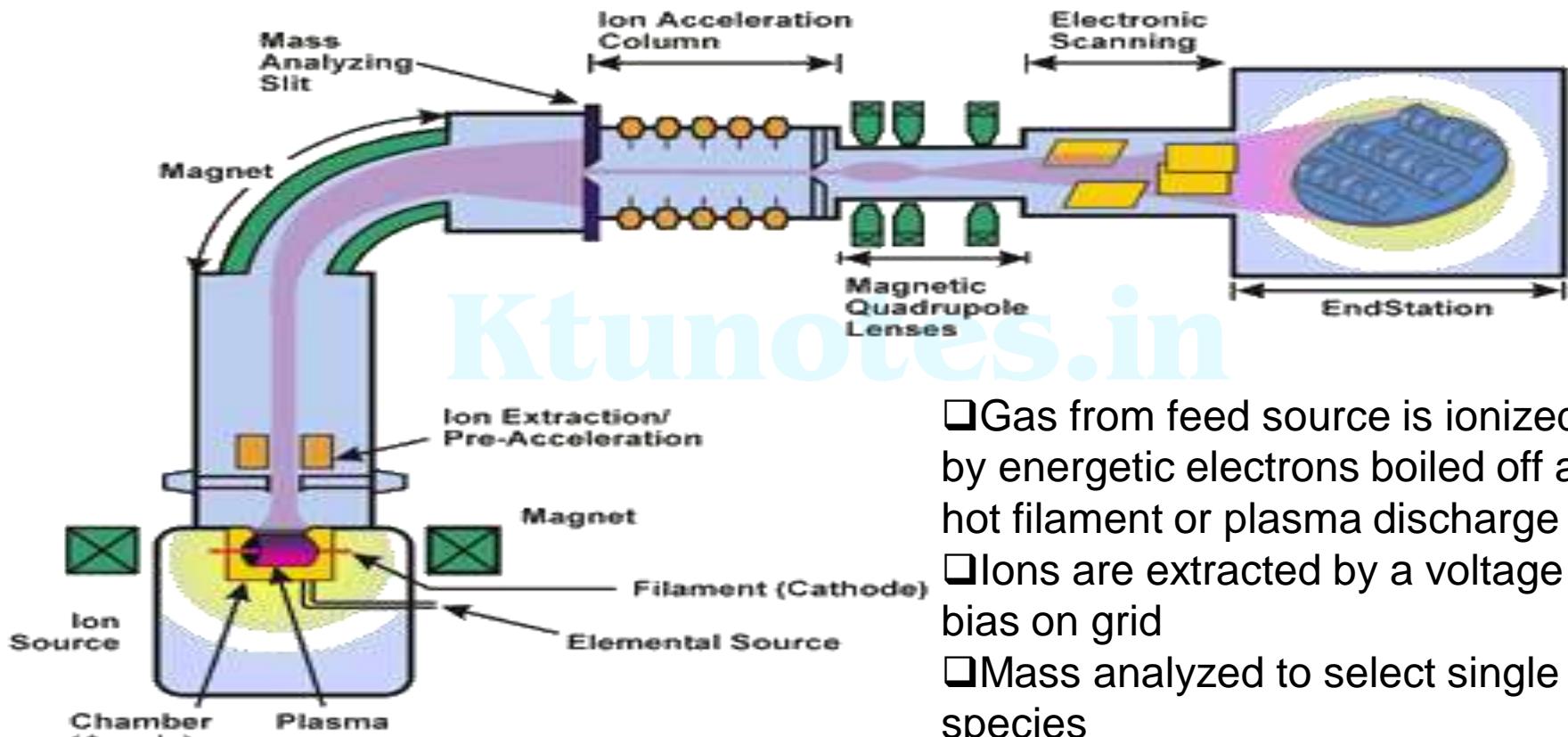
- Dominant doping technique for past 20 yrs
- Ionized impurity atoms are accelerated by an electrostatic field and made to strike the surface of wafer.



- Direct bombardment of accelerated dopant ions onto the substrate
- Cascade of damages created in the perfect Si lattice -removed by annealing
- Precise control on the amount and distribution of the dose
- Energy of ions control the distribution
- Ion beam current controls the dose

Implantation System

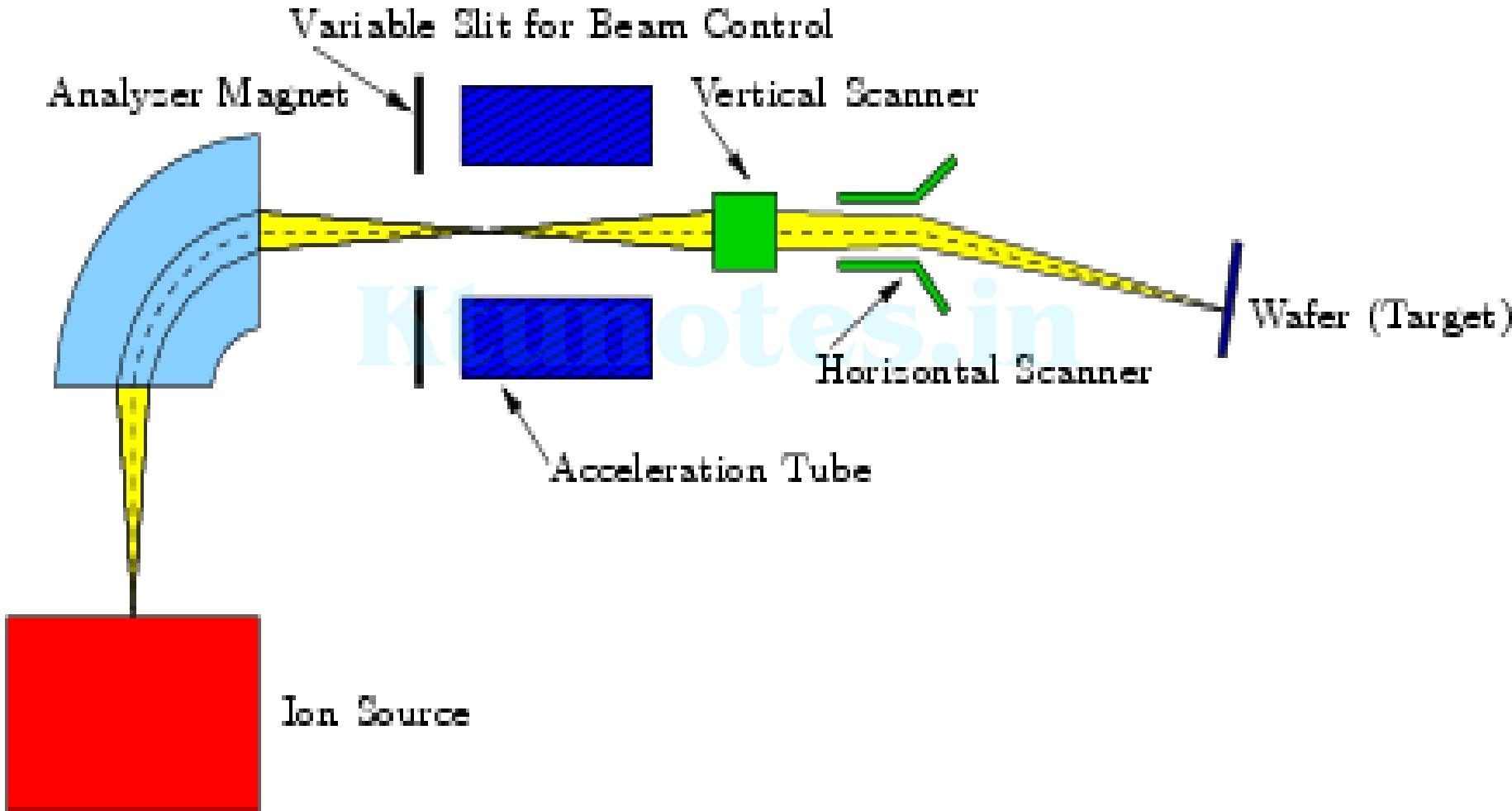
- It consists of **Ion Source, Mass Analyzer, Acceleration Tube , End Station**



❑ Electrons accelerated towards the plate.

- ❑ Gas from feed source is ionized by energetic electrons boiled off a hot filament or plasma discharge
- ❑ Ions are extracted by a voltage bias on grid
- ❑ Mass analyzed to select single ion species

Generalized Block diagram



Ion source

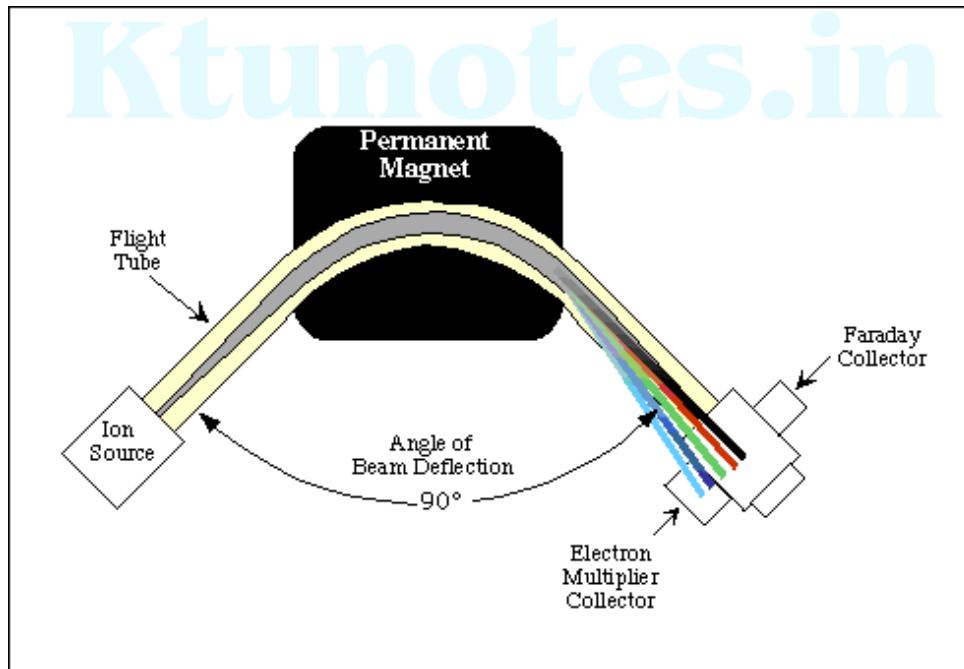
- Ion source starts with feed gas that contains the desired implant specious
 - Consists of feed gas of impurity atom
 - For ntype-Phosphorus,As
 - Ptype-Boron,Galium
 - BF₃ for B and PH₃ for P
- Electron beam collide with feed gas molecules ,transferring some of their energy
- Transfer energy is large enough, molecular dissociation occur
 - Different Ions are formed.

Eg:B+,BF₂+,F+ etc

Negative ions are less abundant

Mass Analyzer

- The ion beam is passed through a magnetic sector that selects a particular ionic species

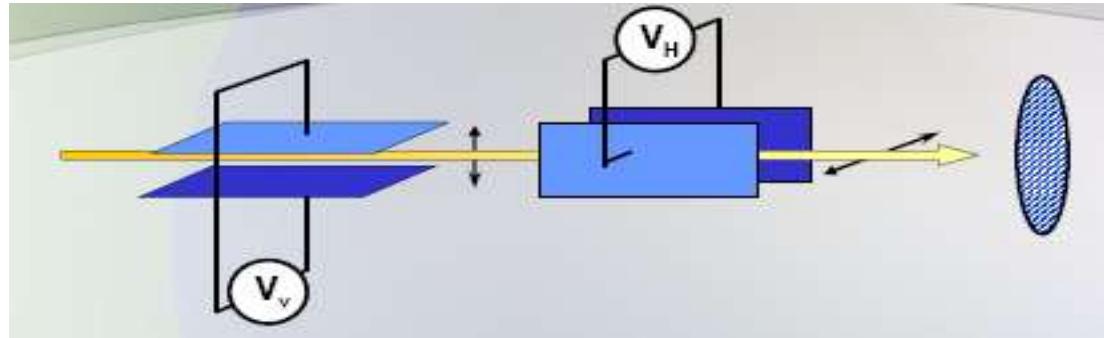


- The purpose of Mass Analyzer is to extract ions with respect to its mass.
- The beam enters a large chamber maintained at low pressure
- Magnetic field applied perpendicular to beam.
- According to the mass, the trajectory will be different. Neutral species are not deflected.
- Lorentz force acting on the charged particle is balanced by the centrifugal force on the particle

$$\frac{Mv^2}{r} = qvB$$

v is the magnitude of ion velocity, q is the charge on the ion, M is the ion mass, B is the magnetic field intensity, r is the radius of curvature

Ion Acceleration



- The mass-analyzed ions are accelerated by an electrostatic linear accelerator
- Horizontal and vertical electrostatic deflection plates are used to raster the beam across the sample to improve implant uniformity

Ion stopping mechanism

- Ions penetrate into substrate
 - Collide with lattice atoms
 - Gradually lose their energy and stop
- ❑ Two stop mechanisms
- Nuclear Stopping:
- Collision of ions with nuclei of the lattice atoms
 - Depends on Ion energy
 - Tends to dominate at the end of the stopping process when ions have lost much of their energy
 - Produces crystal structure damage
- Electronic Stopping:
- Proportional to velocity of incident ion
 - Crystal structure damage is negligible
 - Energy transfer is very small

- Nonlocal electronic Stopping:
 - Drag experiences by the moving ion in a dielectric medium;
 - dissipative, does not alter the trajectory
 - Depends on ionization state of the ion
- Local electronic Stopping
 - If ion passes close enough to the lattice atoms so that their electron wave functions overlap, there can be charge exchange and momentum exchange
 - This reduces the ion energy and give rise to a force on ion which slow it down Crystal structure damage is negligible
- The total stopping power
$$S_{total} = S_n + S_e$$
- S_n : nuclear stopping, S_e : electronic stopping

Range theory

- The theory provides a statistical description of the dopant profile
- **Range R** of an ion is the actual distance travelled by it before stopping
- stragggle → deviation or variance
- **Projected Range R_p** is the average distance travelled normal to the surface
- Higher energies → deeper range and more stragggle.
- Lighter ions → deeper range and more stragggle.

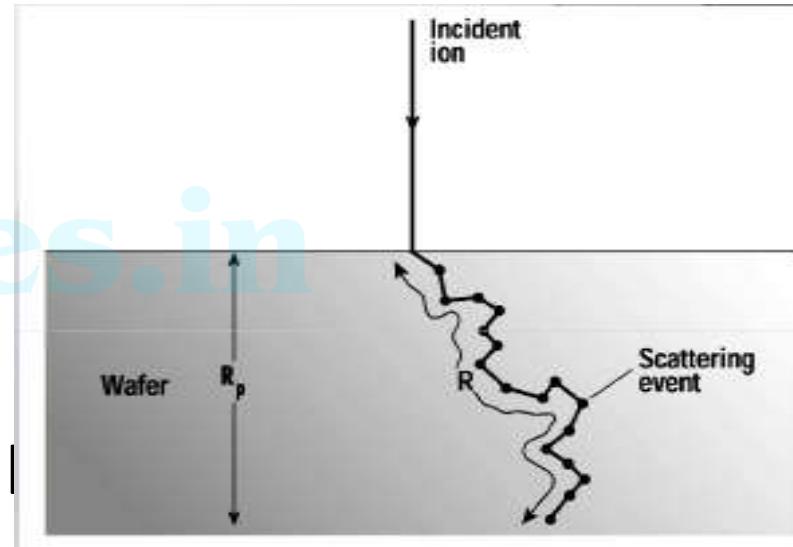
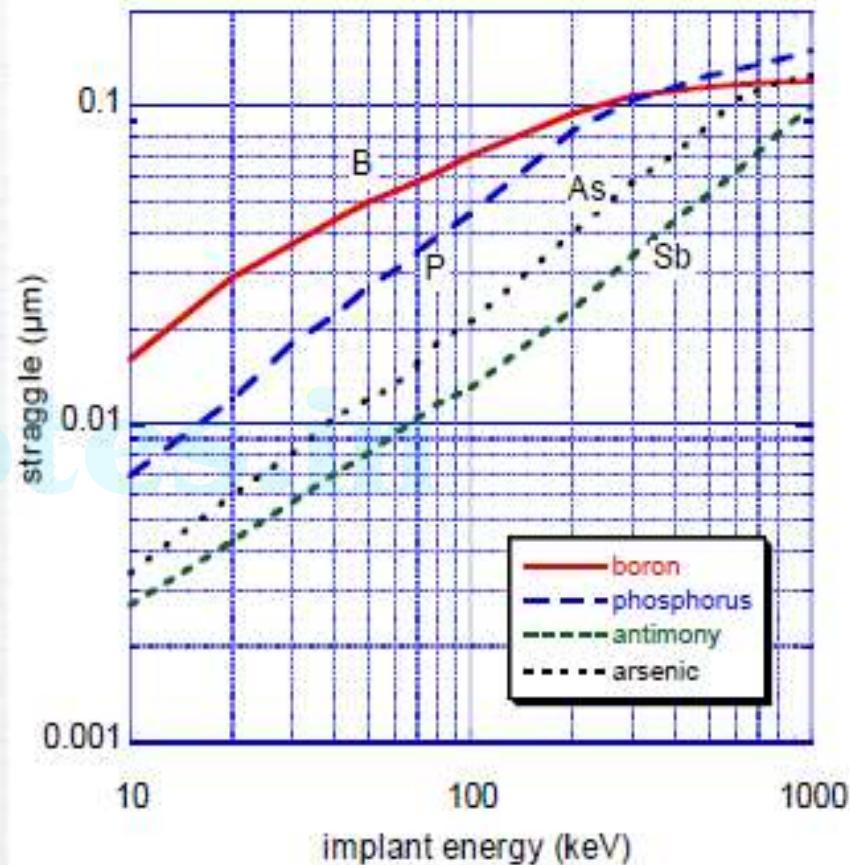
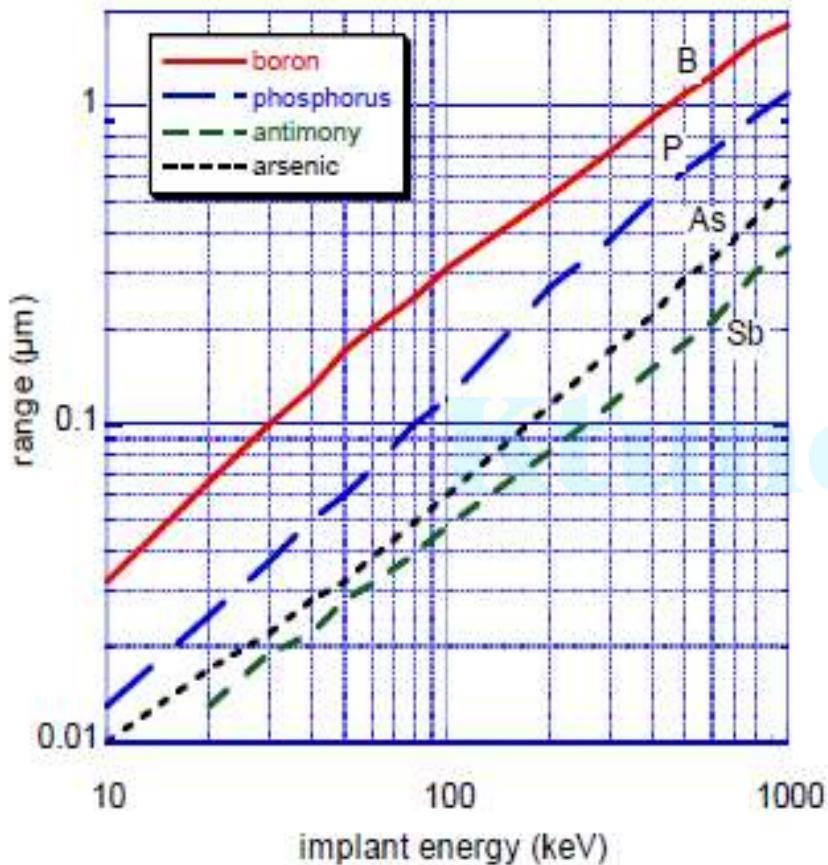


Figure 5.7 The total distance that an ion travels in the solid is the range. The projection of this distance along the depth axis is the projected range, R_p .

Range and straggle for implants into silicon



R_p and ΔR_p are determined by ion energy.

Implant profile

simplest description

$$N(x) = \frac{Q}{\sqrt{2\pi}\Delta R_p} \exp\left[-\frac{(x - R_p)^2}{2(\Delta R_p)^2}\right]$$

$Q \rightarrow$ dose

$R_p \rightarrow$ range (average depth of ion travel)

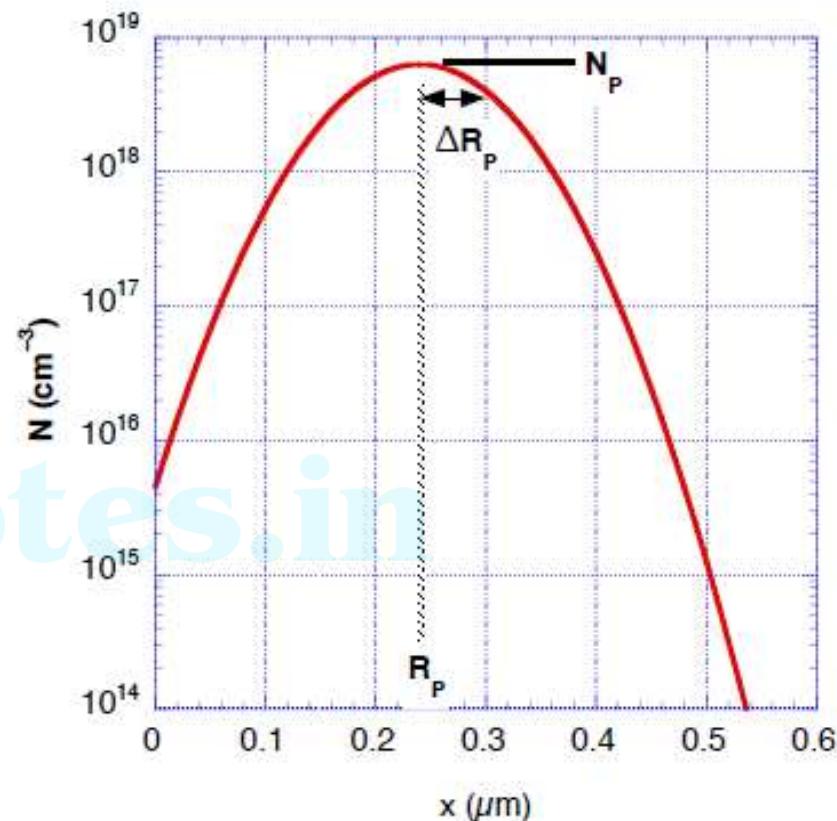
$\Delta R_p \rightarrow$ straggle (variance in ion depth)

Q is fixed by the implant time

$$Q = \frac{1}{q} \int_0^t I_{beam}(t') dt'$$

Measure the beam current. Stop after the required amount of charge (in the form of dopant atoms) has arrived.

Impurity concentration as a function of depth in solid will be given by



peak concentration

$$N_p = \frac{Q}{\sqrt{2\pi}\Delta R_p}$$

Phosphorous is implanted in a p-type silicon sample with a uniform doping concentration of 5×10^{16} atoms per cm^3 . If the beam current density is $2.5 \mu\text{A}$ per cm^2 and the implantation time is 8 minutes, calculate the implantation dose and peak impurity concentration. Assume $\Delta R_p = 0.3 \mu\text{m}$

Solution

Implantation dose, $Q = \frac{J \times t}{q}$

$$Q = \frac{J \times t}{q} = \frac{2.5 \times 10^{-6} \times 8 \times 60}{1.6 \times 10^{-19}} = 7.5 \times 10^{15} \text{ cm}^{-2}$$

-----2 marks

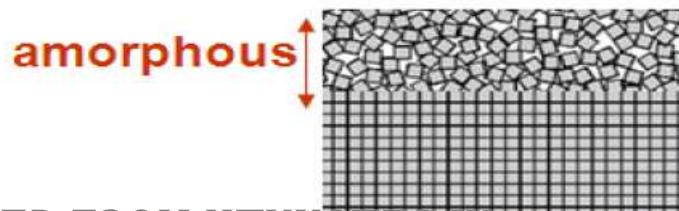
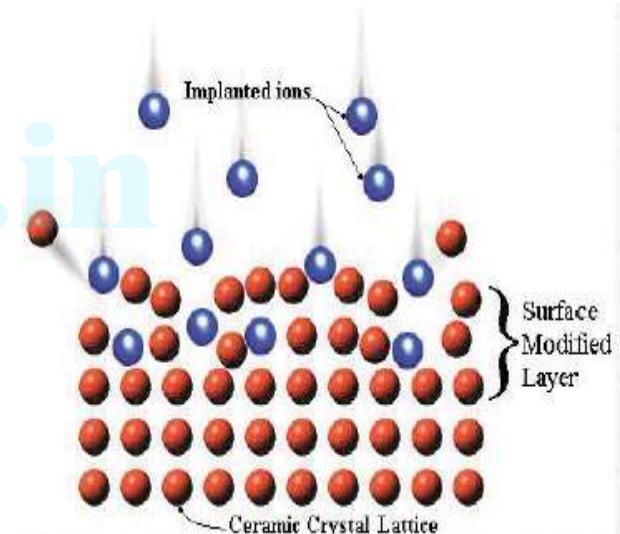
$$\frac{Qo}{\Delta R_p \sqrt{2\pi}}$$

Peak impurity concentration=

$$\frac{Q}{\Delta R_p \sqrt{2\pi}} = \frac{7.5 \times 10^{15}}{0.3 \times 10^{-6} \times 100 \times \sqrt{(2 \times 3.14)}} = 9.97 \times 10^{19} / \text{cm}^3$$

Damage During implantation

- Nuclear stopping – ions transfer energy to lattice atoms; crystalline structure damaged
- Energy required to displace a Si atom to create a Frenkel pair is 15eV
- Damage to the crystal is in the following ways:
 - Creation of interstitials and vacancies
 - Creation of local zones of amorphous material
- High dose implants might turn crystal to amorphous state
- The above two types of damage are called Primary crystalline damage Repaired by thermal process known as **annealing**



Annealing

- The main purpose is to repair lattice damage and to put the dopant atoms on substitutional sites

Different methods of annealing are

- Furnace annealing
- Rapid thermal annealing
- Furnace annealing**
 - annealing characteristics depends on the dopant type and dose involved
 - Amorphous layer recrystallizes when annealed at 600°C for 30min (called solid phase epitaxy)
 - Due to the high activation energies required to annihilate defects (~5eV), it is often easier to regrow the crystal from an amorphous layer via SPE (activation energy ~2.3eV in Silicon) than it is to anneal out defects. Thus, two schemes for implants are used:
 - Implant above the critical dose and use low temperature anneal to re grow material.
 - Implant below the critical dose and use high temperature anneal to get rid of defects.

Rapid thermal processing/annealing

Dopants can diffuse during high temperature anneal (activation energy ~3-4eV)

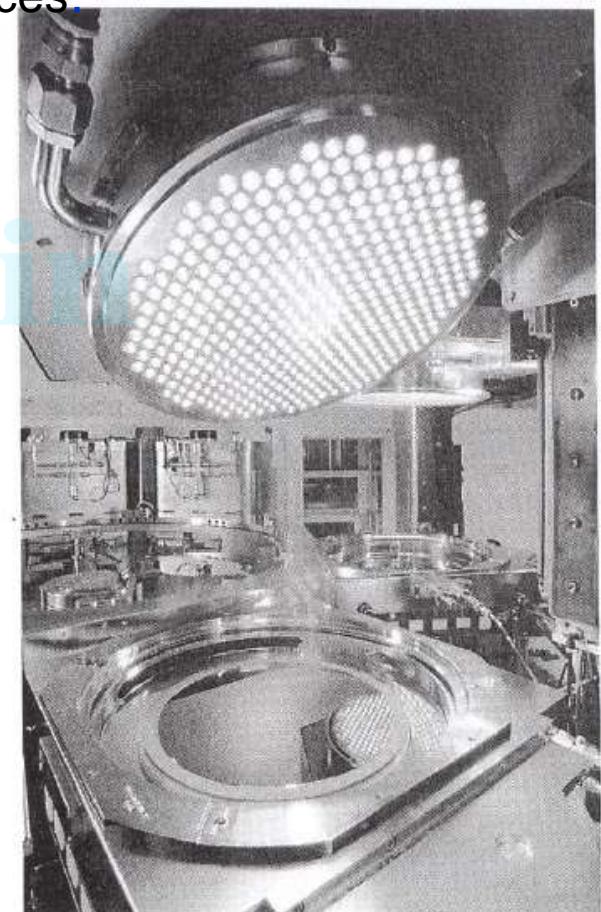
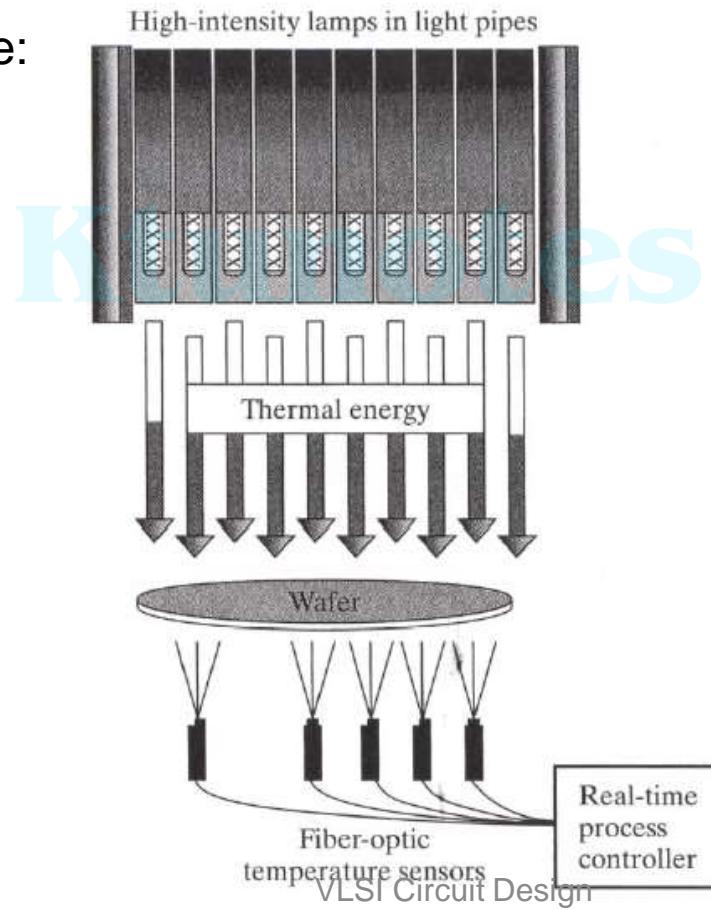
To minimize this unwanted diffusion, one can use Rapid Thermal Processing (RTP) or Rapid Thermal Anneal (RTA).

RTA is extremely important for shallow junction devices.

Rapid heating source:

- high power laser
- electron beam
- high intensity halogen lamp

Applied Materials
300mm RTP System



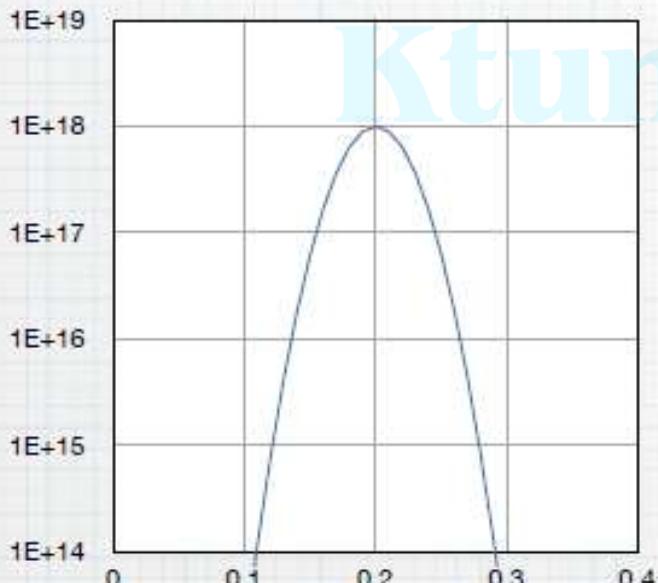
(b)

- RTA is divided in to three categories
 1. Adiabatic-heating time too short
 2. Thermal flux-time scale between 10^{-7} and 1 s
 3. Isothermal-heating process longer than 1s
- RTA heating occurs because photons are absorbed by free carriers in the si,when they transfer energy to the lattice
- The rate of heating depends on the number of carriers ,which is a function of temperature ,doping and on surface emissivity

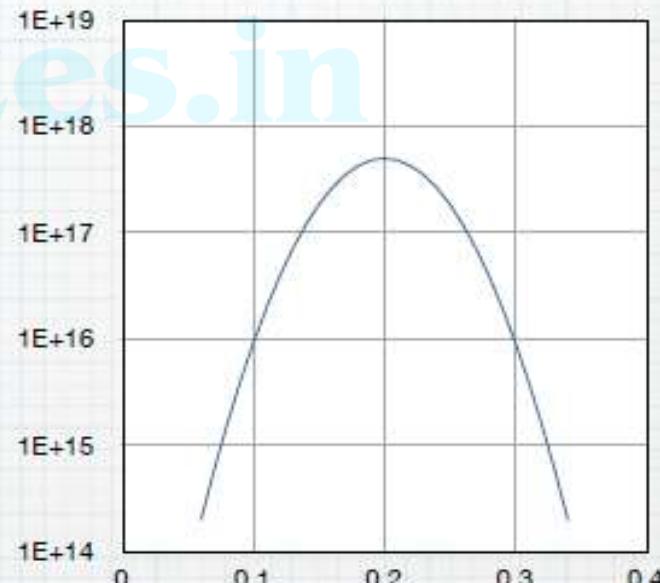
Dopant diffusion during annealing

Of course, during the anneal, dopant will diffuse.

Before anneal



After anneal



Steps of Silicon Device Manufacturing

- Oxidation
- Photolithography
- Etching
- Ion Implantation
- Diffusion
- Deposition

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Diffusion

- Mass transport by atomic motion.
- Diffusion is a consequence of the constant thermal motion of atoms, molecules and particles that results in material moving from areas of high to low concentration.

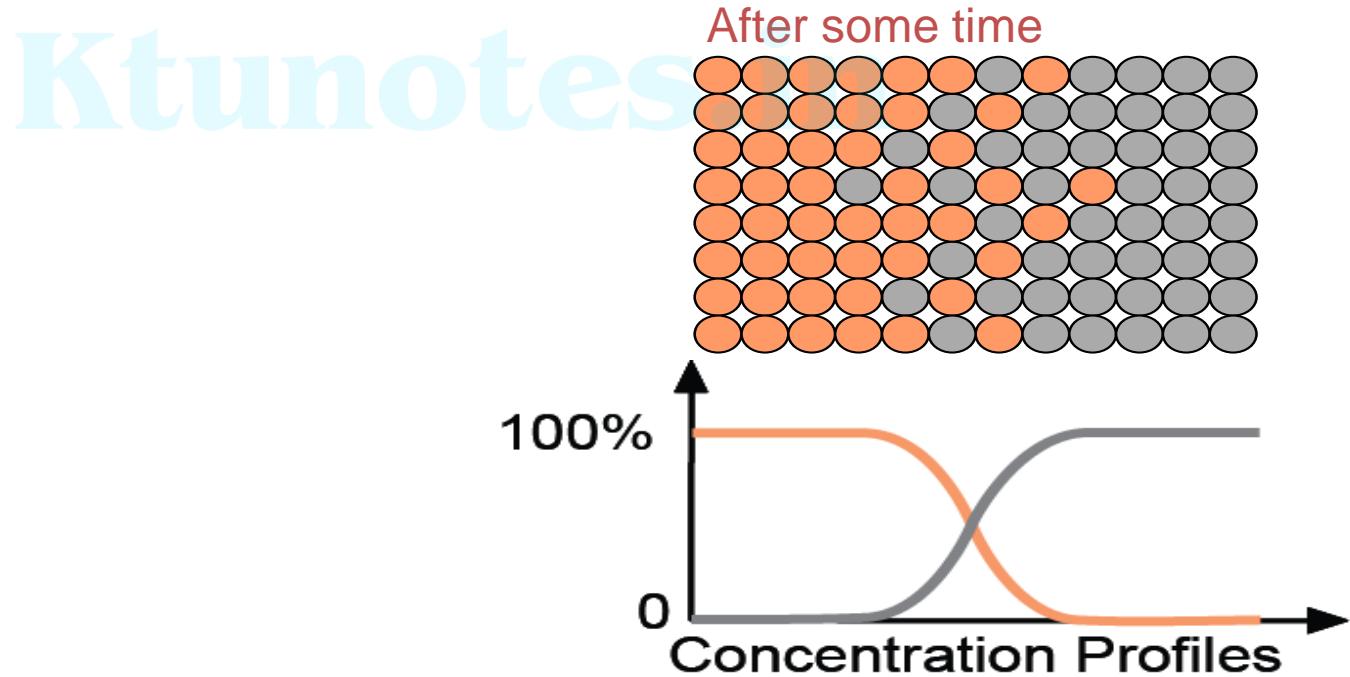
Microscopic Point of View :

- Considers the motion of dopant at atomic scale
 - Computationally expensive and used in simulation tools
 - More accurate
- Macroscopic Point of View :
 - Considers overall motion of dopant profile
 - Fick's Laws
- Considering the macroscopic point of view is important
- because it gives a sufficiently accurate first hand picture

Interdiffusion

- **Interdiffusion (impurity diffusion):** In an alloy, atoms tend to migrate from regions of high concentration to regions of low concentration.

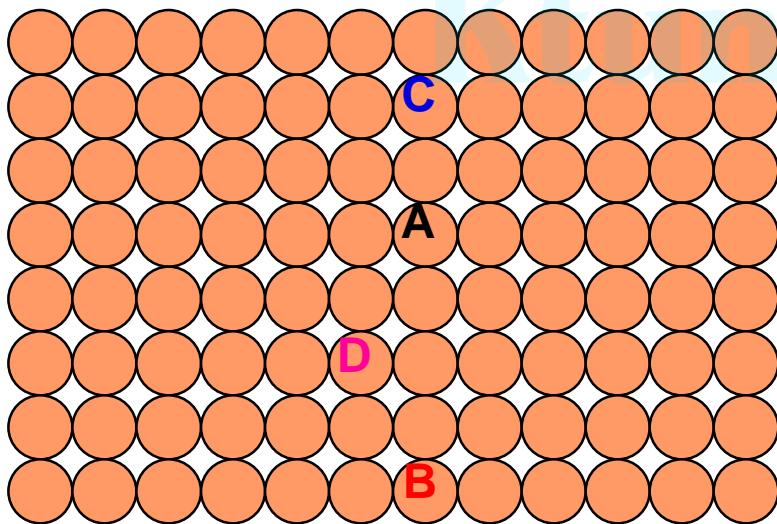
Initially



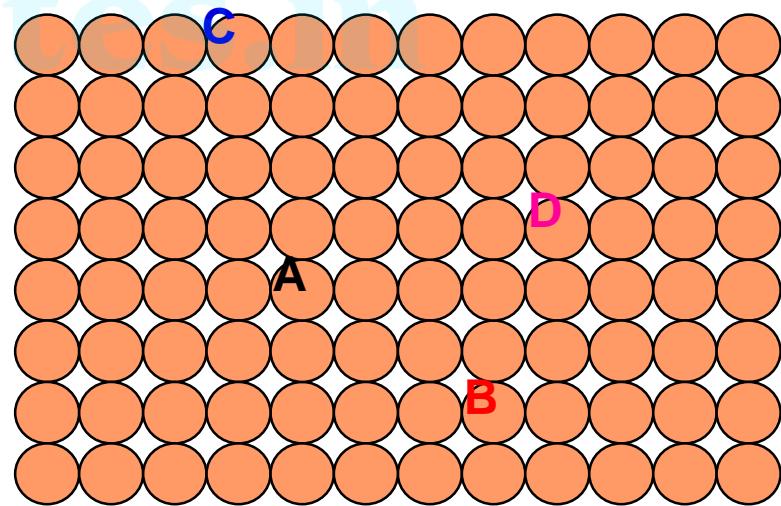
Self-Diffusion

- Self-diffusion: In an elemental solid, atoms also migrate.

specific atom movement



After some time



Diffusion Mechanisms

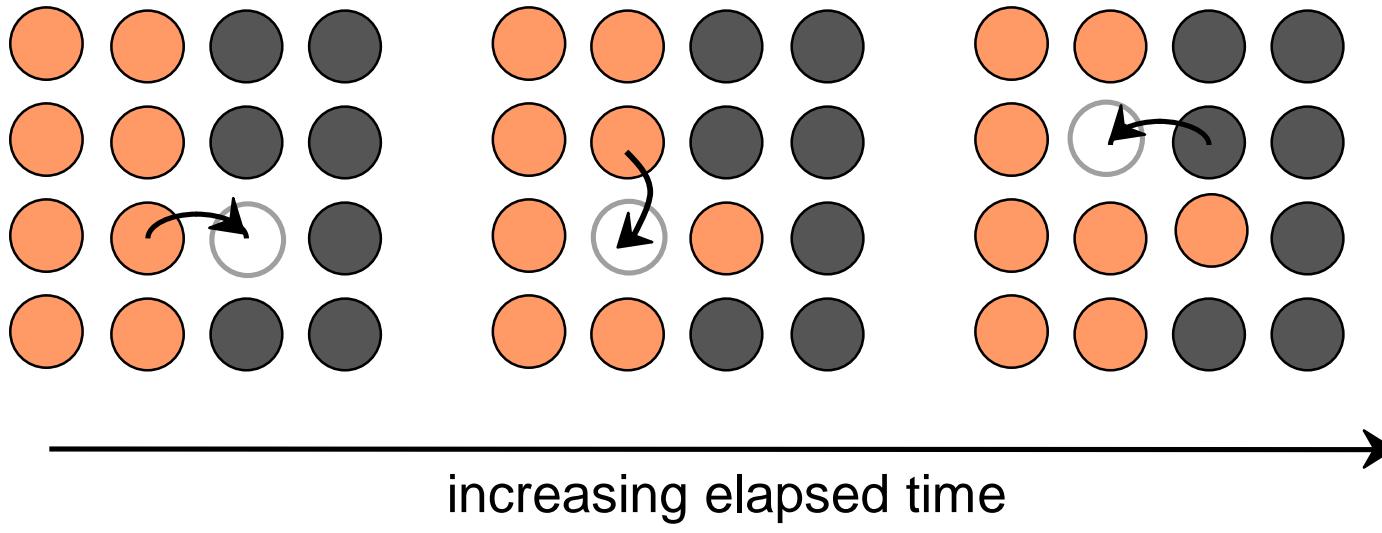
- Atoms in solid materials are in constant motion, rapidly changing positions.
- For an atom to move, 2 conditions must be met:
 1. There must be an **empty adjacent site**, and
 2. The atom must have **sufficient** (vibrational) **energy** to break bonds with its neighboring atoms and then cause lattice distortion during the displacement.
- There are 2 dominant models for metallic diffusion(Microscopic Point of View):
 1. **Vacancy Diffusion**
 2. **Interstitial Diffusion**

Vacancy Diffusion

Vacancy Diffusion:

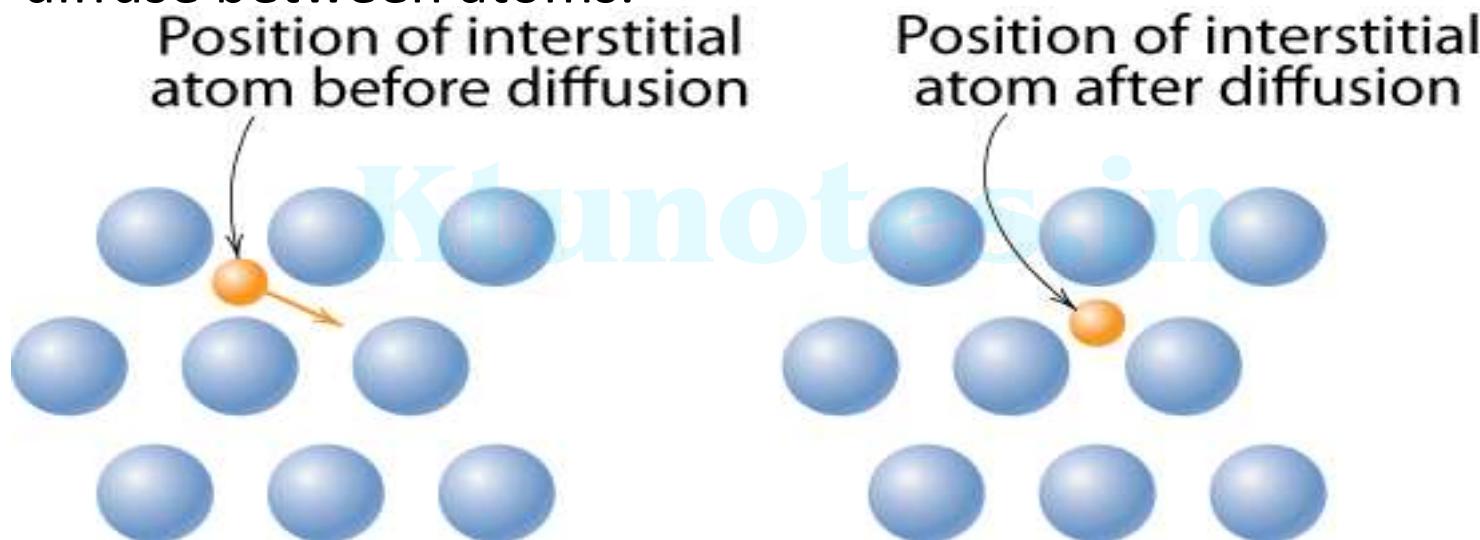
- atoms exchange with vacancies
- applies to substitutional impurity atoms
- rate depends on:
 - number of vacancies
 - activation energy to exchange.

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Interstitial Diffusion

- **Interstitial diffusion** – smaller atoms (H, C, O, N) can diffuse between atoms.



Fick's Laws of Diffusion

- Fick's First Law

Flux of dopants is proportional to concentration gradient

$$J = -D \frac{\partial C(x,t)}{\partial x}$$

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- where J is the particle flux, C is the concentration of the solute, D is the diffusion coefficient, x is the distance into the substrate, and t is the diffusion time.
- The negative sign indicates that the diffusing mass flows in the direction of decreasing concentration.
- Here flux is the no. of dopant atoms passing through a unit area in a unit time

- Fick's Second Law
- Rate of change of concentration is proportional to change of concentration gradient with depth

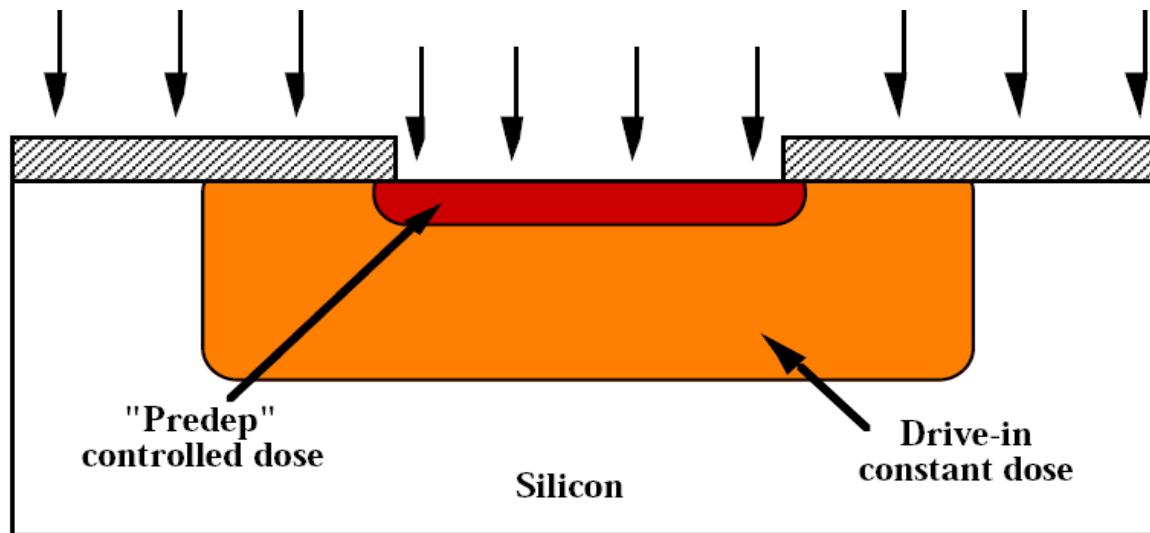
$$\frac{\partial C}{\partial t} = \mathbf{D} \frac{\partial^2 C}{\partial x^2}$$

(Or)

in other words the rate of decrease of concentration at a point is equal to the net number of particles moving away from that point

Creating Doped regions

- **Step1 : Pre-deposition**
Controllably introduce desired dopant atoms
- **Step2 : Drive-in**
The introduced dopants are driven deeper into the wafer without further introduction of dopant atoms



- Solution to 2nd law gives concentration as a function of depth and time; solution depends on boundary conditions
- Case-1 *Infinite-source diffusion (pre-deposition)*
- Infinite-source diffusion requires a constant surface concentration of diffusing atoms
- $C(x, 0) = 0$
- $C(0, t) = C_s$
- $C(\infty, t) = 0$
- C_s is the surface concentration

- The solution to Fick's Law under these conditions is:
$$C(x,t) = C_s \operatorname{erfc} \left(\frac{x}{2\sqrt{Dt}} \right)$$
- \sqrt{Dt} is a common feature in the solution of diffusion problems and is known as the **characteristic diffusion length**
- The dose of predeposition diffusion varies with time of diffusion .To obtain the dose, the profile can be integrated

VLSI Ci
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$$Q = \int_0^{\infty} C(x, t) dt = 2C_s \sqrt{\frac{Dt}{\pi}}$$

Case-2 Limited-source diffusion (drive-in))

- In this case an initial amount of impurity QT introduced into the wafer and diffused subject to the boundary condition that QT is fixed
- constant amount of total dopant per unit area of the diffusing surface
- $C(x, 0) = 0; x \neq 0$
- $C(\infty, t) = 0$
- $\int_0^{\infty} C(x, t) dx = Q$
- The solution to Fick's second law for these condition is

$$C(x, t) = \frac{QT}{\sqrt{\pi Dt}} \exp\left[-\frac{x^2}{4Dt}\right]$$

- Surface concentration Cs, decreases with time as

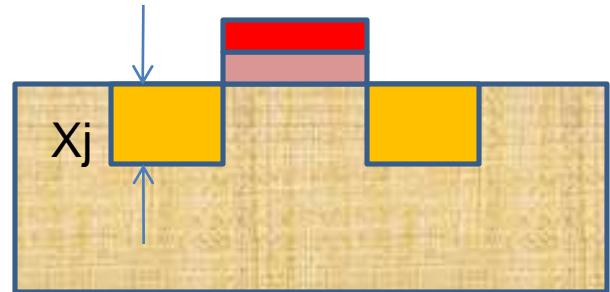
$$C_s = C(0, t) = \frac{Q_T}{\sqrt{\pi Dt}}$$

Junction Depth(X_j)

- Assume B diffusing in Si wafer that has uniform concentration of phosphorous. Assume $C_s \gg C_B$
- When concentration of impurity is equal to background doping concentration, that depth is called as junction depth (since B is a p-type dopant and phosphorus is an n-type dopant, a p-n junction exist at this depth)

$$C_a x_j = 2 \cdot \sqrt{Dt} \cdot erfc^{-1} \left(\frac{C_B}{C_s} \right)^{\frac{1}{n}}$$

$$C_a x_j = \sqrt{4 \cdot Dt \cdot \ln \left(\frac{Q_T}{C_B \sqrt{\pi Dt}} \right)}$$



Diffusion and Temperature

- Diffusion coefficient increases with increasing T.

$$D = D_o \exp\left(-\frac{Q_d}{RT}\right)$$

D = diffusion coefficient [m²/s]

D_o = pre-exponential [m²/s]

Q_d = activation energy [J/mol or eV/atom]

R = gas constant [8.314 J/mol-K]

T = absolute temperature [K]

Activation energy - energy required to produce the movement of 1 mole of atoms by diffusion.

Factors that influence diffusion

Table 6.2 A Tabulation of Diffusion Data

Diffusing Species	Host Metal	$D_0(m^2/s)$	Activation Energy Q_d		Calculated Values	
			kJ/mol	eV/atom	T(°C)	$D(m^2/s)$
Fe	α -Fe (BCC)	2.8×10^{-4}	251	2.60	500	3.0×10^{-21}
					900	1.8×10^{-15}
Fe	γ -Fe (FCC)	5.0×10^{-5}	284	2.94	900	1.1×10^{-17}
					1100	7.8×10^{-16}
C	α -Fe	6.2×10^{-7}	80	0.83	500	2.4×10^{-12}
					900	1.7×10^{-10}
C	γ -Fe	2.3×10^{-5}	148	1.53	900	5.9×10^{-12}
					1100	5.3×10^{-11}
Cu	Cu	7.8×10^{-5}	211	2.19	500	4.2×10^{-19}
Zn	Cu	2.4×10^{-5}	189	1.96	500	4.0×10^{-18}
Al	Al	2.3×10^{-4}	144	1.49	500	4.2×10^{-14}
Cu	Al	6.5×10^{-5}	136	1.41	500	4.1×10^{-14}
Mg	Al	1.2×10^{-4}	131	1.35	500	1.9×10^{-13}
Cu	Ni	2.7×10^{-5}	256	2.65	500	1.3×10^{-22}

Source: E. A. Brandes and G. B. Brook (Editors), *Smithells Metals Reference Book*, 7th edition, Butterworth-Heinemann, Oxford, 1992.

- The **diffusing species, host material and temperature** influence the diffusion coefficient.
- For example, there is a significant difference in magnitude between **self-diffusion** and carbon **interdiffusion** in α iron at 500 °C.

Comparison of Diffusion and Ion implantation

- **Diffusion**

Advantages:

- ❑ No damage created
- ❑ Batch fabrication possible

Disadvantages:

- ❑ Limited to solid solubility
- ❑ High temperature process
- ❑ Shallow junctions difficult

- **Ion Implantation**

Advantages:

- ❑ Low temperature process
- ❑ Precise dose and junction depth Control
- ❑ Implantations through thin layers of oxide/nitride possible
- ❑ Short process times

Disadvantages:

- ❑ Implant damage enhances diffusion
- ❑ Additional cost of annealing
- ❑ Dislocations may cause junction leakage
- ❑ Channeling

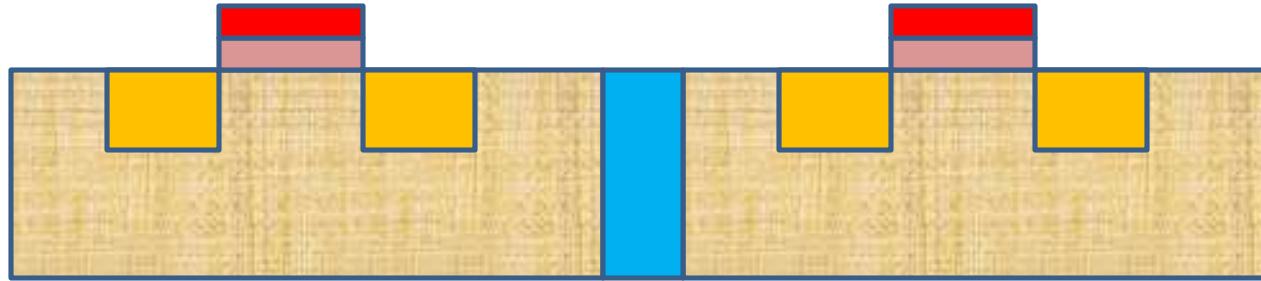
Steps of Silicon Device Manufacturing

- Oxidation
- Photolithography
- Etching
- Ion Implantation
- Diffusion
- Deposition

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Deposition

- It is the opposite process of etching
- Thick oxides used for isolation between metal interconnects,
- Polysilicon for gate contacts

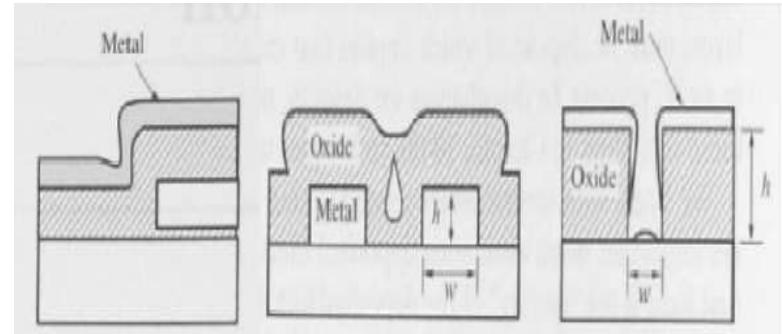


Deposition Characteristics

- Step coverage: ability to uniformly cover all parts of a step (or trench) on wafer
- Thickness of horizontal surface should be same as the thickness of the vertical surface

(Depends on Aspect ratio)

Aspect ratio = H/W



- Deposition Rate: Thickness deposited per unit time
- Depends on deposition method, Temp, material deposited.
- Throughput: number of wafers processed per hour
- Single wafer or multiple wafer system
- Depends on deposition technique and cost of equipment

Deposition Methods

- Physical
 - Evaporation
 - Physical Vapor Deposition(PVD)
- Chemical
 - Chemical Vapor Deposition(CVD)
 - Metal Organic CVD(MOCVD)
 - Atomic Layer Deposition
- Epitaxial
 - Molecular Beam Epitaxy
 - Liquid and Vapor phase Epitaxy

Epitaxy

- Greek word
 - Epi=>'above'
 - Taxi=>' in ordered manner'
- Two types
 - Homoepitaxy
 - In homoe epitaxy, a crystalline film is grown on a substrate or film of the same material
 - This technology is used to grow a film which is more pure than the substrate and to fabricate layers having different doping levels
 - Hetero epitaxy
 - In heteroepitaxy, a crystalline film grows on a crystalline substrate or film of a different material
- Parameters
 - ✓ Temperature
 - ✓ Pressure

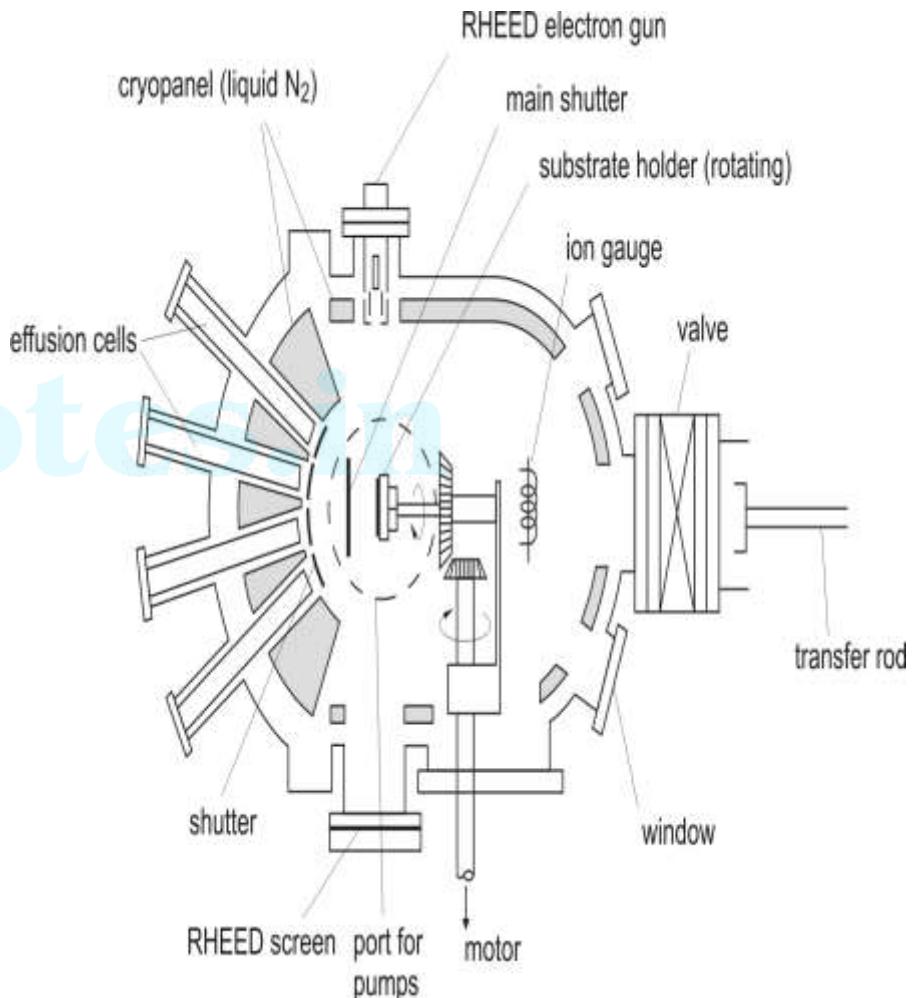
Molecular Beam Epitaxy (MBE)

- To deposit single crystal thin films
- Very/Ultra high vacuum (10^{-10} torr)
- Important aspect: slow deposition rate (1 micron/hour)
- Slow deposition rates require proportionally better vacuum.
- Reactants are introduced by molecular beams.
- The beams are created by heating a source of material in an effusion (or Knudsen) cell.
- Several sources & several beams of different materials are aimed at the substrate

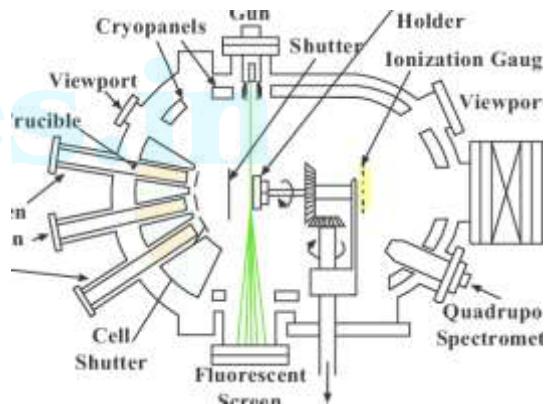
Molecular Beam Epitaxy: Process

- Ultra-pure elements are heated in separate quasi-knudson effusion cells (e.g., Ga and As) until they begin to slowly sublime
- Gaseous elements then condense on the wafer, where they may react with each other (e.g., GaAs).
- The term “beam” means the evaporated atoms do not interact with each other or with other vacuum chamber gases until they reach the wafer.

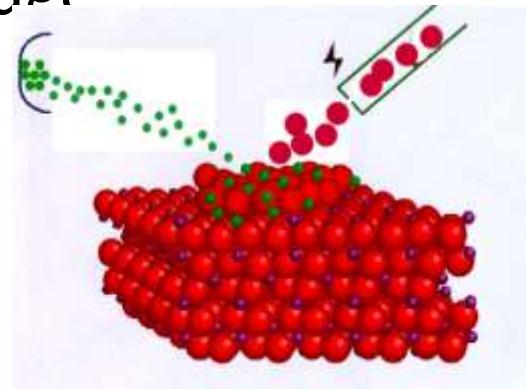
- Here separate effusion ovens made of pyrolytic are used or Ga, As and the dopants
- All effusion ovens are housed in an ultra high vacuum chamber.
- Each oven kept at a temperature that gives the required evaporation rate
- The substrate holder rotate continually to achieve uniform epitaxial layer.



- Sample exchange load lock at the extreme right permits the maintenance of ultrahigh vacuum while changing the substrate
- An over pressure of As is maintained to grow GaAs
- In case of si MBE system, an electron gun is used to evaporate si
- One or more effusion ovens are used for the dopants



- The substrate is located with a line-of-sight to the oven aperture
- Atoms on a clean surface are free to move until finding correct position in the crystal lattice to bond.
- Growth occurs at the step edges formed: More binding forces at an edge



- RHEED (Reflection High Energy Electron Diffraction) is used to monitor the growth of the crystal layers.

- Computer controlled shutters of each furnace allows precise control of the thickness of each layer, down to a single layer of atoms.
- Systems requiring substrates to be cooled: Cryopumps and Cryopanels are used using liquid nitrogen.

Benefits and Drawbacks of MBE

Advantages	Disadvantages
■ Clean surfaces, free of an oxide layer	■ Expensive (10^6 \$ per MBE chamber)
■ <i>In-situ</i> deposition of metal seeds, semiconductor materials, and dopants	■ ATG instability
■ Low growth rate (1 μ m/h)	■ Very complicated system
■ Precisely controllable thermal evaporation	■ Epitaxial growth under ultra-high vacuum conditions
■ Separate evaporation of each component	
■ Substrate temperature is not high	
■ Ultrasharp profiles	

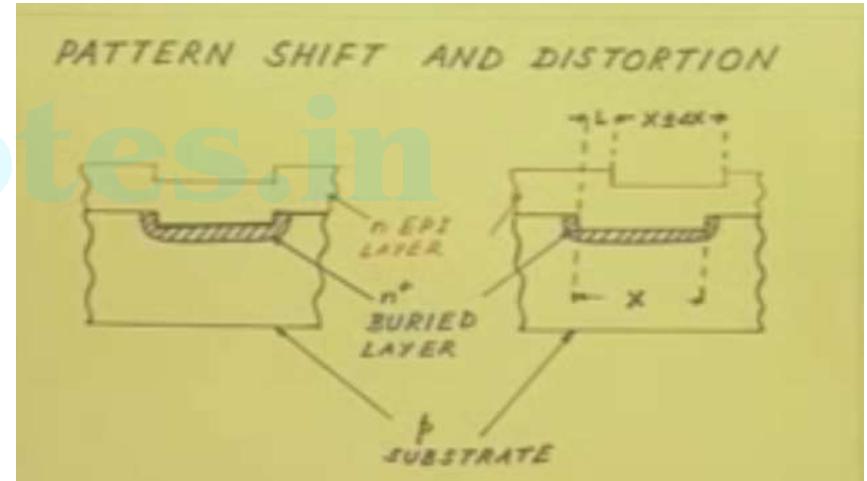
Conclusions

- Typically in ultra-high vacuum
- Deposition rates are very low (1 monolayer/second)
- Very well controlled (Shuttering: 0.1s)
- Grow films with good crystal structure
- Often use multiple sources to grow alloy films
- Deposition rate is so low that substrate temperature doesn't need to be as high
- Expensive
- Sophisticated system

Defects in Epitaxial Growth

1).PATTERN SHIFT AND PATTERN DISTORTION

- When there is a step in the surface that will transfer in to the epitaxial layer
- Once the epitaxial layer formed it step will where the underlying buried layer is
- Actual case step is not aligned but get shifted.
- Length of buried layer not match with length of step.
- Pattern on the substrate may get shifted by an amount L and also it get distorted by an amount $+\Delta x$



Reason

- Crystal growth depends on crystal orientation
- Whenever there is a step on the surface we are exposing no of crystal plane
- When epitaxial growth taking place anisotropically , we will not get uniform growth rate

How to minimize this?

Pattern shift is minimized by

- high deposition temperature
- Operate at low growth rate region
- Low Cl concentration
- Low pressure
- $<100>$ sample perfectly oriented, $<111>$ samples it is misoriented to minimize pattern shift
- Masking layer can use

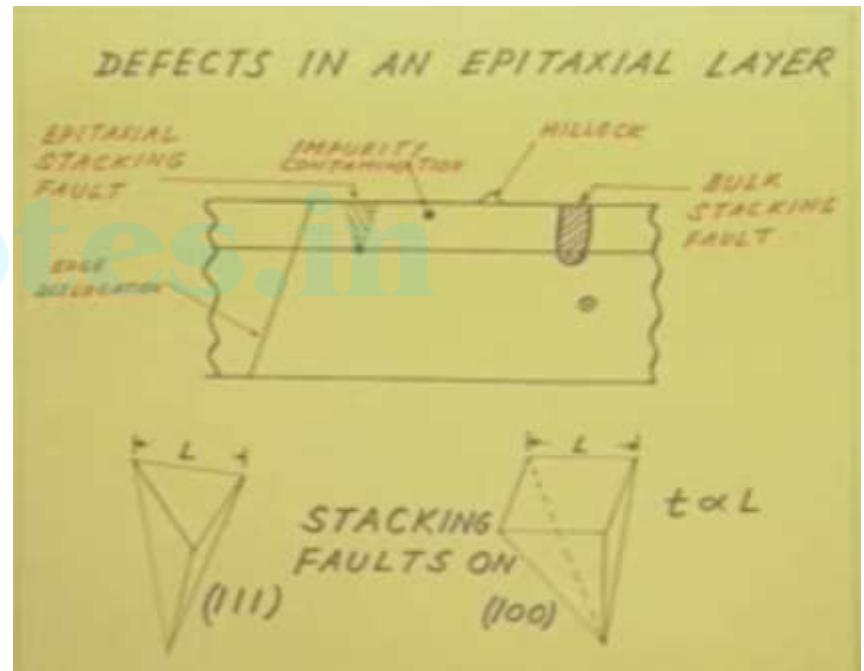
2). Due to the effect of crystal defects

- Quality of epitaxial layer depends on quality of bulk layer
- Bulk crystal defects transformed in to epitaxial layer

a). **edge dislocation**:-Line represents edge dislocation(extra plane inserted viewed in 2D as extra line)will transformed in to epitaxial layer

b) **Impurity contamination**:-

- Due to impurity present in the gas stream or reactor chamber which is incorporated in to the epitaxial layer

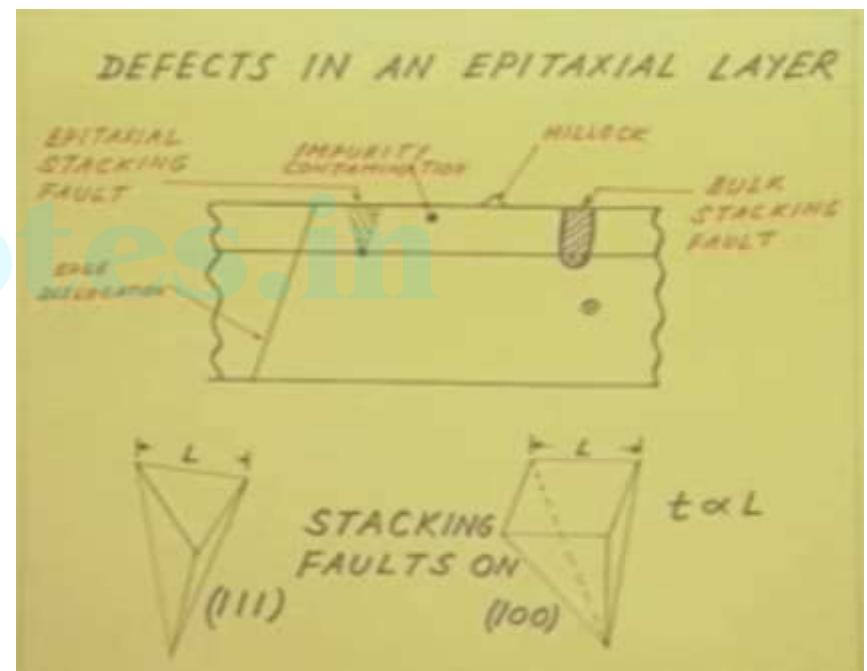


c) **Hillock:** growth may not uniform

d). **Stacking faults:-**

- small patch of native oxide on the surface .Stacking faults originate from there.
- As epitaxial layer grown stacking faults also will grow
- If the sample surface is (111) the we can get triangular pit
- If the sample surface is (100) we can get rectangular pit.

e) **Bulk stacking fault**



Metal-semiconductor contacts

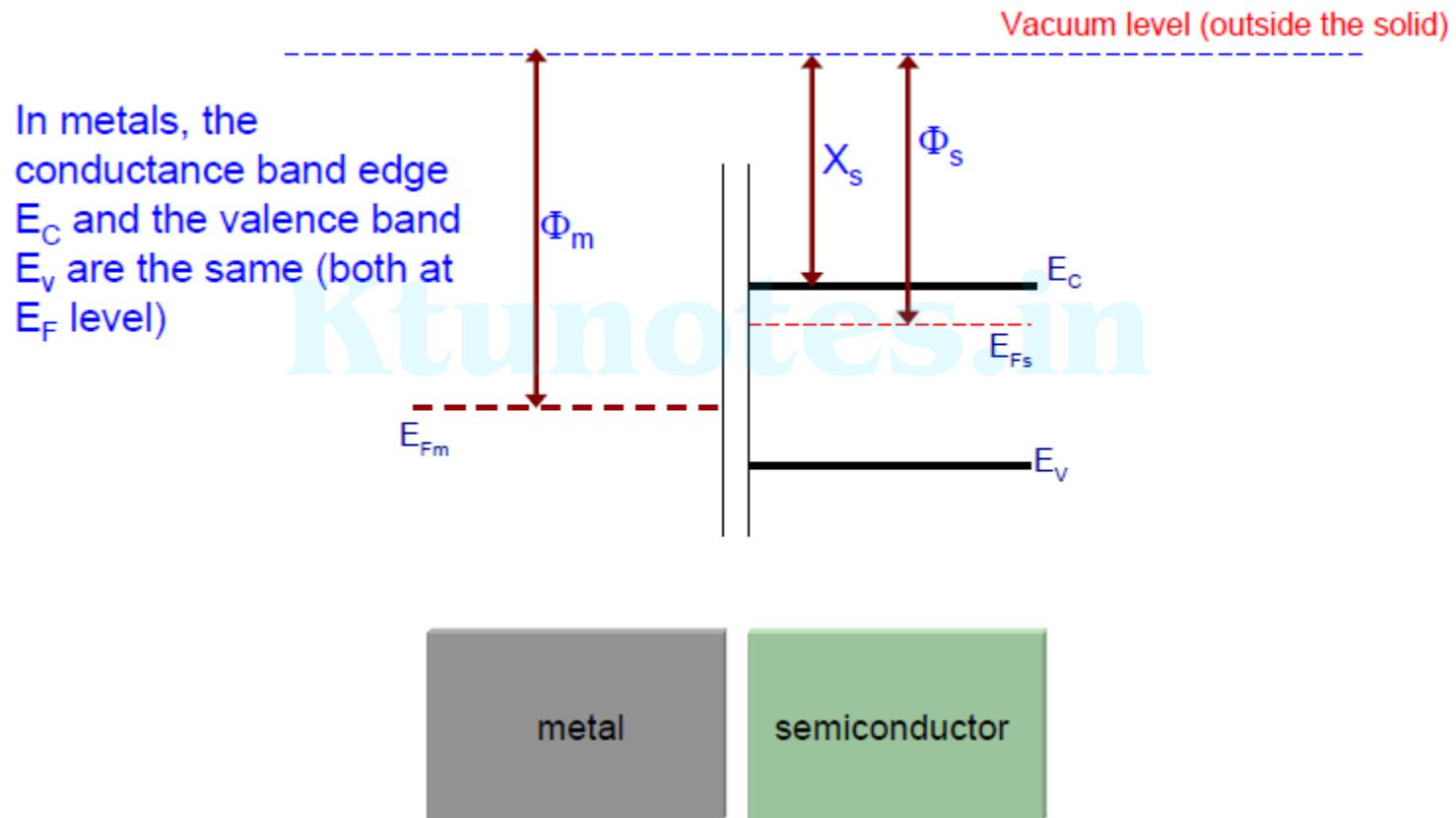
Two types 1).schottky contact 2).ohmic contact

- Generally four types of metal semi conductor contact
 - 1)contact between metal-n type semiconductor, $\Phi_m > \Phi_s$
 - 2) contact between metal-p type semiconductor, $\Phi_m < \Phi_s$
 - 3)contact between metal-n type semiconductor, $\Phi_m < \Phi_s$
 - 4) contact between metal-p type semiconductor, $\Phi_m > \Phi_s$
- 1 & 2 called rectifying contact or schottky contact
- 3&4 called ohmic contact

Schottky diode :

Schottky diode consists of a metal – semiconductor junction. There is no p-n junction in Schottky diode

Metal – n-type semiconductor before contact



- The parameter ϕ_m is the metal work function (measured in volts),
- ϕ_s is the semiconductor work function, X is known as the electron affinity.
- In order for the Fermi level to become a constant through the system in thermal equilibrium, electrons from the semiconductor flow into the lower energy states in the metal

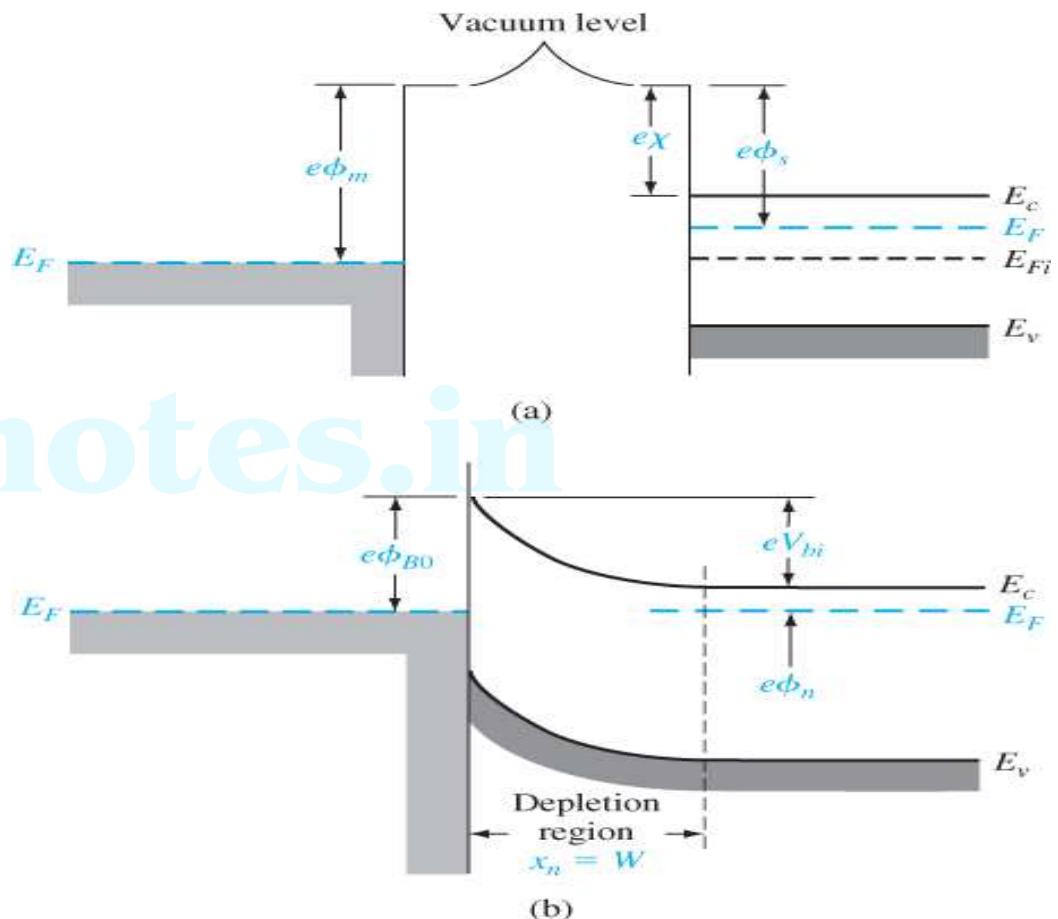
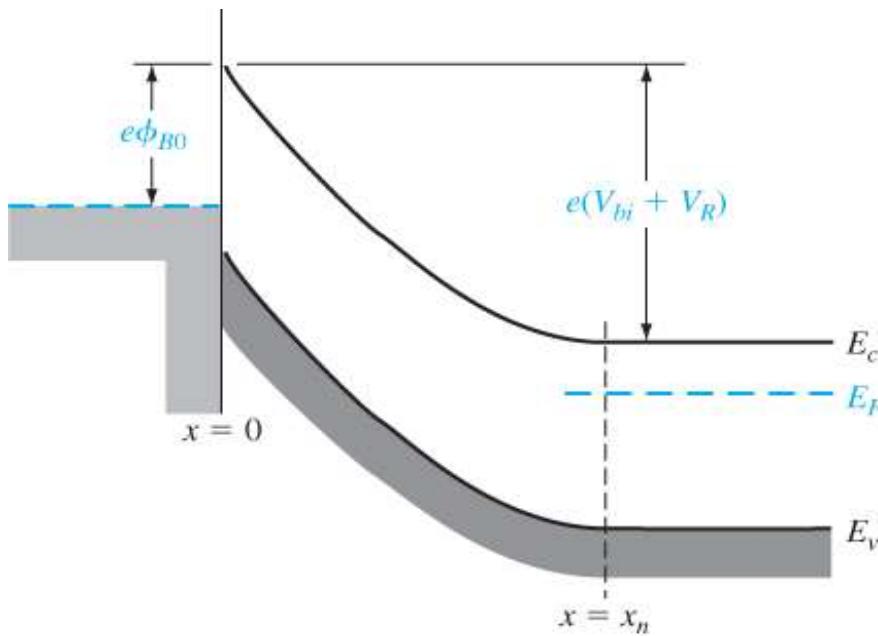
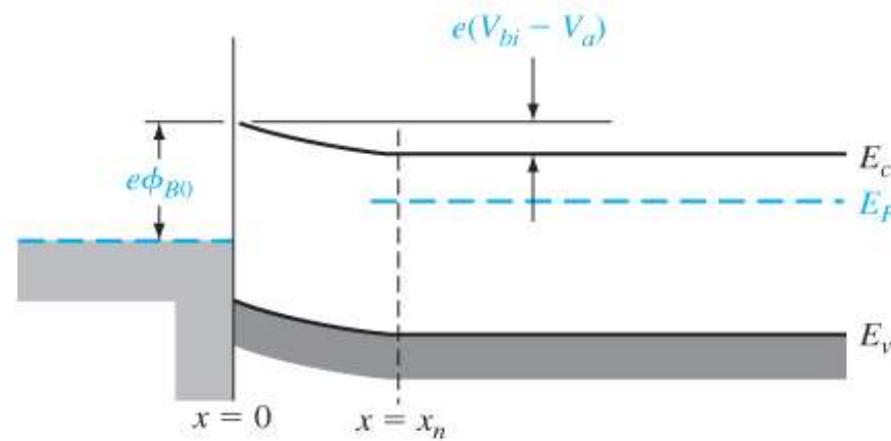


Figure 9.1 | (a) Energy-band diagram of a metal and semiconductor before contact; (b) ideal energy-band diagram of a metal-n-semiconductor junction for $\phi_m > \phi_s$.



(a)



(b)

Figure 9.2 | Ideal energy-band diagram of a metal–semiconductor junction (a) under reverse bias and (b) under forward bias.

This barrier is known as the *Schottky barrier* and is given, ideally, by

$$\phi_{B0} = (\phi_m - \chi) \quad (9.1)$$

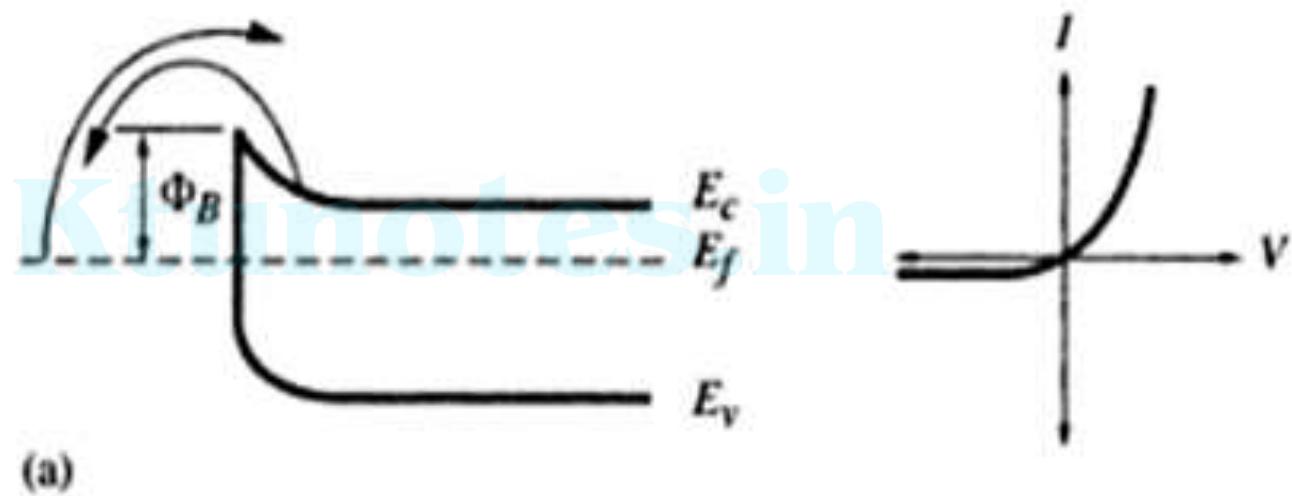
trying to move into the metal. The built-in potential barrier is given by

$$V_{bi} = \phi_{B0} - \phi_n \quad (9.2)$$

V_R is the magnitude of the reverse-biased voltage and V_a is the magnitude of the forward-biased voltage

After Contact (with n-type material):

Vacuum level (outside the solid)



(a)

Schottky
barrier for
electrons



Ohmic contact

- Contacts must be made between any semiconductor device, or integrated circuit, and the outside world. These contacts are made via ohmic contacts.

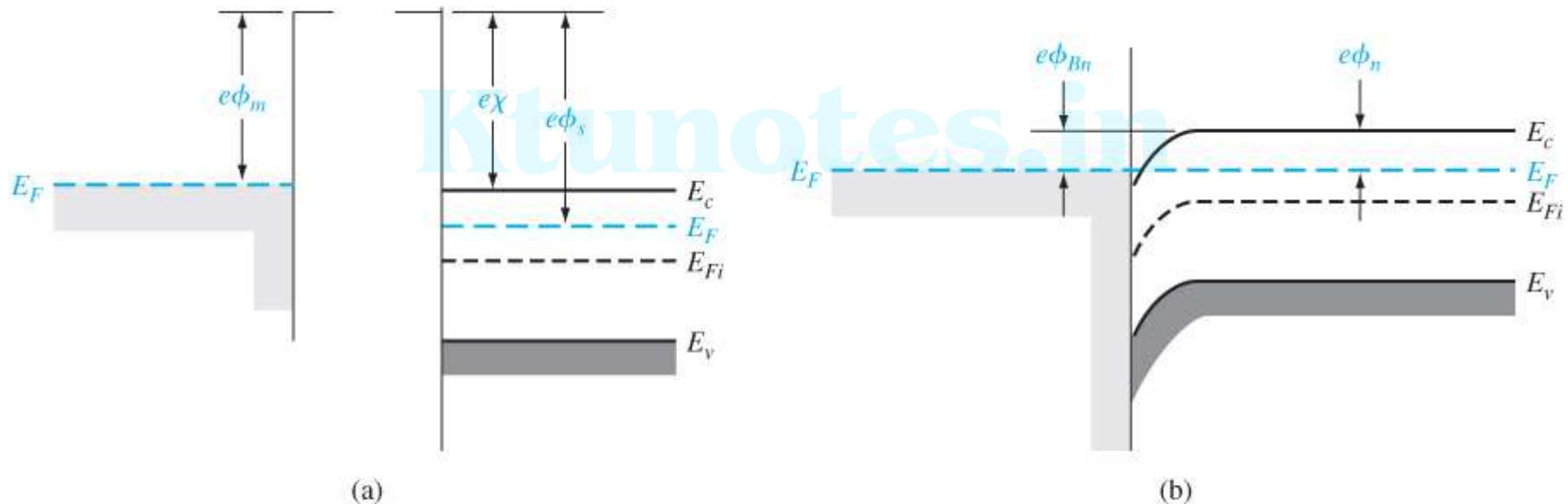


Figure 9.11 | Ideal energy-band diagram (a) before contact and (b) after contact for a metal-n-type semiconductor junction for $\phi_m < \phi_s$.

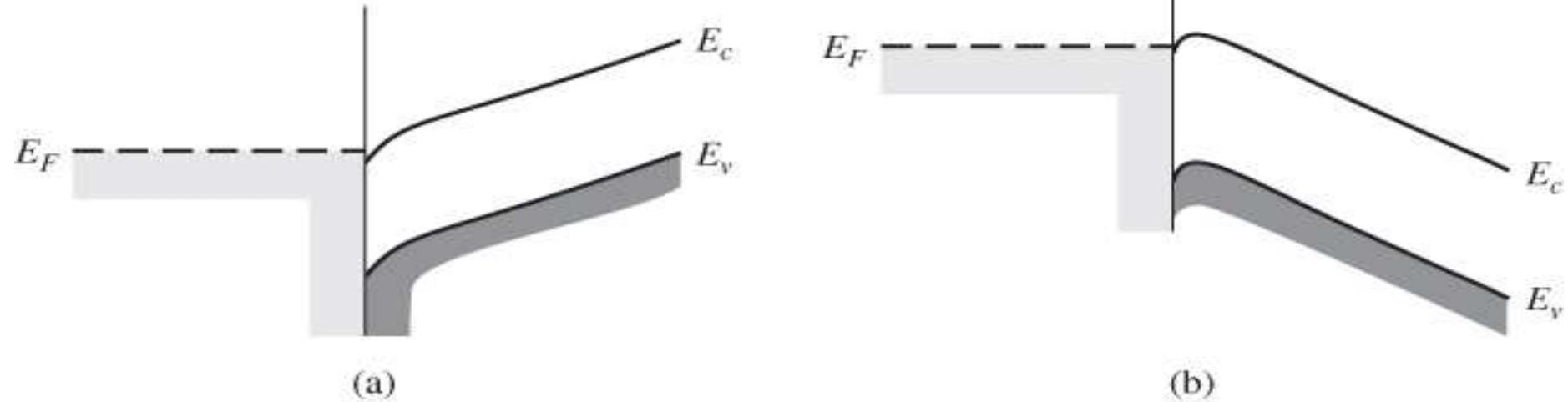
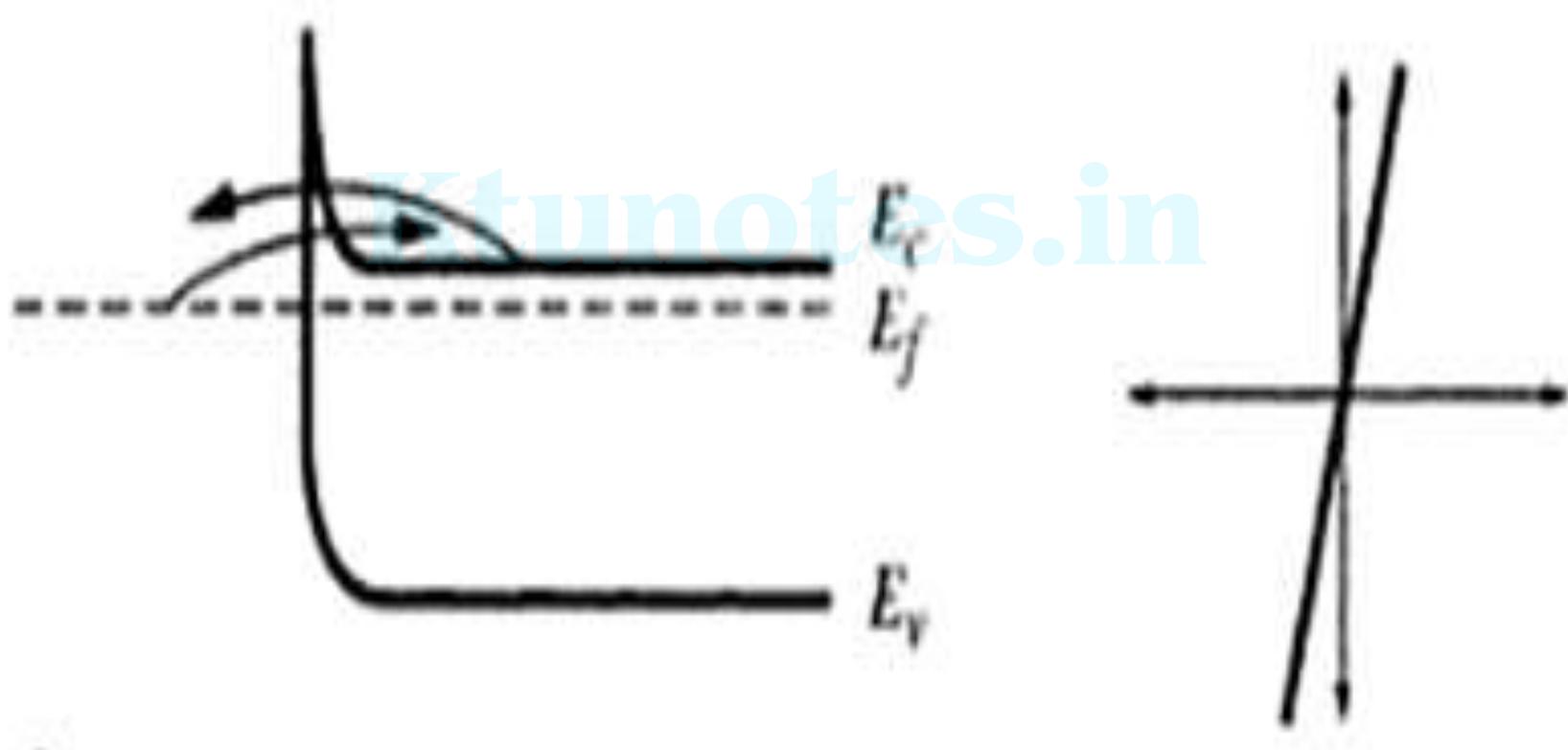


Figure 9.12 | Ideal energy-band diagram of a metal-n-type semiconductor ohmic contact (a) with a positive voltage applied to the metal and (b) with a positive voltage applied to the semiconductor.

- If a positive voltage is applied to the **metal**, there is no barrier to electrons flowing from the semiconductor into the metal.
- If a positive voltage is applied to the **semiconductor**, the effective barrier height for electrons flowing from the metal into the semiconductor will be approximately $\phi_{Bn} = \phi_n$

Ohmic contact



Metallization

- Important step in VLSI technology
- Metal contact is connection of IC to outside world
- Depending on the purpose of the contact ,metallization scheme in to two parts
1). ohmic contact metallization 2).gates and interconnect metallization

1). ohmic contact metallization

if we want ohmic contact it must have

low contact ~~resistant~~

$$R_c = \frac{V}{\partial J} \quad \text{where } V=\text{applied voltage}$$

$V > 0$ $J = \text{current density}$

- When we put a metal on a semiconductor we get a Schottky barrier
- in schottky movement of carrier cross over the barrier

- In schottky if the current is due to thermionic emission ,the current density is given by

$$J_s = A^* T^2 \exp\left(-\frac{q\Phi_B}{kT}\right) \left(\exp\left(\frac{qV}{kT}\right) - 1\right)$$

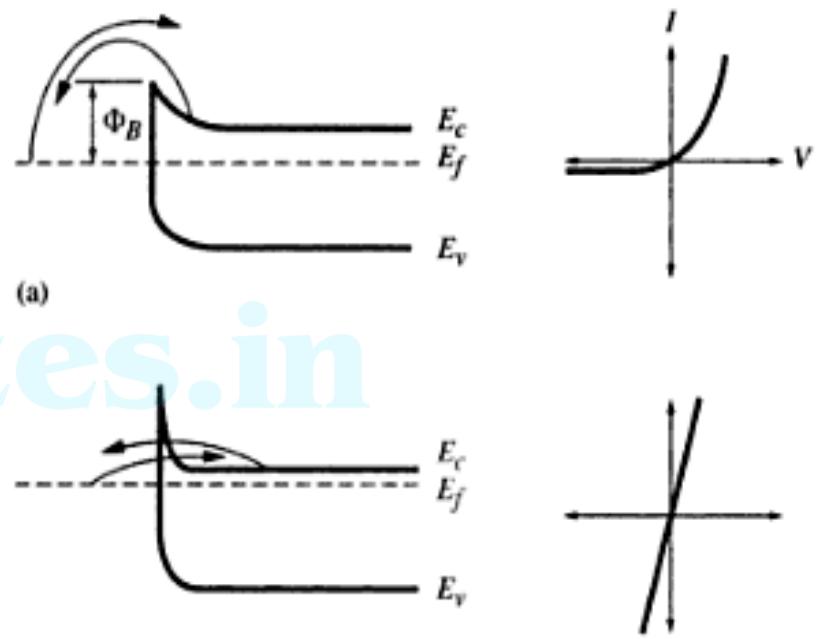
A* is Richardson's constant

- The specific contact resistance is given by

$$R_c = \frac{k}{qA^*T} \exp\left(\frac{q\Phi_B}{kT}\right)$$

ie.if bigger the barrier, bigger the contact resistance

- This is for moderately doped semiconductor



Band diagram and I-V characteristics for metal/semiconductor junction or contact for schottky contact ,illustrating different mode of current transfer a).Schottky or rectifying contact b).tunneling or ohmic contact

- For heavily doped semiconductor, we can get a narrow barrier and movement of carrier through barrier by tunneling through barrier
- Here current is given by tunneling parameter this also depend on contact resistance

$$R_c \propto \exp \frac{\phi_b}{E_{\text{gap}}}$$

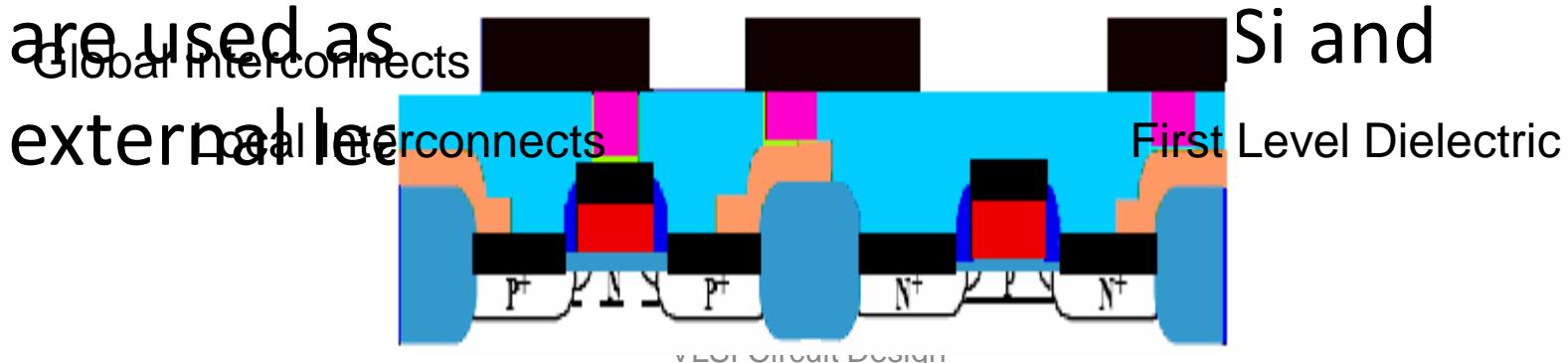
Eoo –tunneling parameter
application of semiconductor

- $N \geq 10^{19}/\text{cm}^3$ ->tunneling
- $N \leq 10^{19}/\text{cm}^3$ ->thermionic , where N is the doping concentration
- If we have a heavily doped region ohmic contact is not a problem.
- If for moderately doped region R_c depends on barrier .that is why it is difficult form ohmic contact to moderately doped n region

How do I form metal contact?

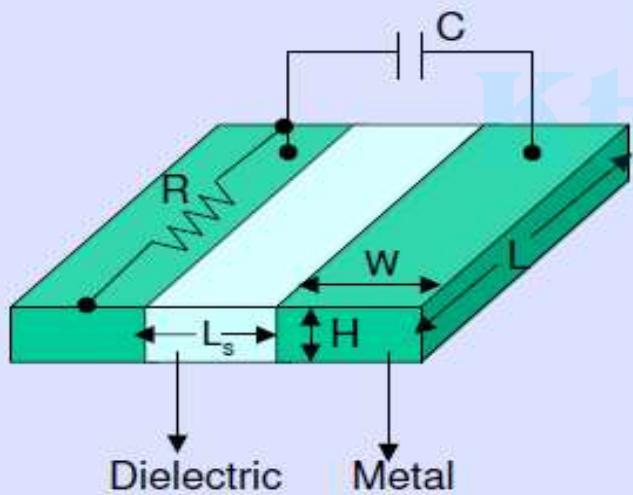
- Primarily metal deposited by physical vapor deposition,no chemical reaction
 - a).evaporation technique
 - b).sputtering technique

- Metallization is the process that makes accessible the IC to the outside world through conducting pads.
- Doped silicon conduct electricity but have large resistance and lack interconnecting facility
- Thin conductive metal films (Al, Cu, Au, Ag etc) are used as external interconnects



Why interconnect structures are important?

Rough Estimation of Interconnect RC Time Delay



Global Interconnect

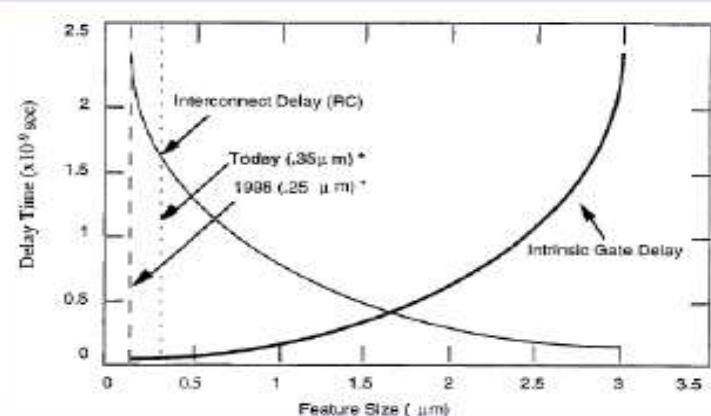
$$R = \rho \frac{L}{WH}$$

$$C = \epsilon \frac{HL}{L_s}$$

$$RC = \epsilon \rho \frac{L^2}{WL_s}$$

As technology progresses, L_s decreases \rightarrow RC delay increases
To decrease RC delay - ρ , ϵ , L should take low values

Fig: Interconnection delay and device delay



Needs of new technology

- Lower resistivity metal for interconnect wiring
- Lower dielectric constant material for the interlayer dielectric
- Smaller wire lengths-**Multilevel Metallization**

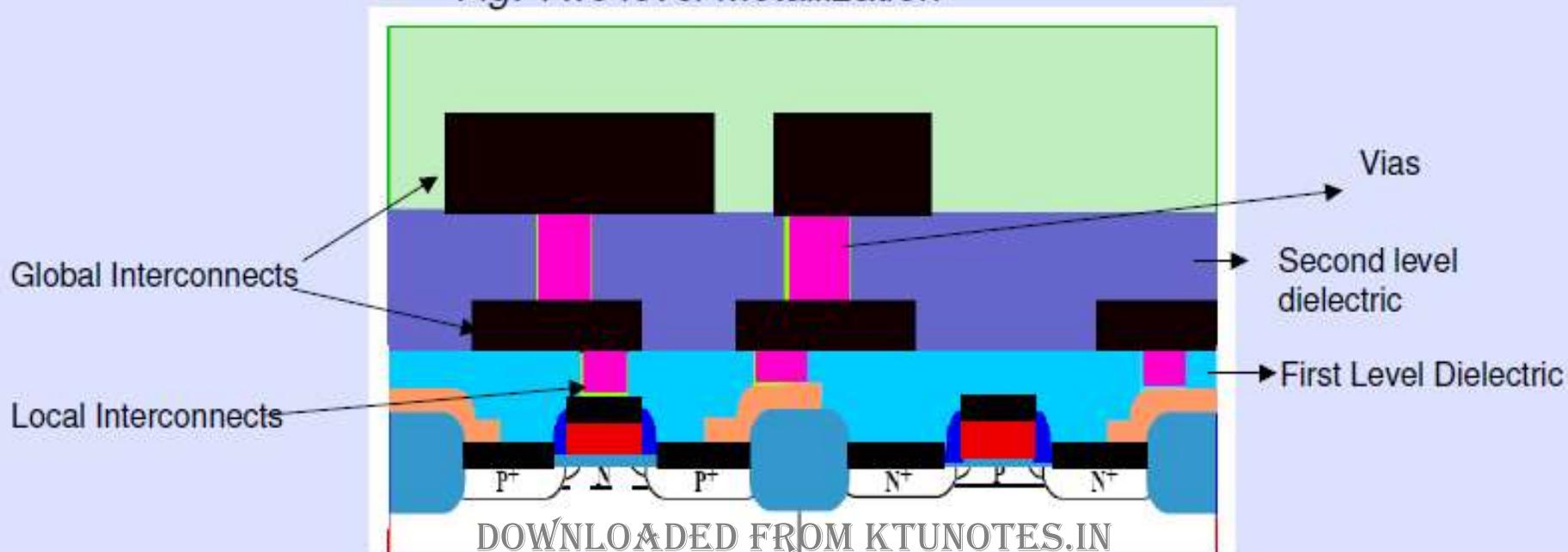
Multi level metallization

Three dimensional network of interconnections is given the name multilevel interconnections

Metal interconnections

- span several planes
- isolated by the insulating dielectric layers
- interconnected by the wiring in the third dimension through the holes in the dielectric planes

Fig: Two level Metallization



Uses -Multi level metallization

- Reduced interconnection lengths-enhanced performance due to reduced RC
- Densification-higher package densities
- Design flexibility

Interconnection materials

- Metals

Metal Issues

- Junction spiking
- Electromigration
- Stress migration

Important metals

- Aluminum
- Copper
- Tungsten
- Silver, Gold
- Dielectrics

- Diffusion barriers and Adhesion promoters

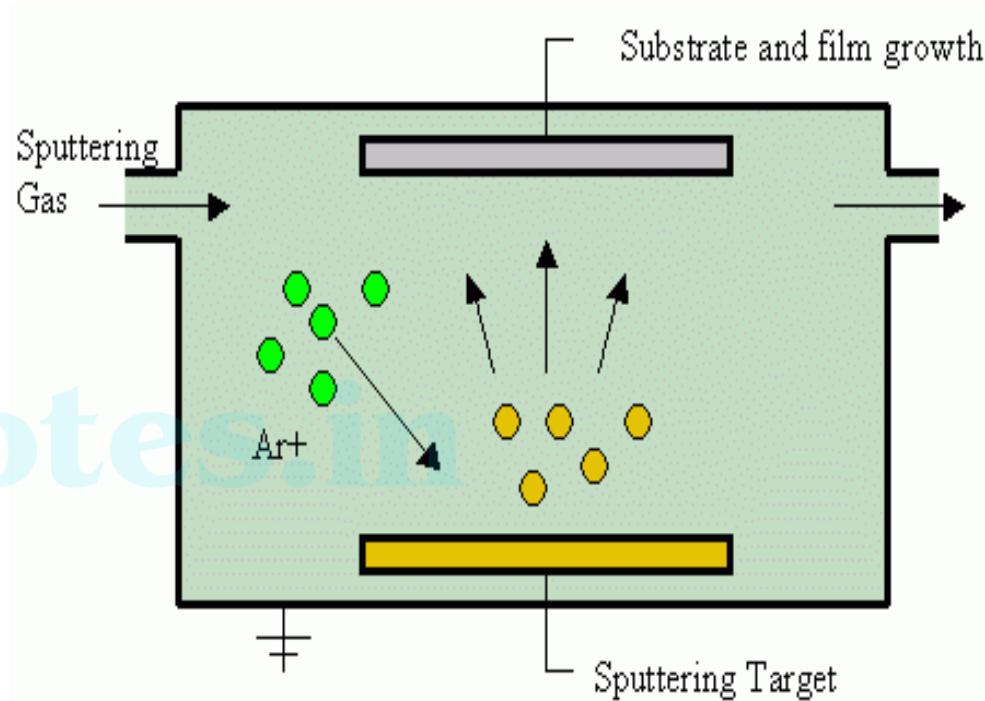
Multilevel Metallization Processing

- Metal deposition
 - PVD
 - Evaporation
 - Resistance heated Evaporation
 - Inductively heated evaporation
 - Electron beam Evaporation
 - Sputtering
 - DC, RF sputtering
 - Magnetron sputtering
 - CVD
 - Electroplating
 - Via and trench formation
 - Chemical mechanical Planarization

Physical Deposition Processes

- Sputtering
 - In the sputtering process, a target material of the species that is desired for deposition is negatively charged and placed in a low pressure environment.
 - Argon or another noble gas is injected into the low pressure chamber and, through use of RF energy or high voltage DC, a plasma is created in the chamber by free electrons striking the argon atoms and ionizing them.
 - The ions are attracted to the negatively charged target and are of sufficient energy to overcome the surface binding energy of the target, dislodging atoms of the target which are deposited on the wafer in the chamber.

- Sputtered atoms land on the plate and are adsorbed.
- As a number of atoms land on the surface, they form nucleation sites and these sites join to form the thin film sputtered deposition.
- Sputtering of metallic species can be done with DC, but is often performed with RF.
- Non-metallic species can also be sputtered, but since they are non-conductors, if DC is used, the target builds up a charge and the process stops. As a result, RF sources are often used..



Advantages

- Low temperature process
- Good Conformal Coating
- Good Step Coverage

Disadvantages

- Dielectrics require RF Source
- RF environment may affect other depositions

Evaporative Deposition

- Utilizes the principle of vapor pressure

Evaporative deposition results when the vapor pressure of a liquid exceeds the chamber pressure.. If the pressure in the chamber is decreased, more evaporation occurs. The process requires melting of the metallic species to be deposited in a crucible.

- Metallic species are melted in a low pressure environment
- Higher vapor pressure metals evaporate first
- Deposition of the vapor on the surface occurs
- A low temperature process on the substrate
- Alternatives include laser ablation
- Laser strikes a target, causing local melting

- Advantages
 - Uniformly covers substrate
 - Simple process without chemicals or gases
- Disadvantages
 - Alloys are difficult to deposit
 - Different metals have different vapor pressures
 - High aspect ratio features are difficult to cover
 - Trajectory of evaporated particles tends to be vertical, which may not pattern sidewalls evenly

Chemical vapor Deposition(CVD)

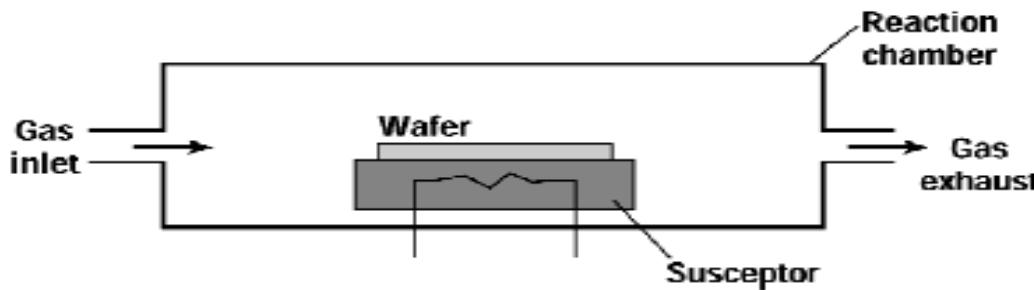
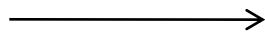
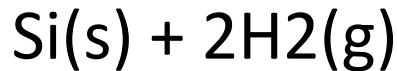


Figure 13.1 A simple prototype thermal CVD reactor.

- The reactant gas fed into the chamber through one inlet
- The wall of the tube maintained at a temperature T_w .
- A single wafer rests on a heated susceptor in the center of the tube.
- Susceptor maintained at T_s , where $T_s \gg T_w$
- Eg:decomposition of silane gas(SiH_4) to form polycrystalline silicon.
- The gas flow through the tube from left to right.

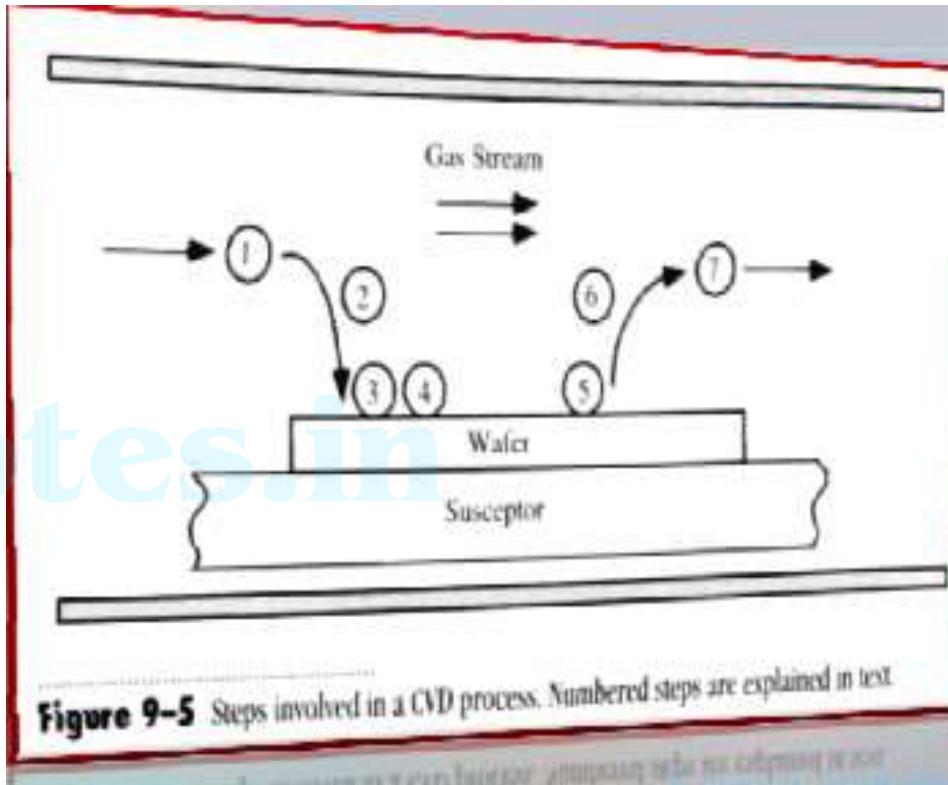
- Silane begin to decompose when it approaches the hot susceptor
- The concentration of silane and there for deposition rate ,decreases along the length of the tube
- To imporove uniformity of deposition – silane mix with inert carrier gas
- common diluent for silane is molecular hydrogen(H₂)
- The reaction products and any un reacted silane flow out of the tube at the right



CVD Mechanism

Steps:

- 1).Transport of reactants to the deposition region
- 2).Transport of reactants by diffusion from the main gas stream through the boundary layer to wafer surface
- 3).Adsorption of reactants on the wafer surface
- 4).Surface reaction
- 5).Desorption of byproducts from the surface
- 6).Transport of byproducts by diffusion through the boundary layer and back to the main gas stream.
- 7).Transport of byproducts away from the deposition region



CVD Reactor

- Two types
 - Hot walled
 - Entire furnace is heated
 - Uniformity is good
 - Contamination of furnace wall may occur
 - Cold walled
 - Only wafer is heated
 - Not a uniform process
 - Clean process
- Four Basic CVD Reactors**
- 1.) Atmospheric Pressure CVD (APCVD)
 - 2.) Low Pressure CVD (LPCVD at ~0.2 to 20 torr)
 - 3.) Metal Organic CVD (MOCVD)
 - 4.) Plasma Enhanced CVD

Advantages and disadvantages of Atmospheric pressure CVD of dielectrics

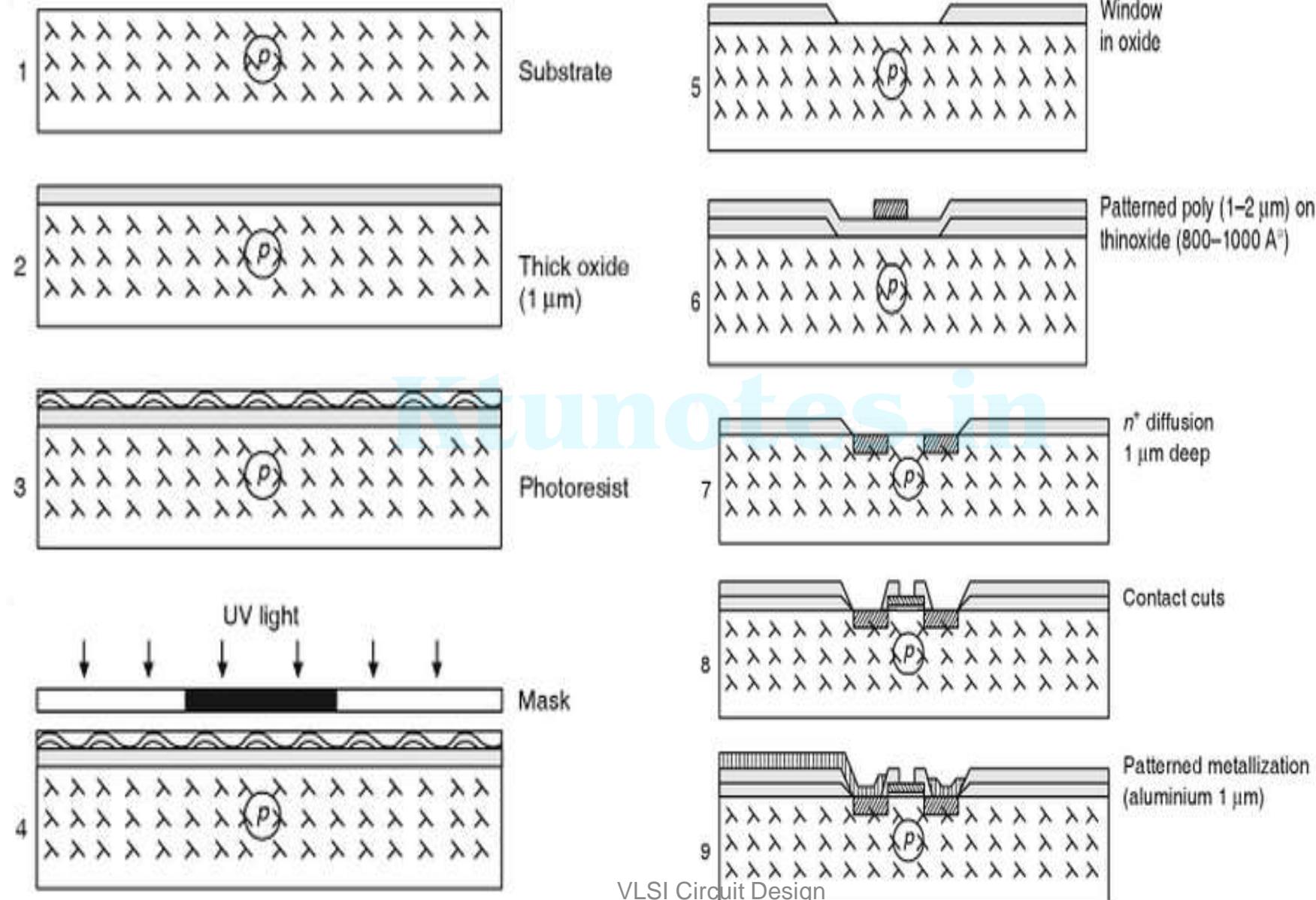
Advantages

- simplicity of the reactor design
- The costs and operating difficulties associated with high vacuum equipment are avoided and the coating may be a continuous
- Large reactivity and simplicity
- High deposition rate
- Not specifying the layer crystalline or not(eg: Silicon nitride,SiO₂)

Disadvantages

- Uniformity is poor
- Particle formation
- low throughput
- purity is less than LPCVD
- Used mainly for thick oxides.

NMOS fabrication



Complementary **MOS** fabrication

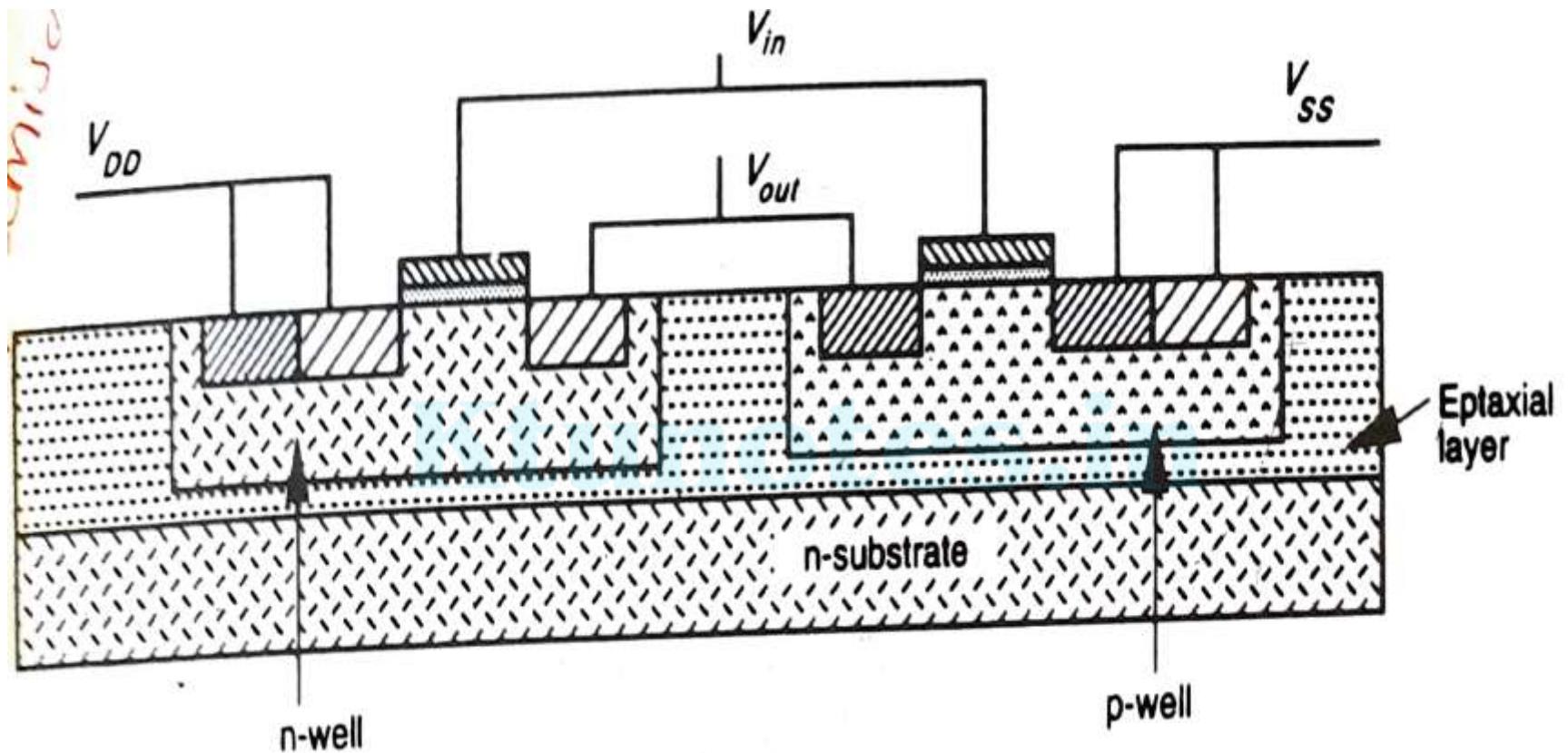
- CMOS Technology depends on using both N-Type and P-Type devices on the same chip.
- The two main technologies to do this task are:
 - P-Well
 - The substrate is N-Type. The N-Channel device is built into a P-Type well within the parent N-Type substrate. The P-channel device is built directly on the substrate.
 - N-Well
 - The substrate is P-Type. The N-channel device is built directly on the substrate, while the P-channel device is built into a N-type well within the parent P-Type substrate.
- Two more advanced technologies to do this task are:

Becoming more popular for sub-micron geometries where device performance and density must be pushed beyond the limits of the conventional p & n-well CMOS processes.

 - Twin Tub
 - Both an N-Well and a P-Well are manufactured on a lightly doped N-type substrate.
 - Silicon-on-Insulator (SOI) CMOS Process
 - SOI allows the creation of independent, completely isolated nMOS and pMOS transistors virtually side-by-side on an insulating substrate.

The Twin-Tub Process

- A logical extension of the p-well and n-well approaches is the twin-tub fabrication process.
- Here we start with a substrate of high resistivity n-type material and then create both n-well and p-well regions. Through this process it is possible to preserve the performance of n-transistors without compromising the p-transistors.
- Doping control is more readily achieved and some relaxation in manufacturing tolerances results. This is particularly important as far as latch-up is concerned.
- in general, the twin-tub process allows separate optimization of the n- and p-transistors



Twin-tub structure

**Mask 1
(well definition)**

Defines the phosphorous doped n-wells

Grow gate oxide, then cover wafer with silicon nitride

Delineate the thin oxide areas above the p-substrate,
leaving all n-well regions covered

Nitride is selectively etched from the regions where
thick oxide is desired

Boron implant is introduced to act as a self-aligned
p-type channel stop

Field oxidation

Nitride layer is selectively etched above n-well

**Mask 3
(pMOS active area)**

Mask 4
(nMOS gates)

(Note that future
p-devices are shielded
by polysilicon gate)

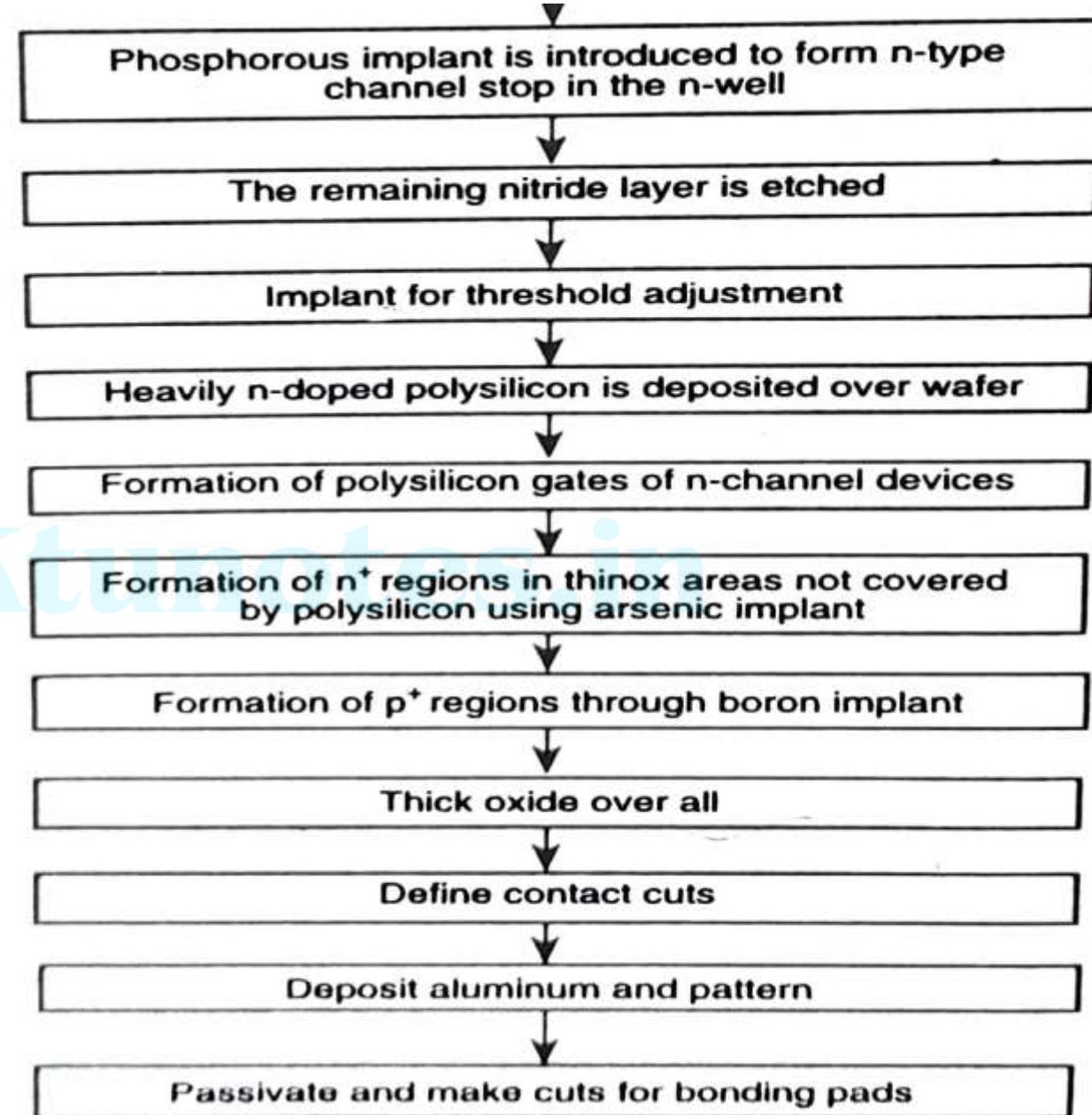
Mask 5
(pMOS polysilicon gate)

Photoresist of this step
masks the n⁺ regions
during boron implant

Mask 6
(cuts)

Mask 7
(metals)

Mask 8 (overglass)



(MOS designs,Stick Diagrams,Designrules)

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Before we start....

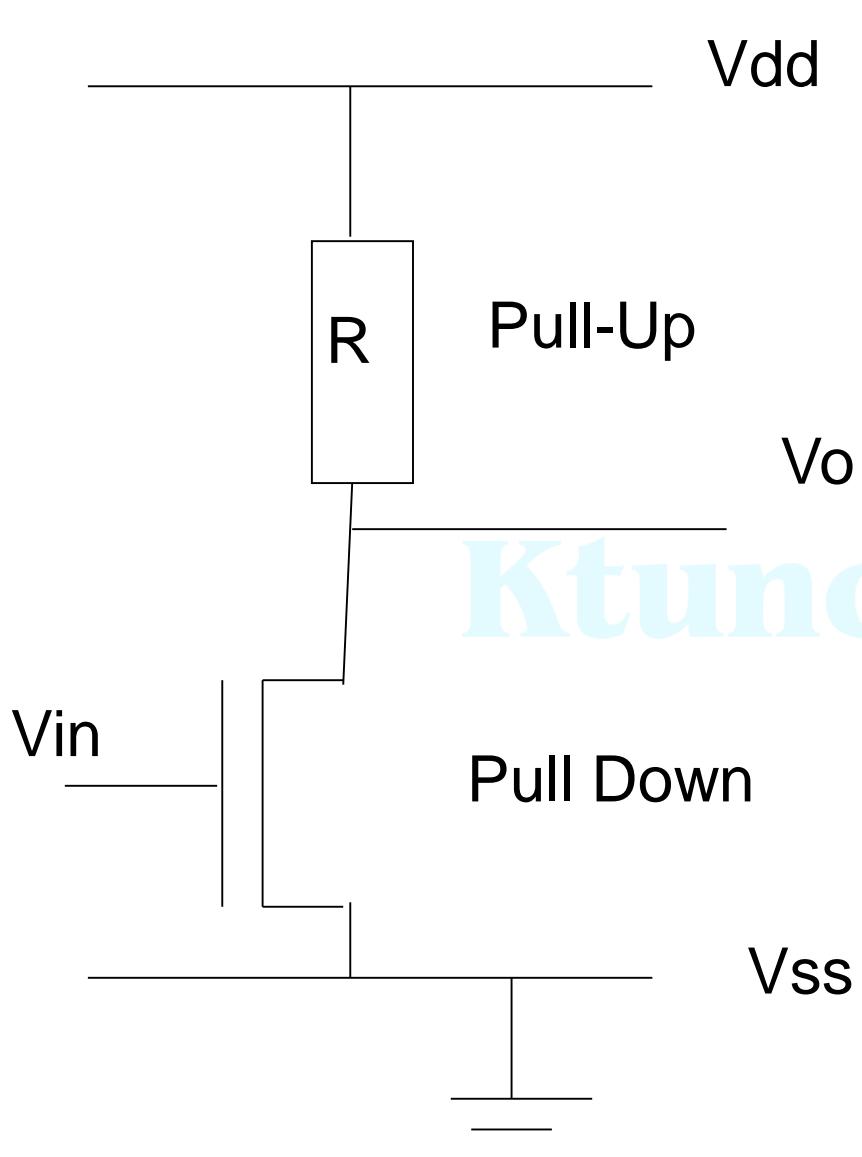
- In this module we are going to study
 - NMOS and CMOS Design Styles
 - Both combinational and sequential
 - Stick Diagrams
 - Layouts
 - Lamda and micron design rules

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- VLSI design aims to translate circuit concepts onto silicon.
- stick diagrams are a means of capturing topography and layer information using simple diagrams.
- Stick diagrams convey layer information through colour codes (or monochrome encoding).
- Acts as an interface between symbolic circuit and the actual layout.
- Design rules are communication link between the designer specifying requirements and fabricator who materializes them.
- Design rules used to produce workable mask layouts from which the various layers in silicon will be formed or patterned

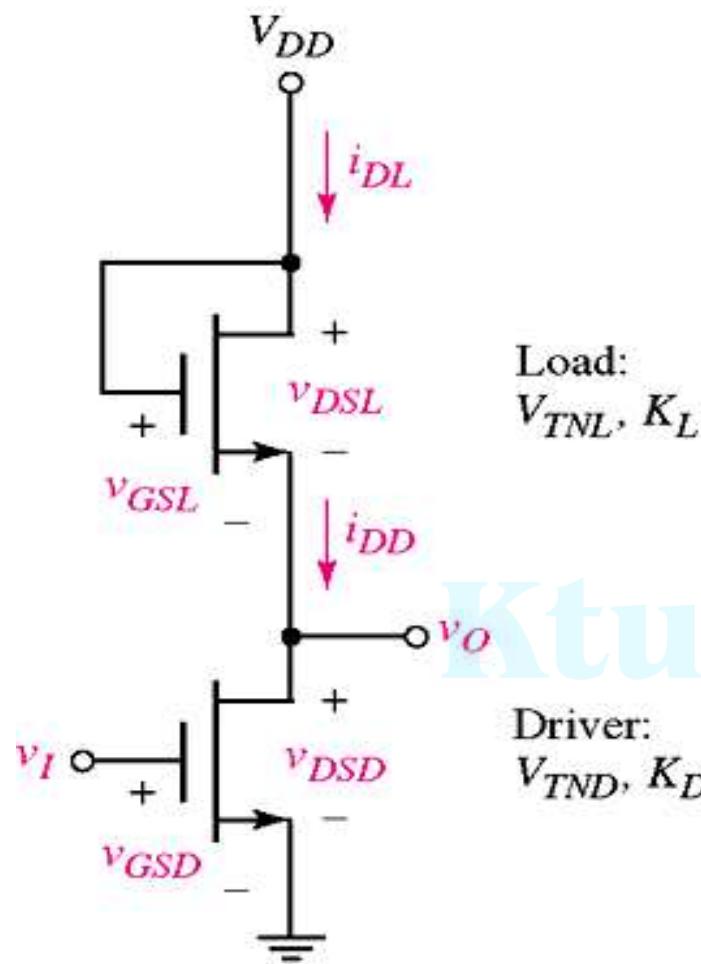
eg: lambda– based design rules

1).NMOS resistor Pull - Up



2).NMOS Depletion Mode Transistor Pull - Up

VLSI Circuit Design
ADARSH K S



(a)

3).NMOS enhancement Mode Transistor

Pull - Up

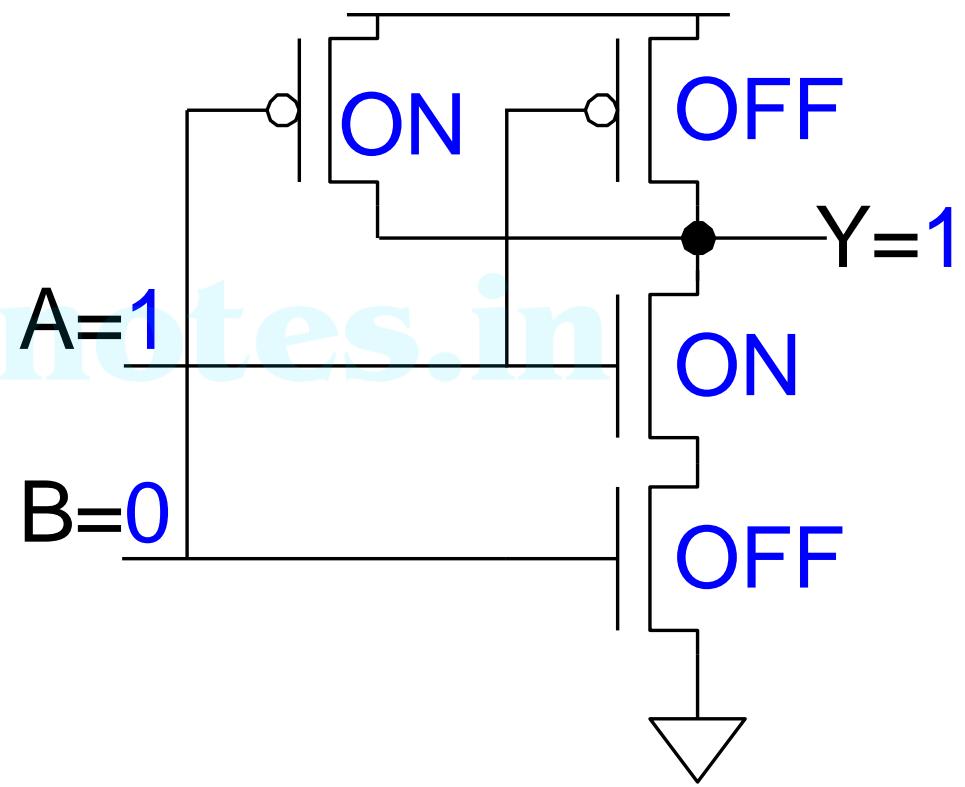
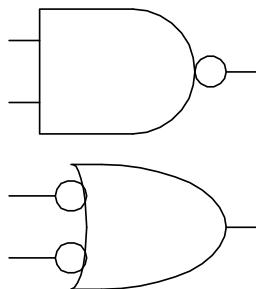
VLSI Circuit Design

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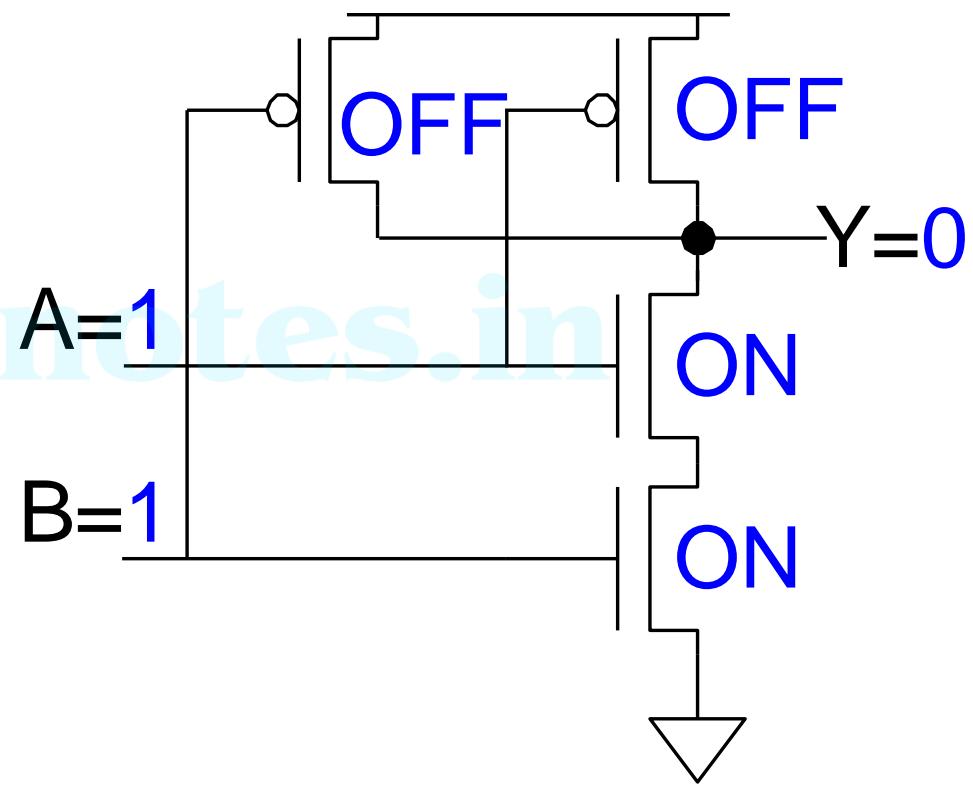
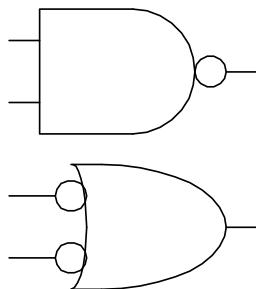
CMOS NAND Gate

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	



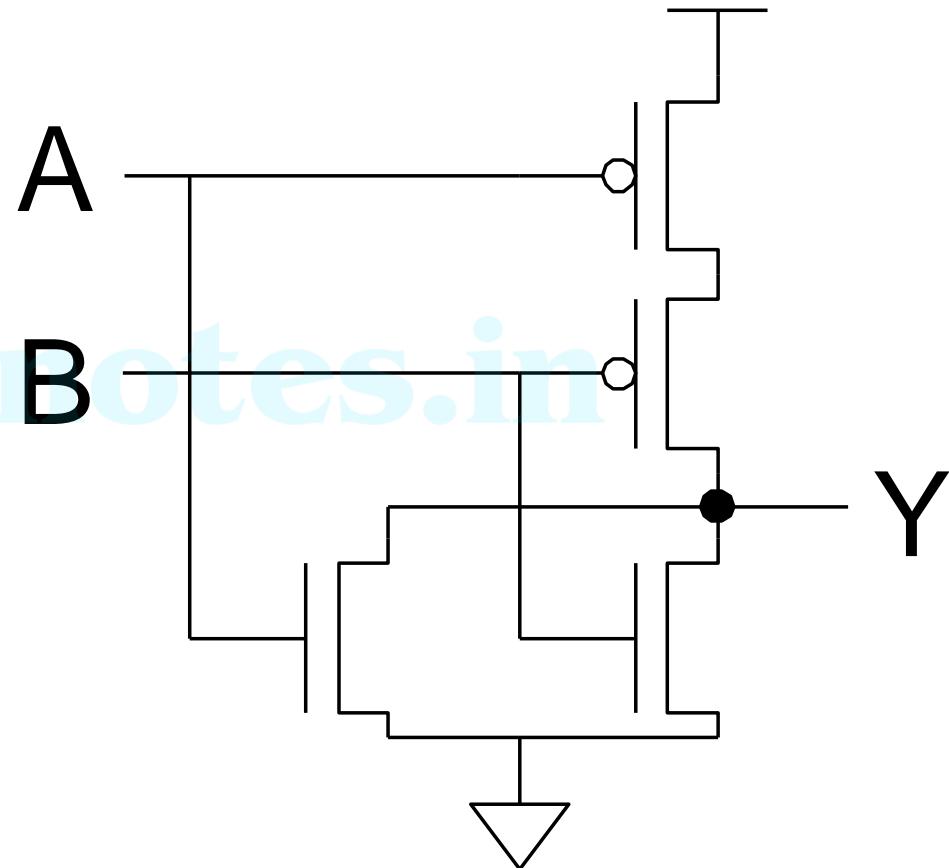
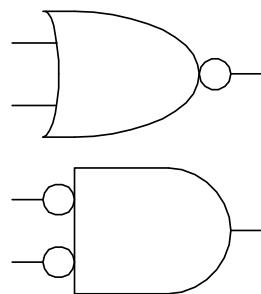
CMOS NAND Gate

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0



CMOS NOR Gate

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0



MOS Layers

- MOS design – turning specification into mask
- MOS circuit formed on four basic layers-n diffusion, p-diffusion , polysilicon and metal which are isolated from one another by thick or thin silicon dioxide insulating layer
- Thin oxide mask region include-n-diffusion,p diffusion and transistor channel
- Polysilicon and thinox region interact so that a transistor is formed where they cross one another

Stick diagrams

- A stick diagram is a cartoon of a layout.
- Does show all components/vias (except possibly tub ties), relative placement.
- Does not show exact placement, transistor sizes, wire lengths, wire widths, tub boundaries.

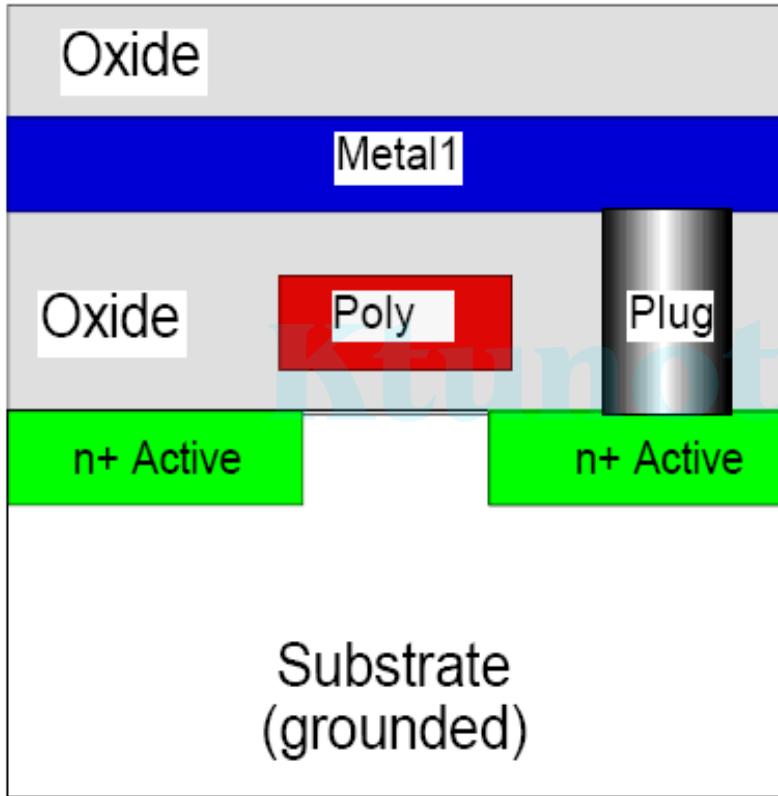
Stick Diagrams

- Key idea: "Stick figure cartoon" of a layout
- Useful for planning layout
 - relative placement of transistors
 - assignment of signals to layers
 - connections between cells
 - cell hierarchy

Stick diaram

COLOR	NAME	FUNCTION
green	ndiff	
yellow	pdiff	source/drain
red	poly	gate
blue	metal 1	
violet	metal 2	
light blue	metal 3	interconnect Can also draw in shades of gray/line style.

MOS structure



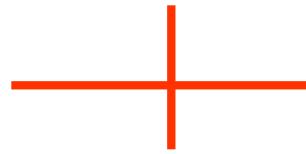
A contact or via is needed to connect two layers

Stick Diagrams – Some rules

Rule 1.

When two or more ‘sticks’ of the same type cross or touch each other that represents electrical contact.

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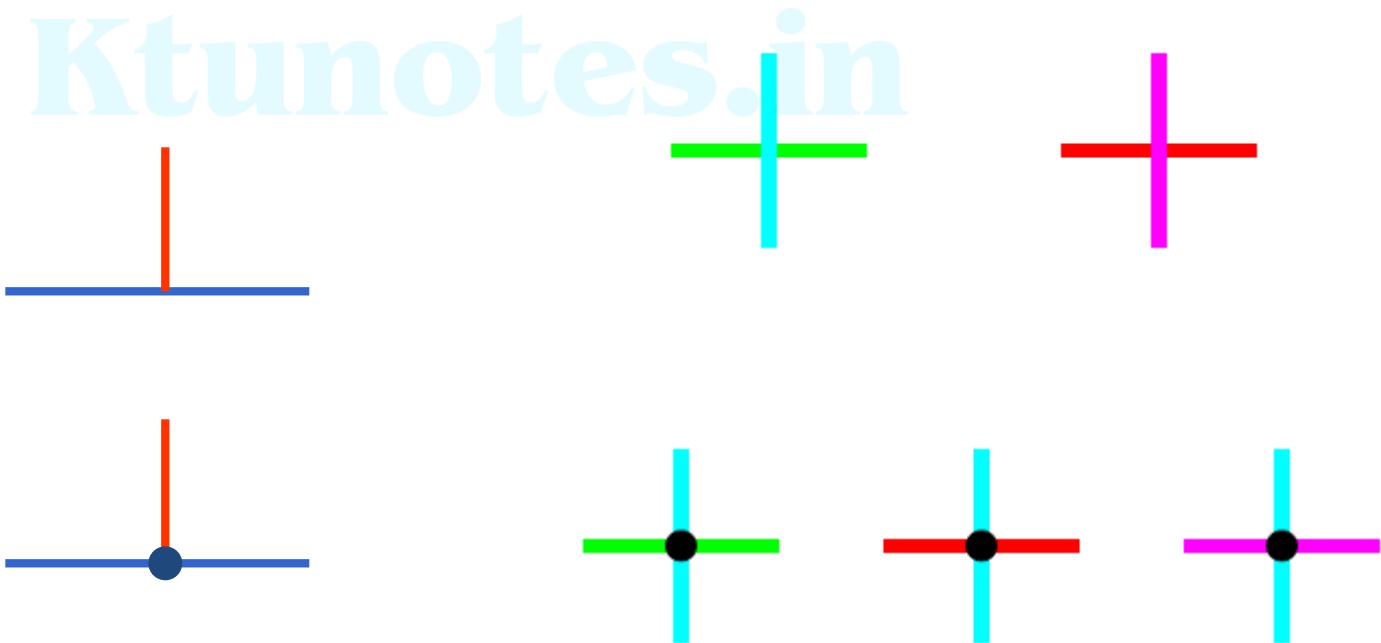


Stick Diagrams – Some rules

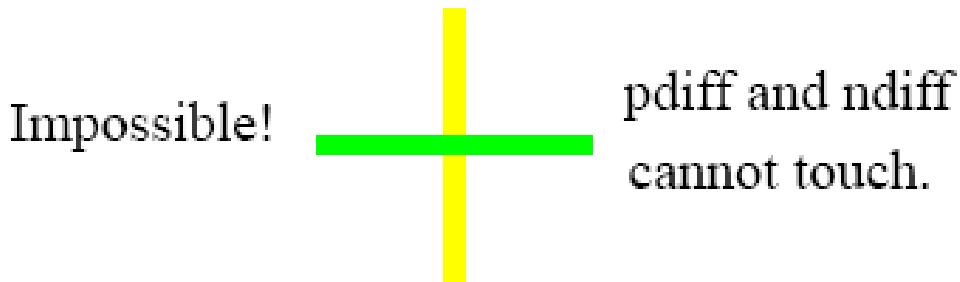
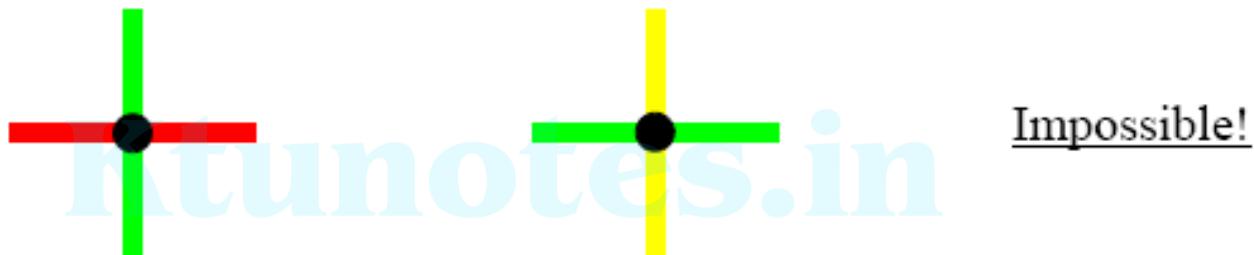
Rule 2.

When two or more ‘sticks’ of different type cross or touch each other there is no electrical contact.

(If electrical contact is needed we have to show the connection explicitly).



- Metal must be one of the layers in the contact



Stick Diagrams – Some rules

Rule 3.

When a poly crosses diffusion it represents a transistor.



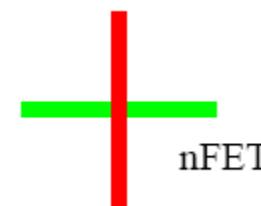
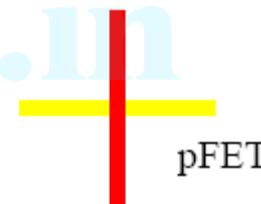
poly crossing diff always makes FET (even if you don't want one there)

Stick Diagrams – Some rules

Rule 4.

In CMOS a demarcation line is drawn to avoid touching of p-diff with n-diff. All pMOS must lie on one side of the line and all nMOS will have to be on the other side.

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nMOS Design style

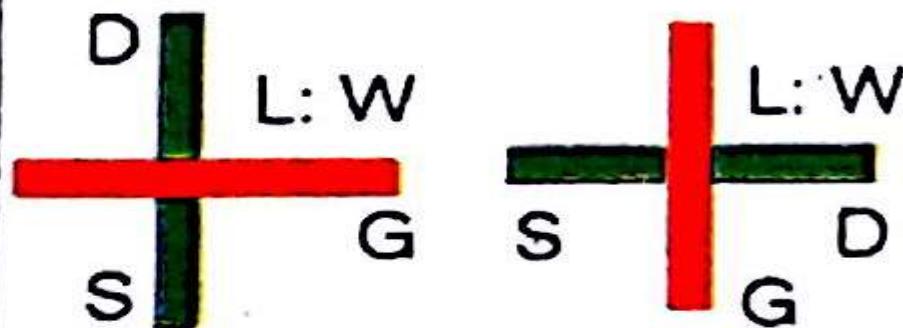
- The layout of nMOS involves:
- N-diffusion
- Polysilicon
- Metal 1
- Implant
- contact

COLOR	STICK ENCODING	LAYERS
GREEN		n-diffusion (n+ active) Thinox*
RED		Polysilicon
BLUE		Metal 1
BLACK		Contact cut
GRAY	NOT APPLICABLE	Overglass
nMOS ONLY YELLOW		Implant
nMOS ONLY BROWN		Buried contact

FEATURE

n-type
enhancement
mode transistor

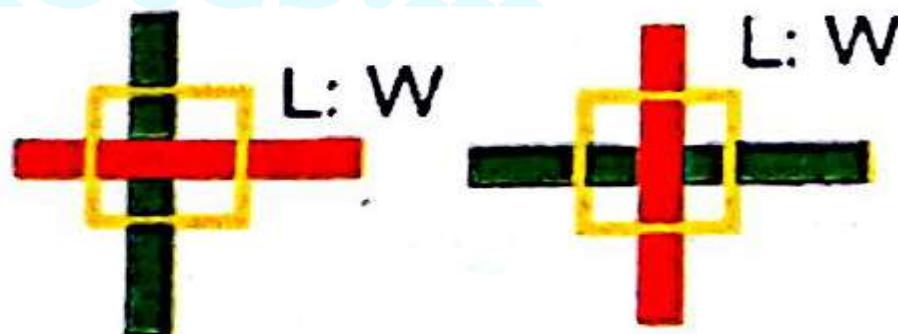
FEATURE (STICK)



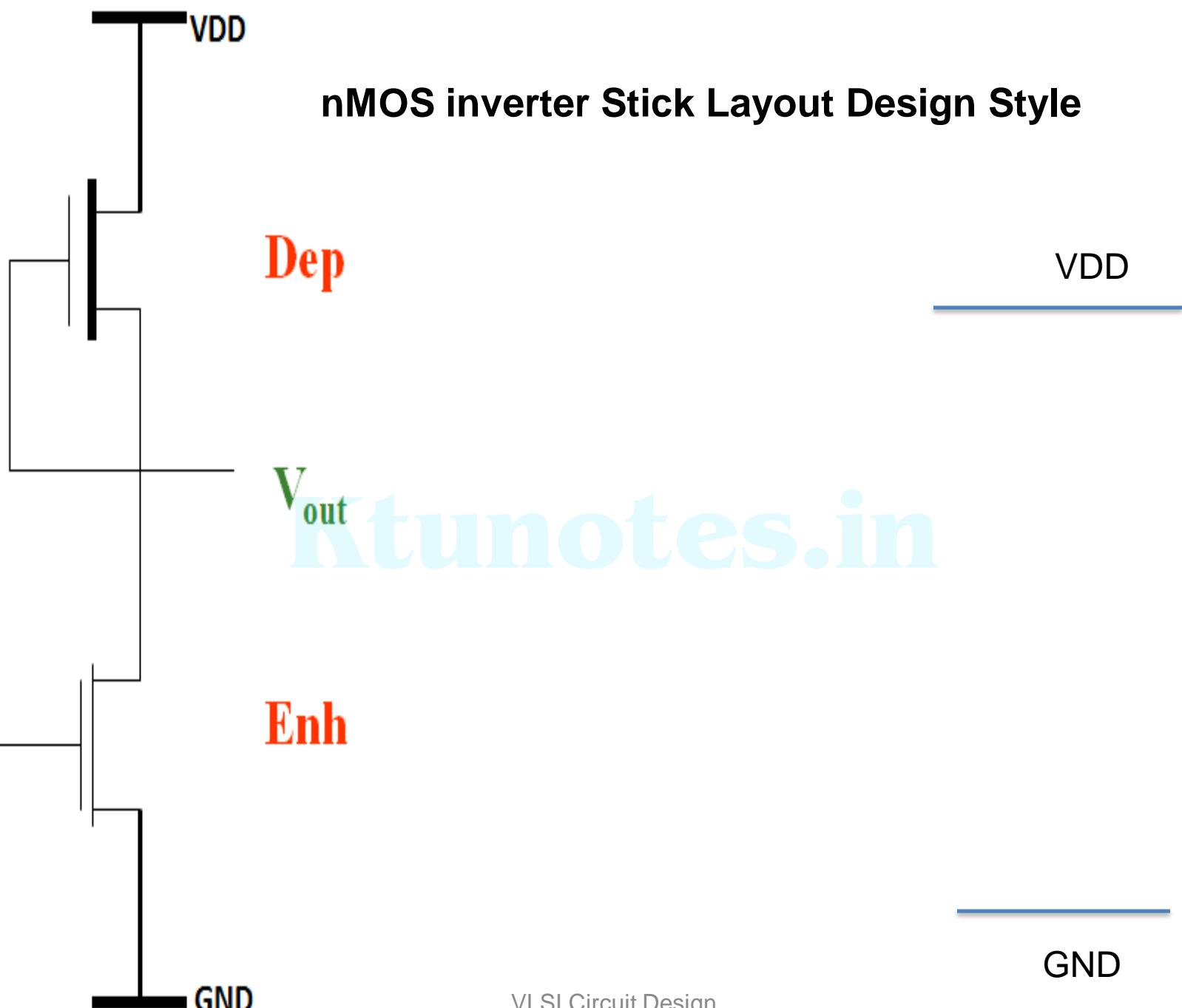
Transistor length to width ratio L:W should be small

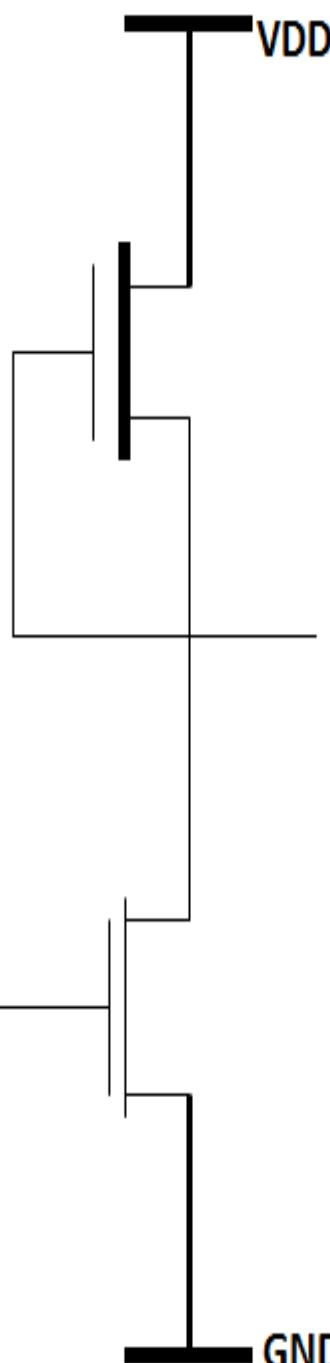
n-type depletion
mode transistor

nMOS only



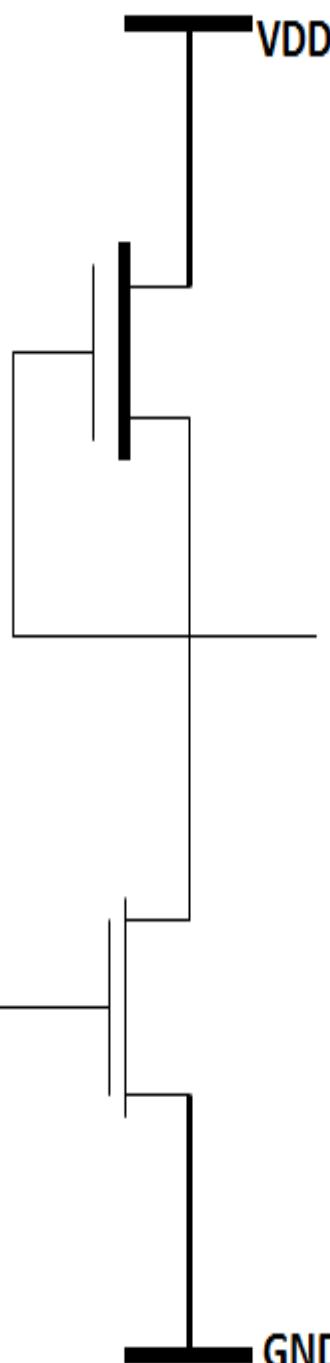
Source, drain and gate labelling





nMOS inverter Stick Layout Design Style

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nMOS inverter Stick Layout Design Style

Dep

V_{out}

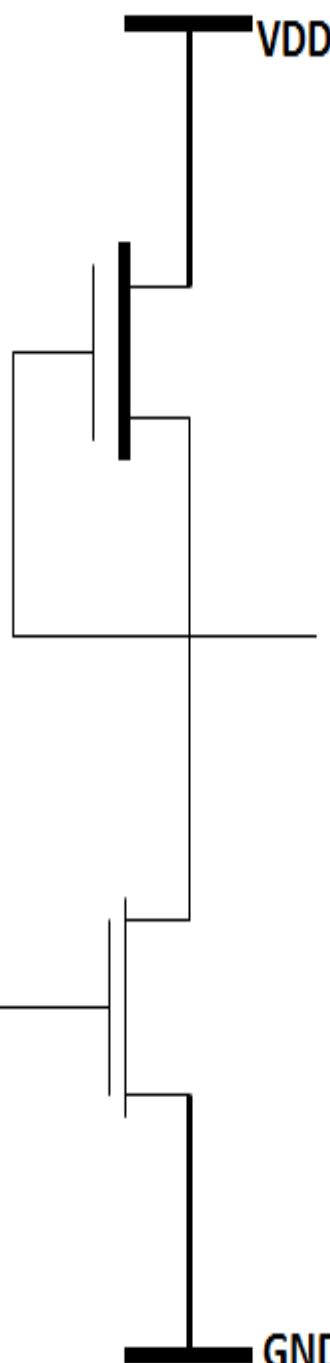
Enh

V_{in}

GND

VDD

GND



nMOS inverter Stick Layout Design Style

Dep

V_{out}

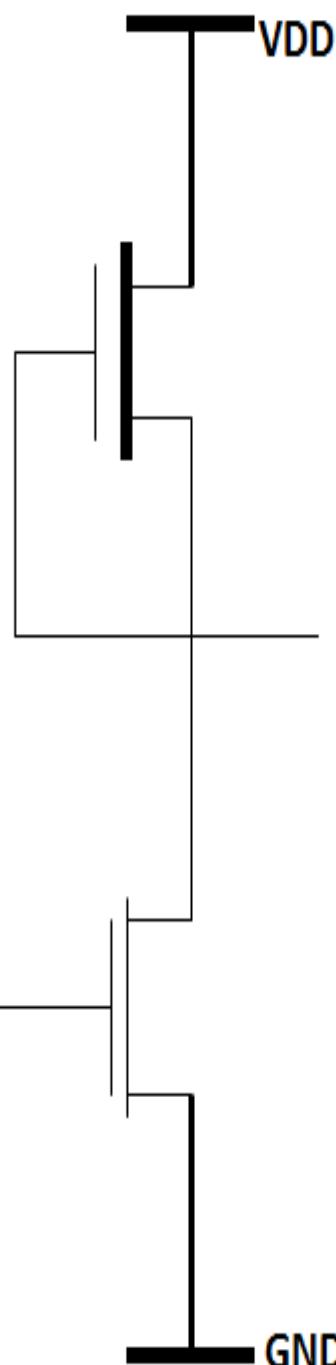
V_{in}

Enh

GND

V_{DD}

GND



nMOS inverter Stick Layout Design Style

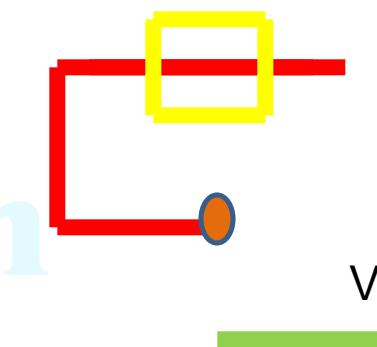
Dep

V_{out}

Enh

V_{in}

GND

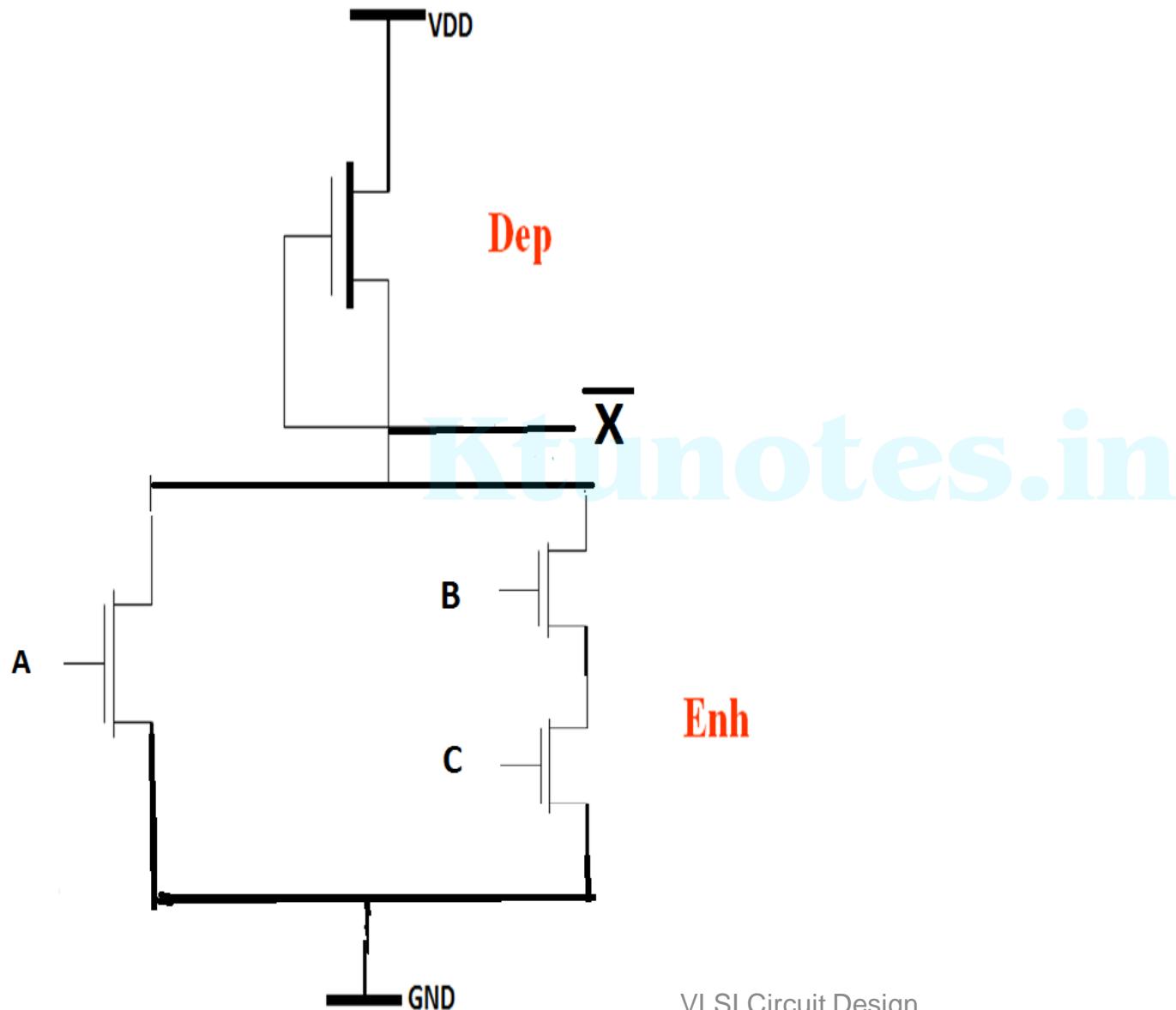


V_{in}

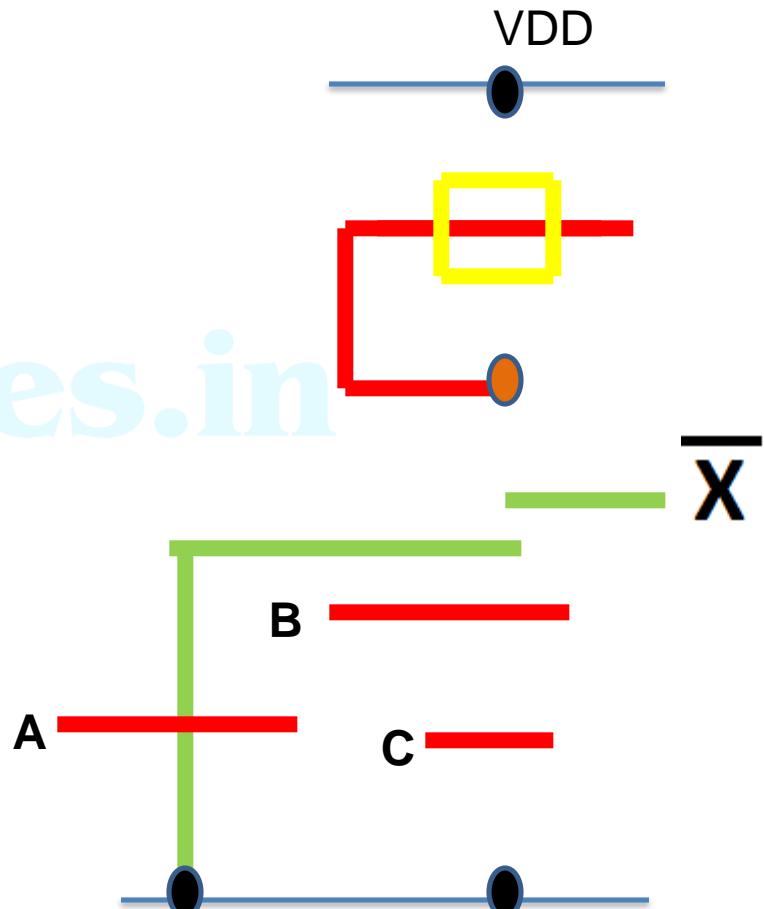
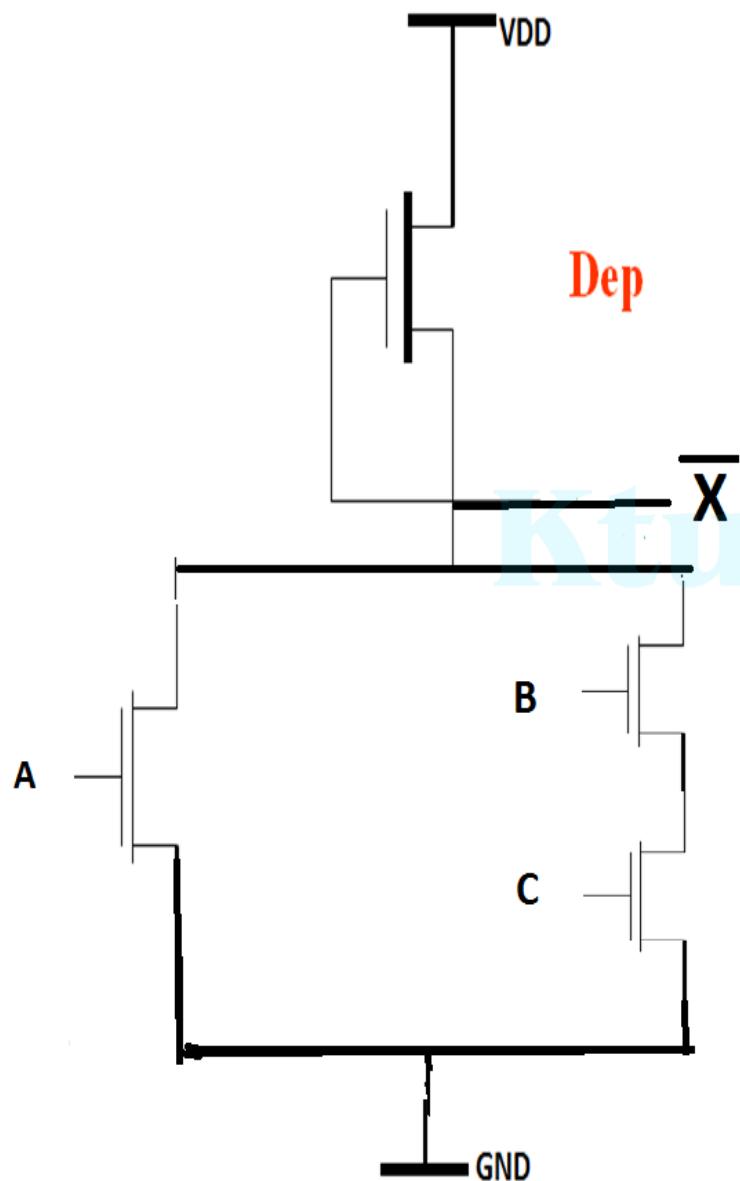
V_{DD}

V_{out}

Eg: $\overline{X} = A + B \cdot C$



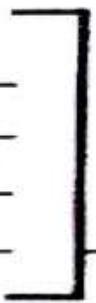
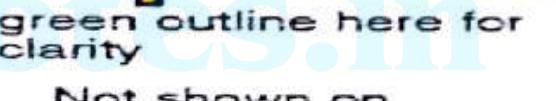
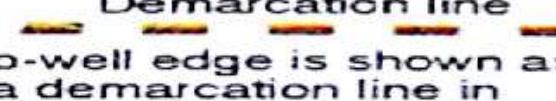
Eg: $\overline{X} = A + B \cdot C$



CMOS Design style

The layout of CMOS involves:

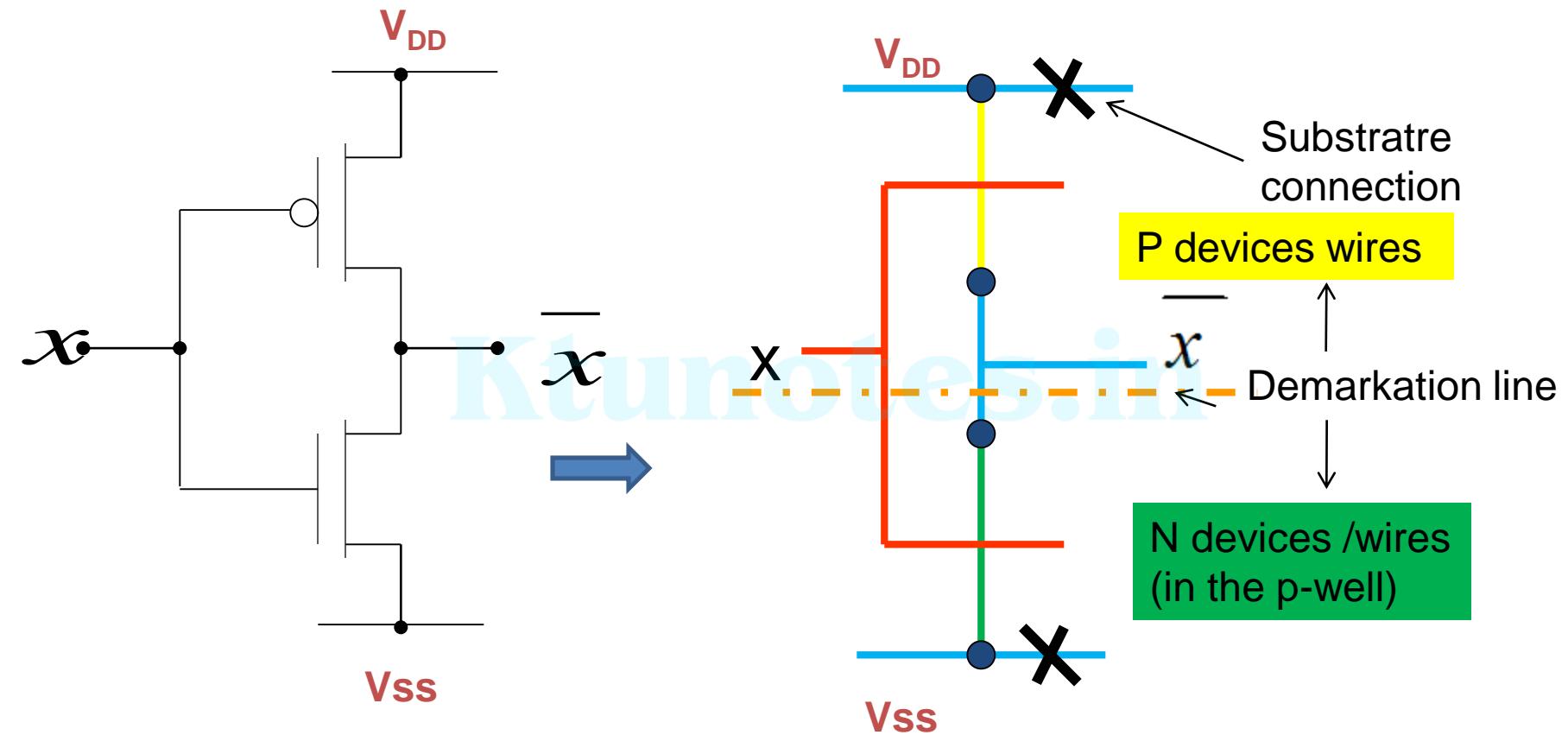
- N-diffusion
- Polysilicon
- Metal 1
- Contact
- P-diffusion
- P-well or N-well

COLOR	STICK ENCODING	LAYERS
GREEN		n-diffusion (n+ active) Thinox*
RED		Polysilicon
BLUE		Metal 1
BLACK		Contact cut
GRAY		Overglass
YELLOW (STICK)	 green outline here for clarity	p-diffusion (p+ active)
YELLOW	 Not shown on diagram	p+ mask
DARK BLUE OR PURPLE		Metal 2
BLACK		VIA
BROWN	 Demarcation line p-well edge is shown as a demarcation line in stick diagrams	p-well
BLACK		V_{DD} or V_{SS} contact

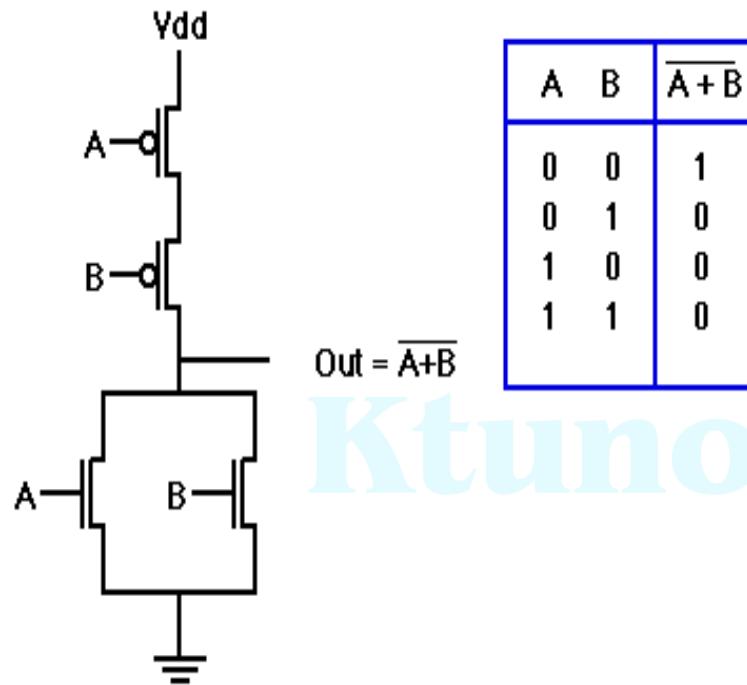
FEATURE	FEATURE (STICK)
<p><i>n-type enhancement mode transistor (as in Color plate 1(a))</i></p> <p>Transistor length to width ratio L:W may be selected.</p>	<p>Demarcation line</p>
<p><i>p-type enhancement mode transistor</i></p>	<p>Demarcation line</p>

Note :-

P-Well CMOS Inverter



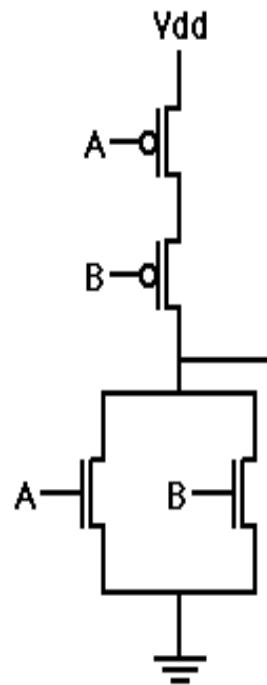
Static CMOS NOR gate



A	B	$\overline{A+B}$
0	0	1
0	1	0
1	0	0
1	1	0

1. Pull-down: Connect to ground If A=1 OR B=1
2. Pull-up: Connect to Vdd If A=0 AND B=0
2. Pull-up: Connect to Vdd If A=0 OR B=0

Static CMOS NOR gate



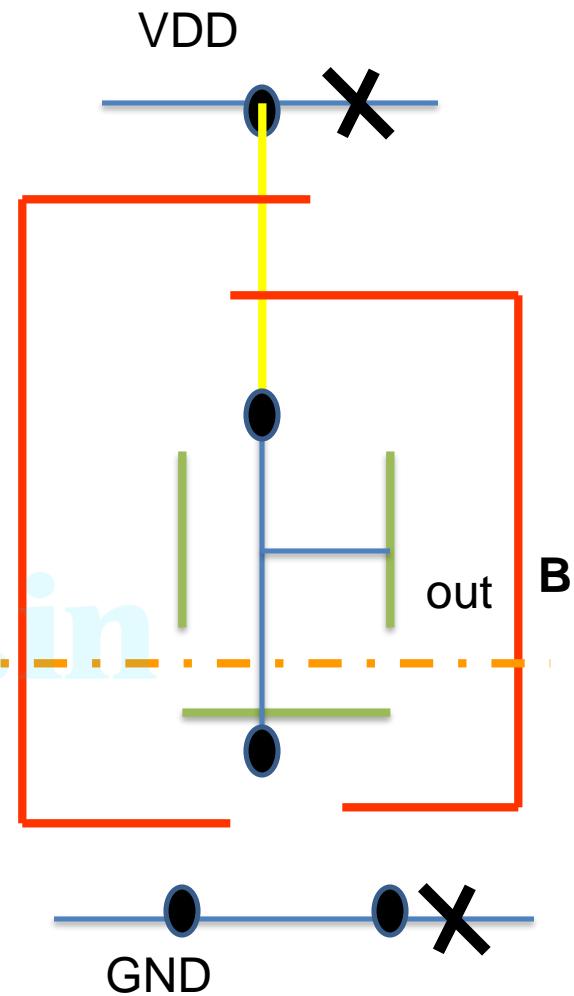
A	B	$\overline{A+B}$
0	0	1
0	1	0
1	0	0
1	1	0

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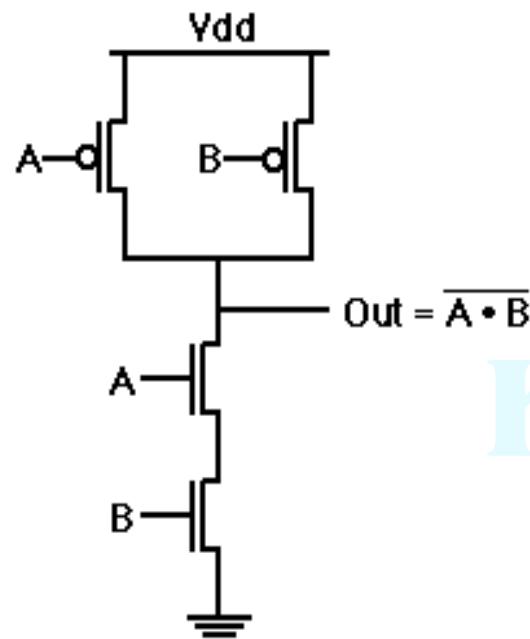
1. Pull-down: Connect to ground If A=1 OR B=1

2. Pull-up: Connect to Vdd If A=0 AND B=0

2. Pull-up: Connect to Vdd If A=0 OR B=0



Static CMOS NAND gate

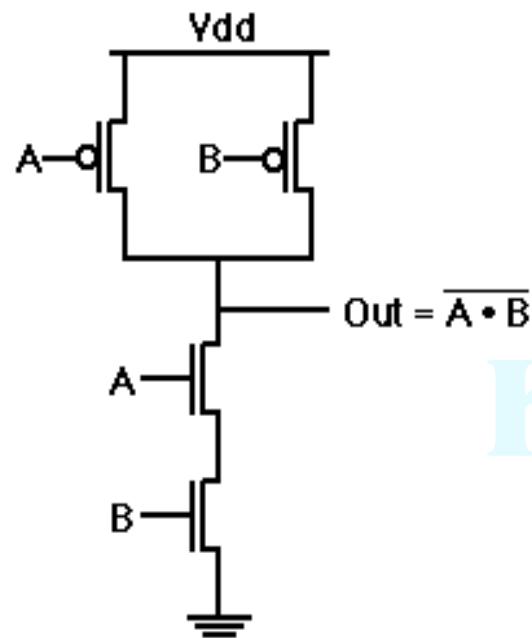


A	B	$\overline{A \cdot B}$
0	0	1
0	1	1
1	0	1
1	1	0

Ktunotes.in

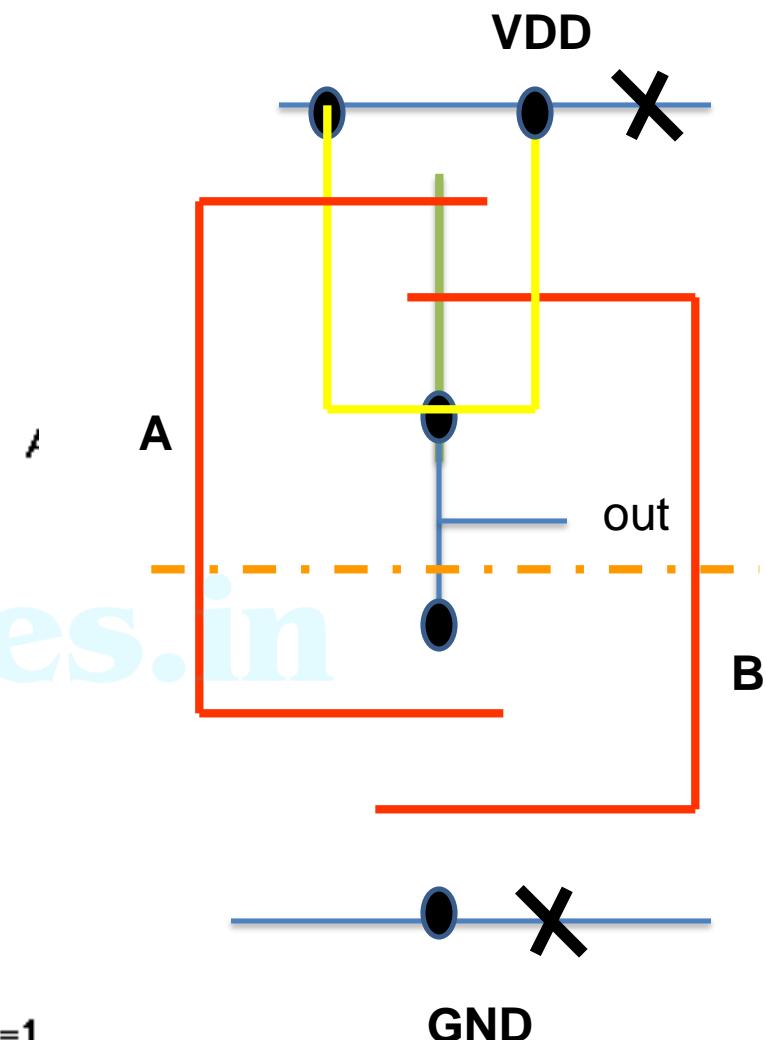
1. Pull-down: Connect to ground If A=1 AND B=1
2. Pull-up: Connect to Vdd If A=0 OR B=0

Static CMOS NAND gate



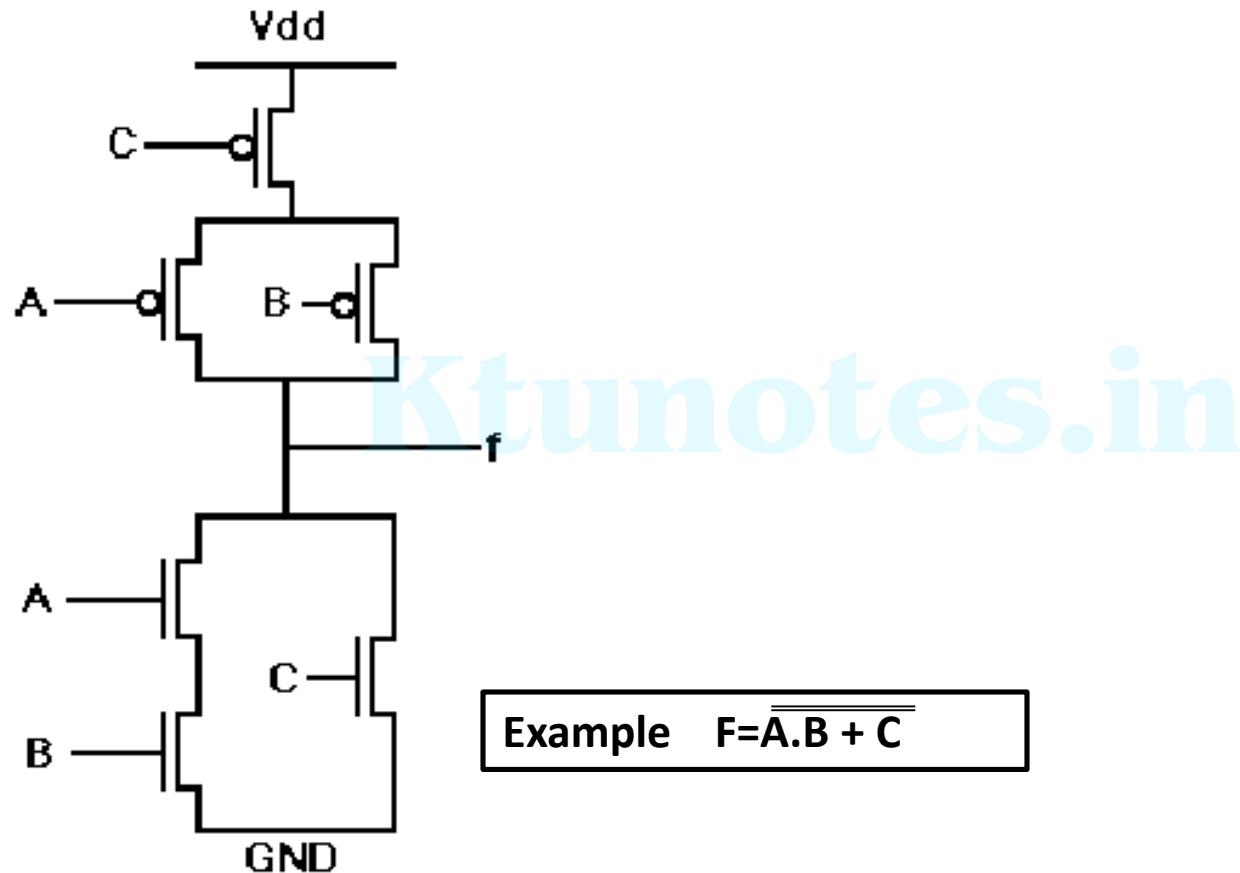
A	B	$\overline{A \cdot B}$
0	0	1
0	1	1
1	0	1
1	1	0

Ktunotes.in

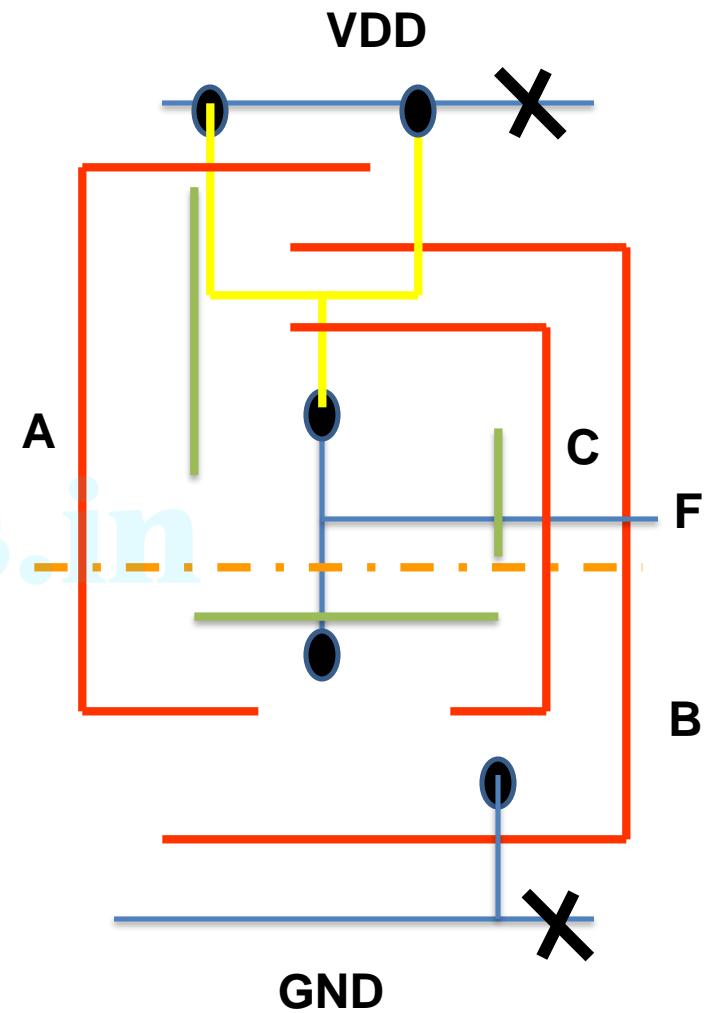
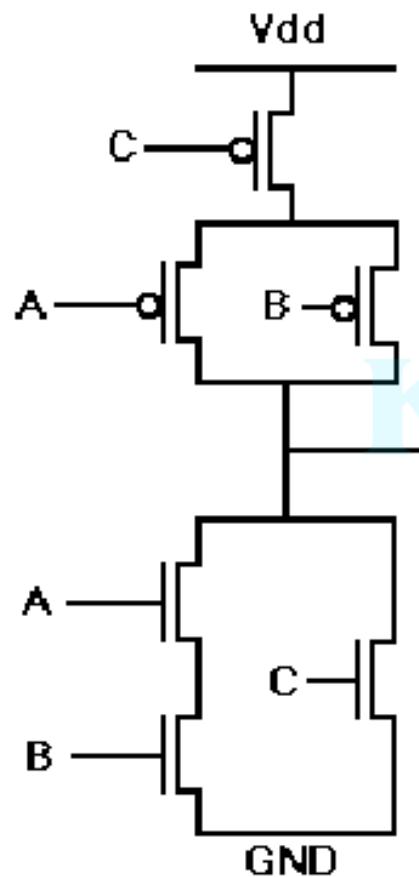


1. Pull-down: Connect to ground If A=1 AND B=1
2. Pull-up: Connect to Vdd If A=0 OR B=0

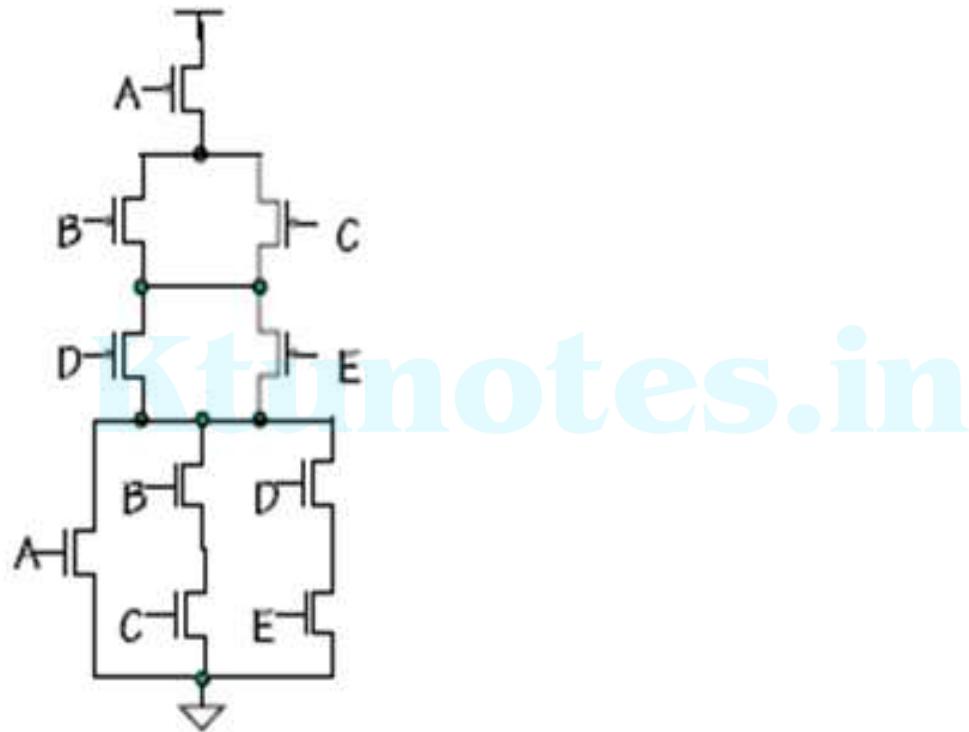
Static CMOS Design Example stick Layout



Static CMOS Design Example stick Layout



Draw the stick diagram



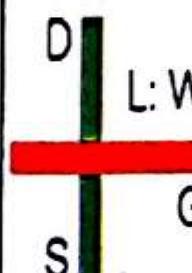
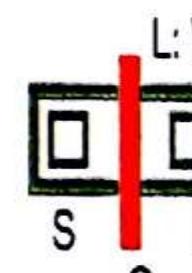
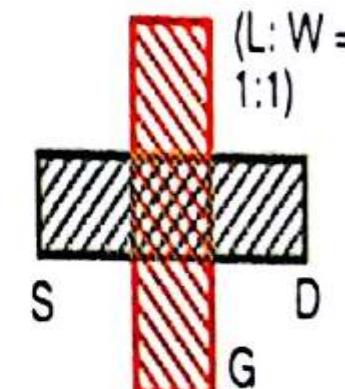
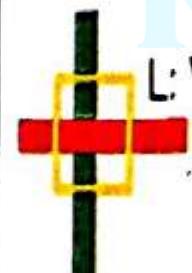
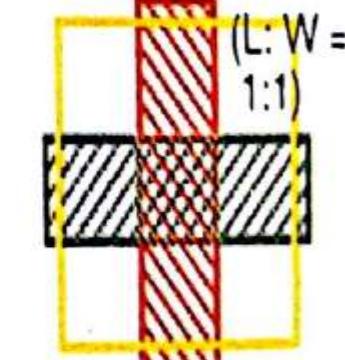
CMOS Layout

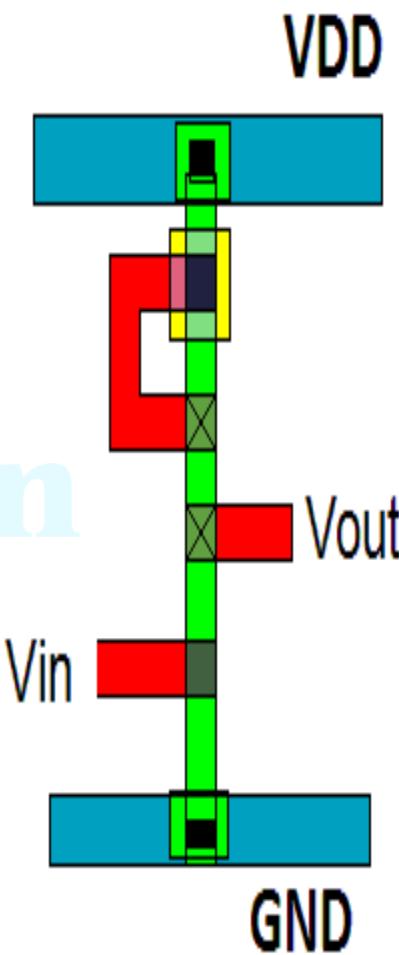
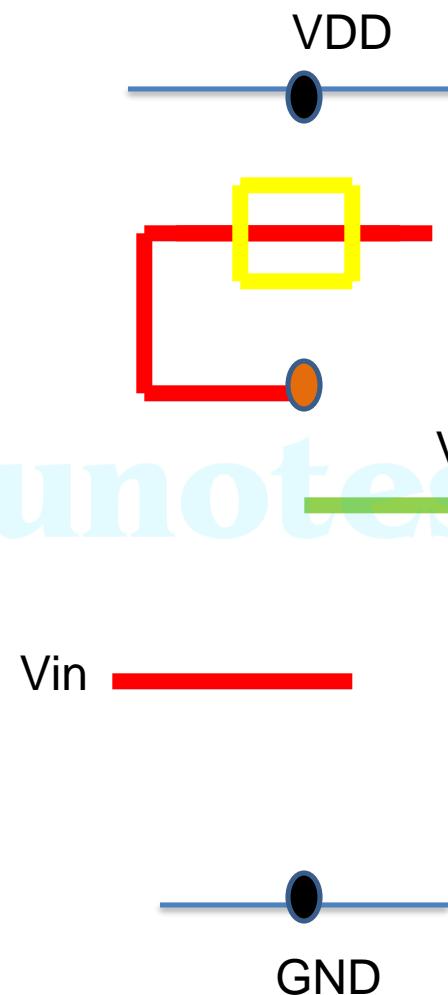
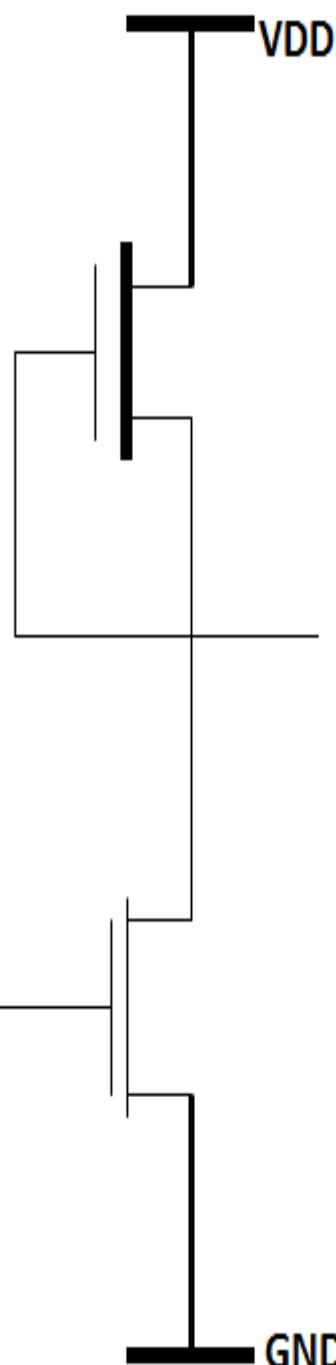
Measure twice, fab once



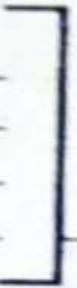
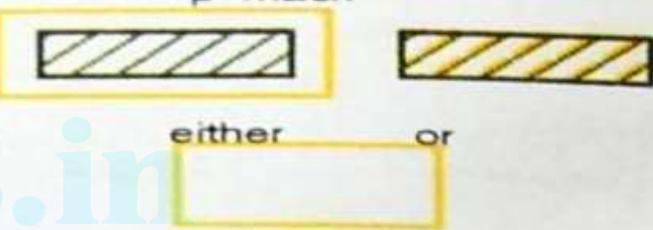
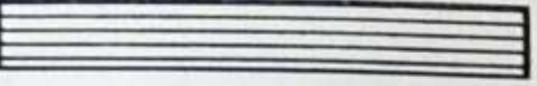
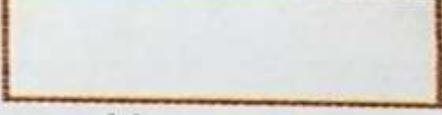
nMOS Design style

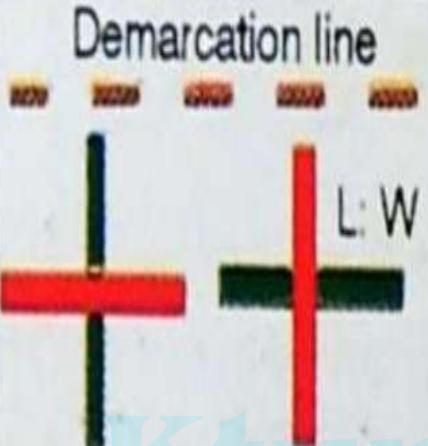
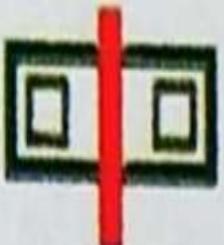
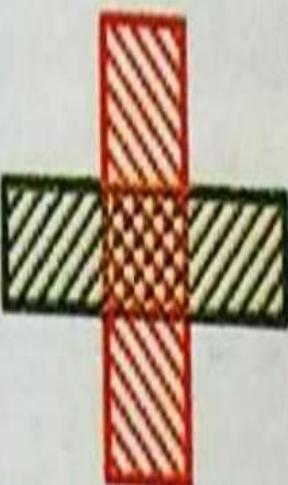
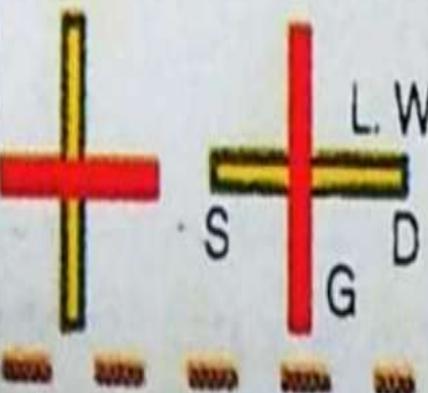
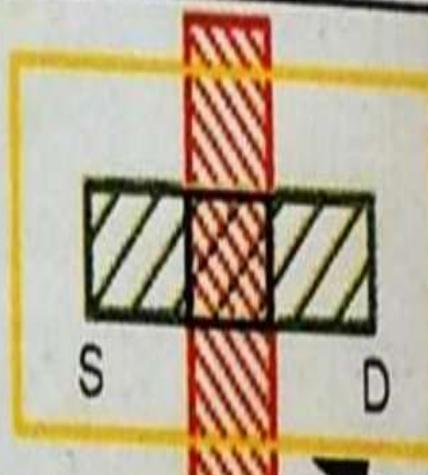
COLOR	STICK ENCODING	LAYERS	MASK LAYOUT ENCODING	CIF LAYER
GREEN		n-diffusion (n+ active) Thinox*	 *Thinox = n-diff. + transistor channels	ND
RED		Polysilicon		NP
BLUE		Metal 1		NM
BLACK		Contact cut		NC
GRAY	NOT APPLICABLE	Overglass		NG
nMOS ONLY YELLOW		Implant		NI
nMOS ONLY BROWN		Buried contact		NB

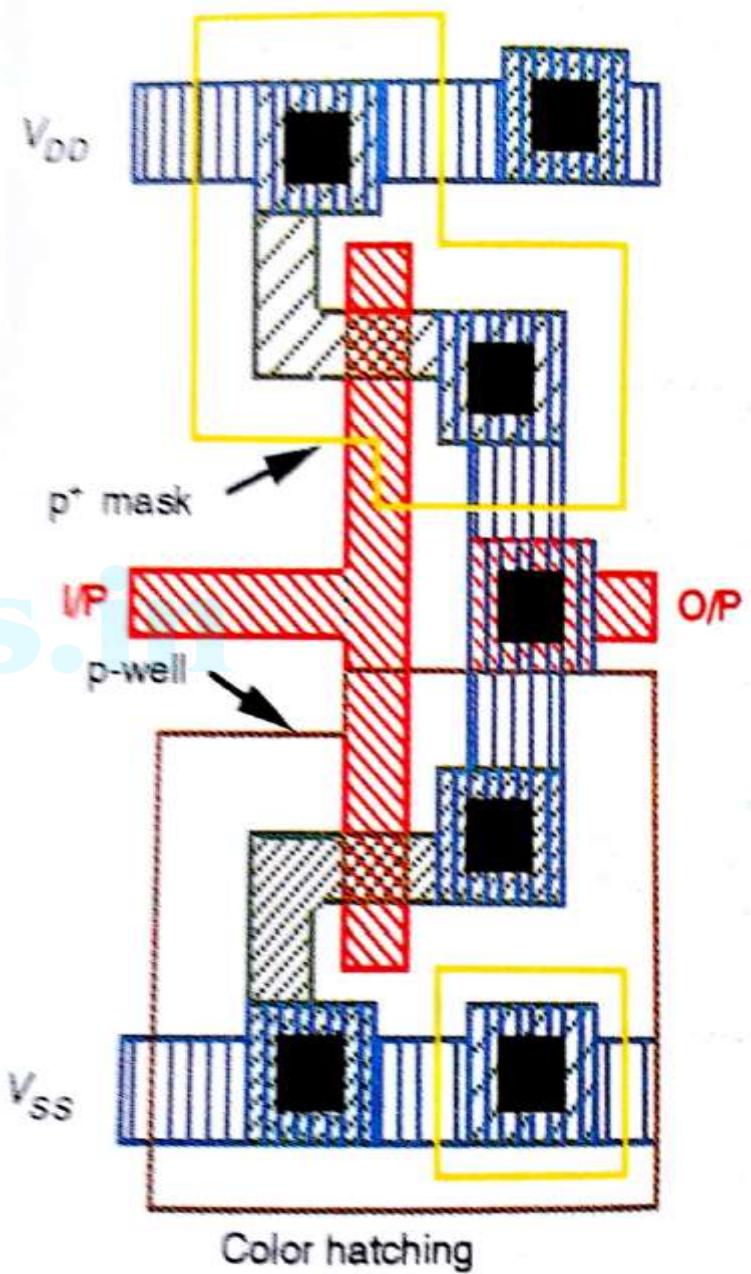
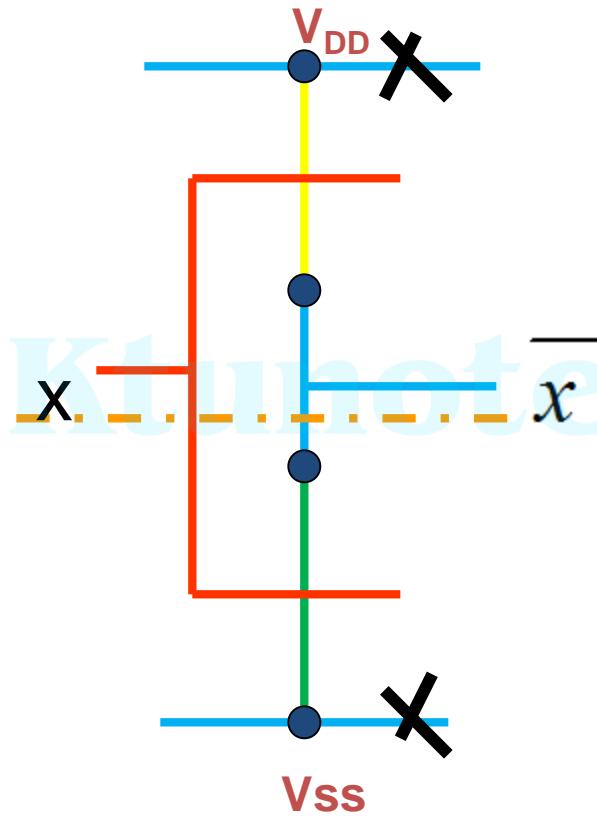
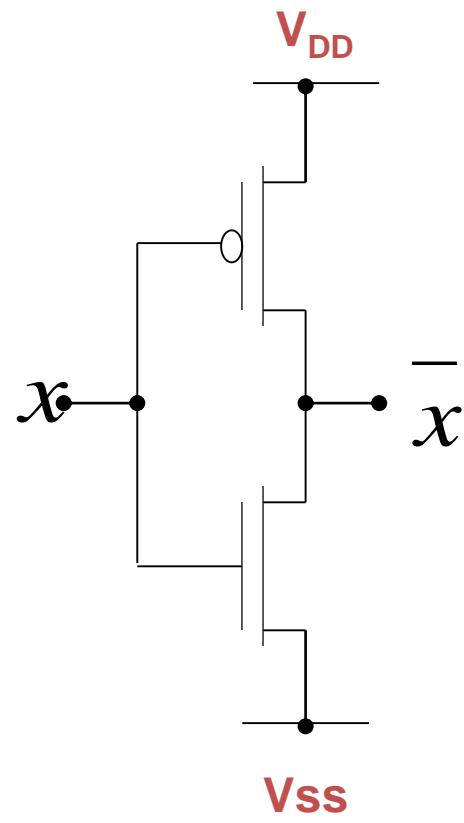
FEATURE	FEATURE (STICK)	FEATURE (SYMBOL)	FEATURE (MASK)
n-type enhancement mode transistor	 		
	Transistor length to width ratio L: W should be shown.		
n-type depletion mode transistor nMOS only	 		
	Source, drain and gate labelling will not normally be shown.		



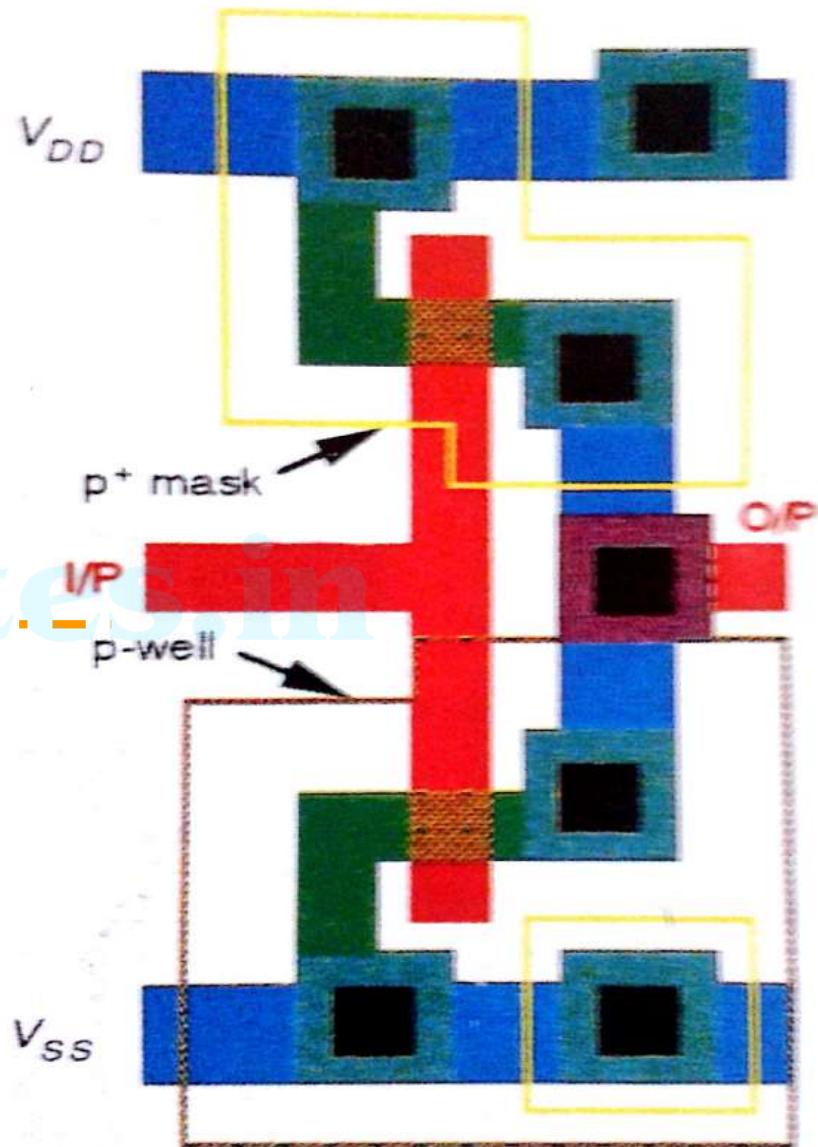
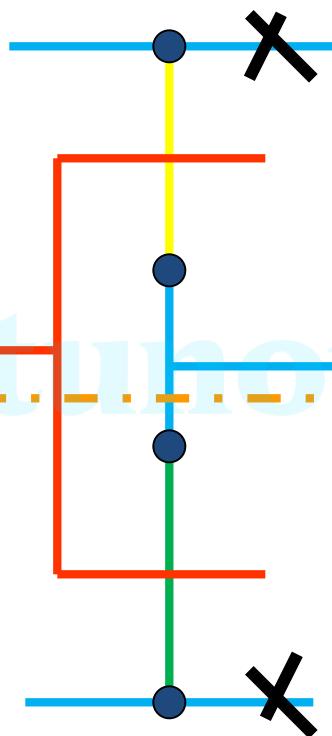
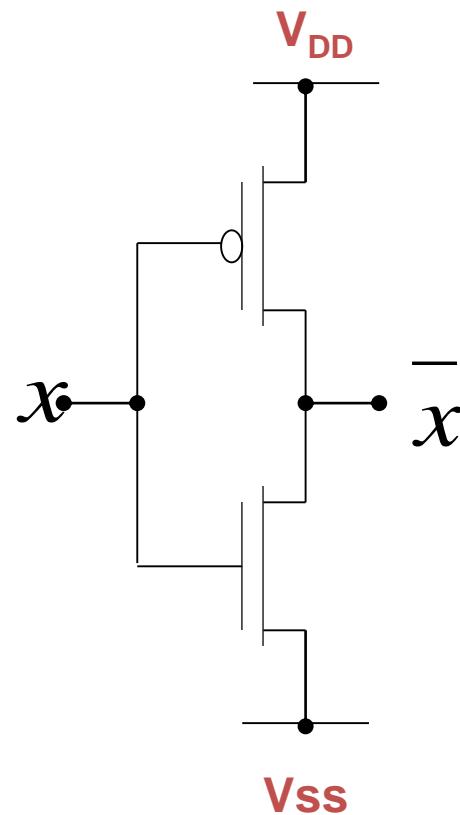
CMOS Design style

COLOR	STICK ENCODING	LAYERS	MASK LAYOUT ENCODING
GREEN		n-diffusion (n+ active) Thinox*	* Thinox = n-diff. + p-diff. + transistor channels
RED			
BLUE			
BLACK		Contact cut	
GRAY		Overglass	
YELLOW (STICK)	 green outline here for clarity	p-diffusion (p+ active)	
YELLOW	Not shown on diagram	p+ mask	or
DARK BLUE OR PURPLE		Metal 2	
BLACK		VIA	
BROWN	 Demarcation line p-well edge is shown as a demarcation line in stick diagrams	p-well	
BLACK		V_{DD} or V_{SS} contact	

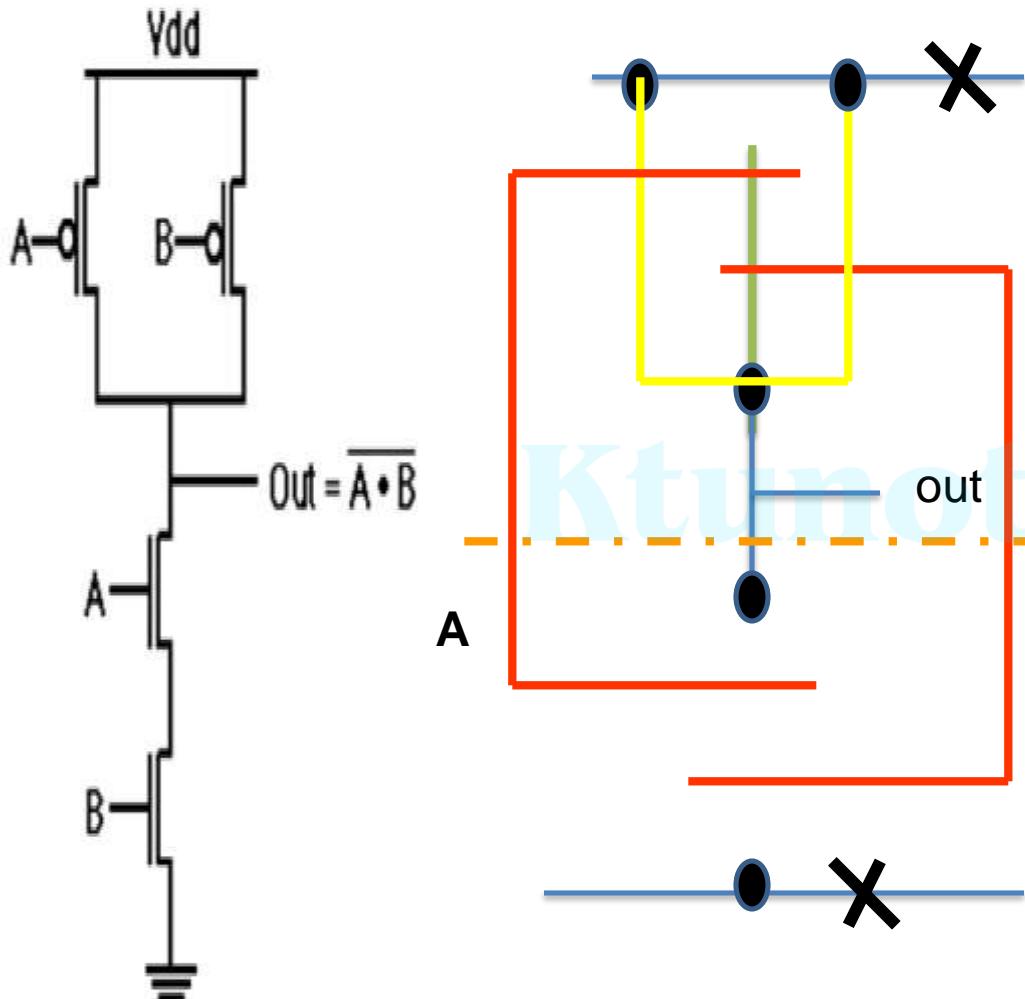
FEATURE	FEATURE (STICK)	FEATURE (SYMBOL)	FEATURE (MASK)
<p><i>n-type enhancement mode transistor (as in Color plate 1(a))</i></p> <p>Transistor length to width ratio L:W may be shown.</p>	<p>Demarcation line</p> 		
<p><i>p-type enhancement mode transistor</i></p>	 <p>Demarcation line</p>		



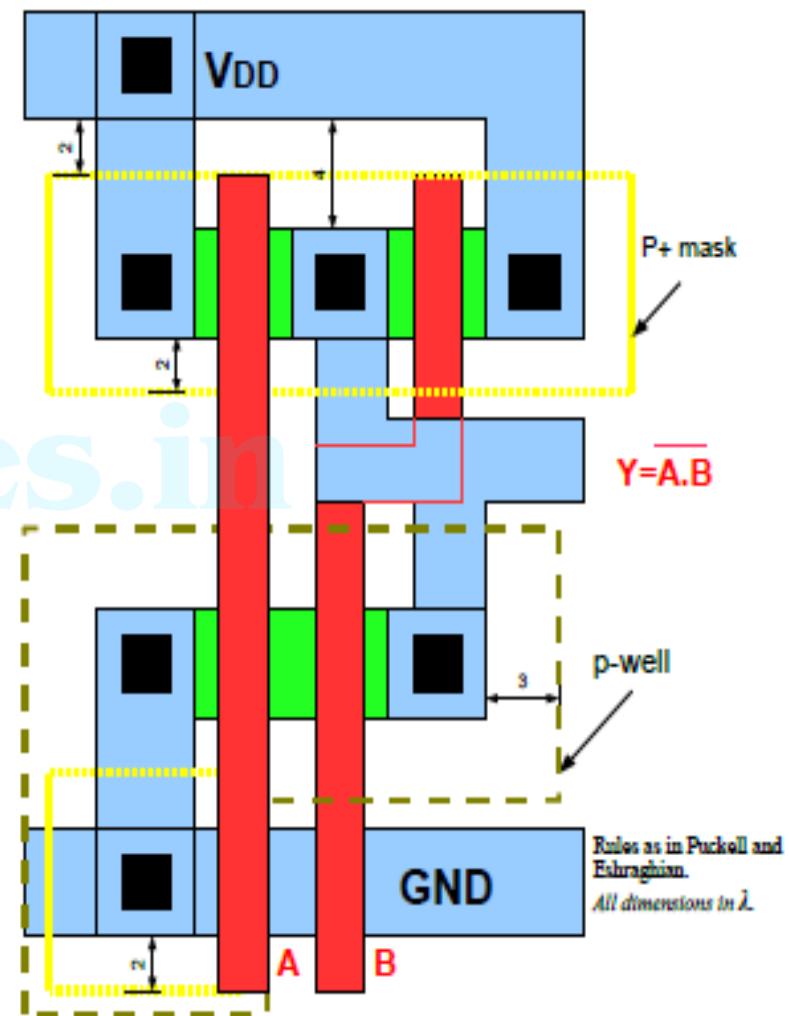
(OR)



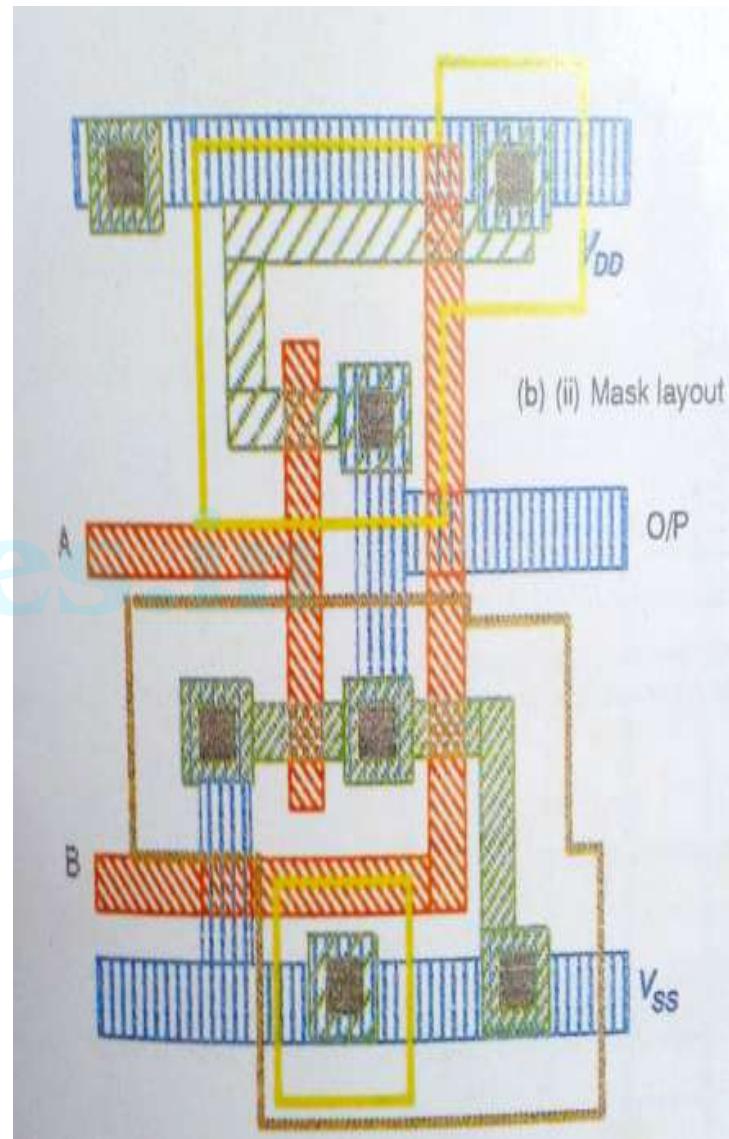
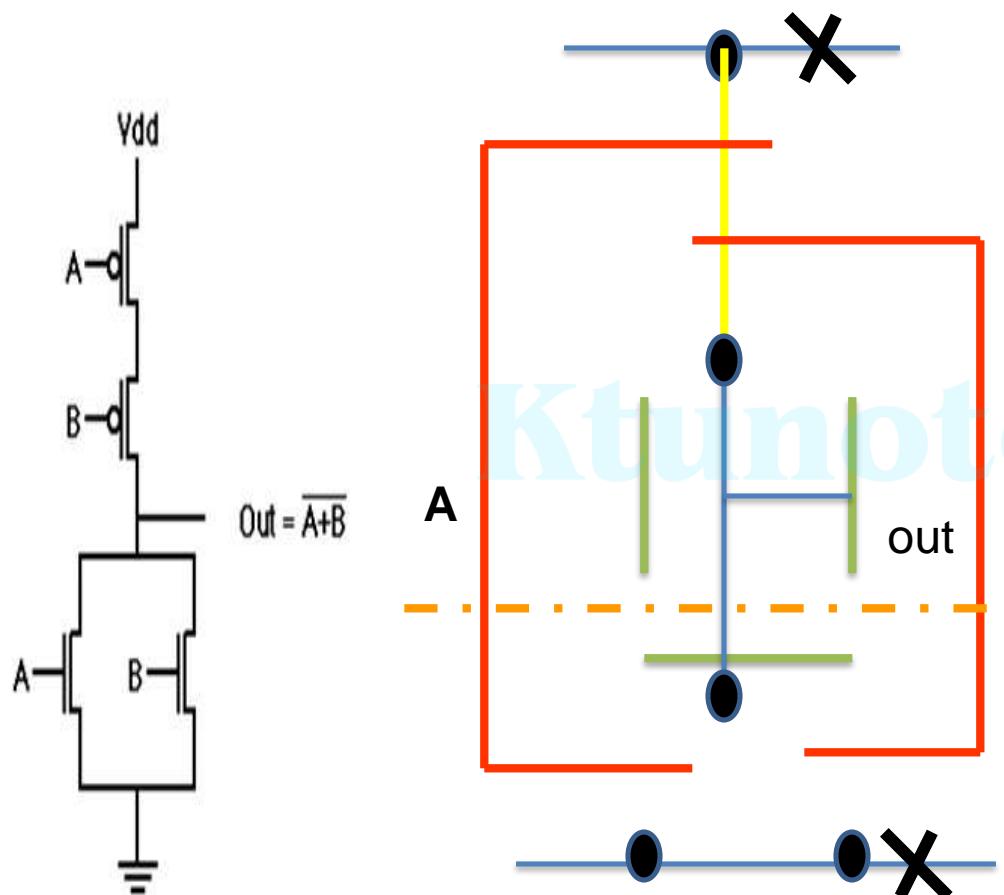
2 input NAND



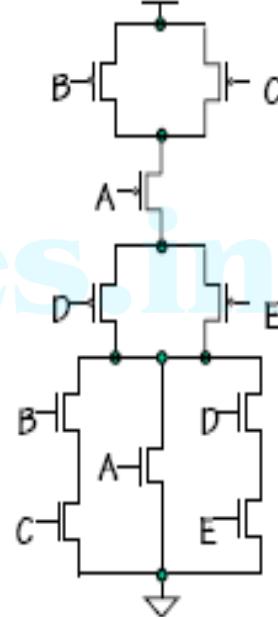
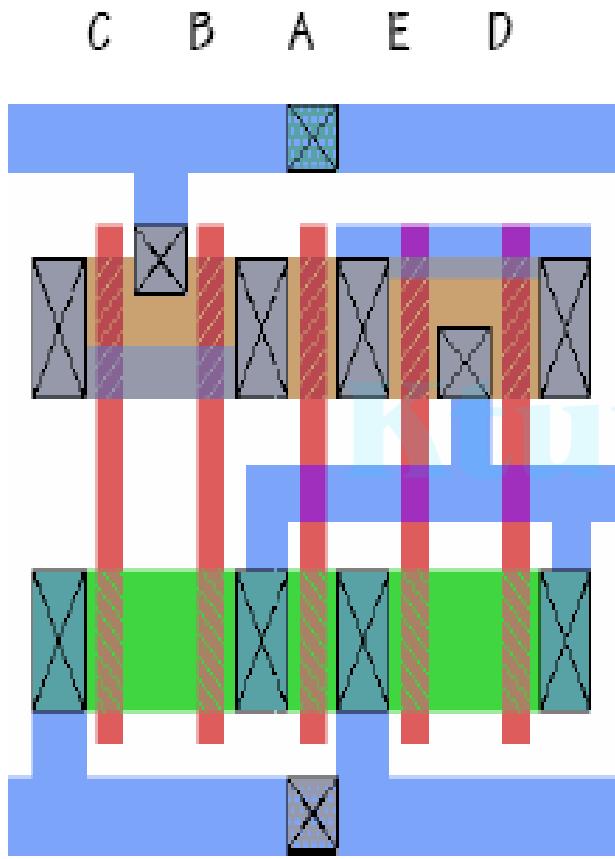
Two-Input P-Well NAND. Layed out by:
Turki Almadhi, College of Engineering,
KSU, Riyadh, Saudi Arabia.



2 input NOR gate



Identify the Circuit



Design Rules

Ktunotes.in

Design Rules

- Allow ready translation of circuit concepts(stick diagram or symbolic form) in to actual geometry in silicon.
- Interface between the circuit designer and process engineer
- Guidelines for constructing process masks
- Mead and Conway developed set of design rules known as **scalable lambda based design rules**
- Unit dimension: minimum line width
 - scalable design rules: lambda parameter
 - absolute dimensions: **micron rules**
- Rules constructed to ensure that design works even when small fab errors (within some tolerance) occur
- A complete set includes
 - intra-layer: relations between objects in the same layer
 - inter-layer: relations between objects on different layers

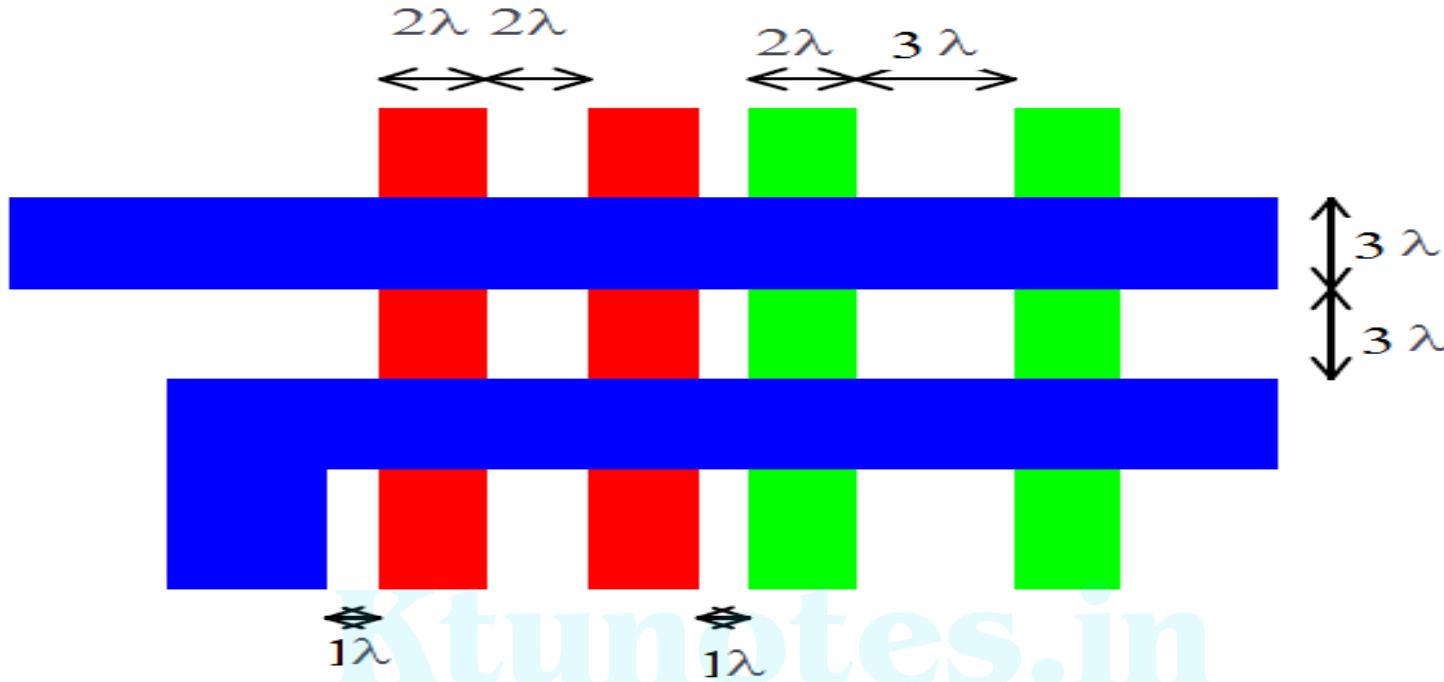
Design rules

- Circuit designer needs to reduce the size but process engineers needs a controllable and reproducible fabrication
- So we needs design rules to get more yield.
- Design rules can never be met exactly at the wafer level because physical nature of semiconductor causes some variations.

λ Based Design Rules

- ▶ Chips are specified with set of masks
- ▶ All paths in all layers will dimensioned in λ units
- ▶ λ can be allocated an appropriate value compactable with the feature size of the fabrication process
- ▶ Minimum dimensions of masks determine transistor size (and hence speed, cost, and power)
- ▶ Feature size f = distance between source and drain
 - ▶ Set by minimum width of polysilicon
- ▶ Feature size improves 30% every 3 years or so
- ▶ Normalize for feature size when describing design rules
- ▶ Express rules in terms of $\lambda = f/2$
 - ▶ E.g. $\lambda = 0.3 \mu\text{m}$ in $0.6 \mu\text{m}$ process

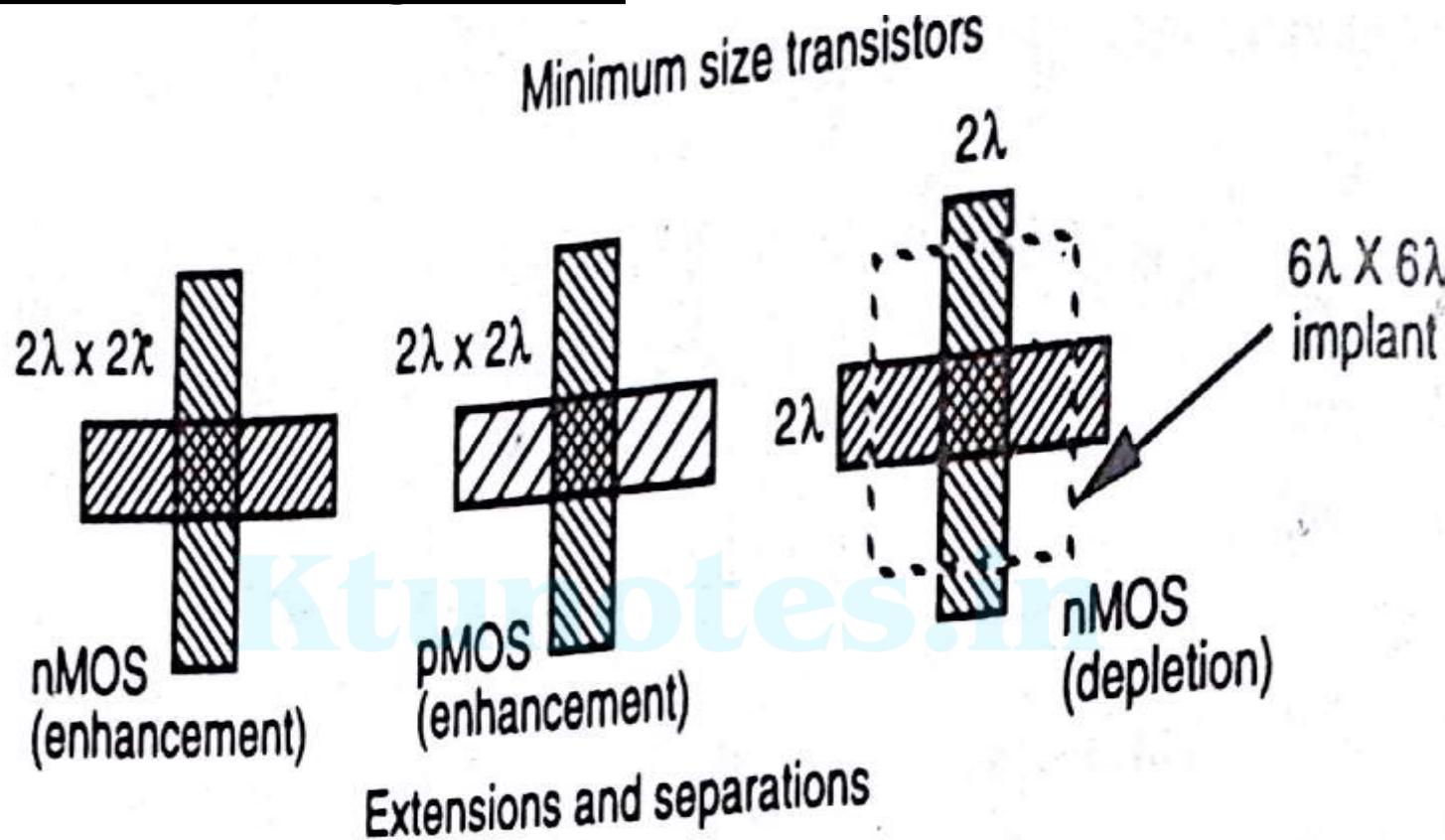
DESIGN RULE FOR WIRES & metal layer (nMOS &CMOS)



- Minimum polysilicon width 2λ
- Minimum polysilicon separation 2λ .
- Minimum diffusion width 2λ .
- Minimum diffusion separation 3λ .
- Minimum polysilicon separation from diffusion 1λ .
- Minimum metal width 3λ
- Minimum metal separation 3λ .
- Minimum polysilicon separation from metal 1λ (where possible).

Transistor design rules

nMOS,pMOS and CMOS)

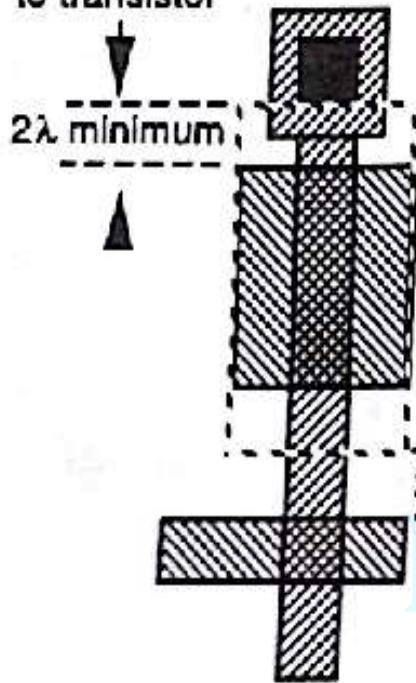


Key:

	Polysilicon		n-diffusion		p-diffusion		Transistor channel (polysilicon over thinox)
--	-------------	--	-------------	--	-------------	--	---

- Minimum transistor size 2λ square (essentially because of minimum track widths for diffusion and polysilicon).

Separation from contact cut to transistor



Key:

Polysilicon

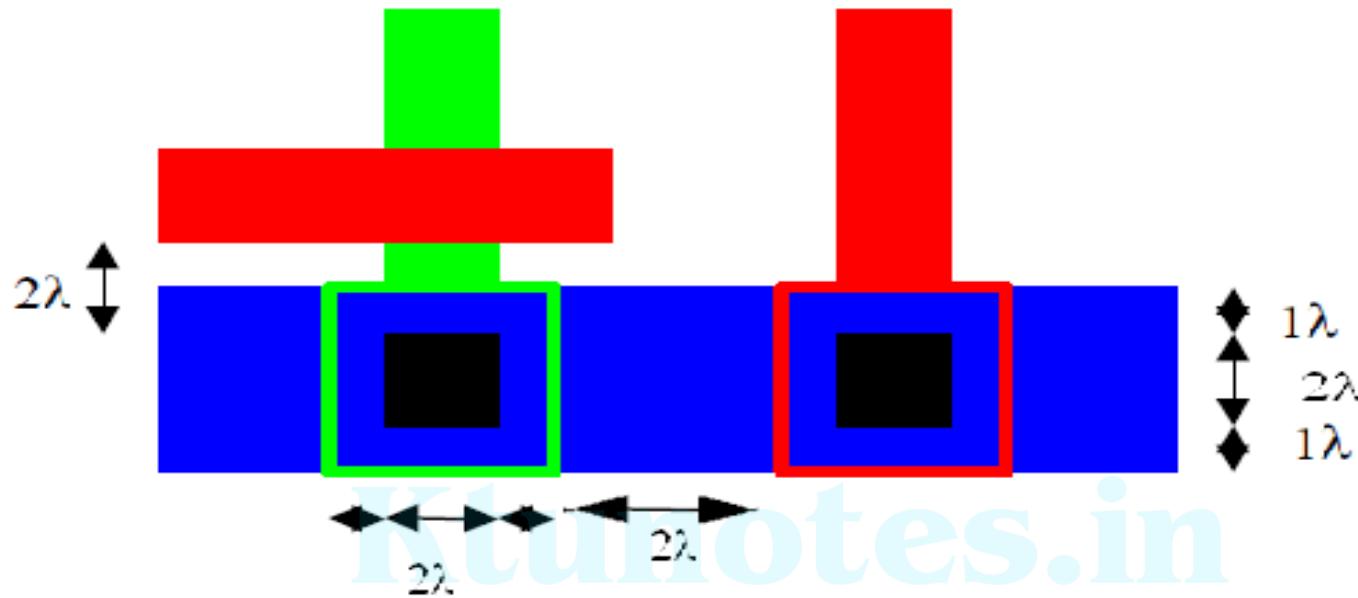
n-diffusion

p-diffusion

Transistor channel (polysilicon over thinox)

- Polysilicon must continue past transistor for at least 2λ .
- Diffusion must continue around transistor for at least 2λ .
- Implant must extend for 2λ around a depletion transistor.
- Minimum separation between implant and enhancement transistor 2λ

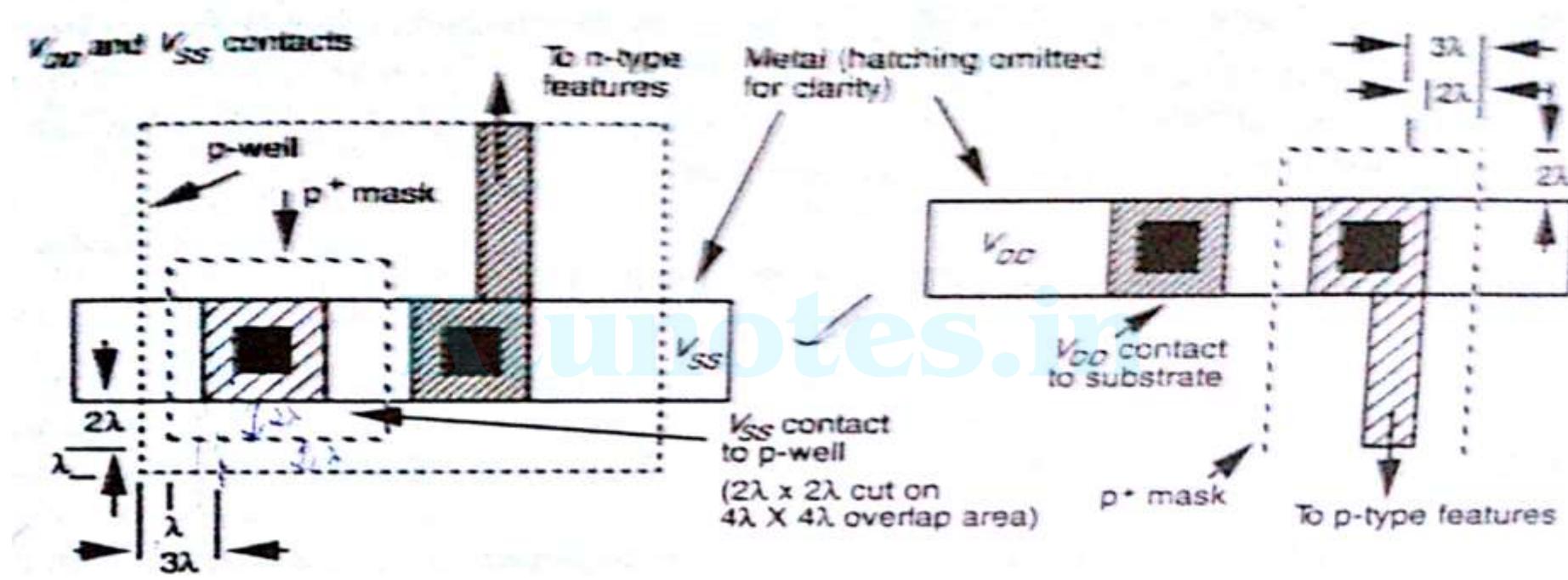
CONTACT (nMOS&CMOS)



- Minimum contact size 2λ square.
- Both materials must extend for 1λ around the contact.
- Minimum separation between contacts 2λ .
- Minimum separation between contact and transistor 2λ .

λ based design rule for p-well CMOS process

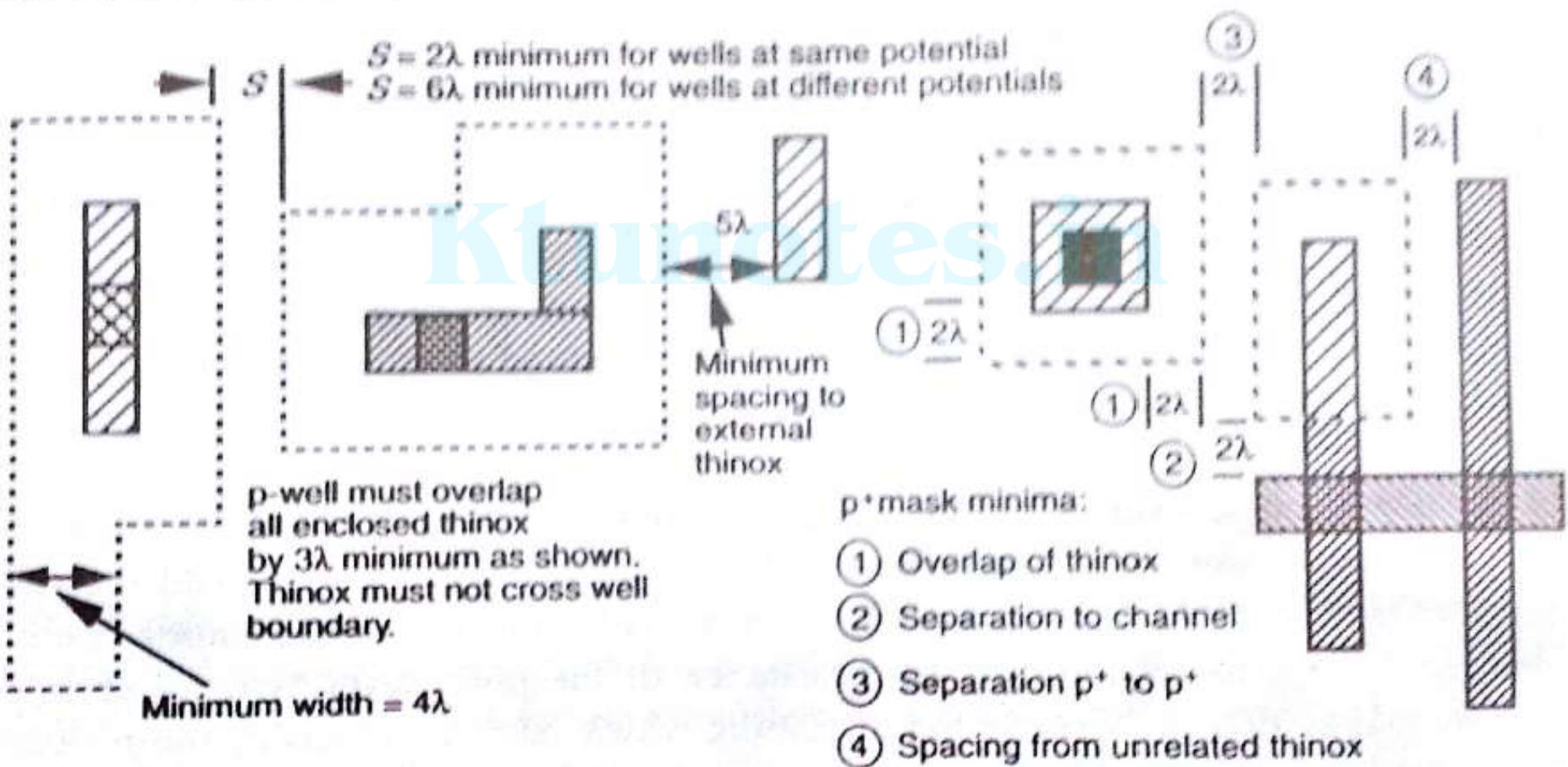
VDD and VSS contact



Conti.....

P-well and p+ mask

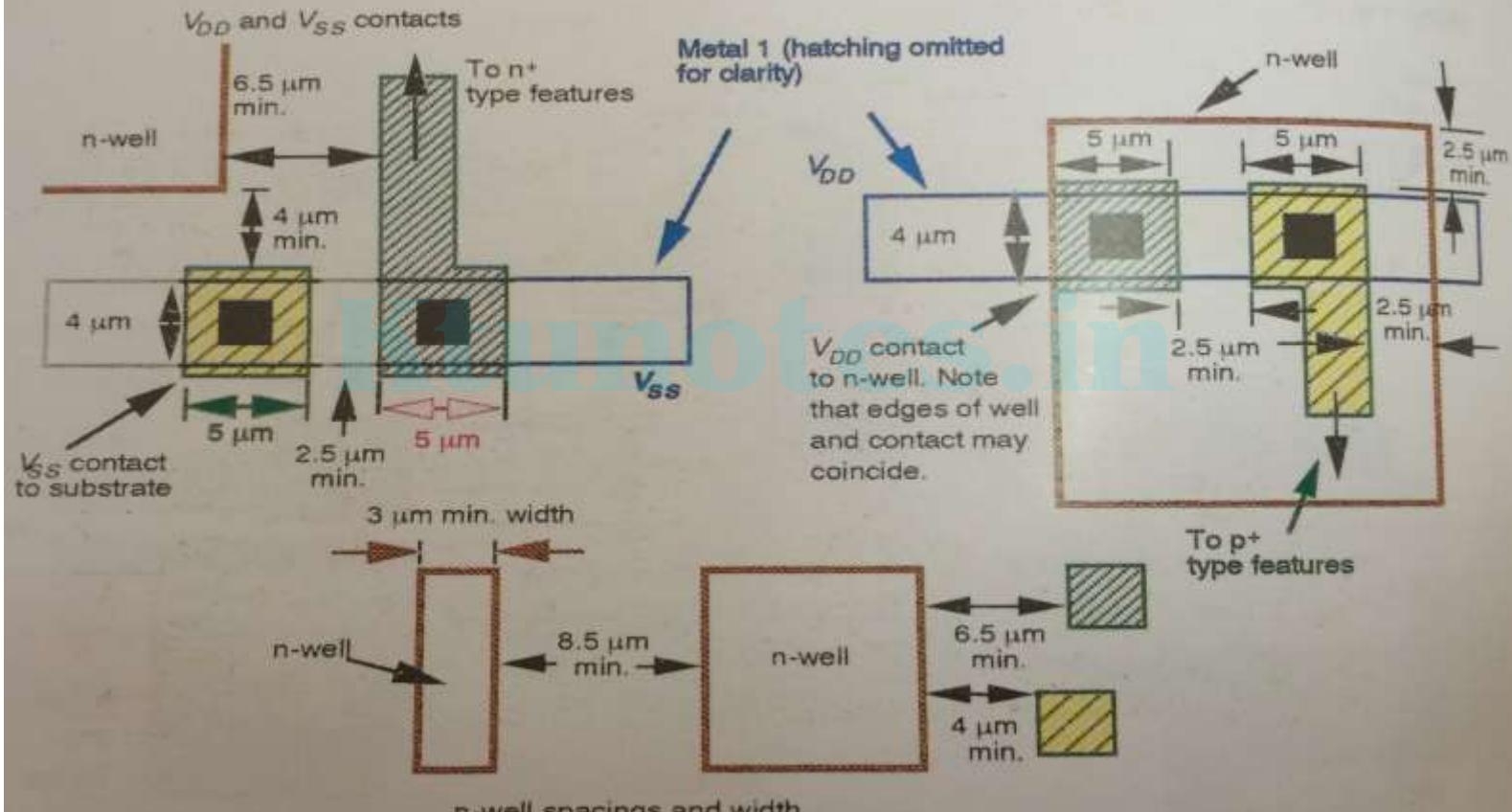
p-well and p+ mask rules



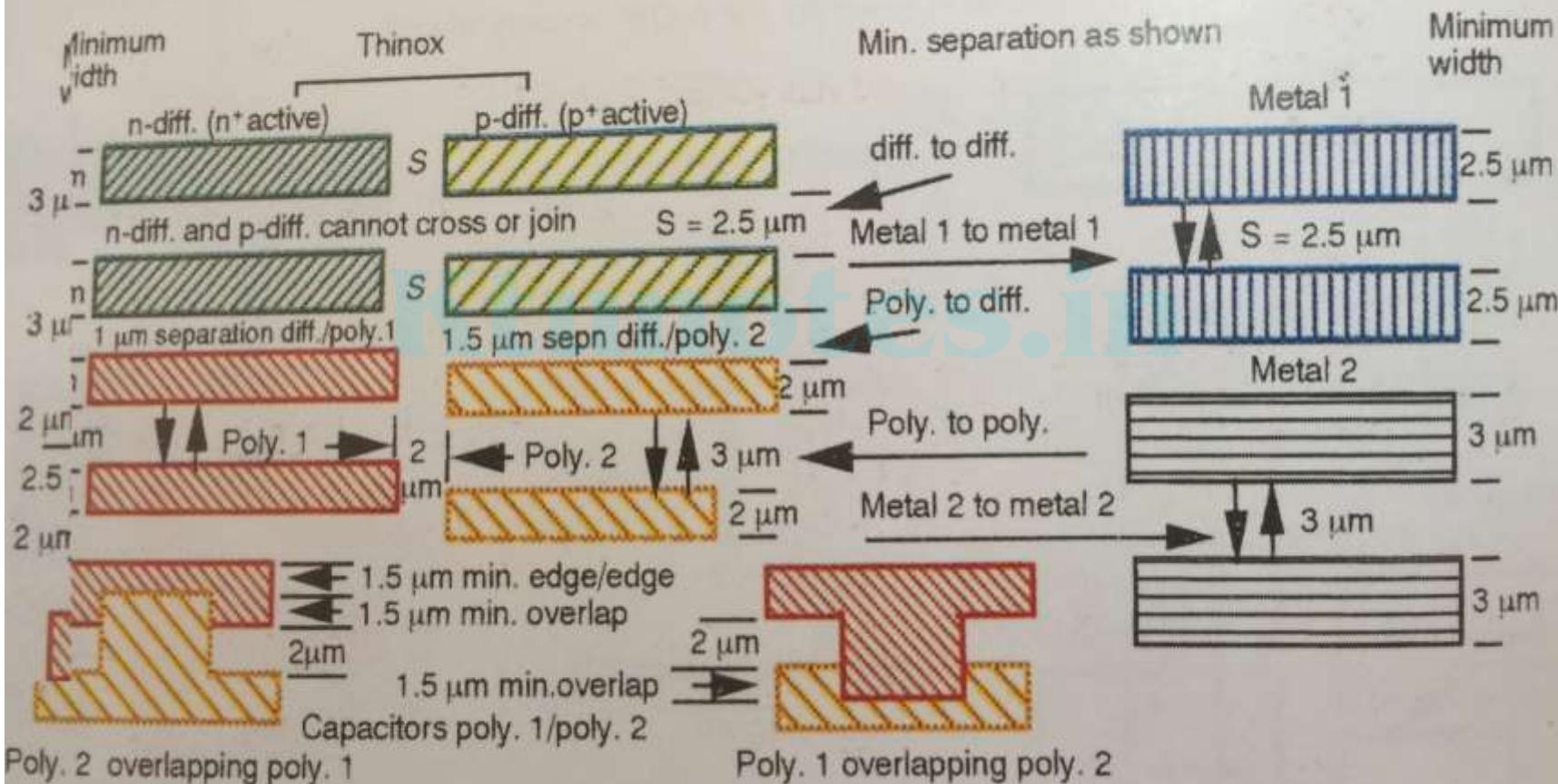
Micron rules

- In order to accomadate the additional feauters present in the technology,it is necessary to extend the range of colour and monochrome encodings previously used for double metal p-well cmos
- Compactable with already described, but as far as colour assignment the following extensions/additions are made
- N well- brown(same as pwell)
- Poly 1-red
- Poly 2-orange
- N diffusion(n-active) –green
- P –diffusion(p-active) –yellow
- Hatching which is compactable with monochrome encoding ,may also added to color mask encoding ,to distinguish underlying layers and to allow for ready copying of color diagram on monochrome copying mechine
- For Bicmos following are added
- Buried n+ subcollector –pale green
- P-base -pink

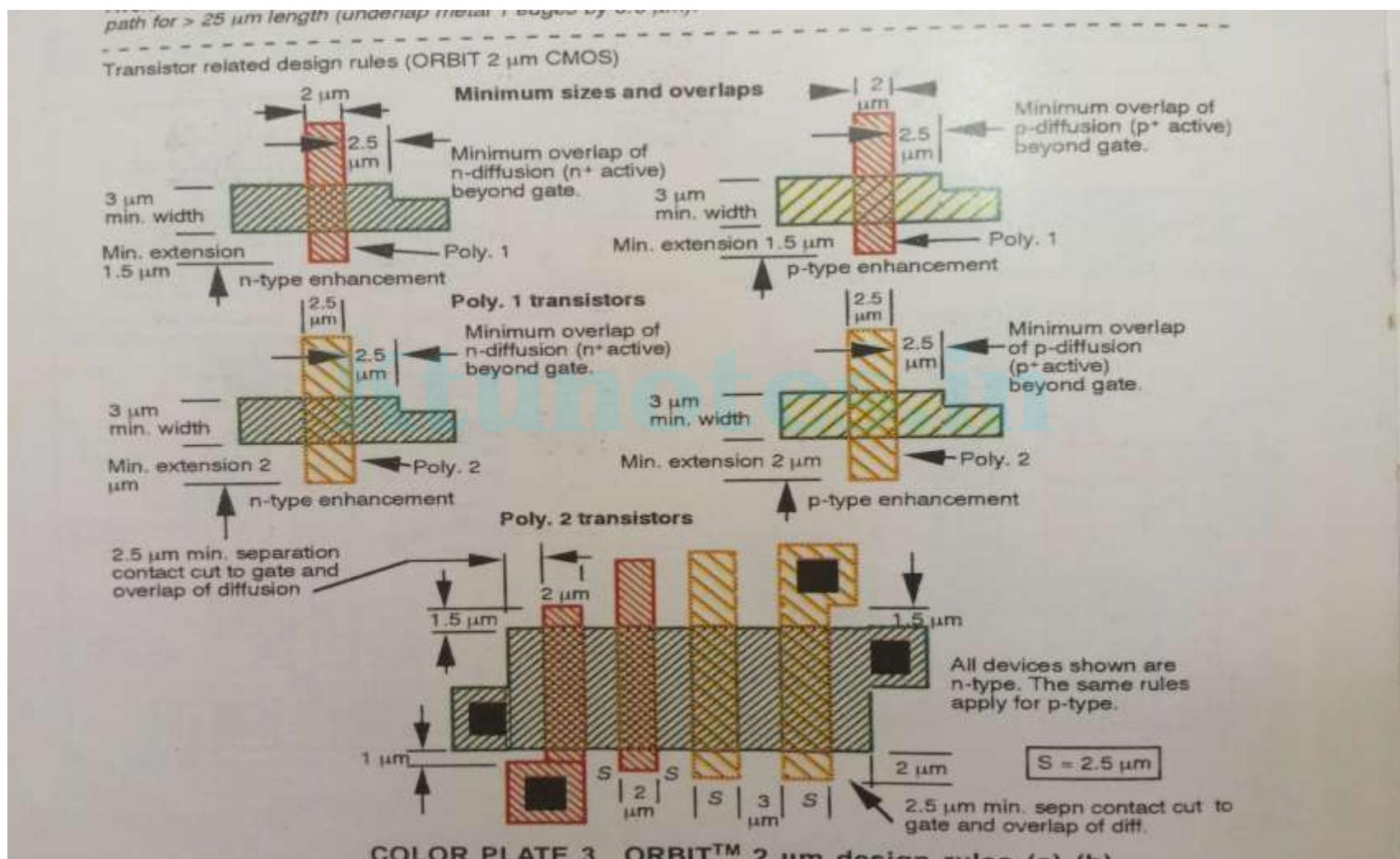
Rules for n-well and V_{DD} and V_{SS} contacts (ORBIT 2 μm CMOS process)



Design rules for wires (interconnects) (ORBIT 2 μm CMOS)

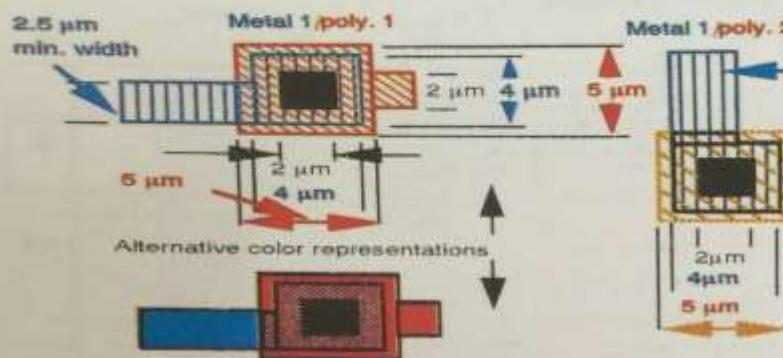


Otherwise poly. 2 must not be coincident with poly. 1

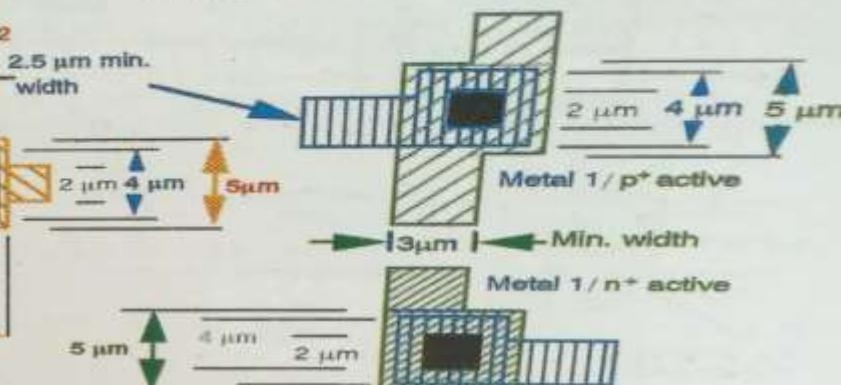


Rules for contacts and vias (ORBIT™ 2 μm design rules)

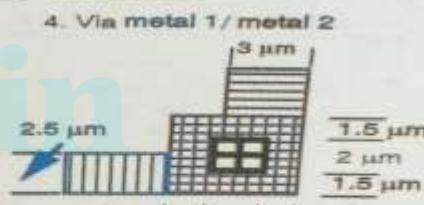
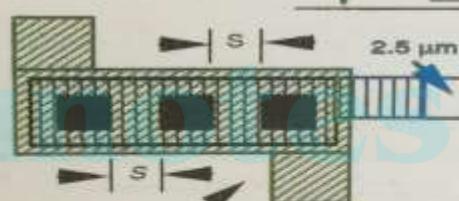
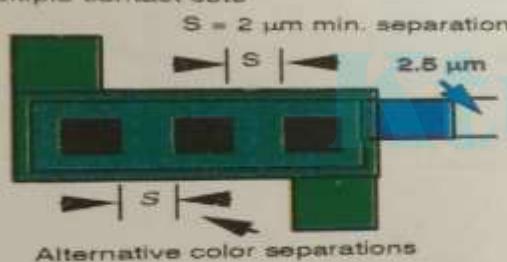
1. Metal 1 to poly. 1 or poly. 2



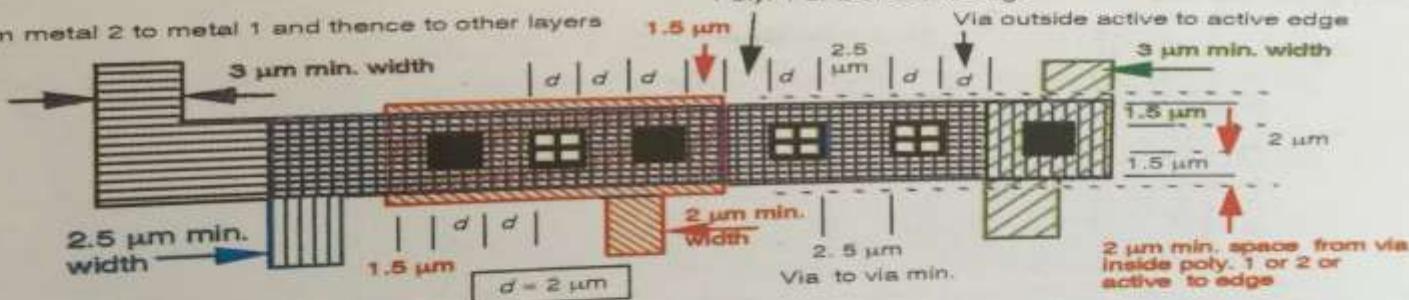
2. Metal 1 to n⁺ or p⁺ active (diff.)



3. Multiple contact cuts



5. Vias from metal 2 to metal 1 and thence to other layers

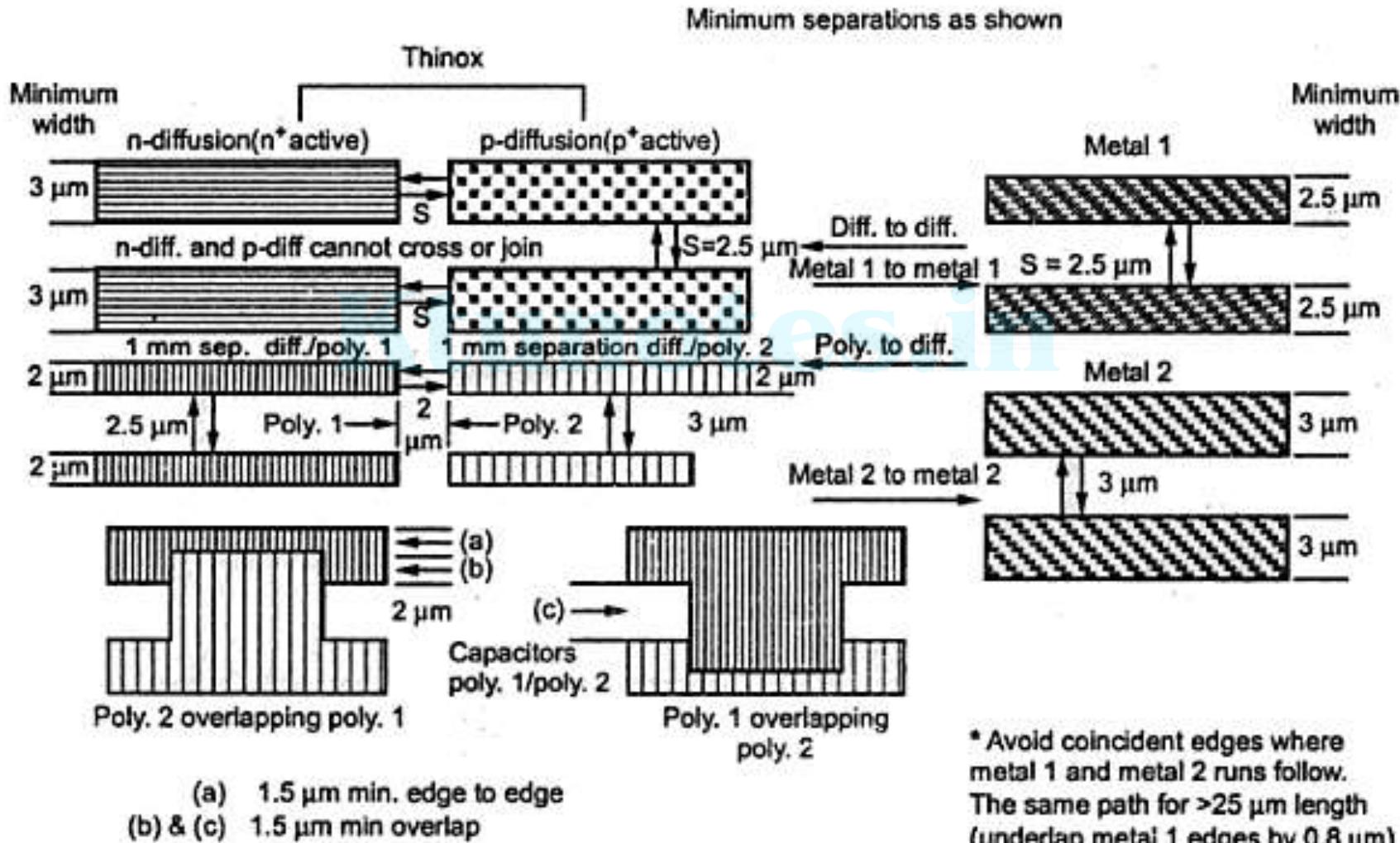


Note that vias must not be placed over contacts.

COLOR PLATE 4 ORBIT™ 2 μm design rules (c).

2 micrometer design rules

Design rule for wires



Please refer the text for more details about the design rules....

Text :Basic VLSI Design

Author:Douglas Apucknell & Kamran Eshraghian
[Ktunotes.in](http://www.ktunotes.in)

Page No: color plate section 3,4,5,6

Text:VLSI Technology

Author:Sujatha Pandey and Manoj Pandey

Page No.:5.36 to 5.44