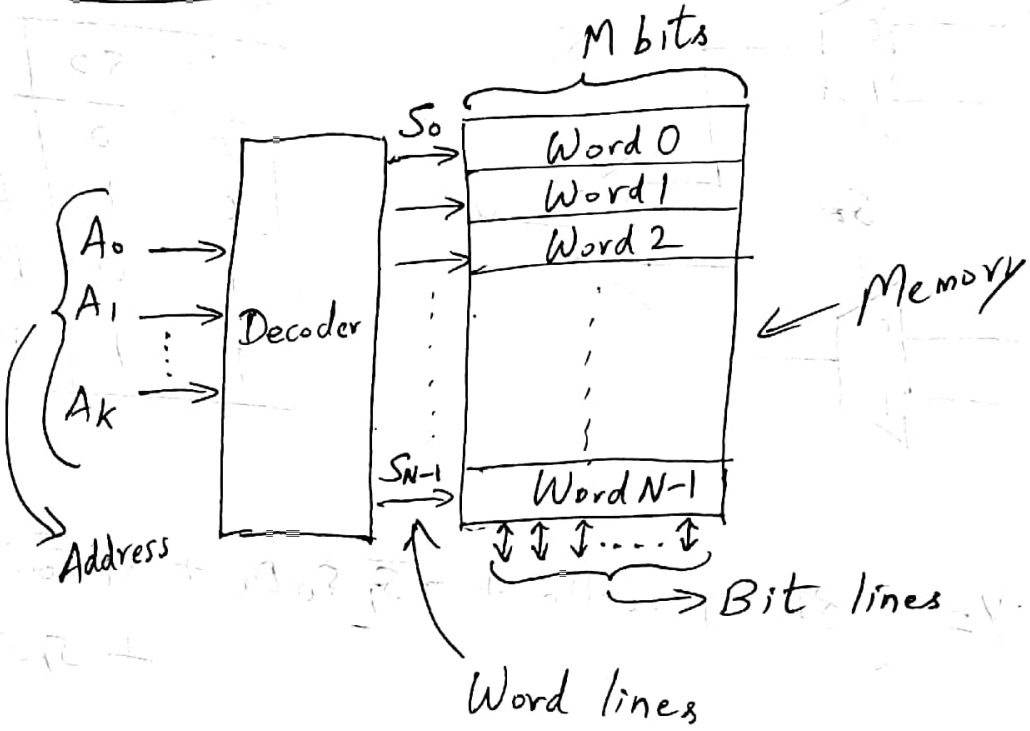
MODULE - 5

Memory organization

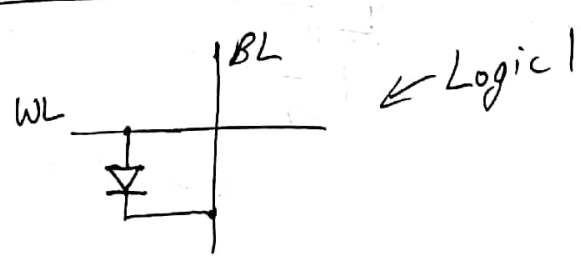


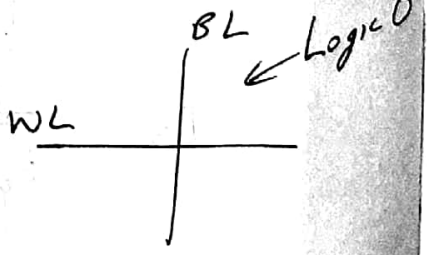
→ Word lines are used to select one particular row (or word) in memory.

→ While read operation, the contents of selected word will be available on bit lines.

Read Only Memory (ROM)

Implementation using diode cell





→ BL is resistively clamped to ground (pulled low to GND using resistor).

→ WL & BL are not interconnected

→ If no diode is present at a cell, then BL is low (Logic 0).

→ If diode is present, then when WL is activated with high voltage V_{WL}, then diode turns on & $V_{WL} - V_{D(on)}$ appears at BL. Thus BL becomes high (Logic 1).

→ These logic values can be read out using bit lines.

→ In ROM, during manufacturing itself locations of diodes are designed depending upon whether a 1 or 0 is needed at a cell.

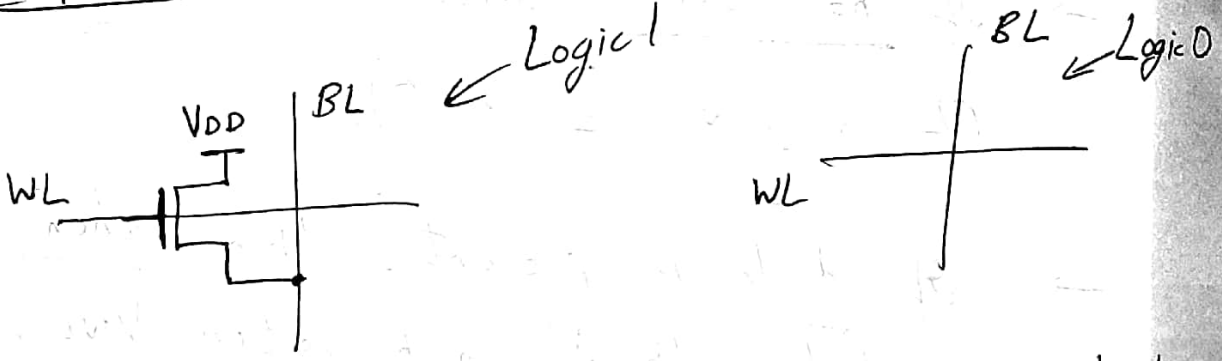
Such ROMs with fixed programs are useful for applications like washing machines, calculators, etc.

Disadvantage of diode cell:-

→ Current required to charge bit line capacitance has to be provided by word line drivers. So it is practical only for small memories, where bit line capacitance is small.

ROM cell implementation using MOSFETs

Option 1 :-



→ If a word is selected, WL turns high, which turns on nMOS & thus BL becomes high. (Logic 1).

→ If nMOS is not present, BL is 0, since it is pulled low to ground through a resistor by default.

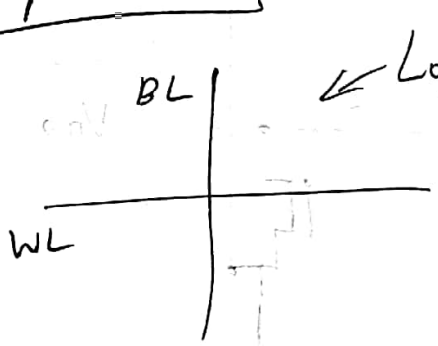
→ Advantage:-

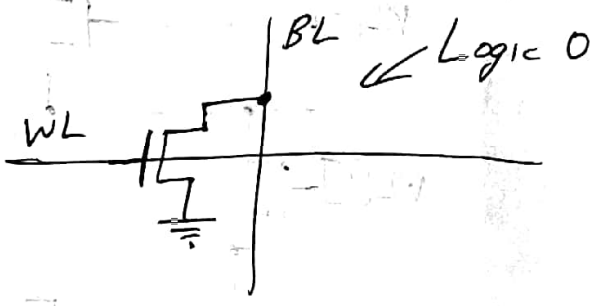
Bit lines are charged from VDD line instead of WL drivers.

→ Disadvantage:

More chip area required to provide additional VDD lines, contact for each ~~word~~ cell.

Option 2 :-





→ BL is pulled up to V_{DD} by default. So if nMOS is absent, then BL is logic 1

→ Upon activating nMOS, BL gets connected to ground through nMOS & becomes logic 0.

→ Options 1 & 2 have similar advantages & disadvantages.

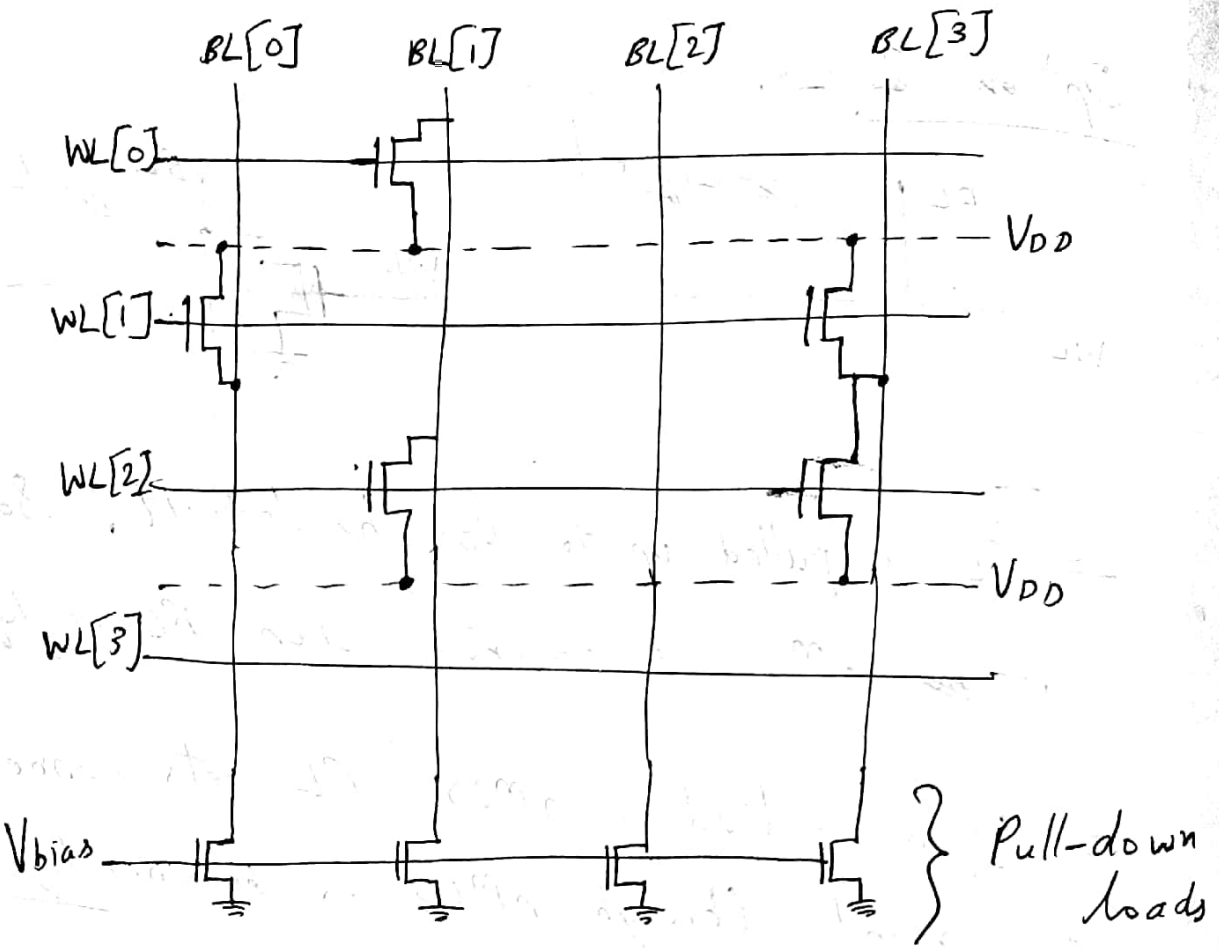
4x4 OR ROM cell array

→ 4 word lines & 4 bit lines.

→ nMOS is connected to V_{DD} to represent logic 1 in a cell.

→ Absence of nMOS represents logic 0.

→ Bit lines are pulled down by default.



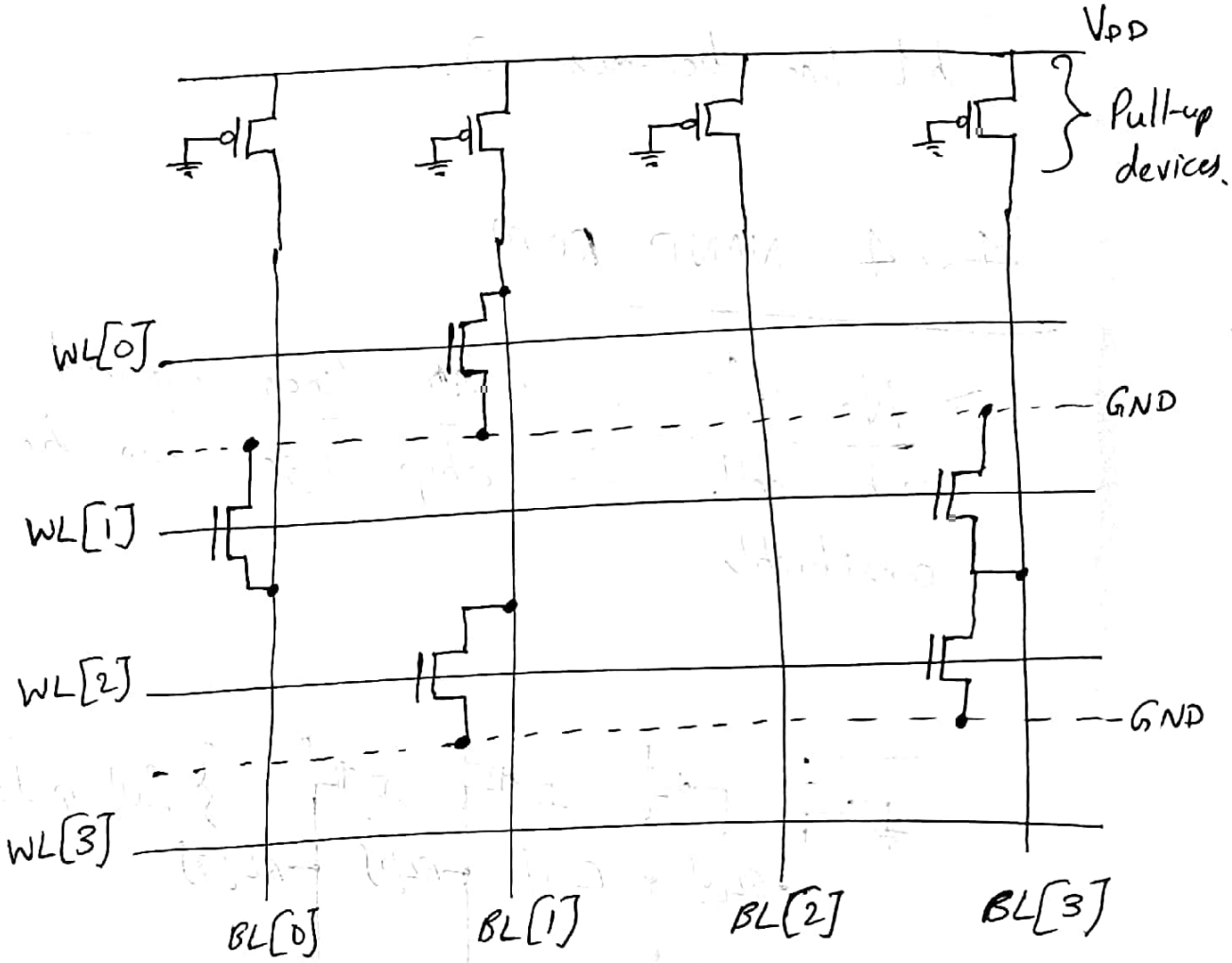
Contents of memory cell (MSB at left):

Word 0 :-	0	0	1	0
Word 1 :-	1	0	0	1
Word 2 :-	1	0	1	0
Word 3 :-	0	0	0	0

→ V_{DD} lines are shared by two words.

→ It is called OR ROM because if any nMOS in a bit line is on, the the whole bit lines becomes 1.

4x4 NOR ROM cell array



→ Bit lines are pulled up by default.

→ Presence of nMOS indicate Logic 0.

→ Absence of nMOS indicate Logic 1

→ nMOS are connected to GND lines.

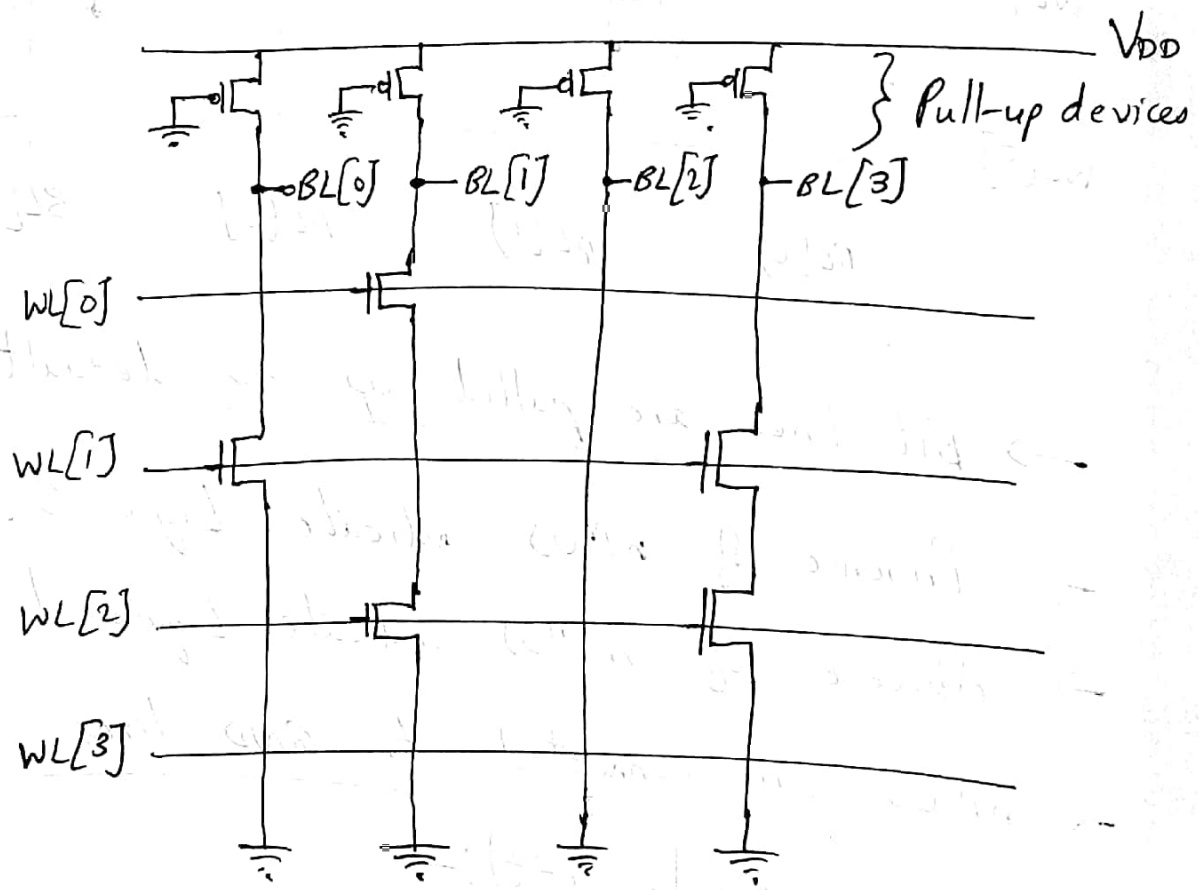
Contents (MSB at left):-

Word 0:	1101
" 1:	0110
" 2:	0101
" 3:	1111

→ It is called NOR ROM because if any nMOS on a bit line is ON, then entire bit line becomes 0.

4×4 NAND ROM

→ No V_{DD} or GND lines required for each cell. So chip size can be reduced considerably



→ All nMOS on a bit line are connected in series

→ Pull-up is given to bit lines.

→ For a bit line to become 0, all transistors on the bit line must be ON. So this configuration is called as NAND ROM.

→ Word lines are operated in reverse logic. ie selected word line will be 0 & others will be 1.

→ If no nMOS is present in a cell, then value will be logic 0. (Since all other transistors in non-selected words on that bit line will be on due to default high values given).

→ If nMOS is present, then due to word line value of 0, nMOS is off. So bit line value is 1 (due to pull-up).

Contents (MSB at left):

Word 0: 0 0 1 0
" 1: 1 0 0 1
" 2: 1 0 1 0
" 3: 0 0 0 0