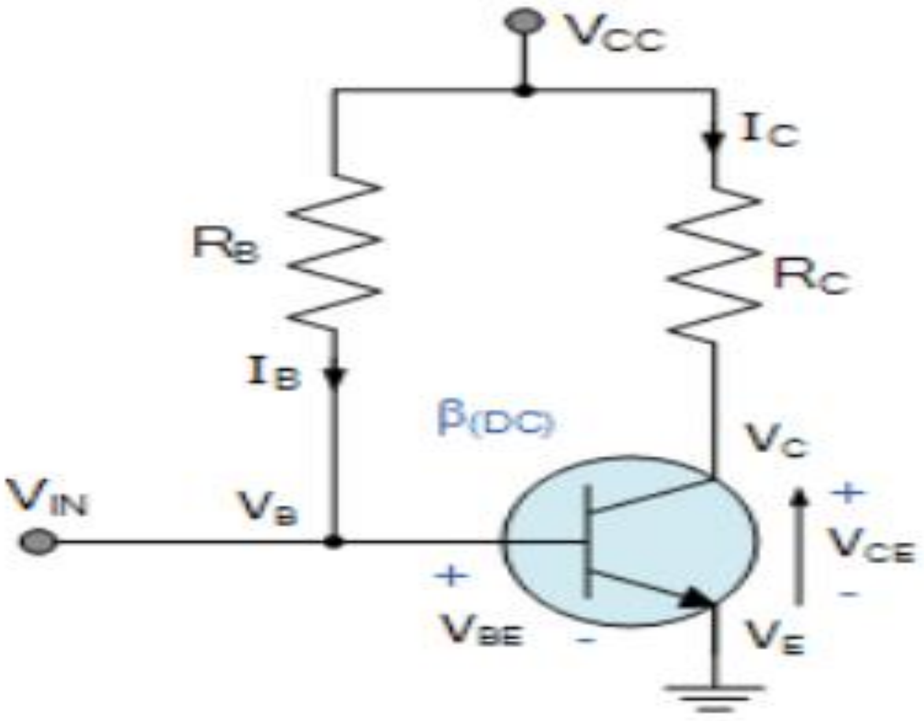
BIASING CIRCUITS

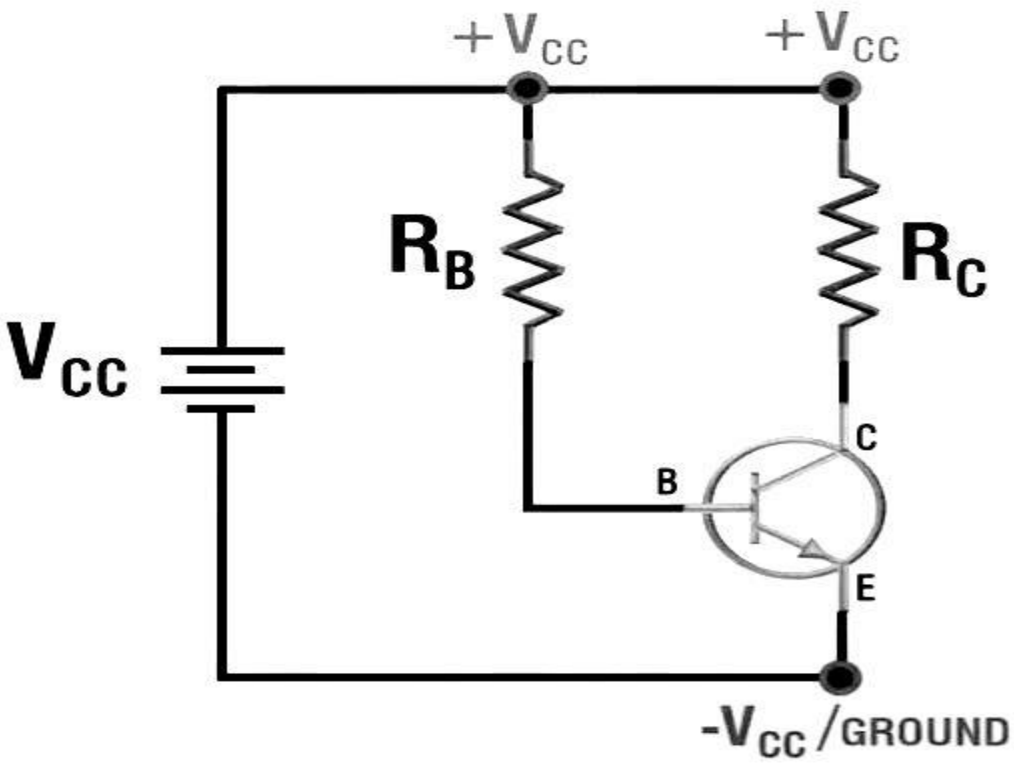
BIASING CIRCUITS

- FIXED BIAS CIRCUIT
- COLLECTOR TO BASE BIAS CIRCUIT
- VOLTAGE DIVIDER BIAS CIRCUIT

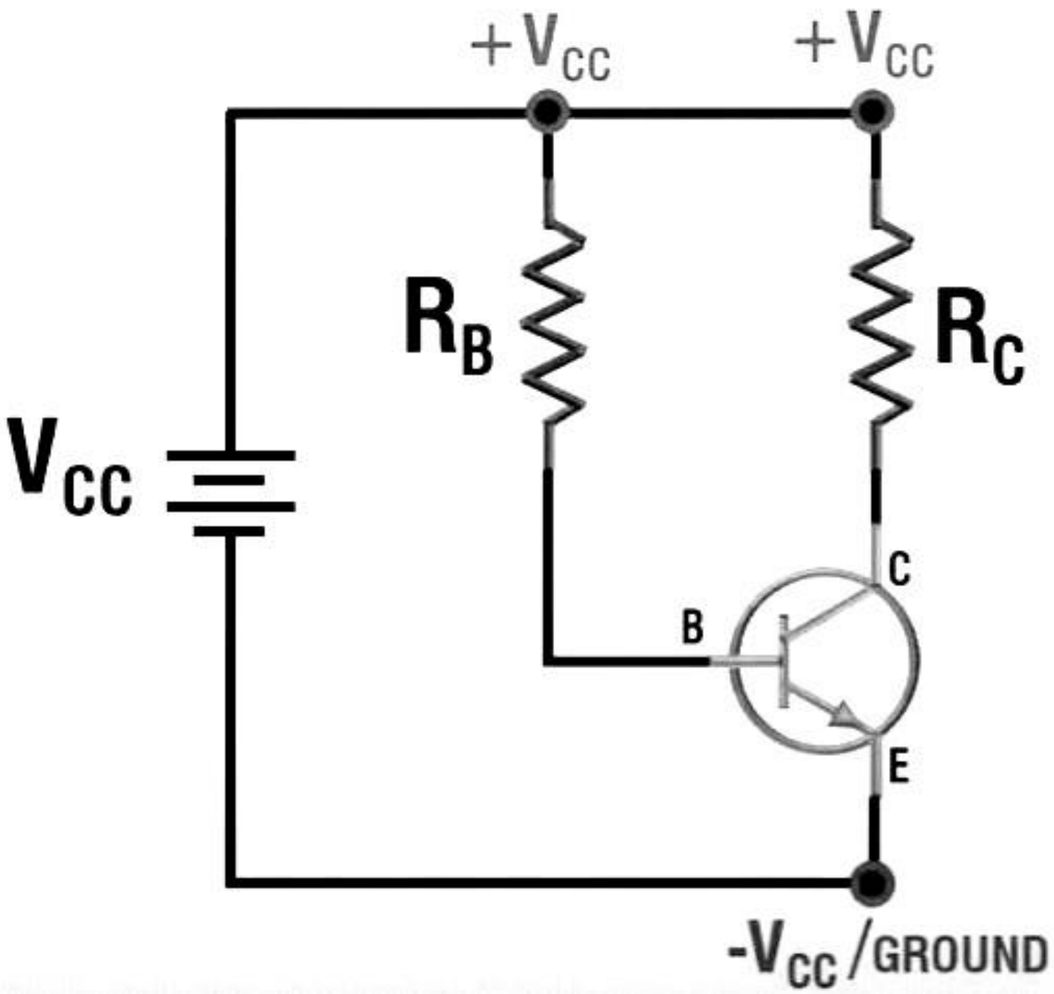
FIXED BIAS CIRCUIT

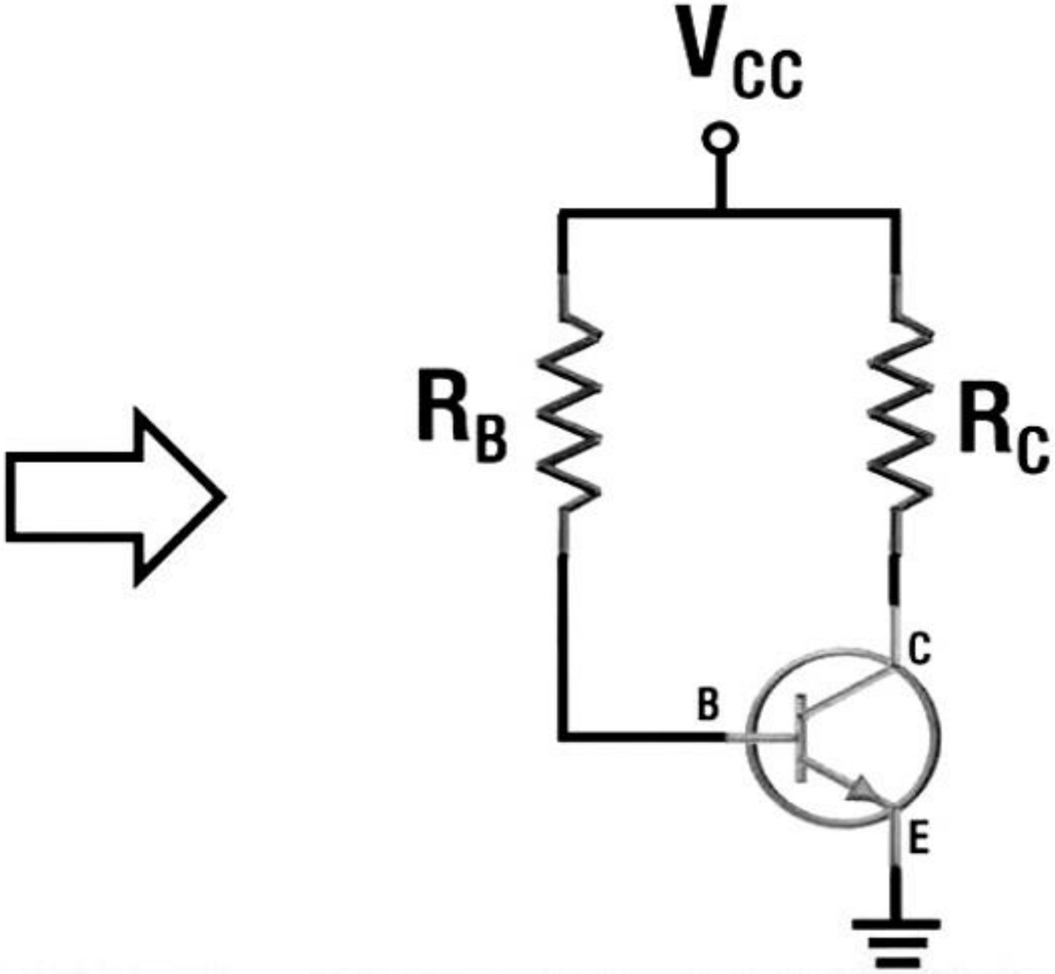
- Simplest DC bias configuration.
- Transistors base current, I_B remains constant for given values of V_{CC}, and therefore the transistors operating point must also remain fixed.
- Positive terminal of Battery is connected to Collector and Base Resistor.



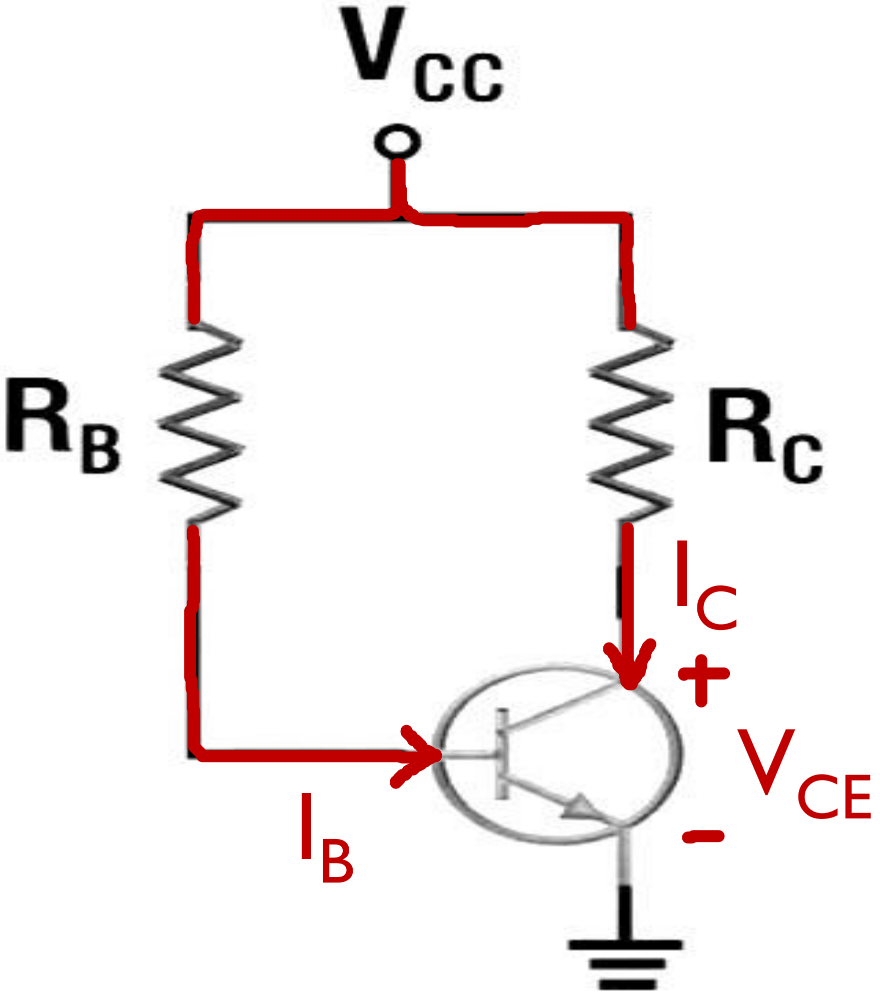


FIXED BIAS CIRCUIT





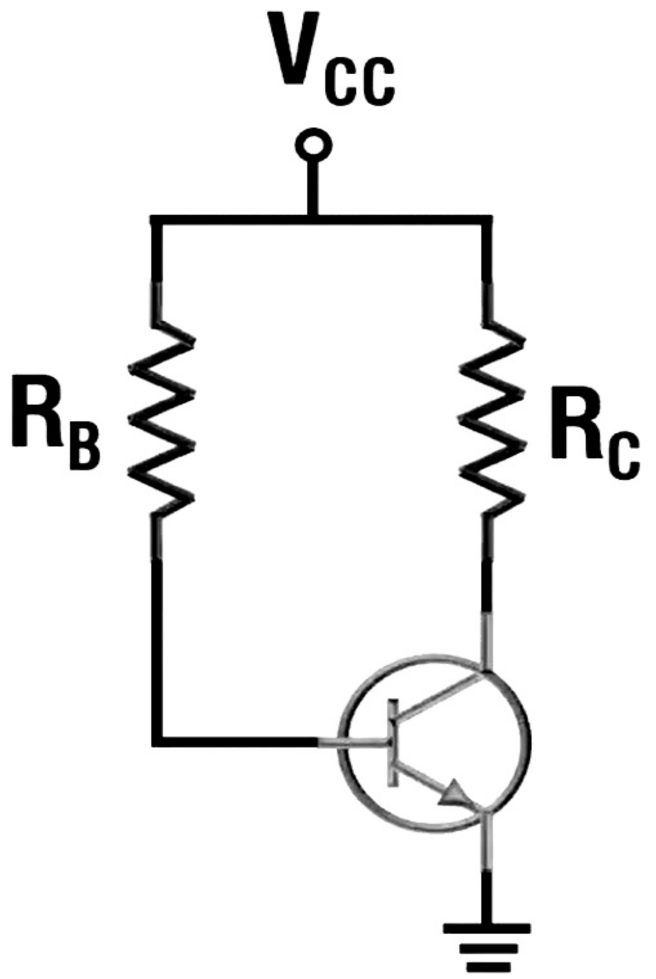
FIXED BIAS CIRCUIT - ANALYSIS



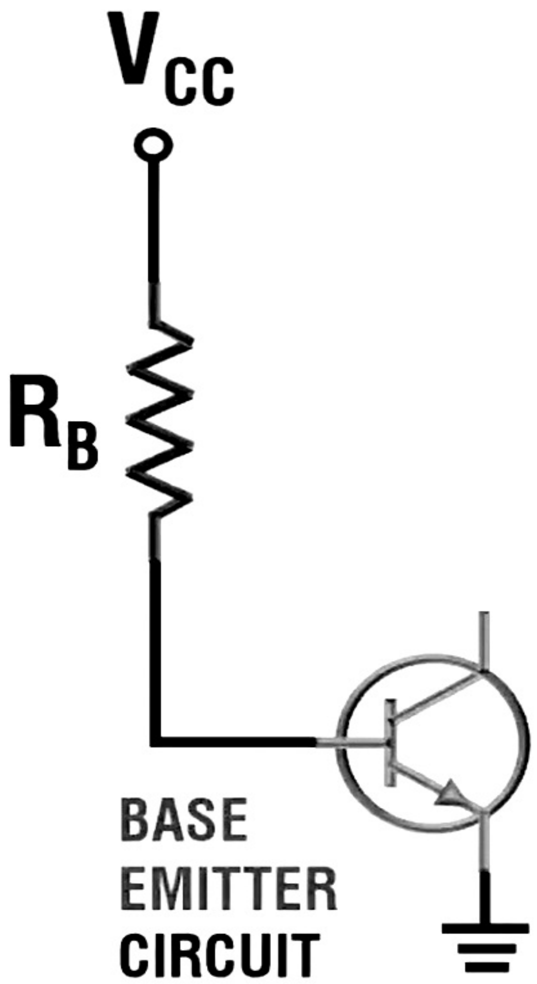
- I_B
- I_C
- V_{CE}

FIXED BIAS CIRCUIT - ANALYSIS

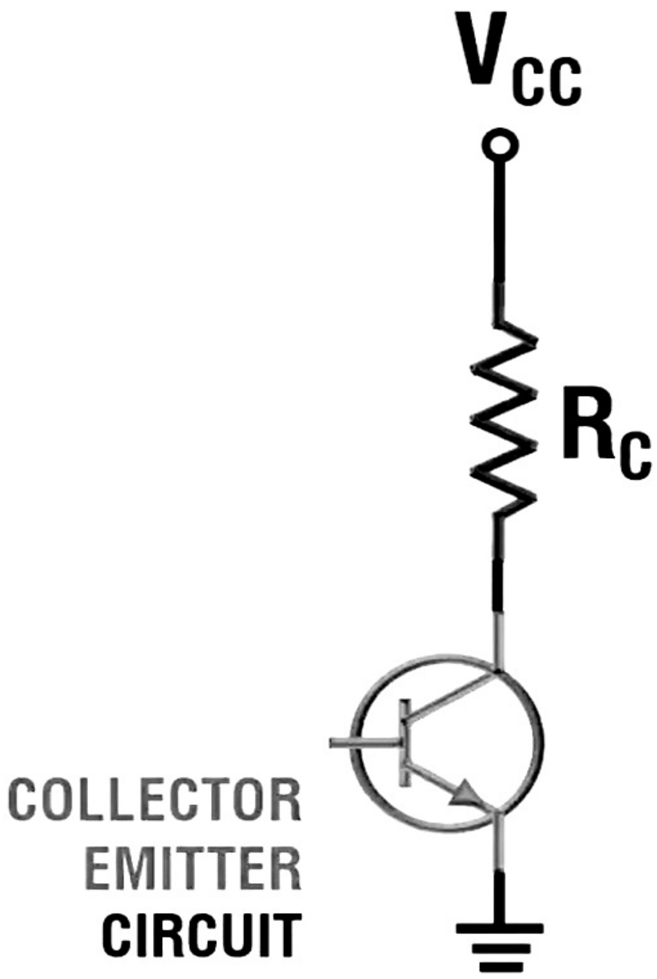
ANALYSIS



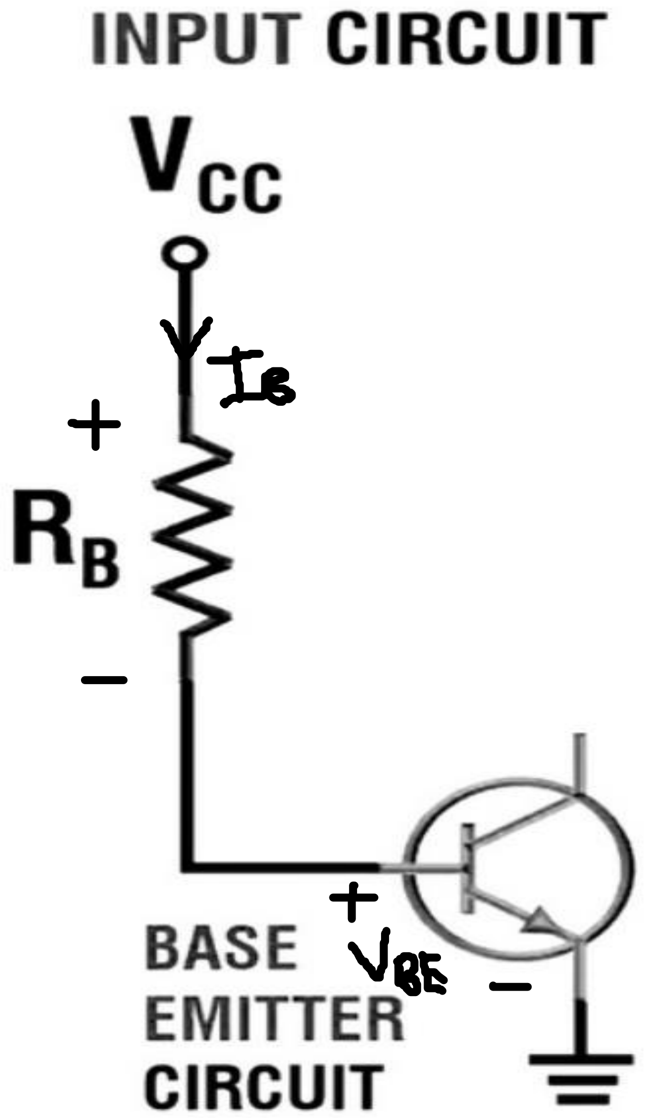
INPUT CIRCUIT



OUTPUT CIRCUIT



FIXED BIAS CIRCUIT - ANALYSIS



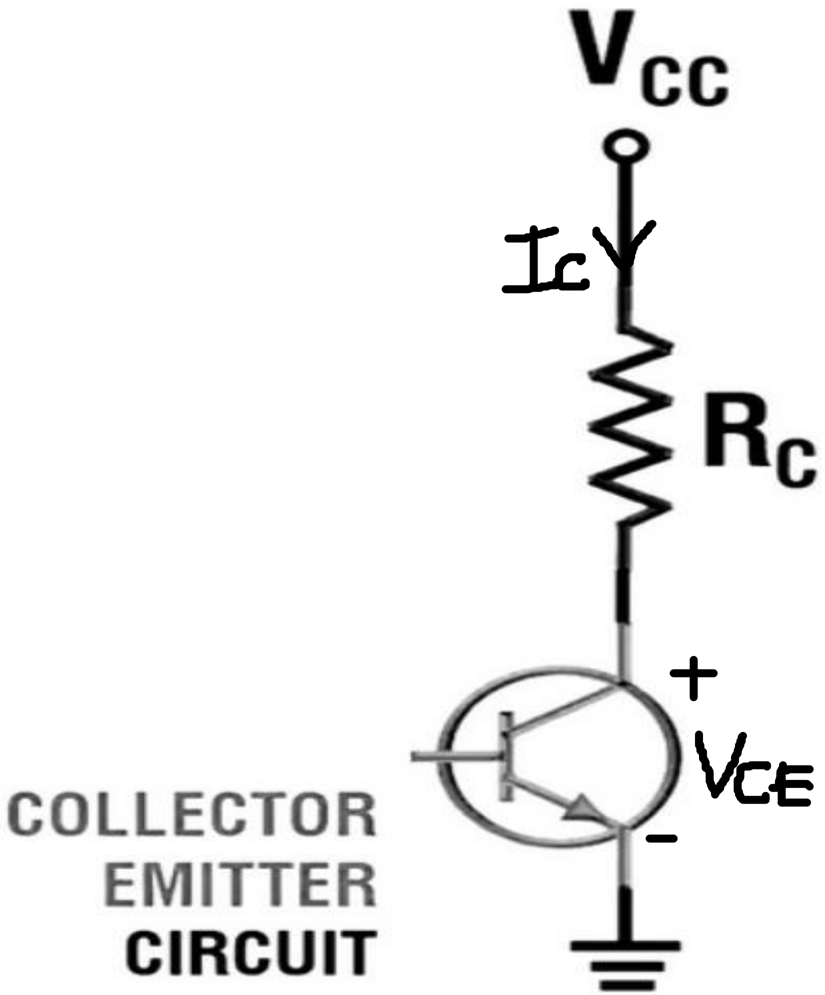
$$V_{cc} - I_B R_B - V_{BE} = 0$$

$$\boxed{I_B = \frac{V_{cc} - V_{BE}}{R_B}}$$

$$I_B \approx \frac{V_{CC}}{R_B}$$

FIXED BIAS CIRCUIT - ANALYSIS

OUTPUT CIRCUIT



$$V_{cc} - I_C R_C - V_{CE} = 0$$

$$\boxed{V_{CE} = V_{cc} - I_c Rc}$$

$$\boxed{Ic = \beta I_B}$$

$$\boxed{I_C = \frac{V_{cc} - V_{CE}}{R_C}}$$

$$\boxed{I_{C(sat)} = \frac{V_{cc}}{R_C}}$$

Given the fixed bias circuit with VCC = 12V, RB = 240 kΩ , RC = 2.2 kΩ and β = 75. Determine the values of operating point.

Equation for the input loop is:

$I_B = [V_{CC} - V_{BE}] / R_B$ where $V_{BE} = 0.7V$

$I_B = [12 – 0.7] / [240 * 10^3]$

$I_B = 47.08\mu A$

$I_C = \beta I_B = 75 * 47.08\mu A = 3.53mA$

$V_{CE} = V_{CC} – I_C R_C = 12 – ((3.53 * 10^{-3}) * (2.2 * 10^3)) = 4.23V$

Determine the Q-point values of IC and VCE for the circuit. Assume VCE = 8 V, RB = 360 kΩ and RC = 2 kΩ . β = 100 Construct the dc load line and plot the Q-point.

Equation for the input loop is:

$I_B = [V_{CC} - V_{BE}] / R_B$ where $V_{BE} = 0.7V$

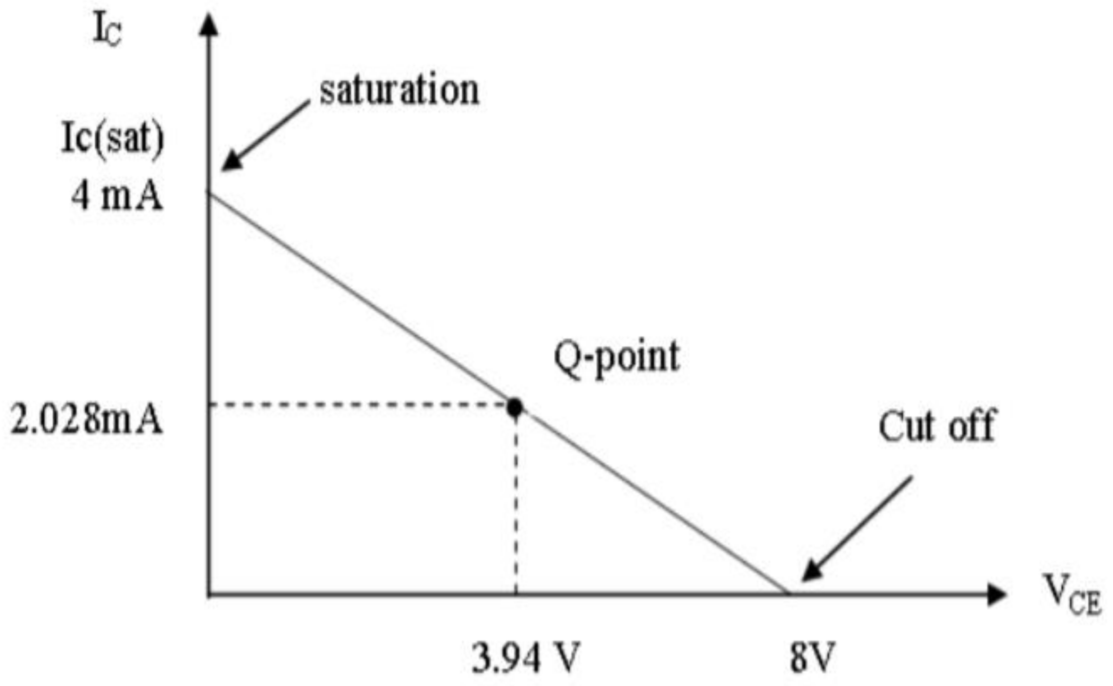
$I_B = [8V - 0.7V] / [360 * 10^3] = 20.28\mu A$

$I_C = \beta I_B = 100 * 20.28\mu A = 2.028mA$

$V_{CE} = V_{CC} - I_C R_C = 8V - (2.028mA * ((2 * 10^3))= 3.94V$

$V_{CE(sat)} = 0$; $I_C = \frac{V_{cc} - V_{CE}}{R_C} = \frac{V_{cc} - 0}{R_C}$; $I_{C(sat)} = \frac{V_{cc}}{R_C} = \frac{8V}{2\ k\Omega} = 4mA$

$I_{C(cutoff)} = 0$; $V_{CE(cutoff)} = V_{CC} = 8V$



FIXED BIAS CIRCUIT

ADVANTAGES

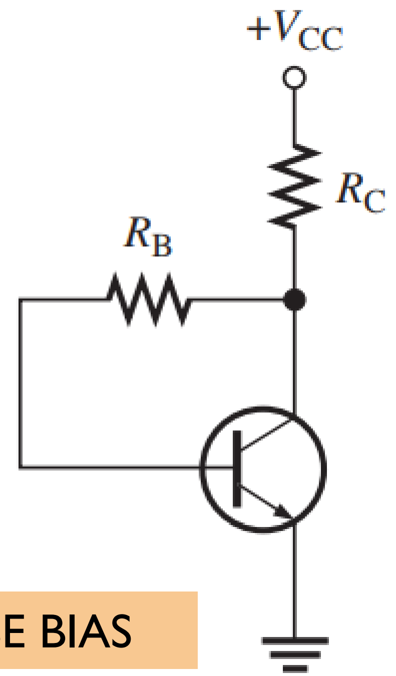
- Simple circuit, uses very few components.
- The operating point can be selected any where in the active region, by simply changing value of $R_{B.}$ Thus it provides maximum flexibility in the design.

DISADVANTAGES

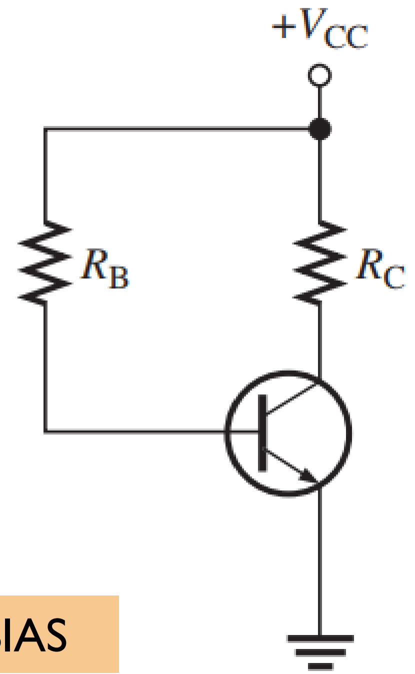
- Thermal stability is not provided in the circuit. Thus Q-point is not maintained.
- Since I_B is already fixed, I_C depends on β which changes unit to unit and shifts the Q-point. Thus stability is very poor.

COLLECTOR TO BASE BIAS CIRCUIT

- Also called Collector-feedback bias.
- The base resistor, R_B, is connected to the collector rather than to V_{CC}, as in the base bias arrangement.
- Collector gives a negative feedback to achieve stability.

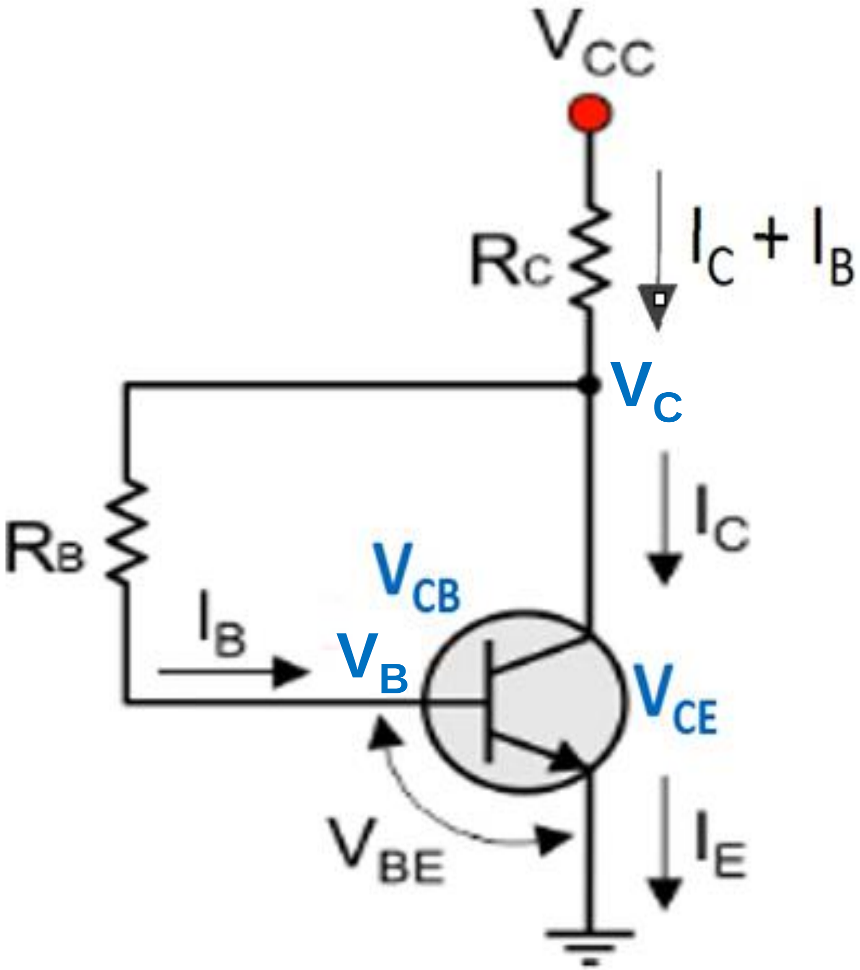


COLLECTOR TO BASE BIAS



FIXED BIAS

COLLECTOR TO BASE BIAS CIRCUIT



- Improved version of Fixed Bias Circuit.
- The negative feedback creates a compensating effect that tends to keep the Q-point stable.
- Assume a temperature Increase, it will increase I_C, which cause more voltage drop across $R_{C.}$
- With more voltage drop across R_C, V_C will decrease
- The decrease in V_C causes, V_{CB} to decrease, which reduces $I_{B.}$
- As I_B is decreased I_C will decrease
- Thus, the original increase in temperature is compensated by a smaller bias current by negative feedback

COLLECTOR TO BASE BIAS CIRCUIT

INPUT ANALYSIS

$$V_{CC} - (I_C + I_B)R_C - I_B R_B - V_{BE} = 0$$

$$V_{CC} = I_C R_C + I_B(R_B + R_C) + V_{BE}$$

$$\boxed{I_C = \beta I_B}$$

$$V_{CC} = \beta R_C I_B + I_B(R_B + R_C) + V_{BE}$$

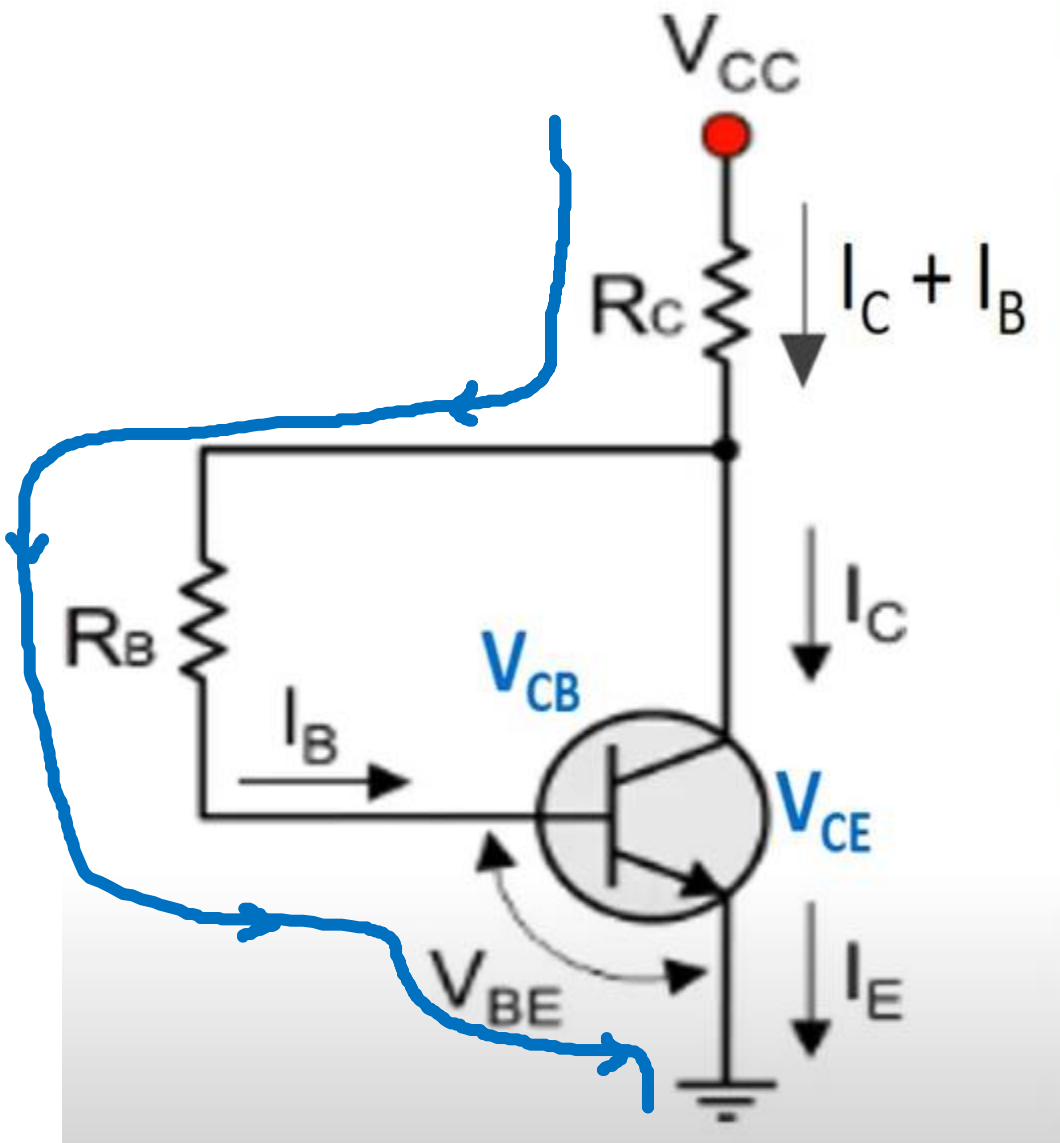
$$V_{CC} = (\beta R_C + R_C + R_B)I_B + V_{BE}$$

$$V_{CC} = ((\beta + 1)R_C + R_B)I_B + V_{BE}$$

$$\boxed{I_B = \frac{V_{CC} - VBE}{(\beta + 1)RC + RB}}$$

When $V_{BE} \approx 0$

$$I_B \approx \frac{V_{CC}}{(\beta + 1)RC + R_B}$$



COLLECTOR TO BASE BIAS CIRCUIT

INPUT ANALYSIS

$V_{CE} = V_{CB} - V_{BE}$

$I_B = V_{CB} / R_B$

When temperature ↑

I_C↑

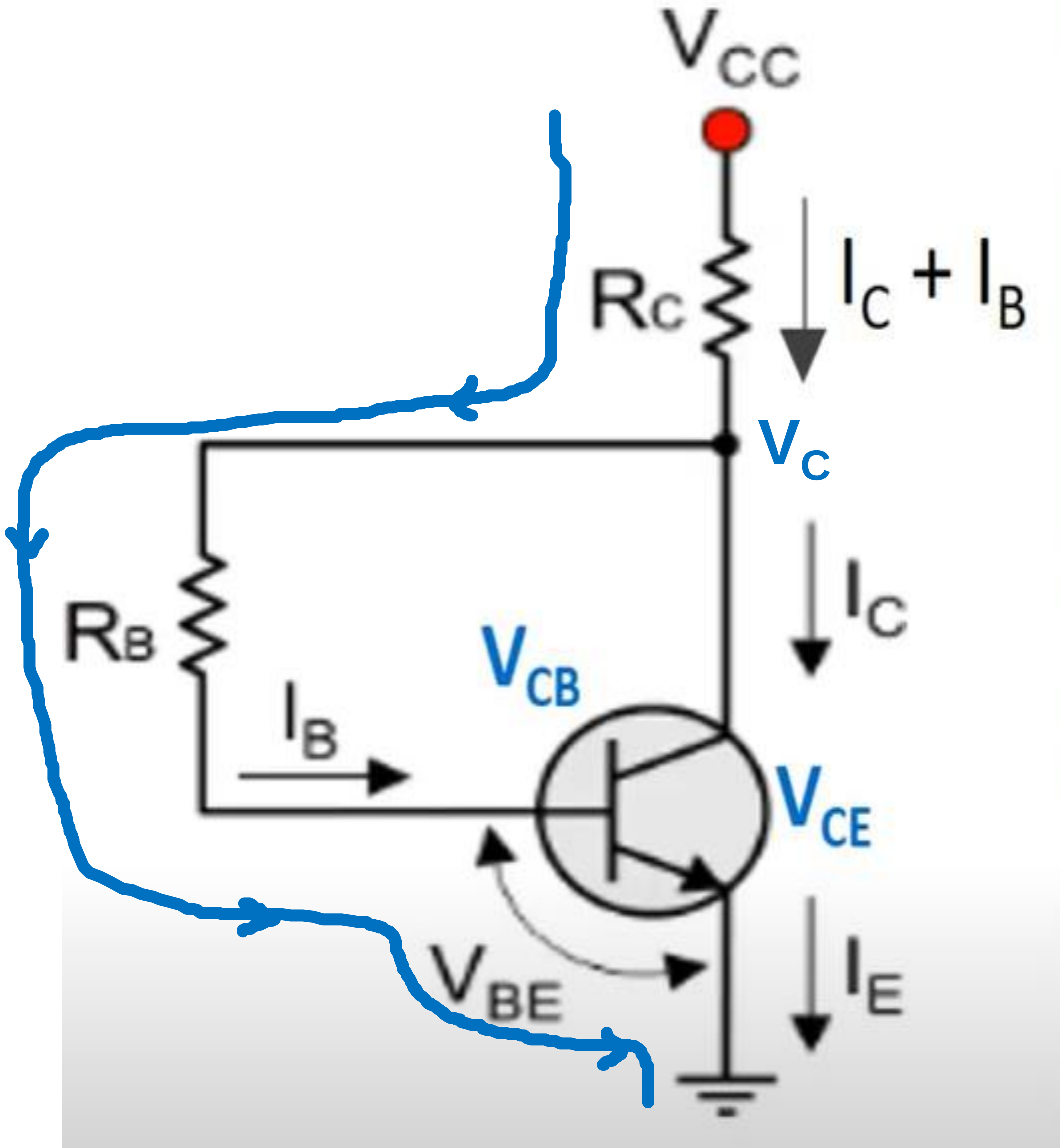
voltage drop across R_C ↑

V_C ↓

V_{CB} ↓

I_B ↓

I_C ↓



COLLECTOR TO BASE BIAS CIRCUIT

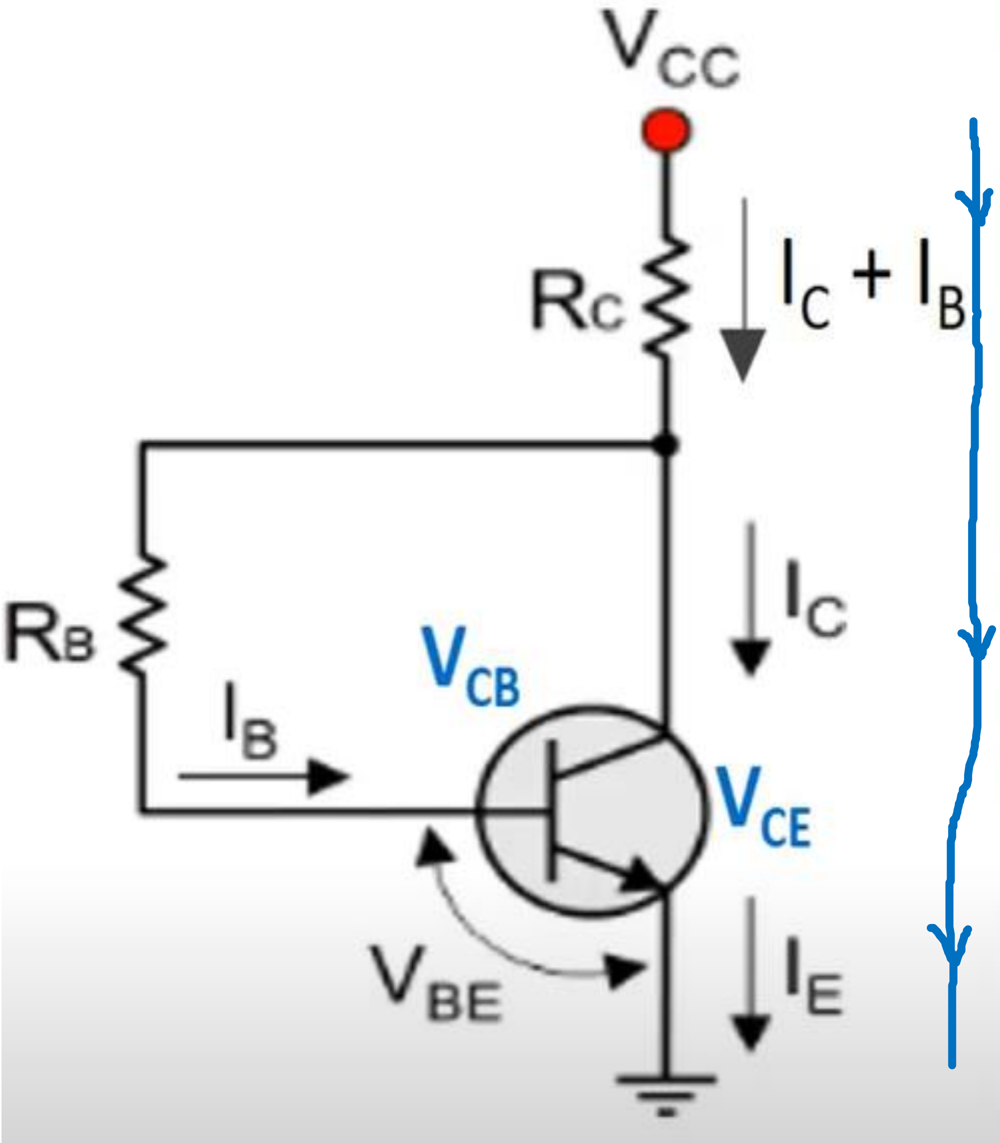
OUTPUT ANALYSIS

$$V_{CC} - (I_C + I_B)R_C - V_{CE} = 0$$

$$\boxed{V_{CE} = V_{CC} - (I_C + I_B)R_C}$$

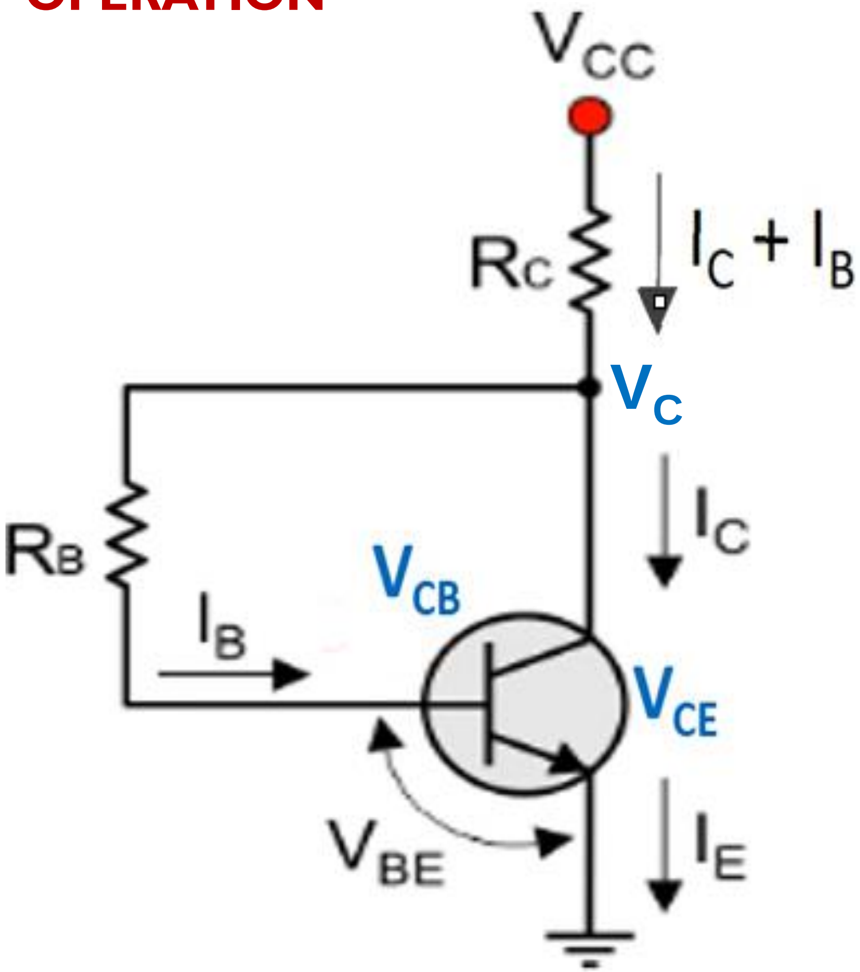
If $I_C >> I_B$,

$$V_{CE} \approx V_{CC} - I_C R_C$$



COLLECTOR TO BASE BIAS CIRCUIT

OPERATION



- If there is change in β due to transistor replacement or change in I_{CEO} increase due to change in increase in temperature then I_C increases
- $I_C = \beta I_B + I_{CEO}$
- Since, $V_{CE} = V_{CC} – (I_C + I_B)R_C$ then if I_C increases, V_{CE} decreases
- Since, $V_{CB} = V_{CE} + V_{BE}$
- With decrease in V_{CE}, V_{CB} decreases
- $IB = V_{CB} / R_B$ base current I_B, decreases
- Thus, the with the decrease in base current the circuit tends to maintain stable value collector current, keeping Q point fixed.

COLLECTOR TO BASE BIAS CIRCUIT

ADVANTAGES

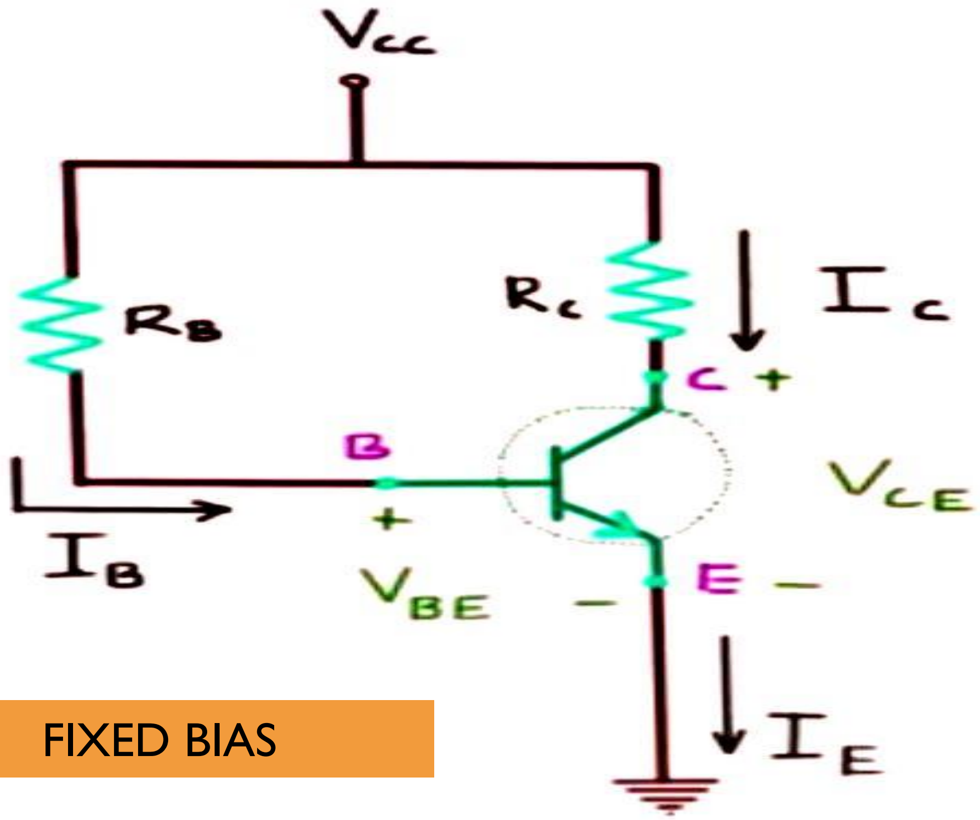
- Simple circuit, as it uses very few components.
- Better stabilization than fixed bias circuit.

DISADVANTAGES

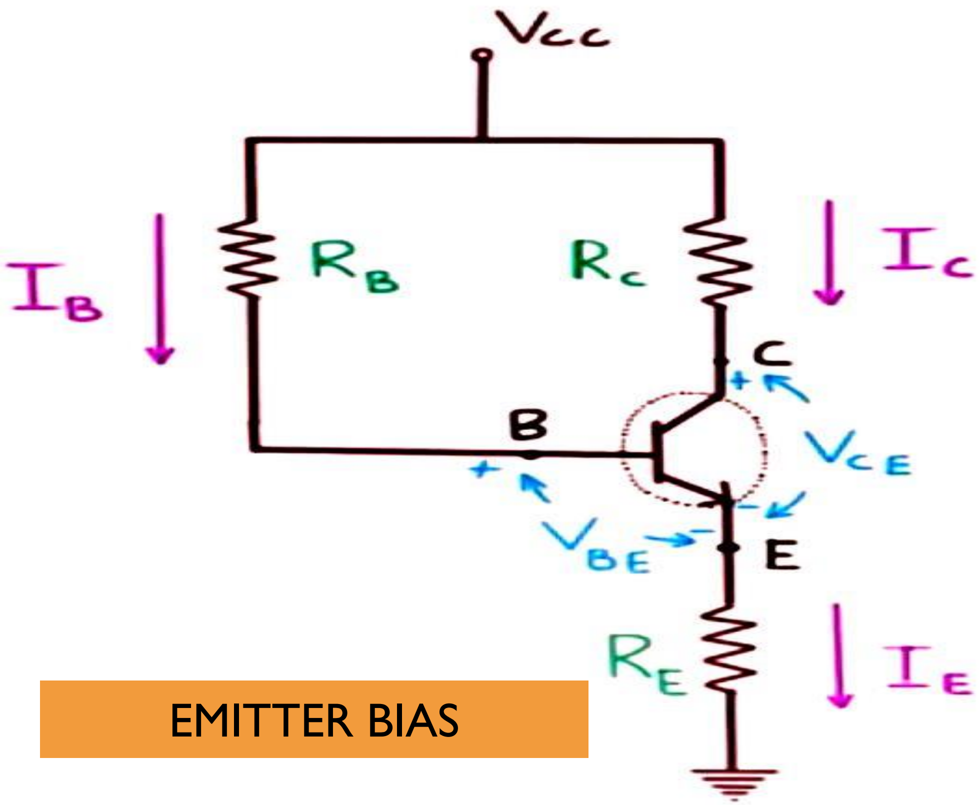
- Poor stability, as Stability factor (S) is high.
- Since it provides negative feedback through R_B, the gain of the amplifier is reduced.

EMITTER BIAS CIRCUIT

- Modification of Fixed Bias or Collector to Base bias circuit by adding a Emitter Resistor R_E
- Emitter Resistance provide more stability.



FIXED BIAS



EMITTER BIAS

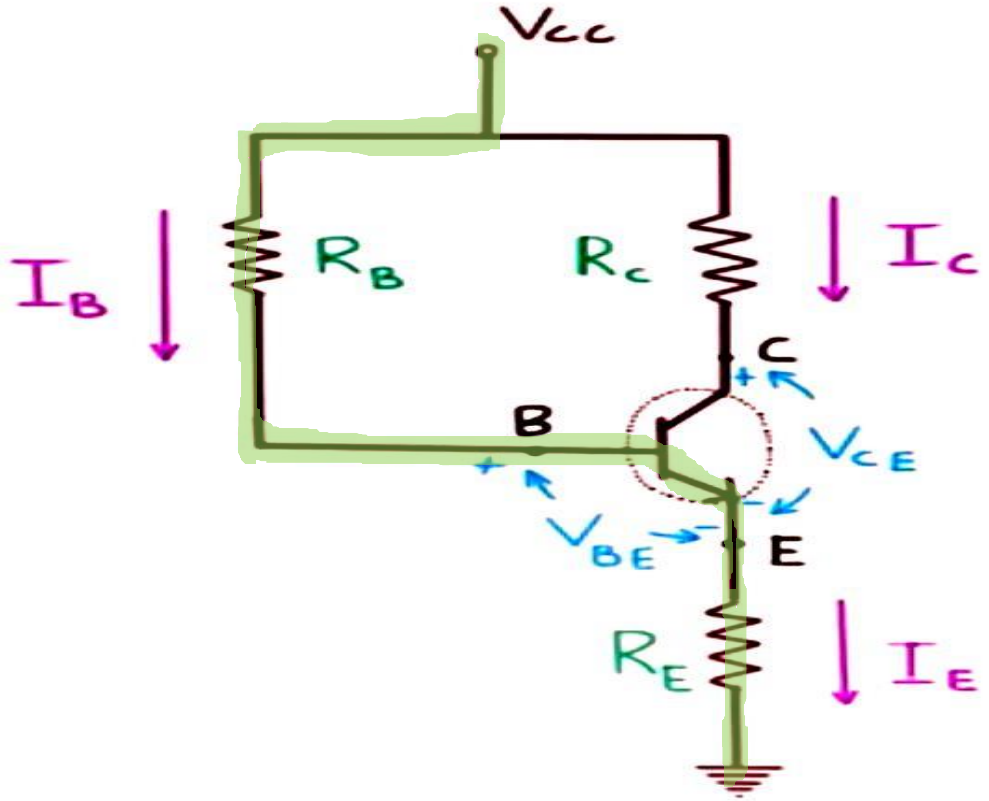
EMITTER BIAS CIRCUIT

INPUT ANALYSIS

$$V_{CC} - I_B R_B - V_{BE} - I_E R_E = 0$$

$$V_{CC} = I_B R_B + V_{BE} + I_E R_E$$

$$\boxed{I_B = \frac{V_{CC} - V_{BE} - I_E R_E}{R_B}}$$



EMITTER BIAS CIRCUIT

OUTPUT ANALYSIS

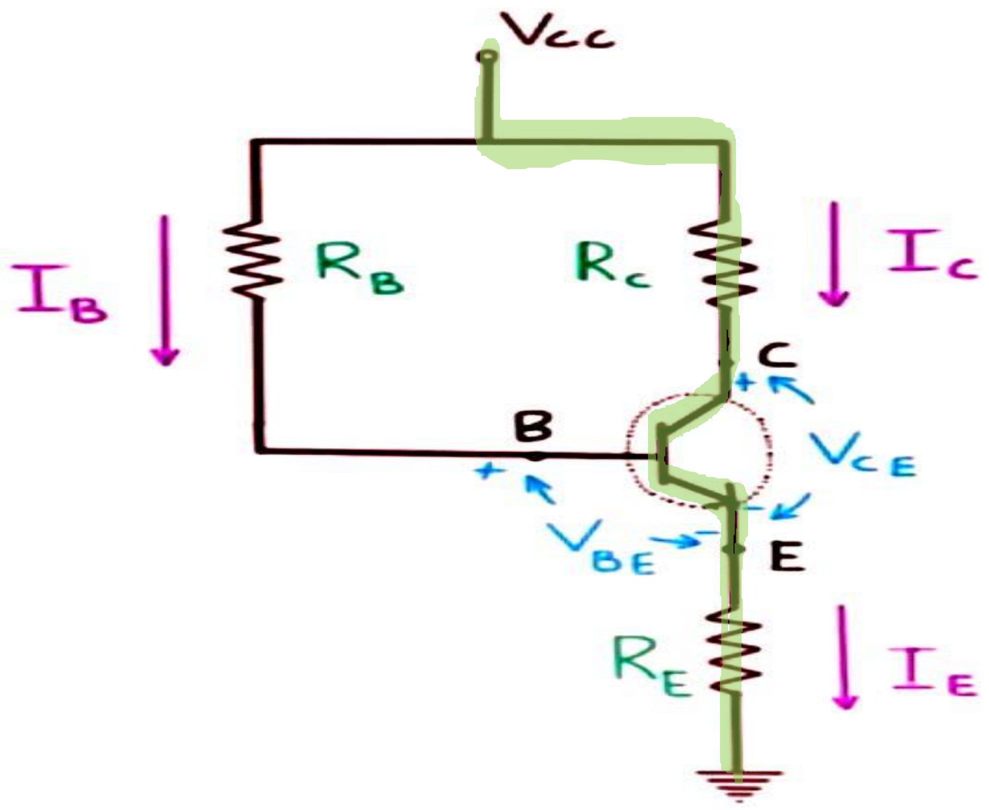
$$V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0$$

$$\boxed{V_{CE} = V_{CC} - I_C R_C - I_E R_E}$$

$$\boxed{I_B = \frac{V_{CC} - V_{BE} - I_E R_E}{R_B}}$$

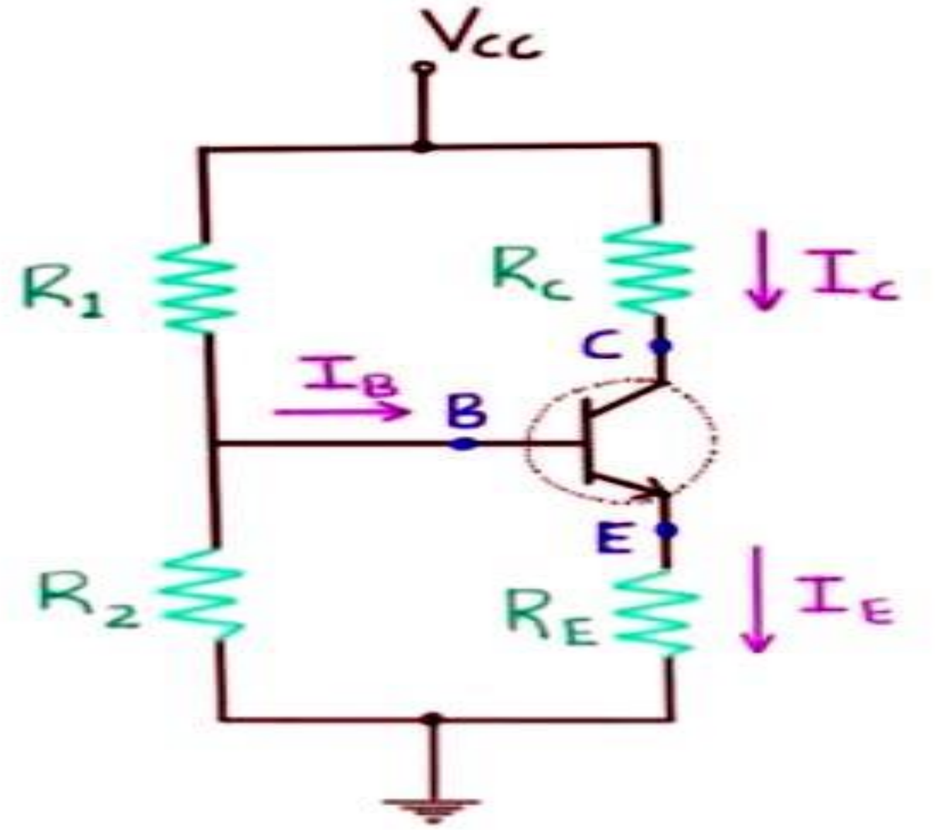
$$I_C = \beta I_B$$

$$\boxed{I_C = \beta \frac{(V_{CC} - V_{BE} - IERE)}{R_B}}$$

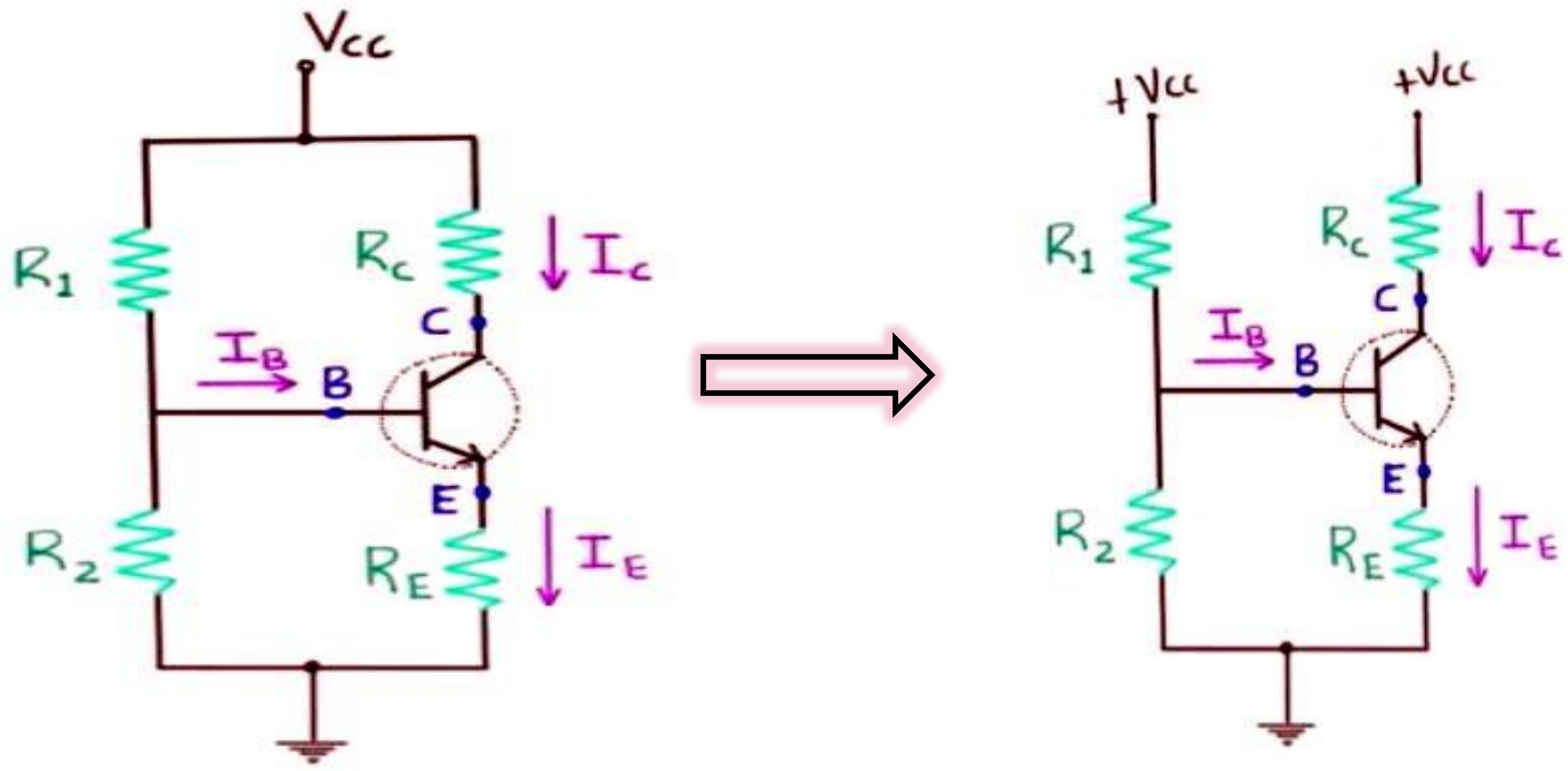


VOLTAGE DIVIDER BIAS CIRCUIT

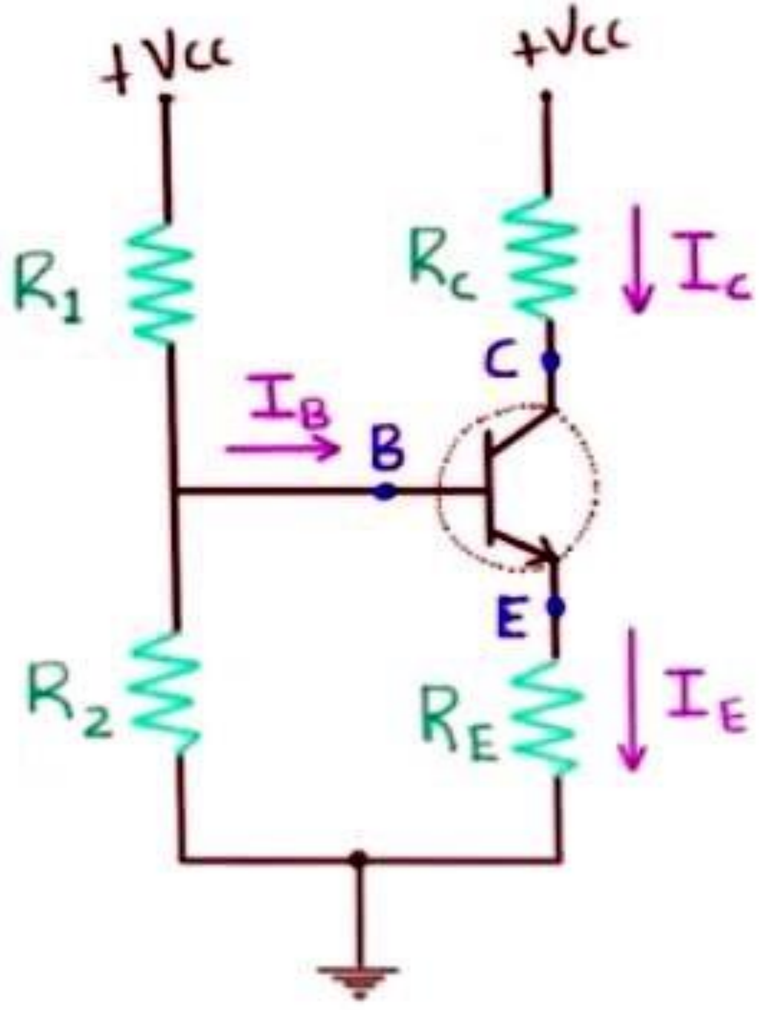
- Voltage Divider Bias Circuit is the most stable circuit of the basic transistor bias circuits.
- Two resistors R1 and R2 are connected to V_{CC} to provide biasing.
- Resistors R1 and R2 constitute a voltage divider that divides the supply voltage to produce the base bias voltage (V_B).
- Collector resistor (R_C) and an emitter resistor (R_E) connected in series with the transistor.
- The emitter resistance R_E provides Stabilization.
- Voltage drop across R2 , make Base emitter junction Forward biased, and the base current produced make collector current to flow in the zero signal conditions.

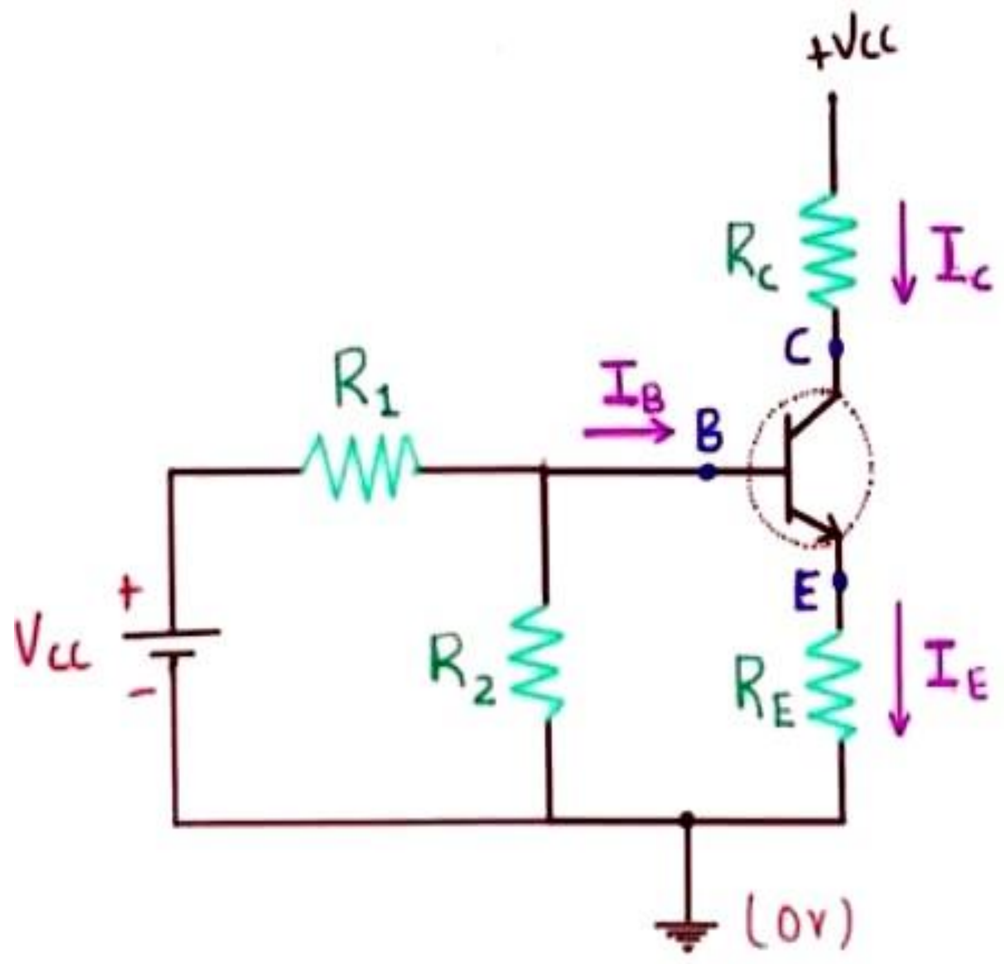


VOLTAGE DIVIDER BIAS CIRCUIT

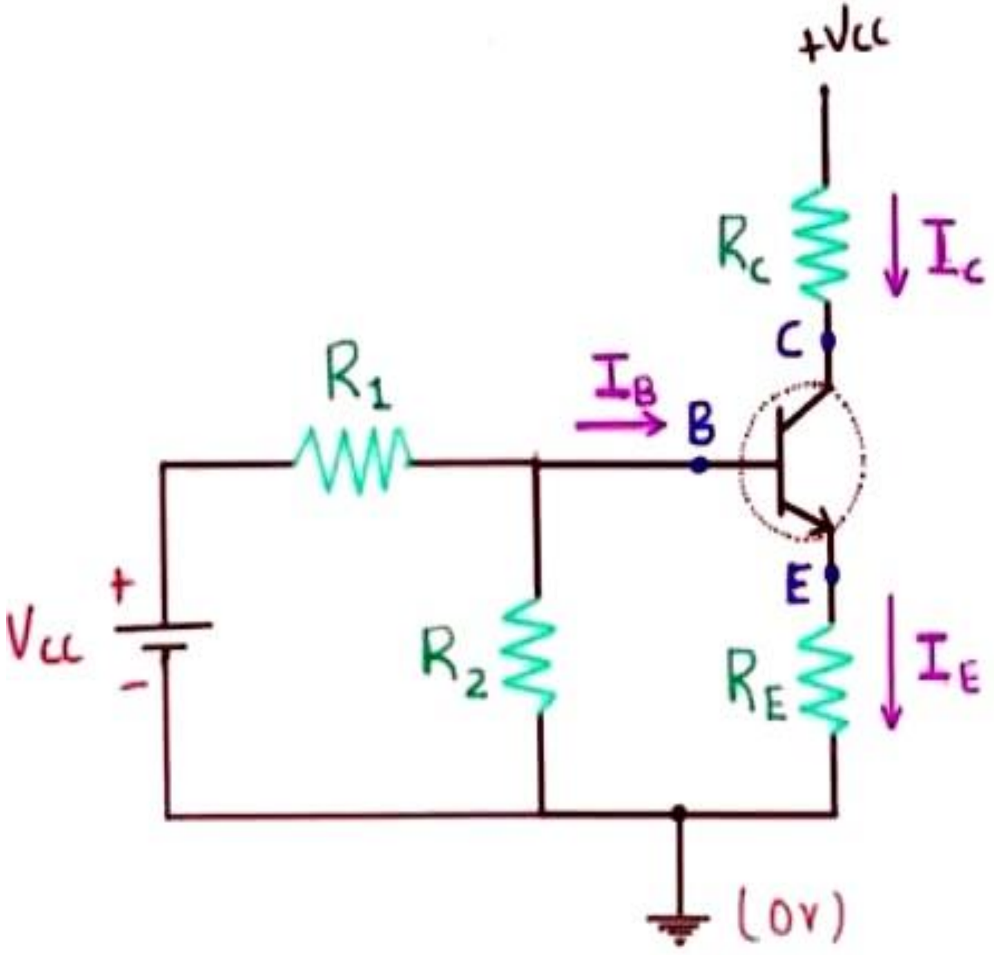


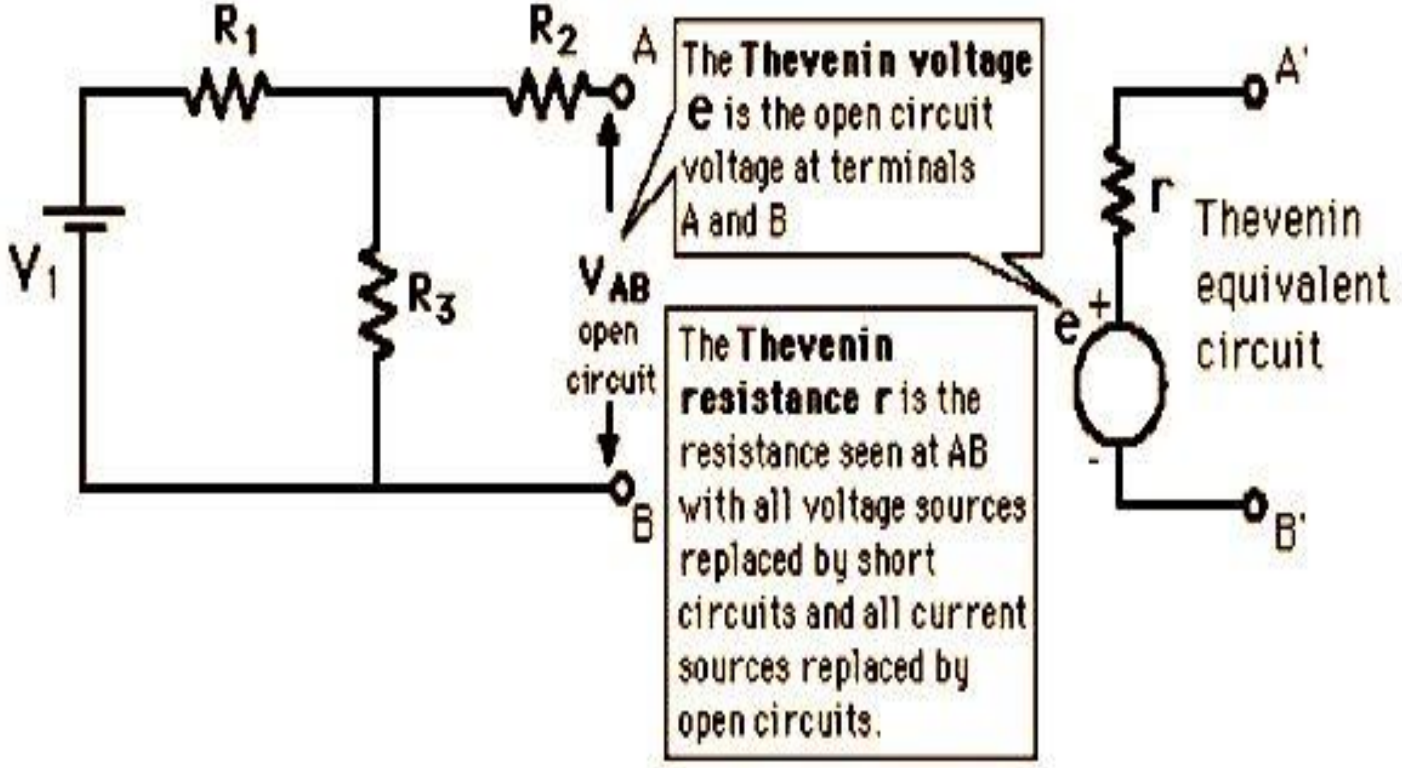
VOLTAGE DIVIDER BIAS CIRCUIT



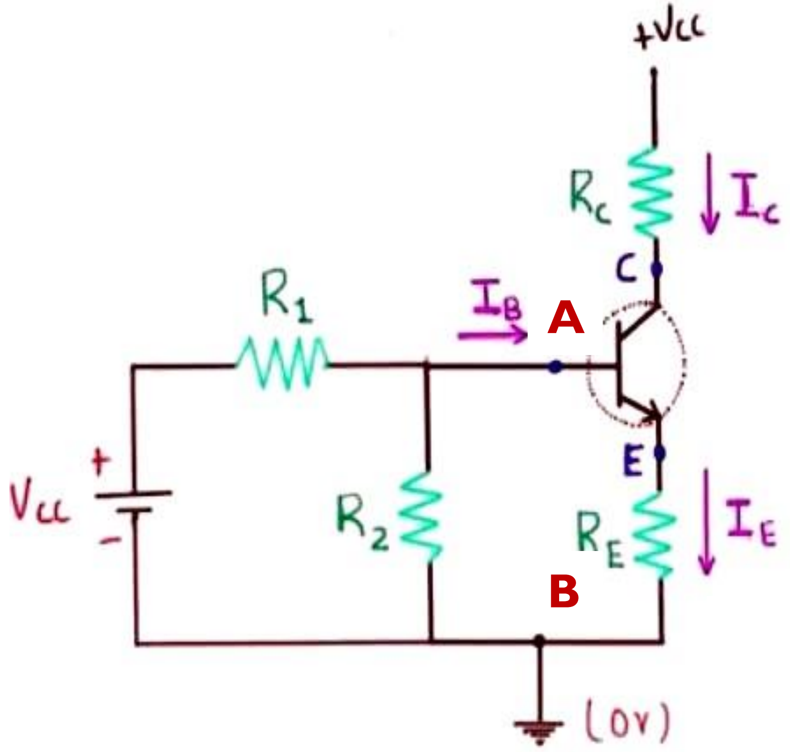


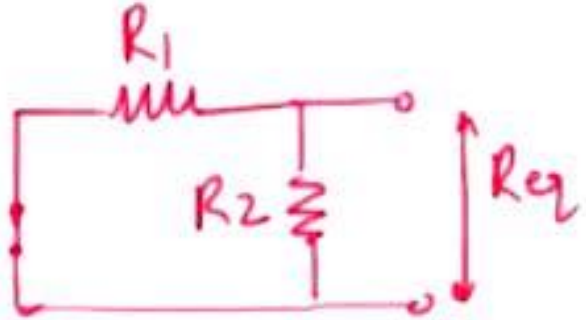
VOLTAGE DIVIDER BIAS CIRCUIT



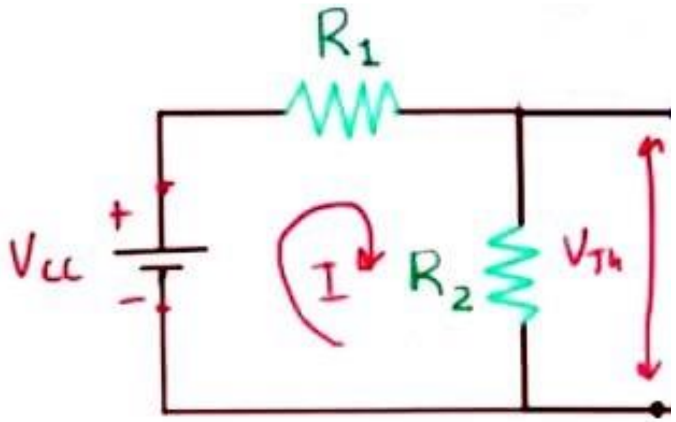


VOLTAGE DIVIDER BIAS CIRCUIT





$$R_{eq} = R_{TH} = \frac{R_1 R_2}{R_1 + R_2}$$

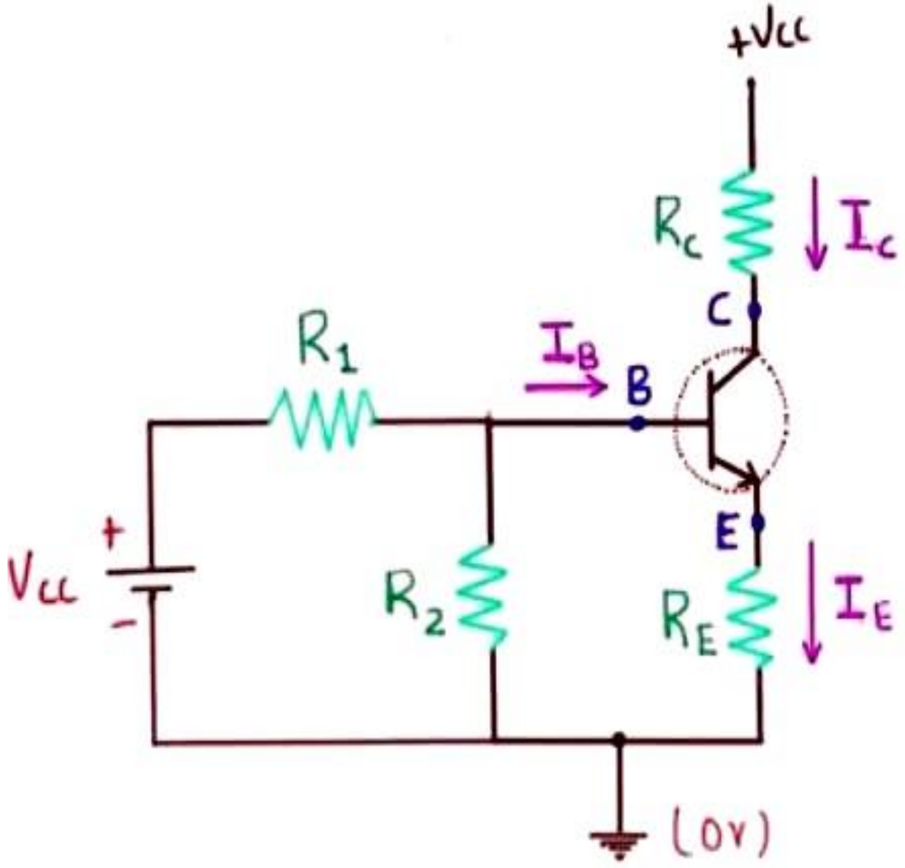


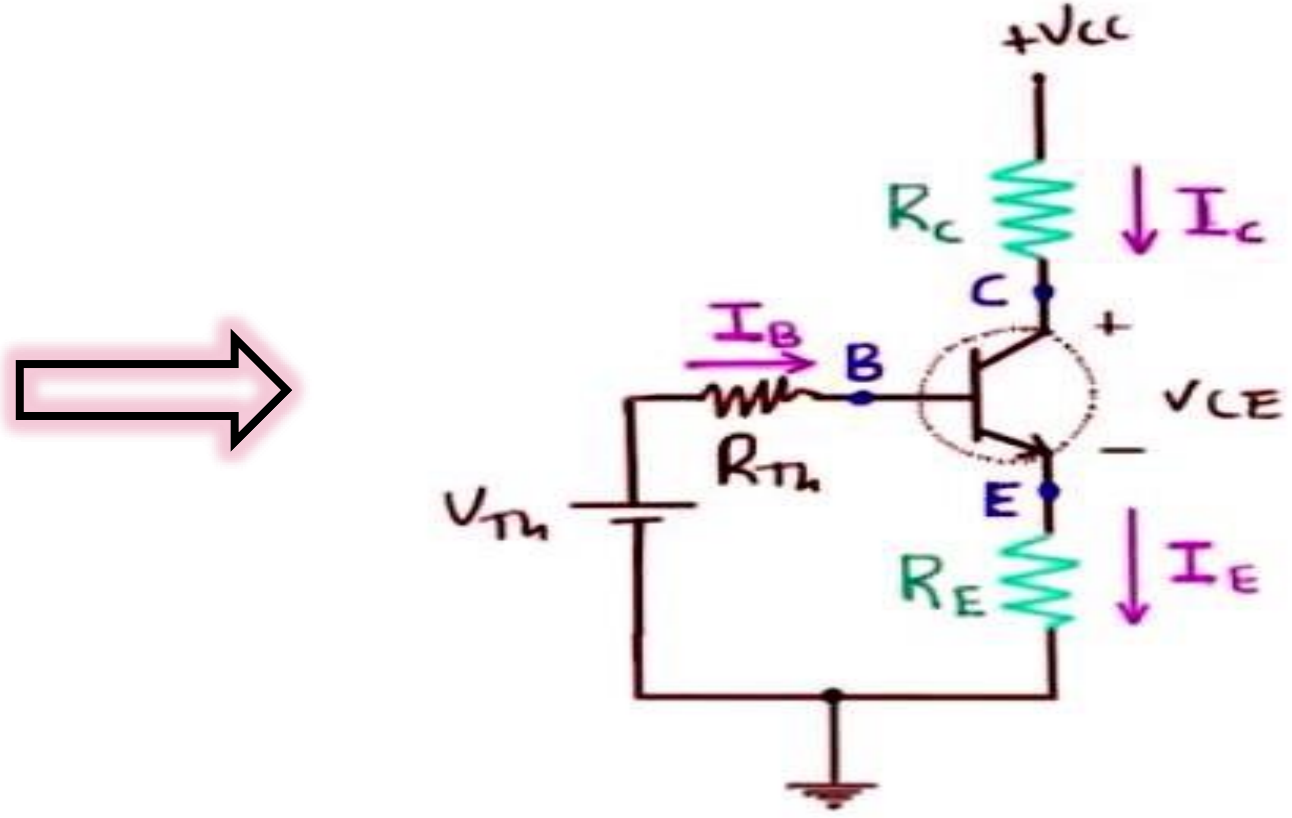
$$I = \frac{V_{CC}}{R_1 + R_2}$$

$$V_{TH} = R_2 \times I$$

$$V_{TH} = \frac{V_{CC}\, R_2}{R_1 + R_2}$$

VOLTAGE DIVIDER BIAS CIRCUIT



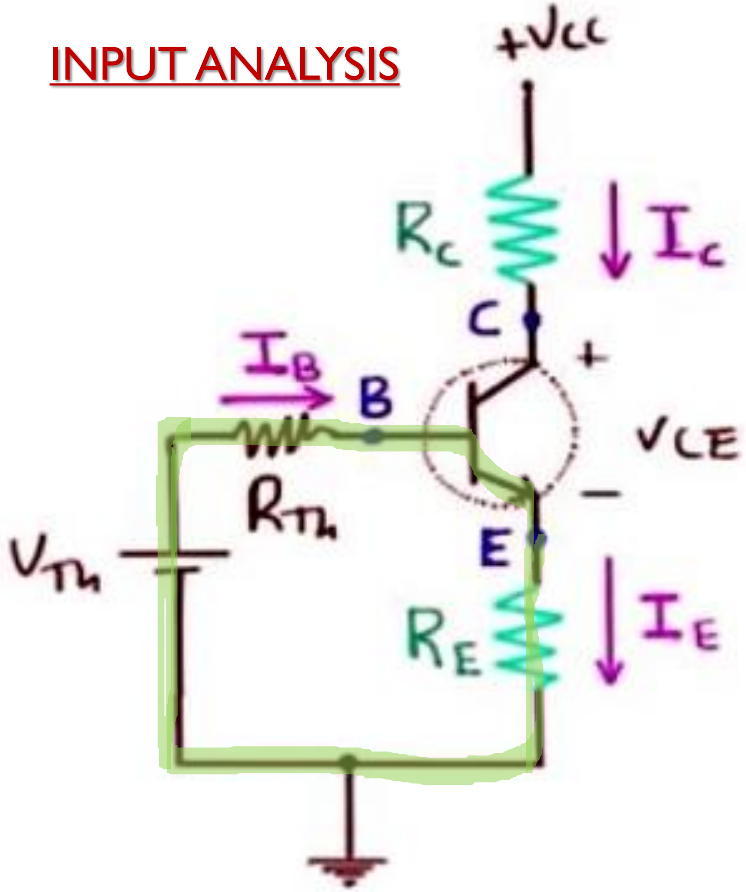


$$R_{TH} = \frac{R_1 R_2}{R_1 + R_2}$$

$$V_{TH} = \frac{V_{CC}\, R_2}{R_1 + R_2}$$

VOLTAGE DIVIDER BIAS CIRCUIT - ANALYSIS

INPUT ANALYSIS



$$V_{TH} - I_B R_{TH} - V_{BE} - I_E R_E = 0$$

$$\boxed{V_{TH} = I_B R_{TH} + V_{BE} + I_E R_E}$$

$$I_E = I_C + I_B\,;\; I_C = \beta I_B$$

$$I_E = (\beta + 1) I_B$$

$$V_{TH} = I_B R_{TH} + V_{BE} + (\beta + 1) I_B R_E$$

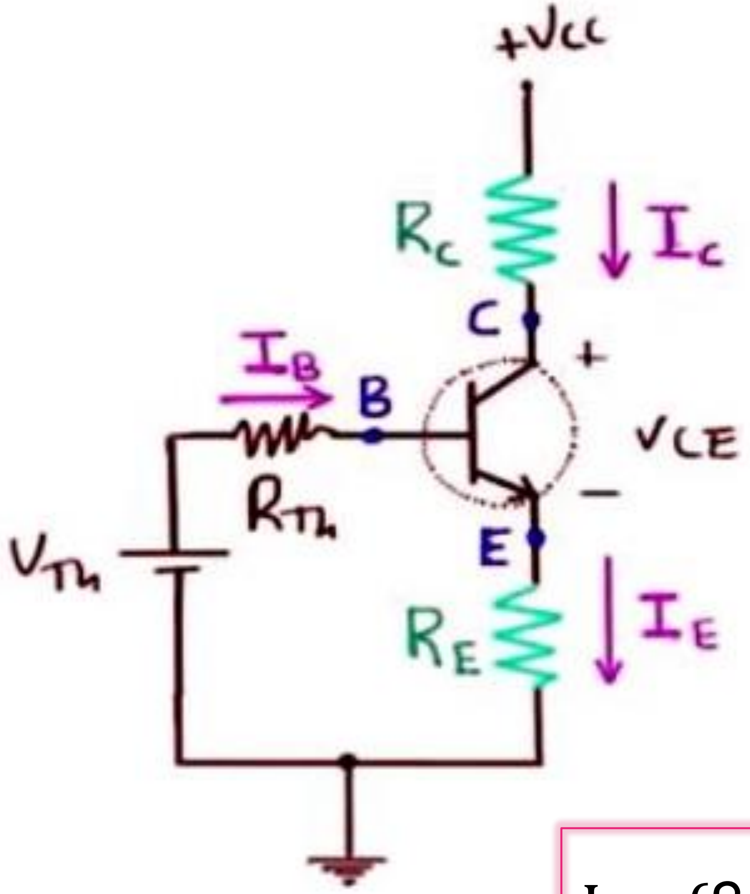
$$V_{TH} = I_B (R_{TH} + (\beta + 1) R_E) + V_{BE}$$

$$\boxed{I_B = \frac{V_{TH} - V_{BE}}{R_{TH} + (\beta + 1) R_E}}$$

If, $V_{BE} \approx 0$, and R_E is very small

$$I_B \approx \frac{V_{TH}}{R_{TH} + \beta R_E}$$

VOLTAGE DIVIDER BIAS CIRCUIT - ANALYSIS



$$I_C = \beta I_B$$

$$\boxed{I_B = \frac{V_{TH} - V_{BE}}{R_{TH} + (\beta + 1)R_E}}$$

$$\boxed{I_C = \beta\left(\frac{V_{TH} - V_{BE}}{R_{TH} + (\beta + 1)R_E}\right)}$$

$$R_{TH} = \frac{R_1 R_2}{R_1 + R_2}$$

$$V_{TH} = \frac{V_{CC} R_2}{R_1 + R_2}$$

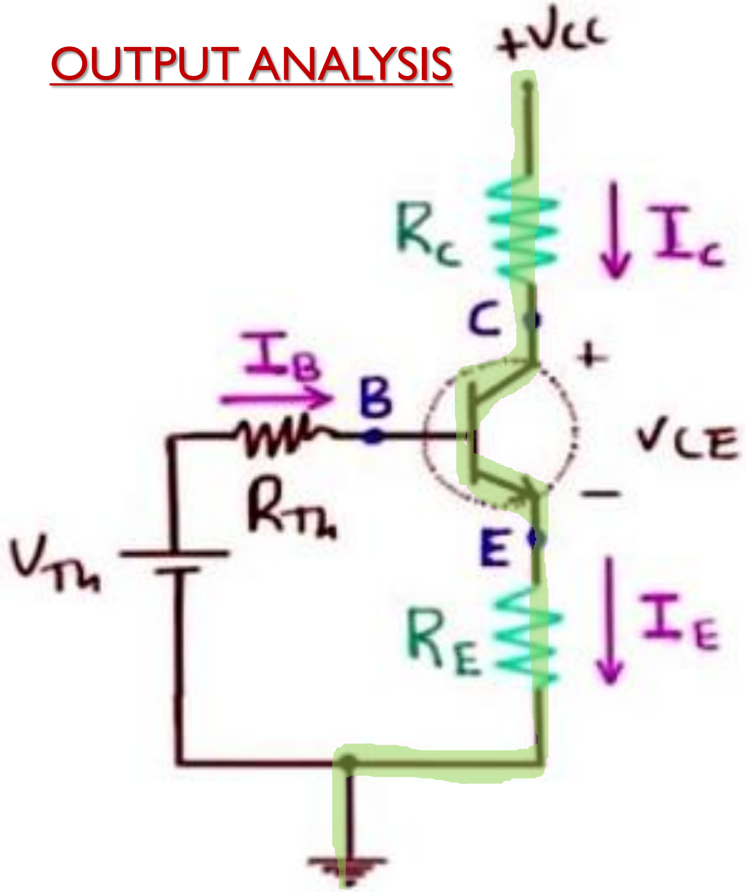
$$\boxed{I_E = (\beta + 1)\left(\frac{V_{TH} - V_{BE}}{R_{TH} + (\beta + 1)R_E}\right)}$$

If, $V_{BE} \approx 0$, and R_E is very small

$$I_C \approx \beta\left(\frac{V_{TH}}{R_{TH} + \beta R_E}\right)$$

VOLTAGE DIDER BIAS CIRCUIT - ANALYSIS

OUTPUT ANALYSIS



$$V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0$$

$$V_{CC} = I_C R_C + V_{CE} + I_E R_E$$

$$\boxed{V_{CE} = V_{CC} - I_C R_C - I_E R_E}$$

If, $I_E \approx I_C$

$$V_{CE} = V_{CC} - I_C (R_C + R_E)$$

VOLTAGE DIVIDER BIAS CIRCUIT

ADVANTAGES

- Stability factor is Independent of β
- Voltage divider biasing is thermally stable.

DISADVANTAGES

- Input resistance affected by parallel combination of R1 and R2. It can overcome by using 2 power supplies.

STABILITY FACTOR

Need For Bias Stabilization?

- Transistor parameters are temperature dependent
- Parameters like β for transistor changes from one unit to the other.
- The process of making operating point independent of temperature, parameter variations or transistor replacement is called **Bias Stabilization.**

Need For Bias Stabilization?

Temperature Dependence of I_C

$$Ic = \beta I_B + I_{CEO} \qquad I_{CE0} = (1+\beta)I_{CBO}$$

- Reverse saturation current I_{CBO} doubles for every **10 degree** rise in temperature.
- So I_{CE0} increases $\beta + 1$ times of I_{CBO}.
- I_C dependent on I_{CE0} , so I_C also increases $\beta + 1$ times of I_{CBO}.
- Power dissipation of transistor, $P = V_C I_C$.
- So power dissipation at the junction Increases with collector current, which further increases temperature.
- The process repeats and excess heat may even burn or destroy transistor, and the situation is described as **Thermal Runaway.**

Requirements of Biasing Circuits

- Operating point is to be fixed in the middle of the Active region to protect the signal from distortion.
- Stabilize the collector current against the variations of temperature.
- Making the operating point independent of transistor parameters.

STABILITY FACTOR

- The **stability factor S**, is the change of collector current with respect to the reverse saturation current, keeping β and V_{BE} constant.

$$\boxed{S = \frac{\delta I_C}{\delta I_{CO}} = \frac{\Delta I_C}{\Delta I_{CO}}}$$

Where I_{CO} – Reverse Saturation Current

STABILITY FACTOR

- The **stability factor S'**, is the variation of collector current with respect to V_{BE}, keeping β and reverse saturation current constant.

$$\boxed{S' = \frac{\delta I_C}{\delta V_{BE}} = \frac{\Delta I_C}{\Delta V_{BE}}}$$

Where V_{BE} – Base emitter voltage

STABILITY FACTOR

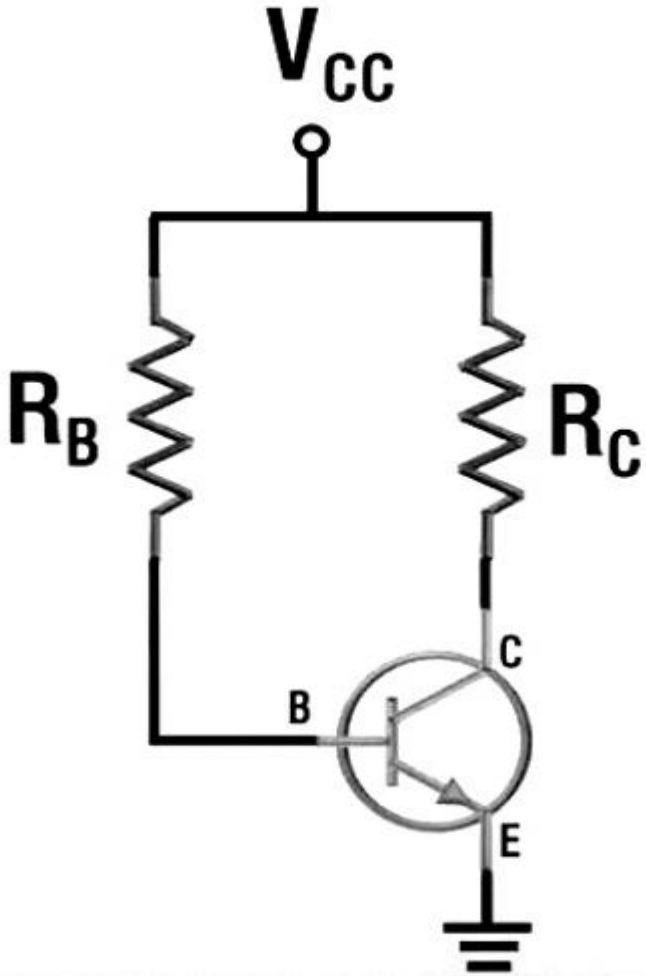
- The **stability factor S"**, is the variation of collector current with respect to β, keeping V_{BE} and reverse saturation current constant.

$$\boxed{S'' = \frac{\delta I_C}{\delta \beta} = \frac{\Delta I_C}{\Delta \beta}}$$

Where β – Current amplification factor

$$\boxed{\Delta I_C = (S * \Delta I_{CO}) + (S' * \Delta V_{BE}) + (S'' * \Delta \beta)}$$

Stability factor for Fixed Bias Circuit



$$Ic = \beta I_B + (\beta + 1)I_{CO}$$

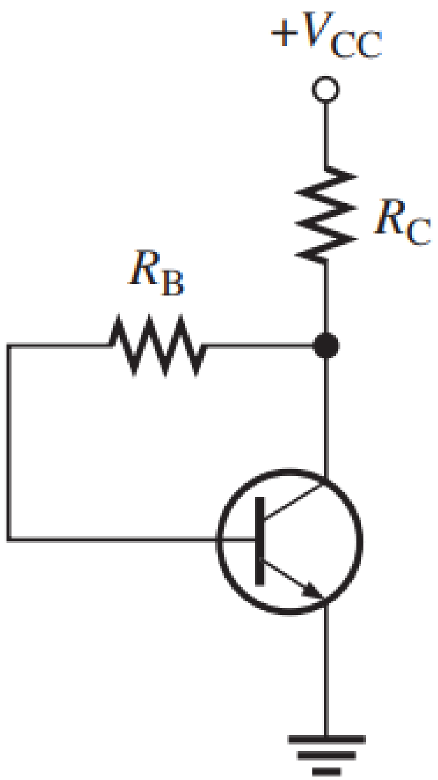
$$I_B = \frac{V_{cc} - V_{BE}}{R_B}$$

$$Ic = \beta(\frac{V_{cc} - V_{BE}}{R_B}) + (\beta + 1)I_{CO}$$

$$1 = 0 + (\beta + 1)\ (1/S)$$

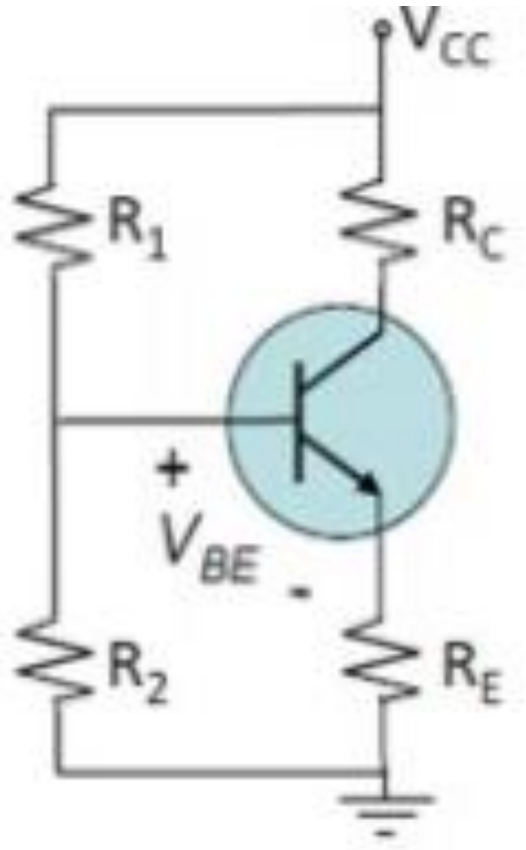
$$\boxed{S = (\beta + 1)}$$

Stability factor for Collector Bias Circuit



$$s = \frac{\beta + 1}{1 + \beta\left(\frac{R_C}{R_C + R_B}\right)}$$

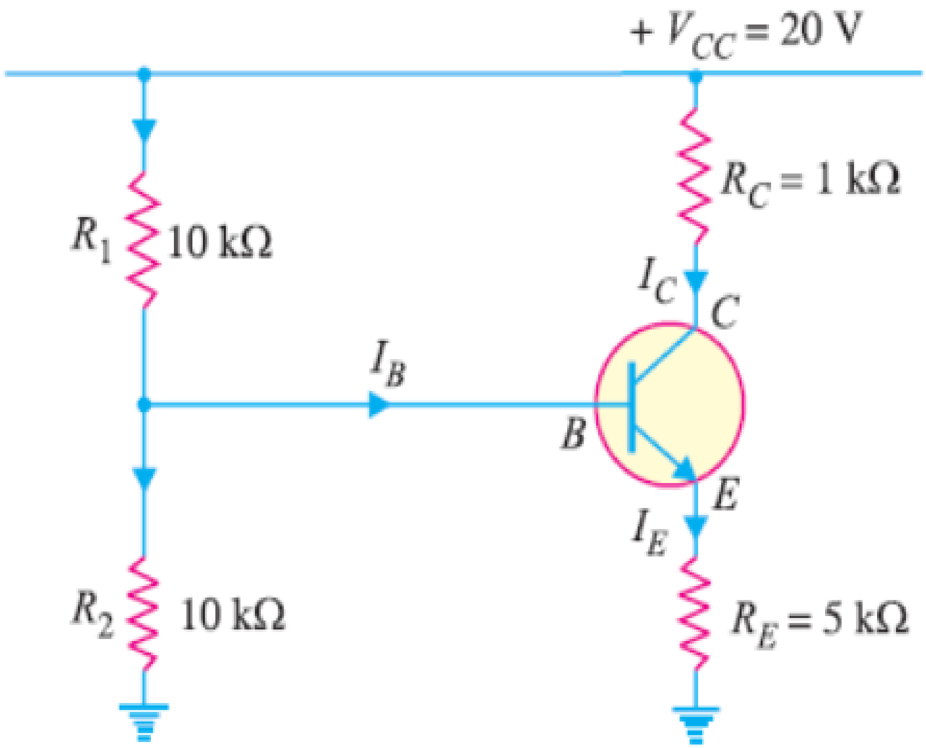
Stability factor for Voltage Divider Bias Circuit



$$\boxed{s = \frac{R_B}{R_E}}$$

NUMERICAL PROBLEMS

QSTN: Calculate the emitter current in the voltage divider circuit shown in Fig
Also find the value of VCE and collector potential VC.



Thevenin's Voltage, V2

$$V_2 = \left(\frac{V_{CC}}{R_1 + R_2}\right)R_2 = \left(\frac{20}{10+10}\right)10 = 10\text{ V}$$

$$V_2 = V_{BE} + I_E R_E$$

As V_{BE} is generally small, therefore, it can be neglected.

$$\therefore \quad I_E = \frac{V_2}{R_E} = \frac{10\text{ V}}{5\text{ k}\Omega} = \mathbf{2\text{ mA}}$$

Now $\quad I_C \simeq I_E = 2\text{ mA}$

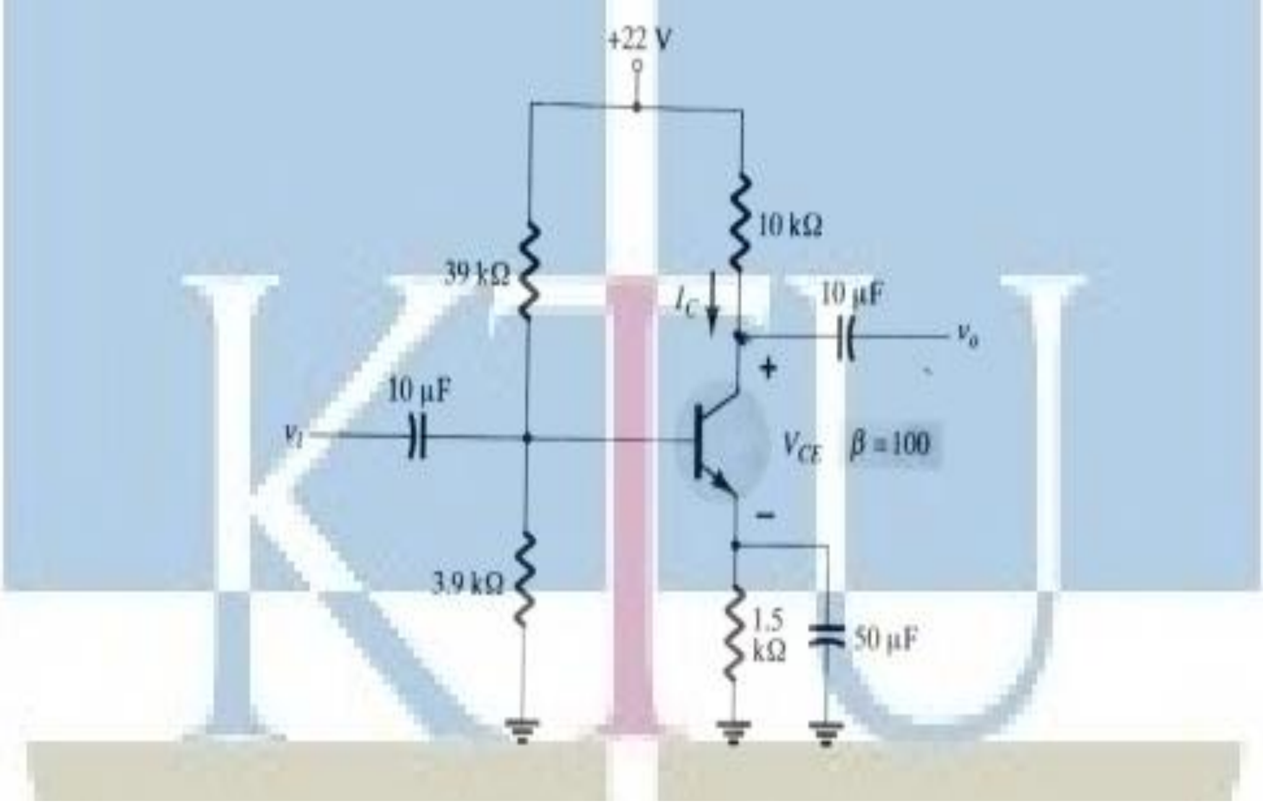
$$\therefore \quad V_{CE} = V_{CC} - I_C(R_C + R_E) = 20 - 2\text{ mA }(6\text{ k}\Omega)$$

$$= 20 - 12 = \mathbf{8\text{ V}}$$

Collector potential, $V_C = V_{CC} - I_C R_C = 20 - 2\text{ mA} \times 1\text{ k}\Omega$

$$= 20 - 2 = \mathbf{18\text{ V}}$$

QSTN: With reference to the following circuit, draw the load line and mark the Q point of the Silicon BJT transistor.



R1 = 39kΩ
R2 = 3.9kΩ
RC = 10kΩ
RE = 1.5kΩ
VBE = 0.7V
VCC = 22V
β = 100

$$R_{TH} = \frac{R_1 R_2}{R_1 + R_2}$$

$$V_{TH} = \frac{V_{CC}\, R_2}{R_1 + R_2}$$

$$I_B = \frac{V_{TH} - V_{BE}}{R_{TH} + (\beta + 1)R_E}$$

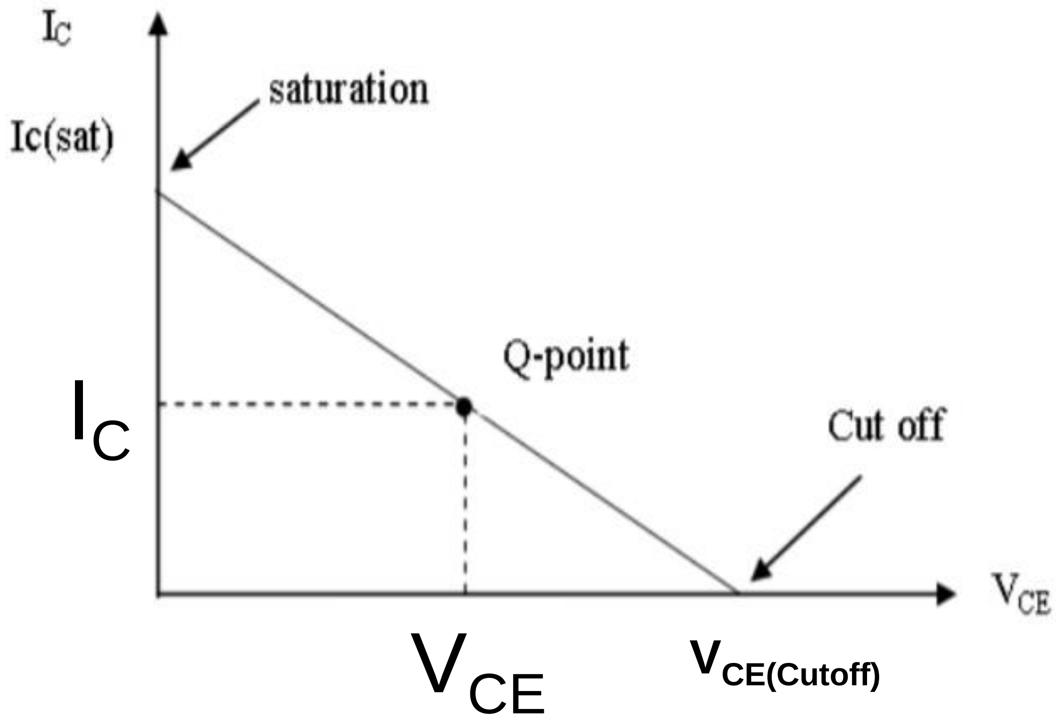
$$I_C = \beta\, I_B$$

$$I_E \approx I_C$$

$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$

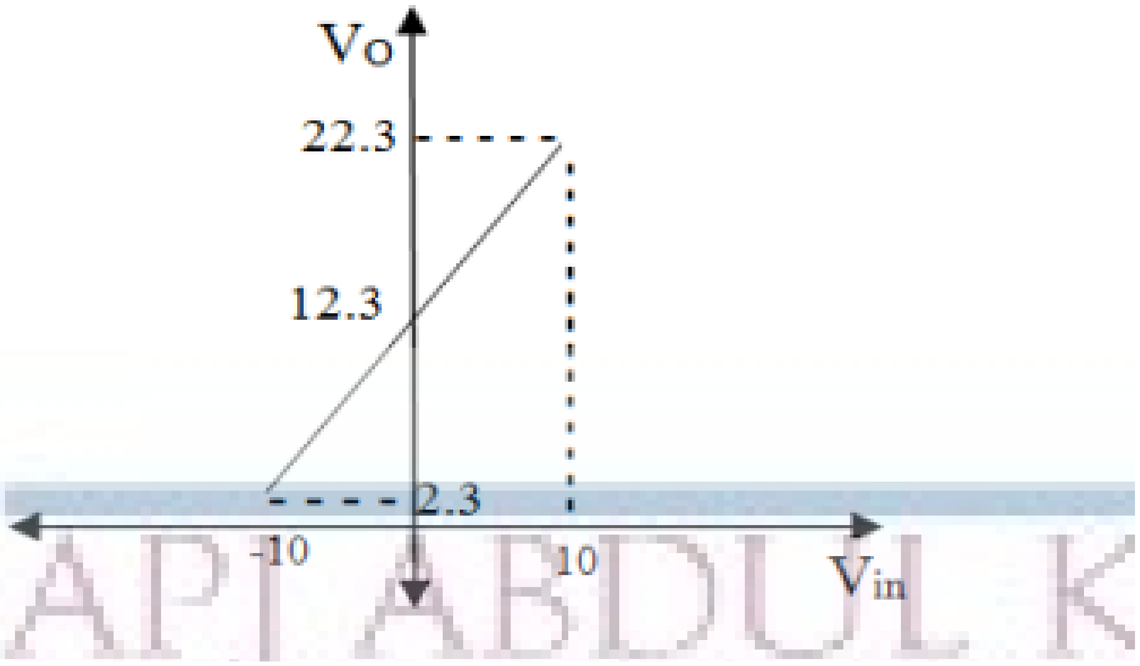
$$V_{CE(Cutoff)} = V_{CC}$$

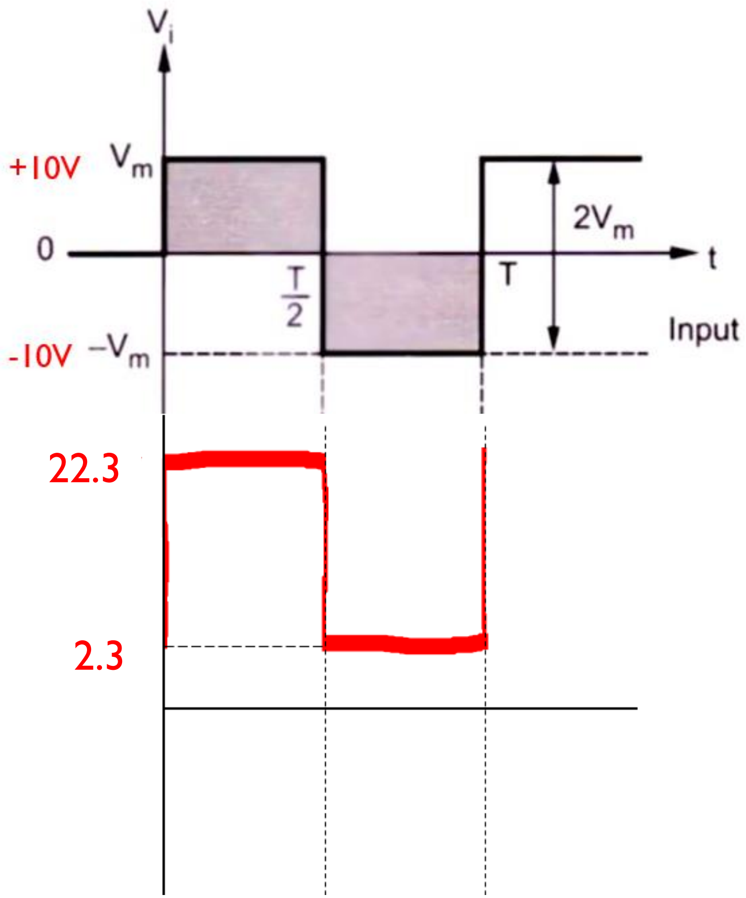
$$I_{C(Sat)} = \frac{V_{CC}}{R_C + R_E}$$

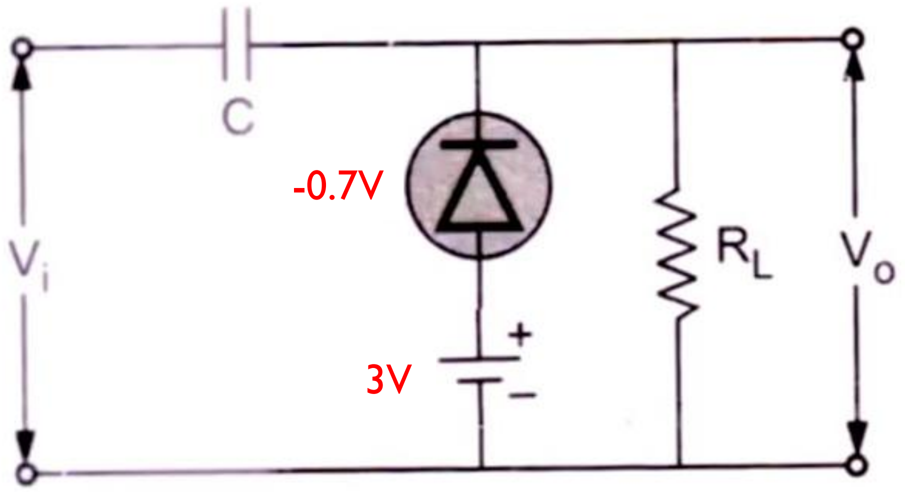


R1 = 39kΩ
R2 = 3.9kΩ
RC = 10kΩ
RE = 1.5kΩ
VBE = 0.7V
VCC = 22V
β = 100

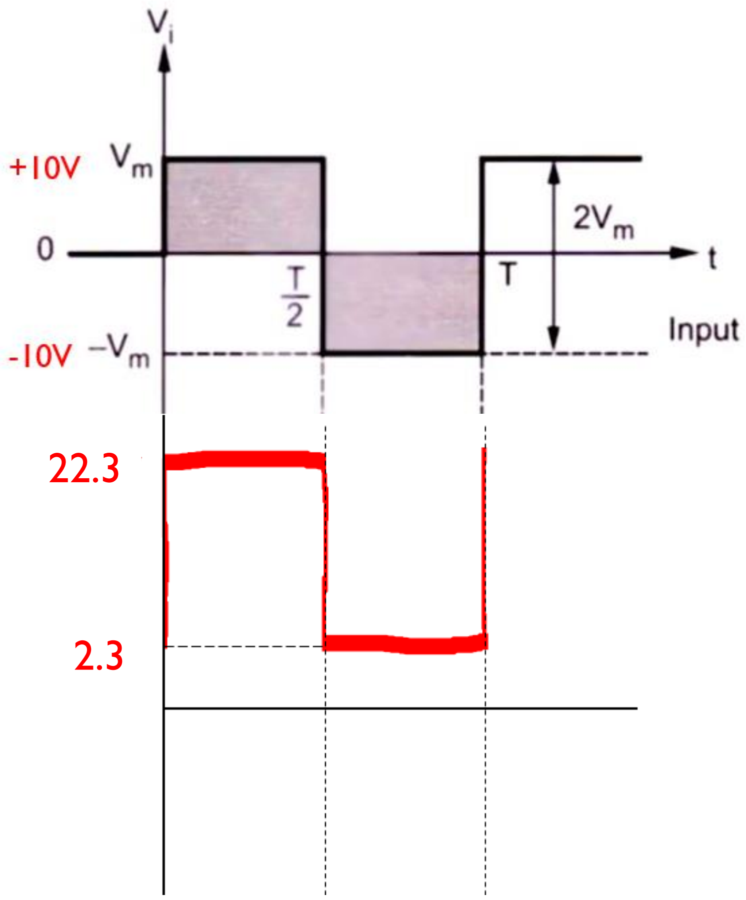
QSTN: Design a clamper circuit to get the following transfer characteristics, assuming voltage drop across the diodes 0.7V.







$-0.7 + X = 2.3$
$X = 2.3 + 0.7 = 3V$



DC LOAD LINE