Ext. No. 3

Date: 21 / 06 / 22

RC COUPLED AMPLIFIER

AIM:

Design an RC coupled amplifier using BJT for the following specifications and plot the frequency response curve.

Midband voltage gain = 60

Output voltage swing = 9V

COMPONENTS REQUIRED:

Transistor, dc source, capacitors, resistors, signal generator, CRO, breadboard.

THEORY:

Common emitter (CE) amplifier is widely used in audio frequency applications in radio and TV receivers. It provides current, voltage and power gains. For the proper functioning of an amplifier the transistor must be biased in the active region when the base current has a complete control over the collector current. Thus a small increase in the base current results in a relatively large increase in the collector current and a small decrease in base current is followed by a large decrease in collector current.

NPN transistor is connected as common emitter ac amplifier in which the voltage divider bias is employed. The name 'voltage divider' bias from the voltage divider network formed by the resistors R_1 and R_2. The voltage divider bias provides good stabilization so that the operating point can be made independent of the variations in h_{FE}. This is acheived by properly selecting the resistor values R_1 and R_2.

The input resistance of the amplifier $R_i = R_1 || R_2 || (1+h_{FE}) r_e$ with bypass capacitor C_E is connected and $R_i = R_1 || R_2 || (1+h_{FE})(r_e + R_E)$ with C_E is removed where r_e is the internal emitter resistance of the transistor. The resistance r_e is given by the expression $r_e = V_T / I_E$ where $V_T = 25mV$, i.e., the equivalent thermal voltage at room temperature. The output resistance of the amplifier $R_o \approx R_C$, where R_C is collector resistance.

The purpose of bypass capacitor C_E is to bypass signal current to the ground. The ac signal (feedback voltage) developed across the emitter resistor R_E is bypassed through the capacitor C_E. Thus the gain of the amplifier increases, since this bypassing reduces to negative feedback across R_E. This implies that when the bypass capacitor C_E is connected gain increases and bandwidth decreases and when it is disconnected, gain falls and bandwidth increases.

The purpose of coupling capacitors C_{C1} and C_{C2} is to couple the ac signal to the input and output of amplifier respectively. Meanwhile they block the dc signal and also determine the lowest frequency which is to be amplified.

PROCEDURE:

1] Check and verify the dc bias conditions without connecting capacitors and ac input signal.

2] Connect the capacitors in the circuit. Apply a 50mVpp sinusoidal signal from the function generator to input. Observe input and output waveform on CRO screen simultaneously.

3) Keep the input voltage constant at 50mVpp vary the frequency input signal from 0 to 1MHz and measure the output and enter in tabular column.

4) Plot the frequency response characteristic on graph with gain in dB on Y axis and f on x axis. Mark f_L and f_H corresponding to 3dB points in semilog graph.

5) Calculate bandwidth of amplifier using the expression

$$BW = f_H - f_L$$

6) Determine midband gain from the graph plotted

7) Calculate gain bandwidth product

8) Remove C_E from circuit and repeat steps 3 to 6. Observe that the bandwidth increases and gain decreases in absence of C_E.

DESIGN:

Selection of transistor:

→ Choose BC107 (minimum guaranteed $h_{FE} = 100$)

Max output swing = 9V

Let $I_C = 1mA$.

DC biasing conditions:

In order to fix the Q point at the middle of load line assume the DC conditions

$V_{RC} = 45\%$ of V_{CC}

$V_{CE} = 45\%$ of V_{CC}

$V_{RE} = 10\%$ of V_{CC}

Fixing Vcc:

Maximum output voltage swing $= 0.9V_{CC} = 9V$

$$V_{CC} = \frac{9}{0.9} = \underline{\underline{10V}}$$

Design of RC:

$V_{RC} = 45\%$ of $V_{CC} = 4.5$

$$R_C = \frac{V_{RC}}{I_C} = \frac{4.5}{1mA} = 4.5k\Omega \approx 4.7k\Omega$$

Design of RE:

$V_{RE} = 10\%$ of $V_{CC} = 1V$

$$R_E = \frac{V_{RE}}{I_E}$$

$$= \frac{V_{RE}}{I_C} = \frac{1V}{1mA} = 1k\Omega$$

Design of R1 and R2

Assume the current through $R_1 = 10I_B$ and that through $R_2 = 9I_B$ for a stable voltage across R_1 and R_2 independent of variations of base current.

$$V_{R2} = V_{BE} + V_{RE}$$

$$I_B = \frac{I_C}{h_{fe}} = \frac{1mA}{100} = 0.01mA$$

$$R_2 = \frac{V_{R2}}{9I_B} = \frac{V_{BE} + V_{RE}}{9I_B}$$

$$= \frac{0.65+1}{0.09mA} = 18.3k\Omega = 18k\Omega$$

$$R_1 = \frac{V_{R1}}{10I_B} = \frac{V_{CC} - V_{R2}}{10I_B}$$

$$= \frac{10-1.65}{0.1} = 83.5k\Omega \approx 82k\Omega$$

Design of RL

Gain of CE amplifier is given by the expression

$$A_V = \frac{-(R_C \| R_L)}{r_e}$$

$r_e \rightarrow$ resistance of base emitter diode

$$r_e = \frac{V_T}{I_E} = \frac{V_T}{I_C} \approx \frac{26mV}{1mA} = 26\Omega$$

$$-60 = \frac{R_C R_L}{(R_C + R_L) r_e} \qquad R_L \approx 2.7k\Omega$$

Design of C_{C1} and C_{C2}

X_{CC1} should be less than the input impedance of transistor

$$X_{CC1} << R_{in}$$

Here $R_{in} = R_1 // R_2 // h_{fe} \cdot r_e$

$$r_e = R_1 // R_2 // \beta r_e$$

$$\frac{1}{2\pi f_L C_{C1}} = \frac{R_{in}}{10} \text{ and}$$

$$f_L = 100Hz$$

$$C_{C1} = \frac{10}{2\pi f_L R_{in}} = 7.2\mu F \approx 10\mu F$$

Similarly,

$$X_{CC2} << R_{out}$$

$$R_{out} = R_C$$

$$\frac{1}{2\pi f_L C_{C2}} = \frac{R_{out}}{10} = \frac{R_C}{10}$$

$$C_{C2} = \frac{10}{2\pi f_L R_C} = 3.3\mu \approx 10\mu F$$

Design of C_E:

To bypass the lower frequency X_{CE} should be less than or equal to R_E

$$X_E = \frac{R_E}{10}$$

$$\frac{1}{2\pi f_L C_E} = \frac{R_E}{10}$$

$$C_E = \frac{10}{2\pi f_L R_E} = 15.9\mu F \approx 22\mu F$$

RESULT:

Designed RC coupled amplifier using BJT and plotted the frequency response curve.

Lower cut-off frequency, $f_1 = 500Hz$

Upper cut-off frequency, $f_2 = 400\times10^3 Hz$

Bandwidth $= f_2 - f_1$

$= 400\times10^3 - 500$

$= 399500 Hz$

$= 399.5 kHz$

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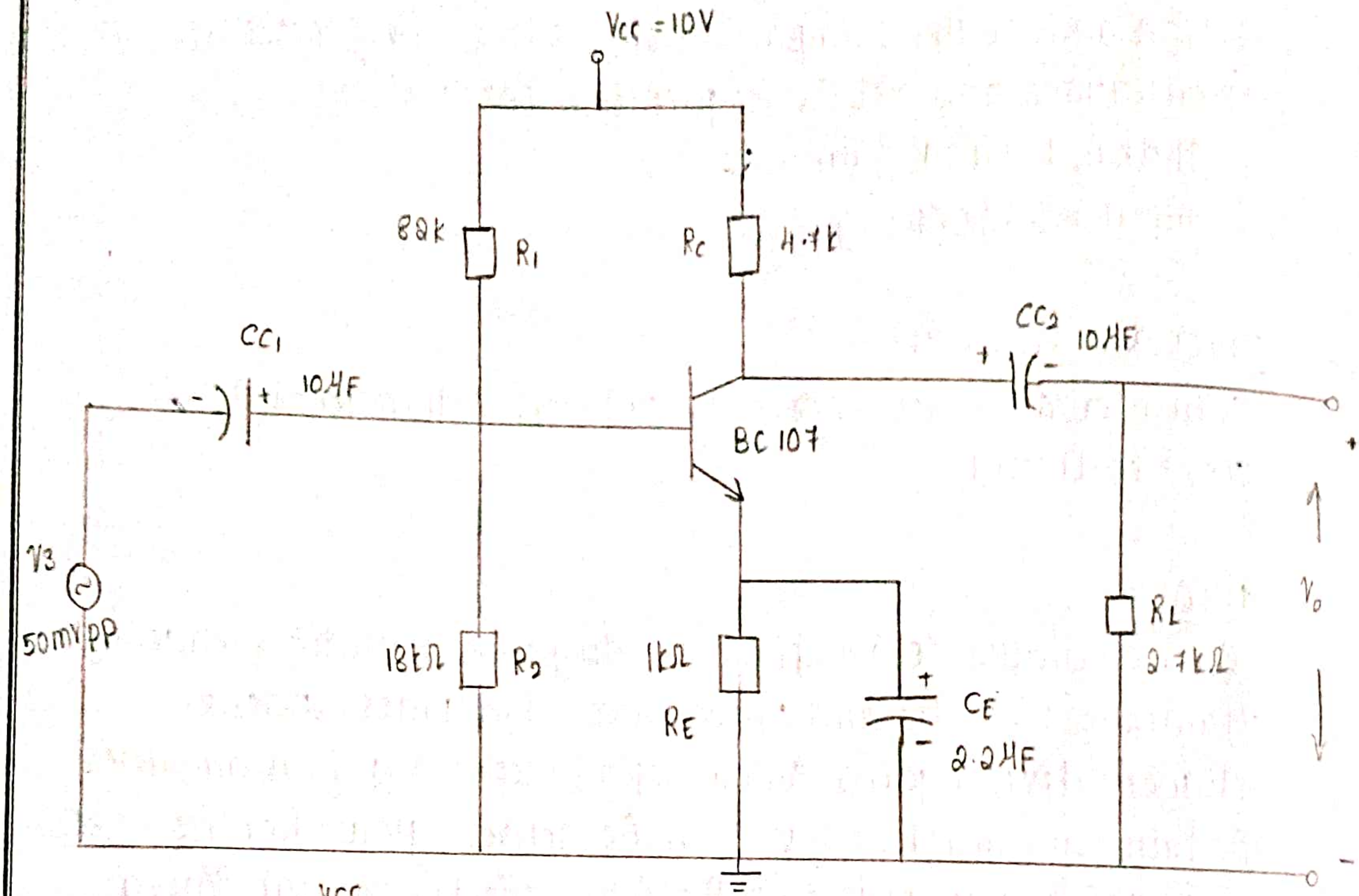
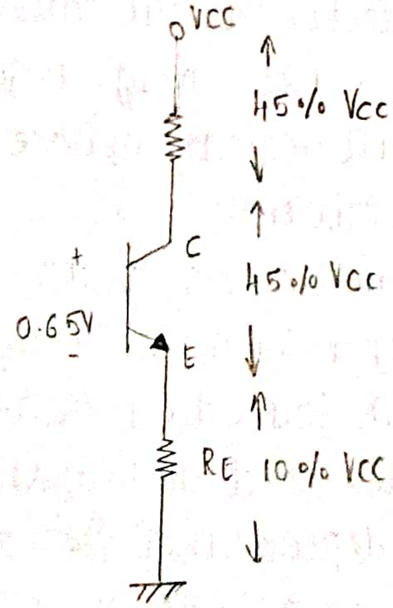
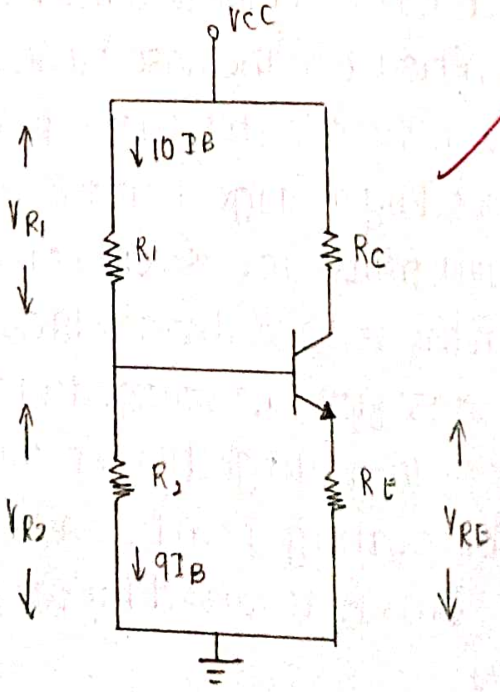
CIRCUIT DIAGRAM



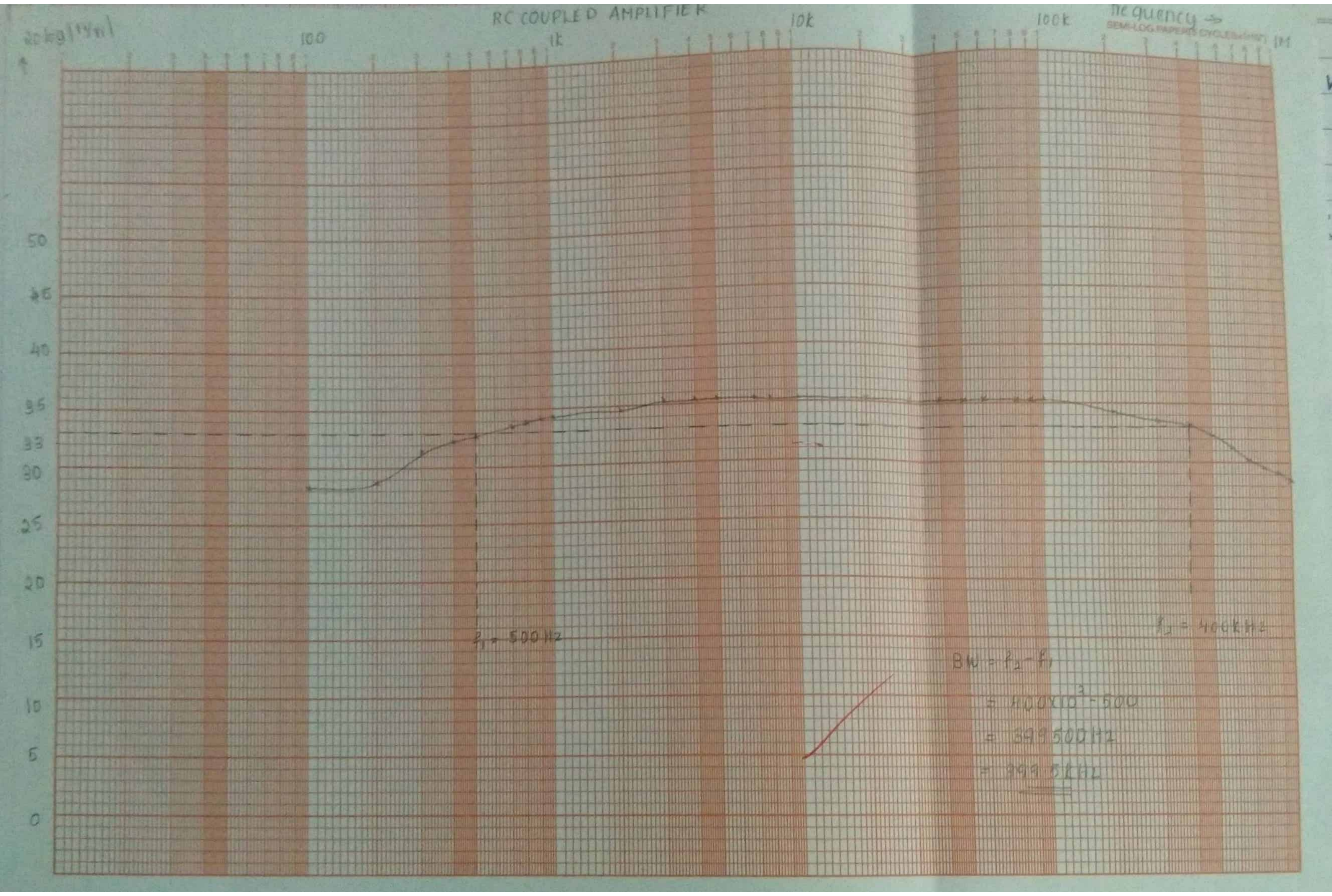




OBSERVATION:

$V_i = 50 mV_{pp}$

freq	V_o	V_o/V_i	$20\log(V_o/V_i)$	freq	V_o	V_o/V_i	$20\log(V_o/V_i)$
100	1.3	26	28.2994	60k	2.88	57.6	35.2085
200	1.4	28	28.9431	80k	2.88	57.6	35.2085
300	1.9	38	31.5956	100k	2.88	57.6	35.2085
400	2	40	32.0412	200k	2.6	52	34.3201
500	2.2	44	32.8690	300k	2.4	48	33.6248
700	2.4	48	33.6248	400k	2.3	46	33.2552
800	2.5	50	33.9794	500k	2.1	42	32.4650
900	2.56	51.2	34.1854	600k	1.8	36	31.1261
1k	2.6	52	34.3201	700k	1.6	32	30.1030
2k	2.8	56	34.9638	800k	1.4	28	28.9432
3k	2.88	57.6	35.2085	900k	1.3	26	28.2995
4k	2.88	57.6	35.2085	1M	1.2	24	27.6042
5k	2.88	57.6	35.2085	2M	0.92	18.4	25.2964
10k	2.88	57.6	35.2085				
20k	2.88	57.6	35.2085				
30k	2.88	57.6	35.2085				
40k	2.88	57.6	35.2085				
50k	2.88	57.6	35.2085				



RC COUPLED AMPLIFIER
20log(Vo/Vi)
frequency →
SEMI-LOG PAPER 5 CYCLES
100
1k
10k
100k
1M
50
45
40
35
33
30
25
20
15
10
5
0
f1 = 500 Hz
f2 = 400kHz
BW = f2 - f1
= 400×10^3 - 500
= 399500 Hz
= 399.5kHz