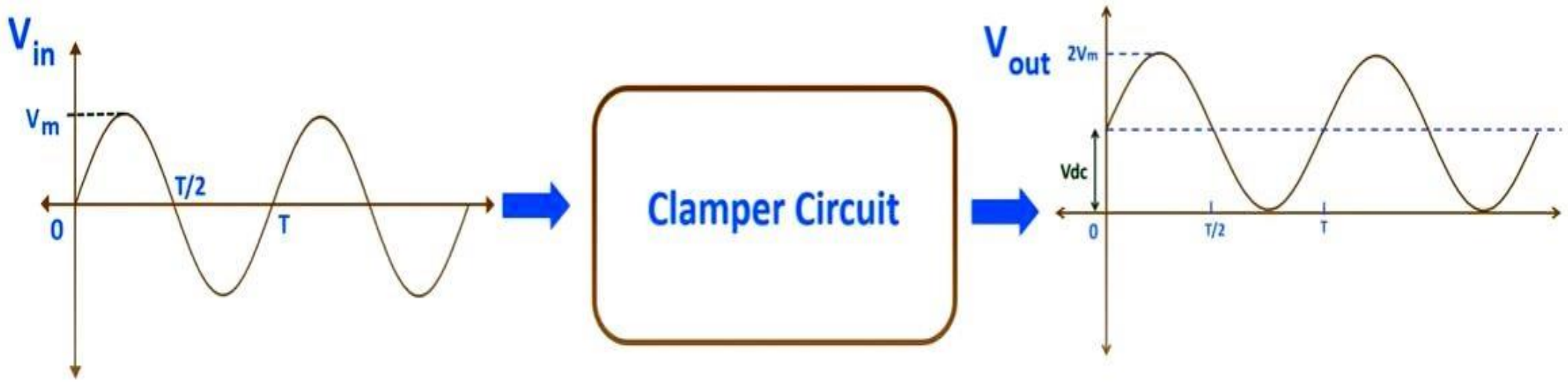
CLAMPER CIRCUIT

- A Clamper circuit is a circuit that shifts the waveform to a desired DC level without changing the actual appearance of the applied signal.
- consists of a diode, a resistor and a capacitor
- Clamper circuits consist of energy storage elements like capacitors
- Clamper circuit changes the DC level of the signal to the desired level without changing the shape of the signal. (**DC Restorers**)

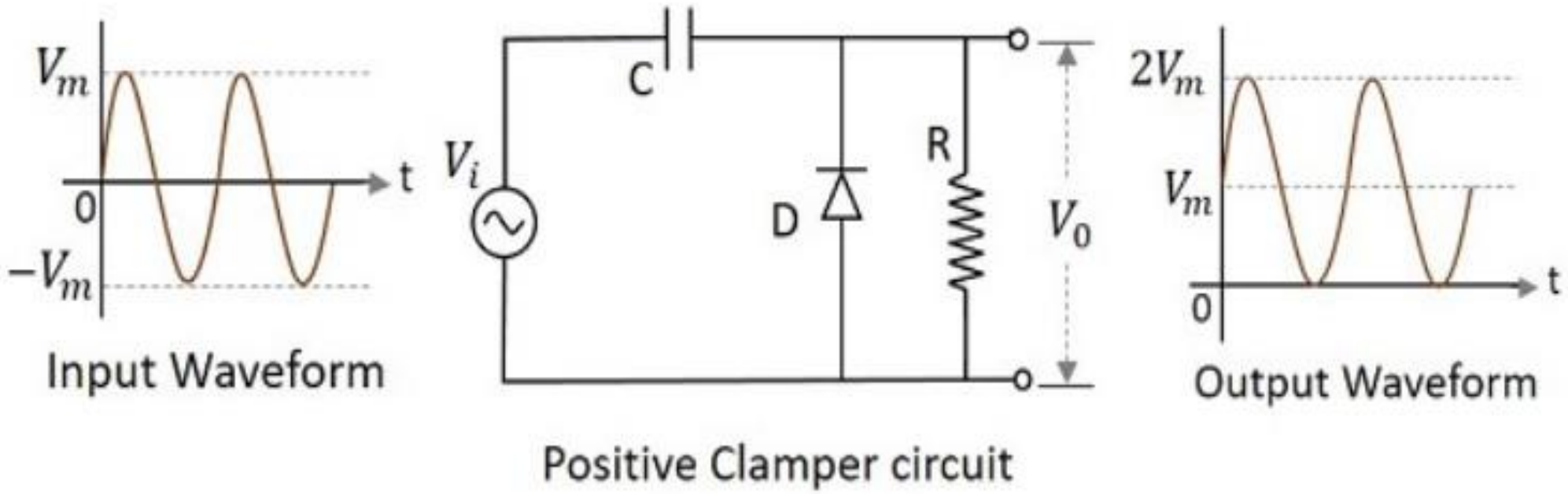


CLAMPER CIRCUIT - CLASSIFICATION

- POSITIVE CLAMPER
- NEGATIVE CLAMPER
- BIASED CLAMPER

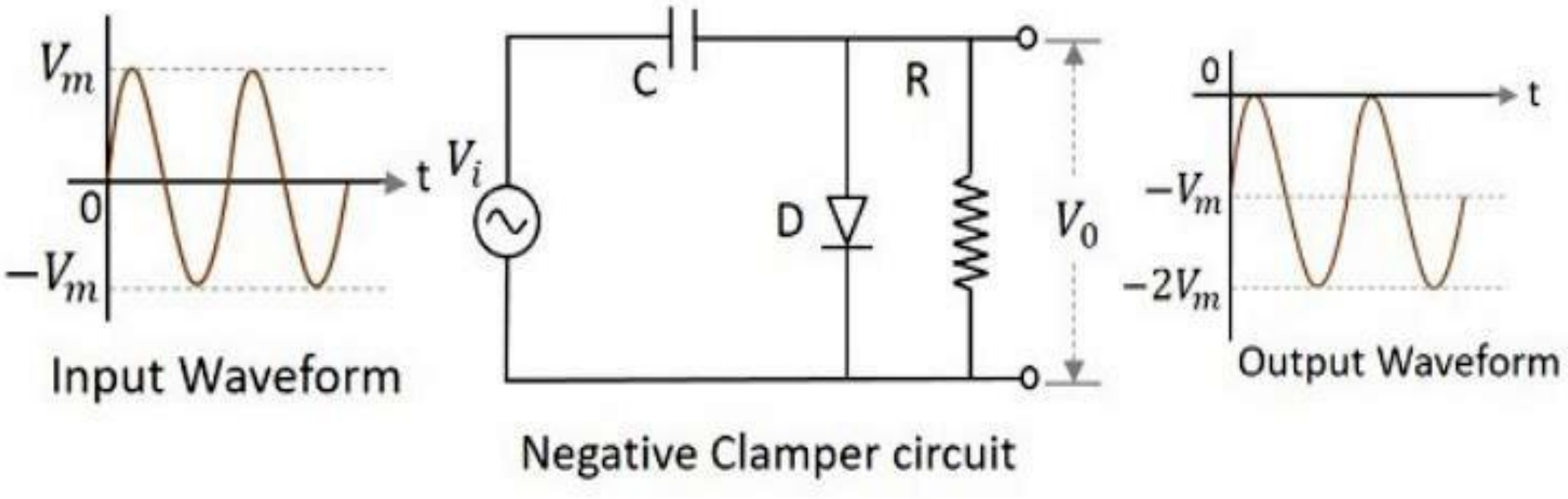
POSITIVE CLAMPER

- A Clamper circuit that shifts the input waveform **above** the input DC reference level or voltage



NEGATIVE CLAMPER

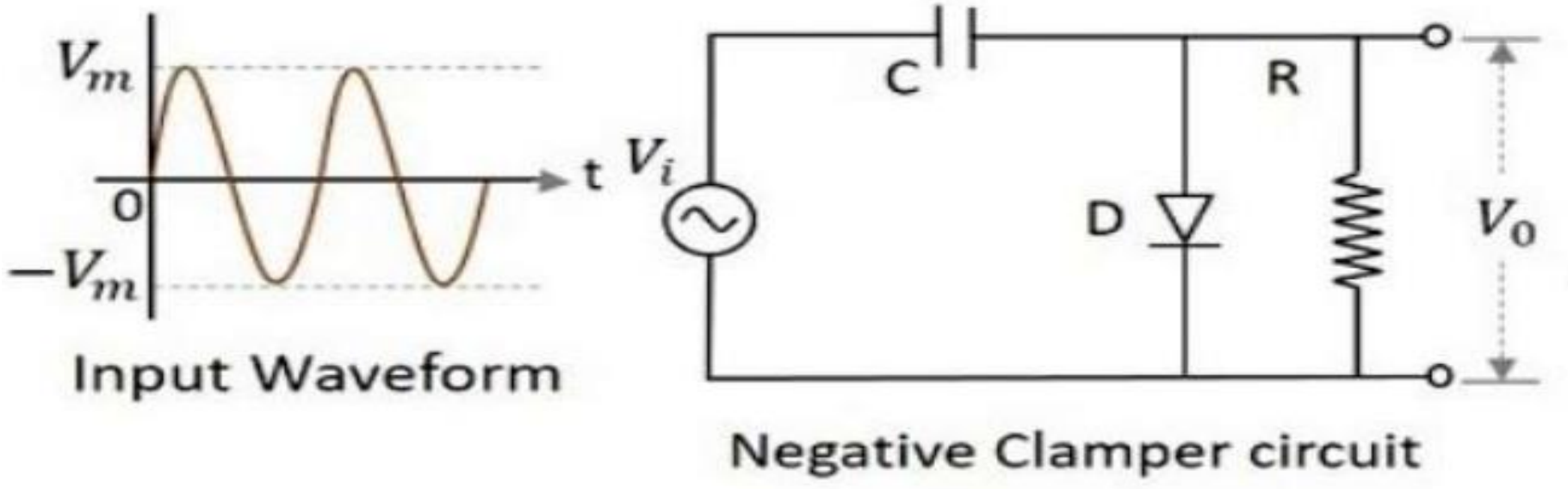
- A Clamper circuit that shifts the input waveform **below** the input DC reference level or voltage



BIASED CLAMPER

- Positive or Negative Clamper circuit with a Biased Voltage.
- contains Diode, Resistor, Capacitor with a Biased Voltage source.
- Biased clampers are divided into
  - Biased Positive Clamper with Positive Bias
  - Biased Positive Clamper with Negative Bias
  - Biased Negative Clamper with Positive Bias
  - Biased Negative Clamper with Negative Bias

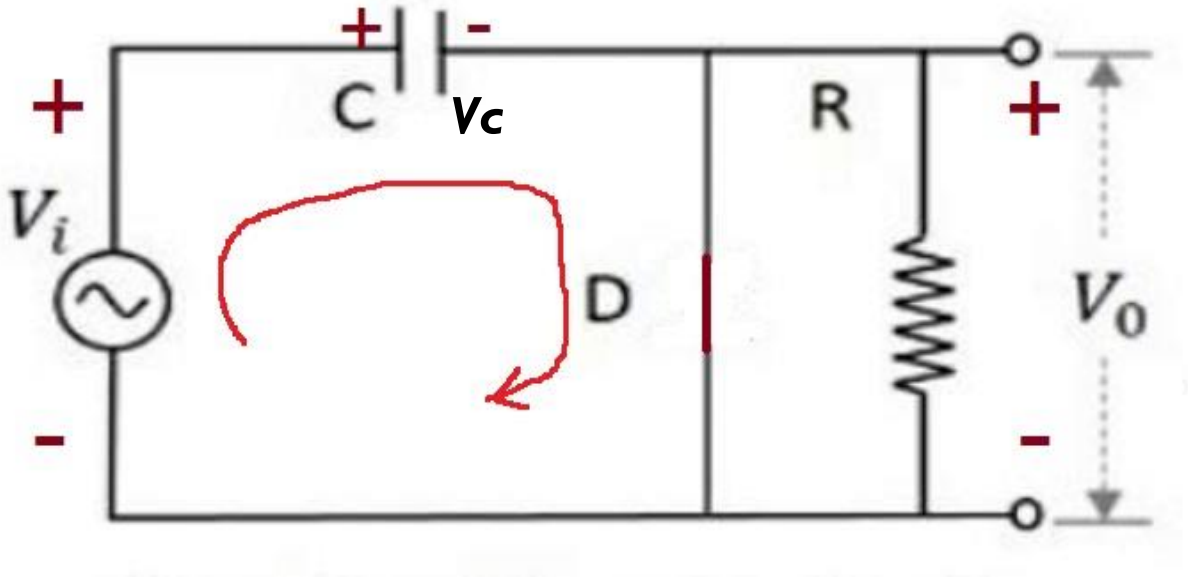
NEGATIVE CLAMPER



- Assume Diode is Ideal
- Time Constant (RC) very much larger than input Time period

NEGATIVE CLAMPER

POSITIVE HALF CYCLE



- Diode FB, Short Circuited
- No voltage across output
- Capacitor Charges to Vm voltage.

From Circuit

$Vo = \mathbf{0}$

From KVL

$Vi - Vc = 0$

$Vc = Vi = Vm$

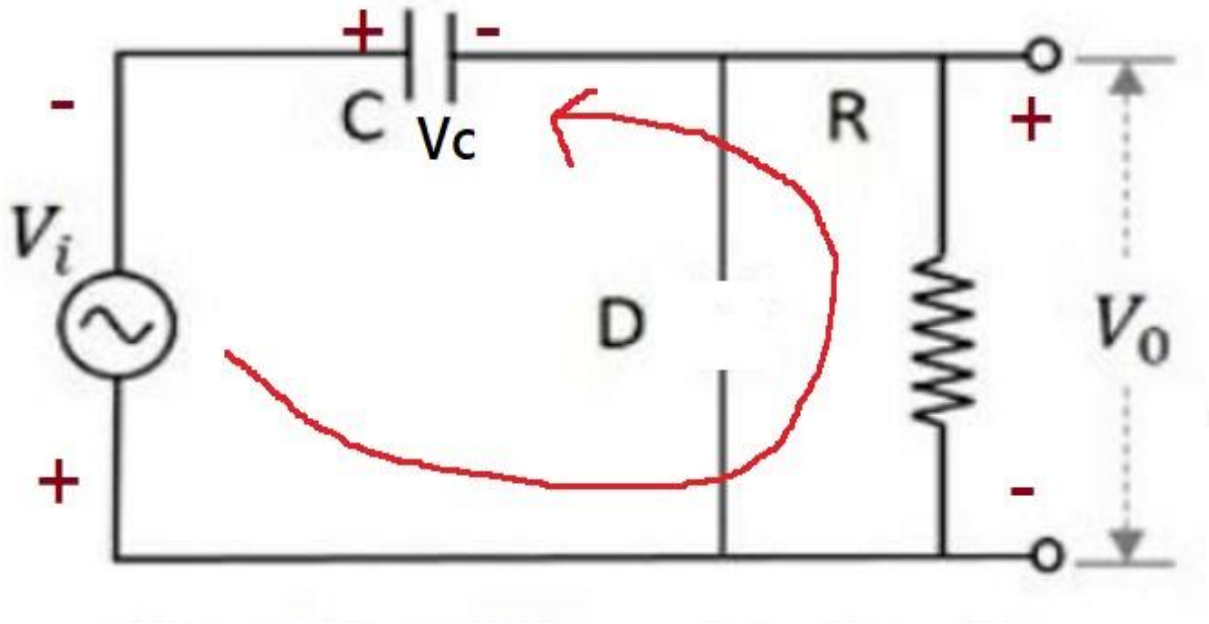
NEGATIVE CLAMPER

POSITIVE HALF CYCLE

- During the positive half cycle of the input AC signal, the diode is forward biased and hence no signal appears at the output.
- In forward biased condition, the diode allows electric current through it. This current will flows to the capacitor & charges it to the peak value of input voltage in inverse polarity -Vm
- As input current or voltage decreases after attaining its maximum value Vm, the capacitor holds the charge until the diode remains forward biased.

NEGATIVE CLAMPER

NEGATIVE HALF CYCLE



- Diode RB, Open Circuited
- Capacitor Discharges Vm voltage across the resistor
- voltage across output is -2Vm

We know

$Vc = Vi = Vm$

From KVL

$Vi + Vo + Vc = 0$

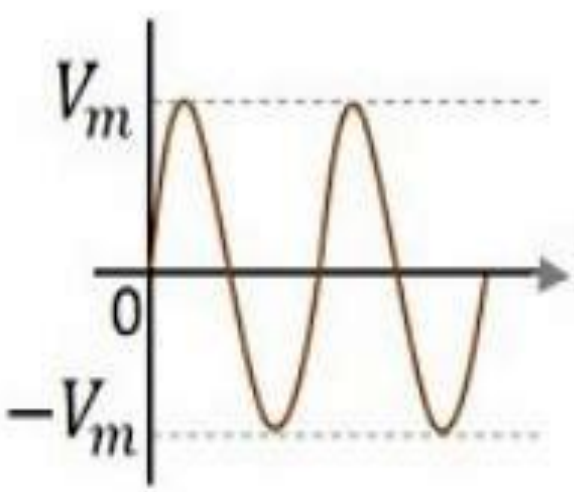
$Vo = - Vi - Vc =$ ***-2Vm***

NEGATIVE CLAMPER

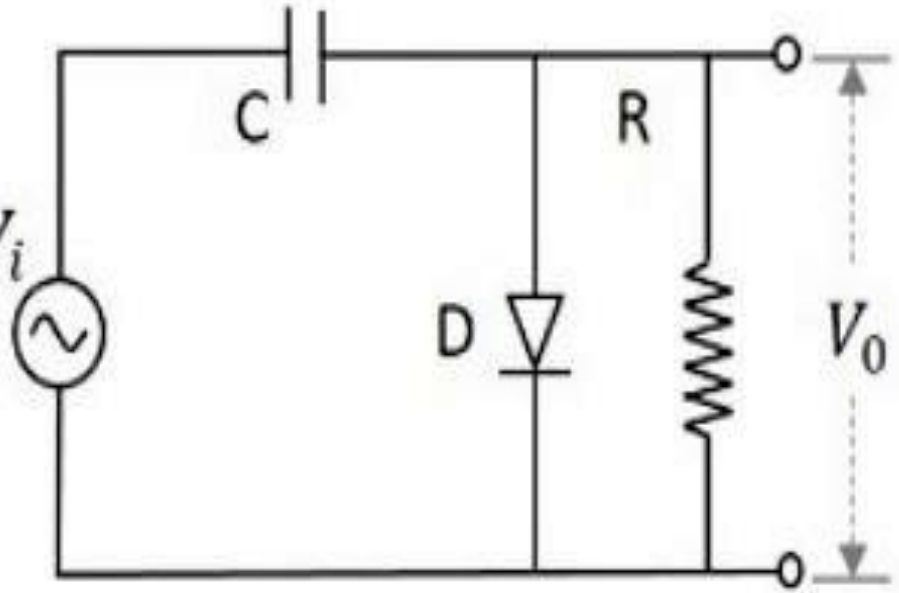
NEGATIVE HALF CYCLE

- During the negative half cycle of the input AC signal, the diode is reverse biased and hence the signal appears at the output.
- In reverse biased condition, the diode does not allow electric current through it. So the input current directly flows towards the output.
- When the negative half cycle begins, the diode is in the non-conducting state and the charge stored in the capacitor is discharged (released).
- Therefore, the voltage appeared at the output is equal to the sum of the voltage stored in the capacitor (***-Vm***) and the input voltage (***-Vm***) {I.e. ***Vo = -Vm- Vm = -2Vm***}
- As a result, the signal shifted downwards.

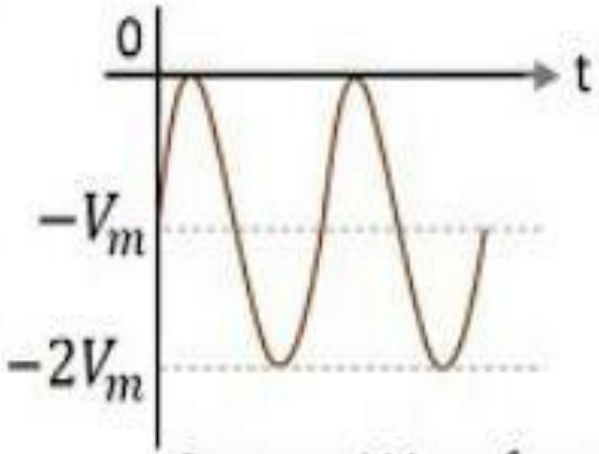
NEGATIVE CLAMPER



Input Waveform

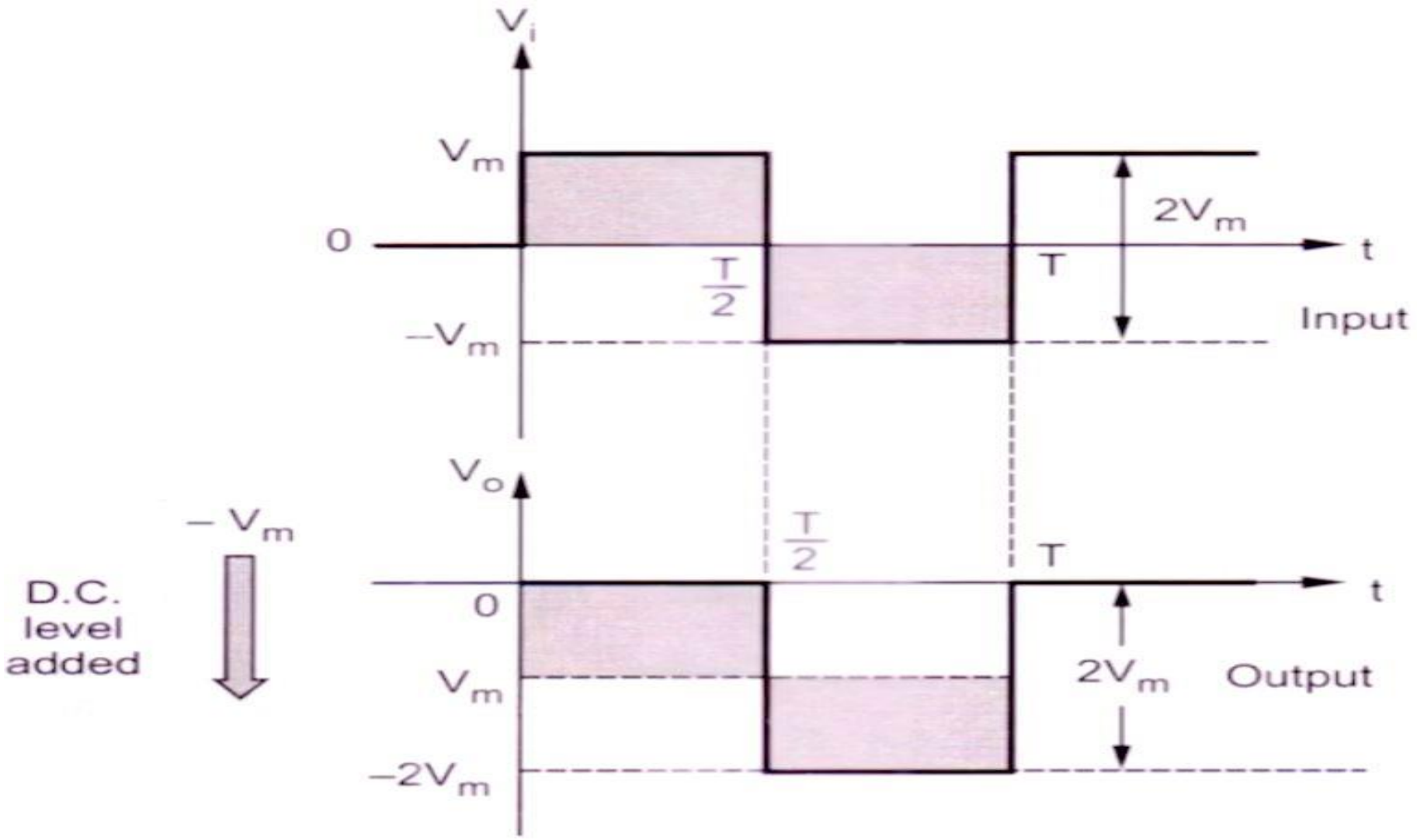


Negative Clamper circuit

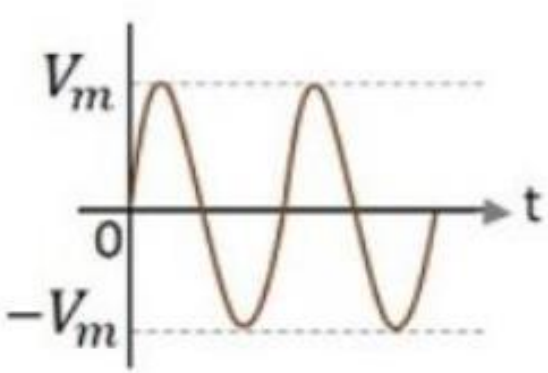


Output Waveform

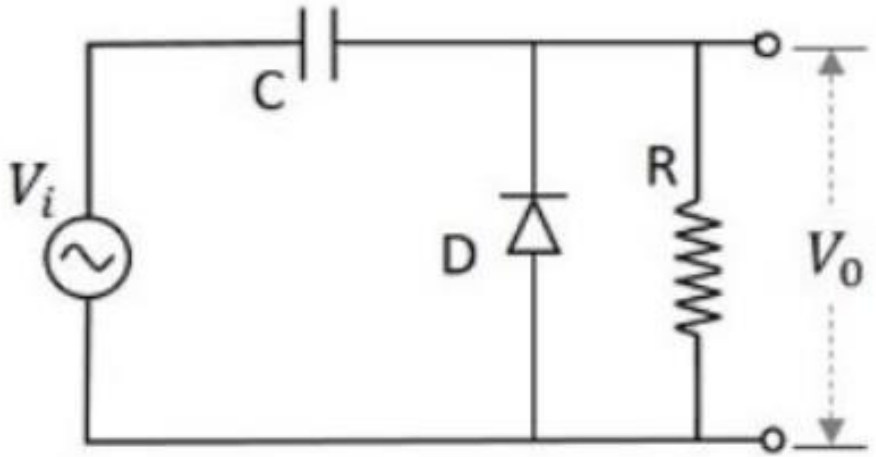
NEGATIVE CLAMPER



POSITIVE CLAMPER



Input Waveform

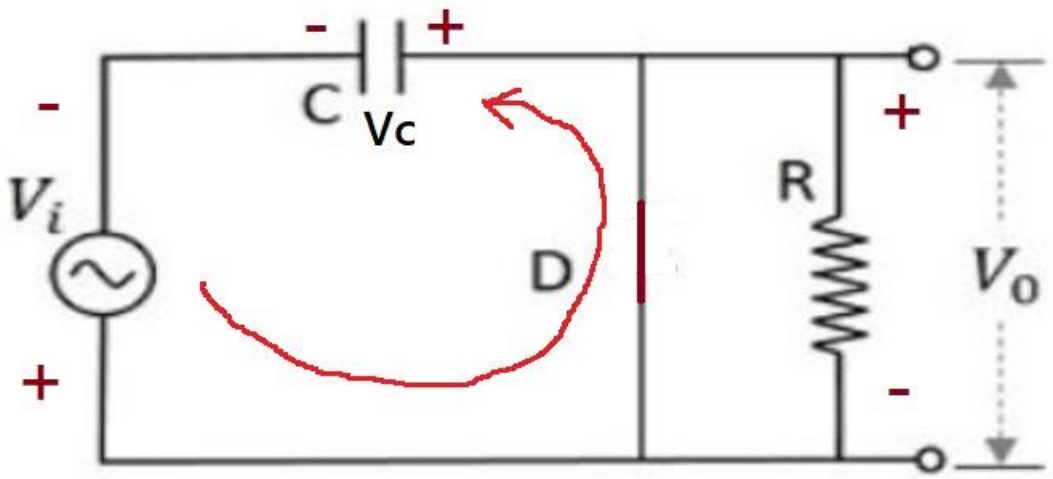


Positive Clamper circuit

- Assume Diode is Ideal
- Time Constant (RC) very much larger than input Time period

POSITIVE CLAMPER

NEGATIVE HALF CYCLE



- Diode FB, Short Circuited
- No voltage across output
- Capacitor Charges to Vm voltage.

From Circuit

$Vo = \mathbf{0}$

From KVL

$Vi - Vc = 0$

$Vc = Vi = Vm$

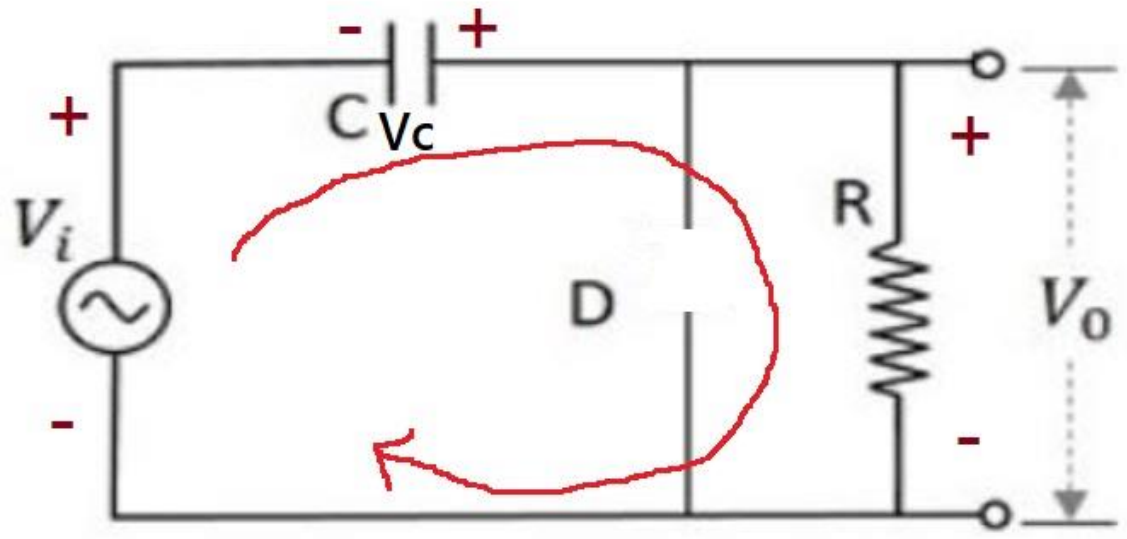
POSITIVE CLAMPER

NEGATIVE HALF CYCLE

- During the negative half cycle of the input AC signal, the diode is forward biased and hence no signal appears at the output.
- In forward biased condition, the diode allows electric current through it. This current will flows to the capacitor and charges it to the peak value of input voltage Vm.
- The capacitor charged in inverse polarity (positive) with the input voltage.
- As input current or voltage decreases after attaining its maximum value -Vm, the capacitor holds the charge until the diode remains forward biased.

POSITIVE CLAMPER

POSITIVE HALF CYCLE



- Diode RB, Open Circuited
- Capacitor Discharges Vm voltage across the resistor
- voltage across output is +2Vm

We know

$Vc = Vi = Vm$

From KVL

$Vi + Vc - Vo = 0$

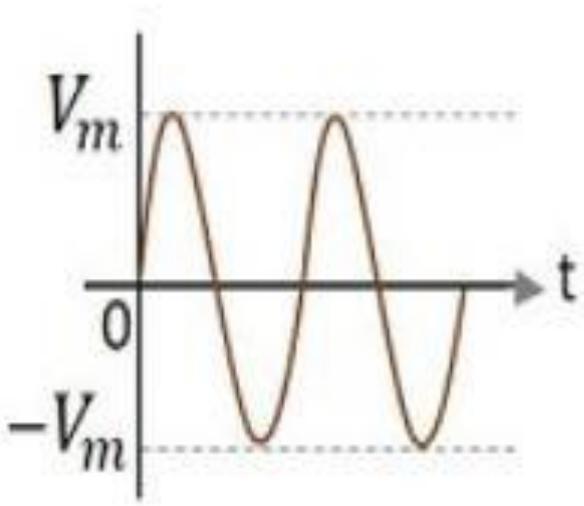
$Vo = Vi + Vc =$ ***2Vm***

POSITIVE CLAMPER

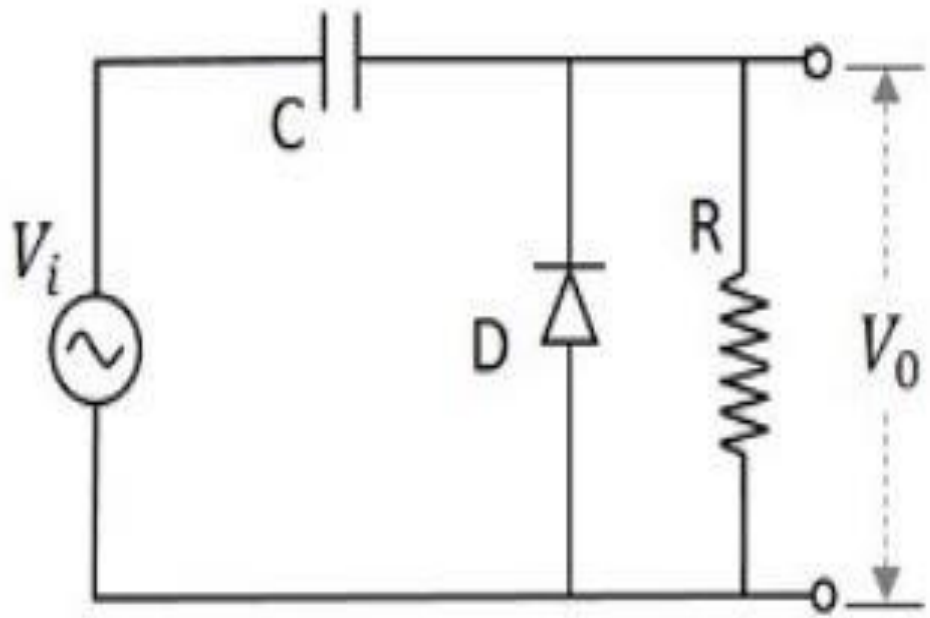
POSITIVE HALF CYCLE

- During the positive half cycle of the input AC signal, the diode is reverse biased and hence the signal appears at the output.
- In reverse biased condition, the diode does not allow electric current through it. So the input current directly flows towards the output.
- When the positive half cycle begins, the diode is in the non-conducting state and the charge stored in the capacitor is discharged (released).
- Therefore, the voltage appeared at the output is equal to the sum of the voltage stored in the capacitor (***Vm***) and the input voltage (***Vm***) { I.e. ***Vo = Vm+ Vm = 2Vm***}
- As a result, the signal shifted upwards.

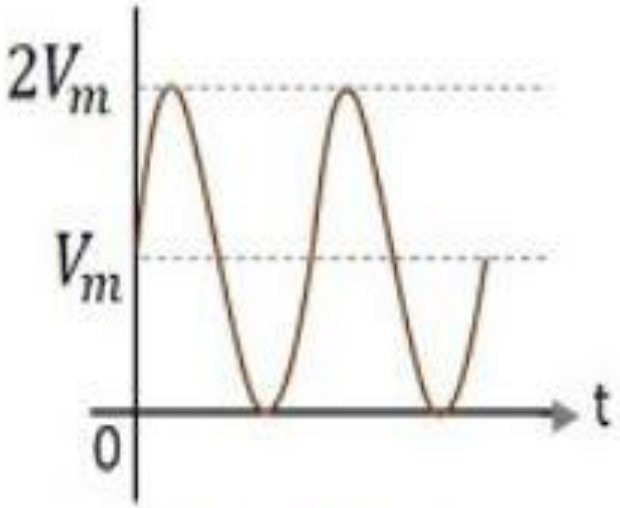
POSITIVE CLAMPER



Input Waveform



Positive Clamper circuit

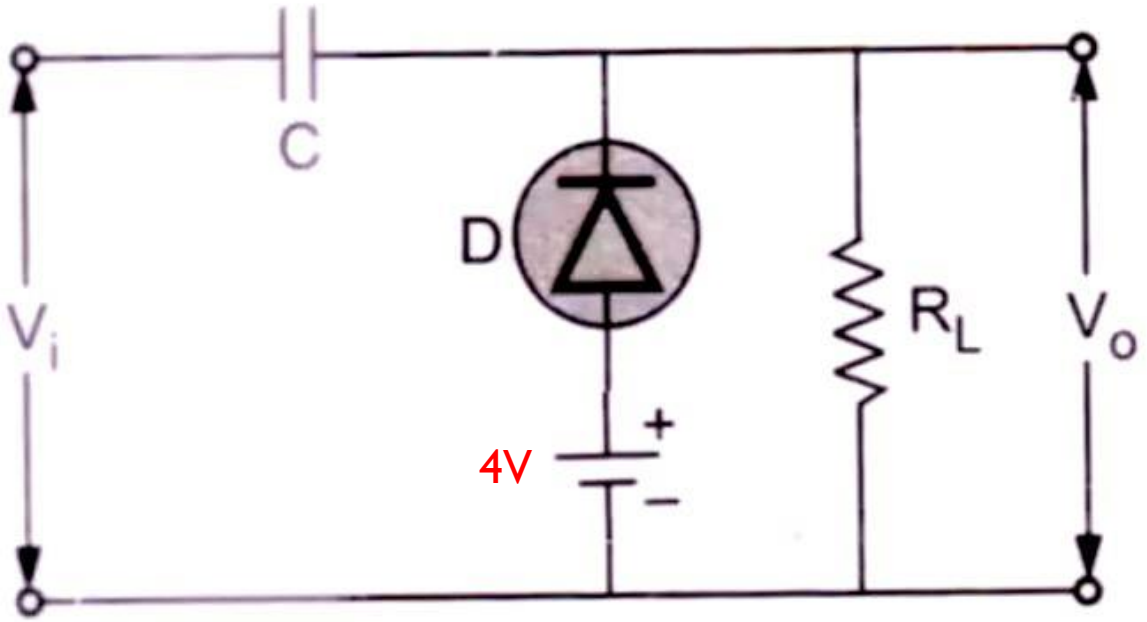


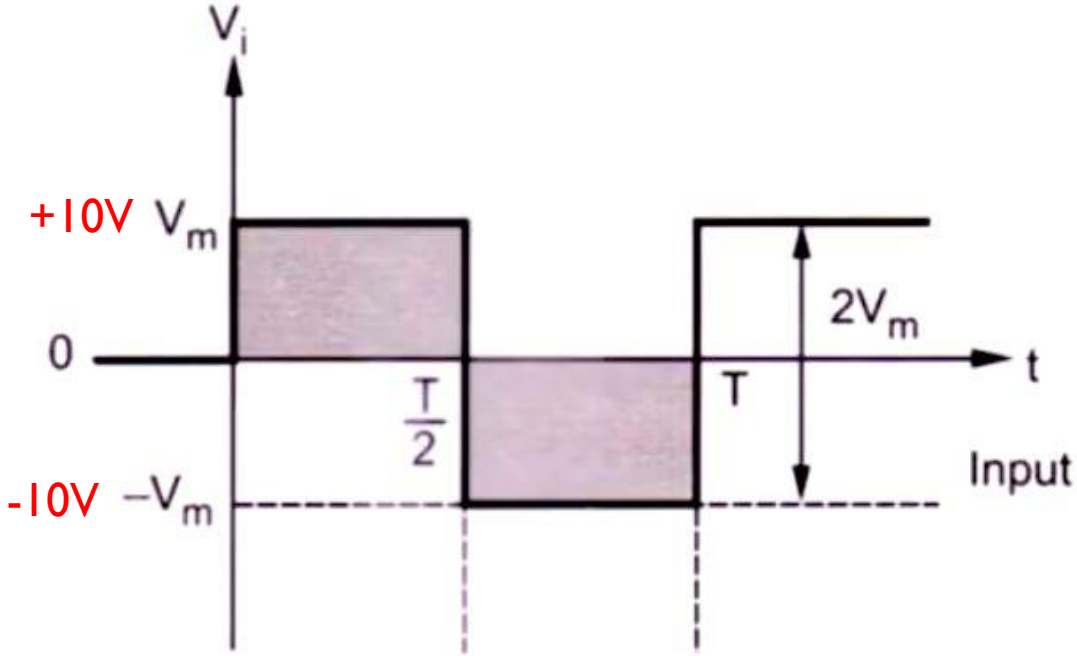
Output Waveform

BIASED CLAMPER CIRCUITS

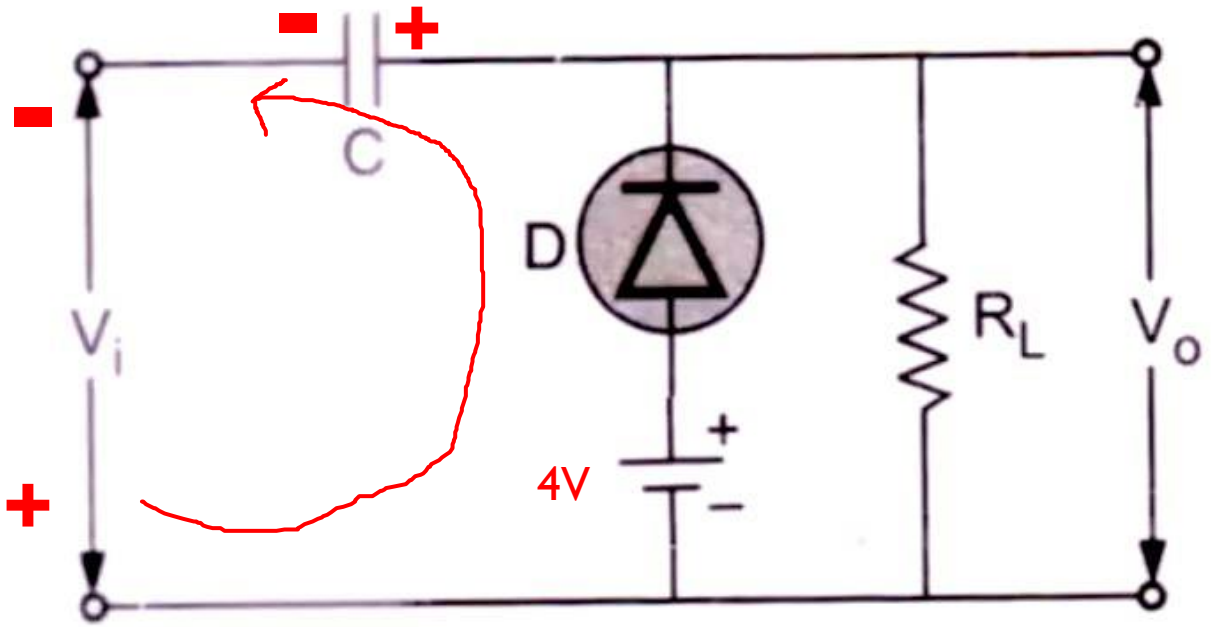
- BIASED POSITIVE CLAMPER WITH POSITIVE BIAS
- BIASED POSITIVE CLAMPER WITH NEGATIVE BIAS
- BIASED NEGATIVE CLAMPER WITH POSITIVE BIAS
- BIASED NEGATIVE CLAMPER WITH NEGATIVE BIAS

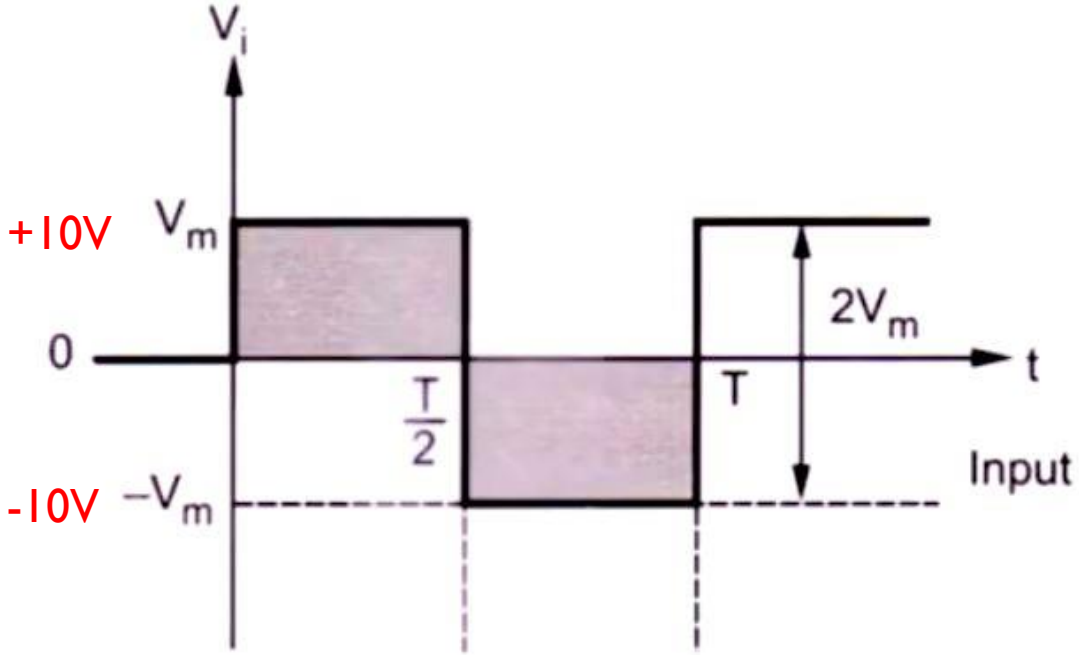
BIASED POSITIVE CLAMPER (POSITIVE BIASED)





BIASED POSITIVE CLAMPER (POSITIVE BIASED)





-ve Half Cycle

0 to -10V ▌ Diode FB ▌ Vo = +4V

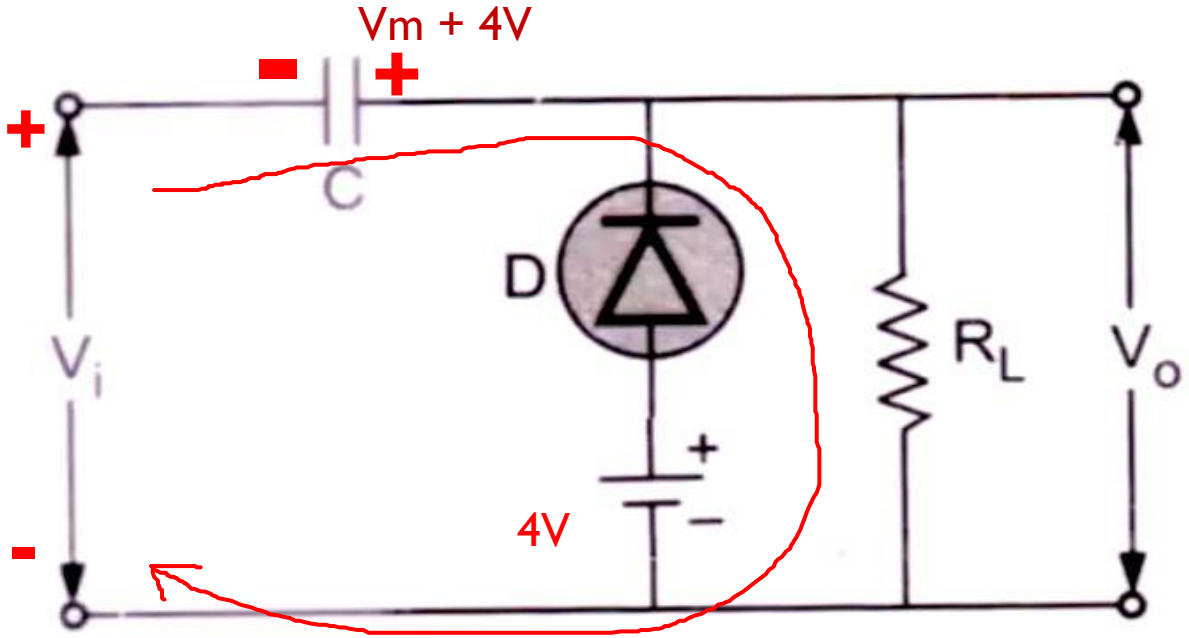
KVL:

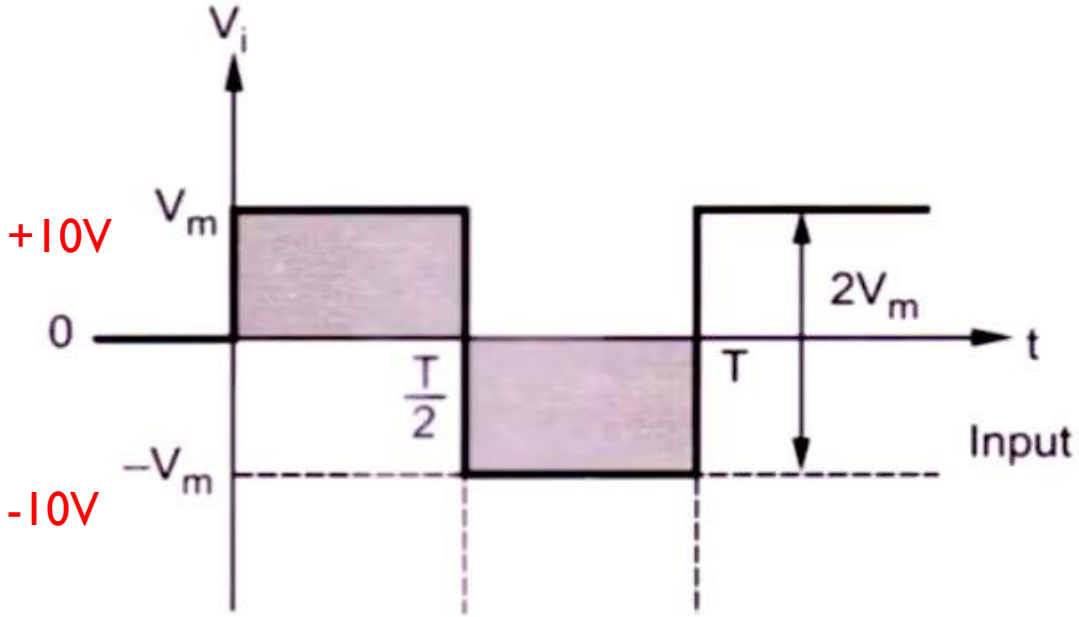
Vi + 4V – Vc = 0

Vc = Vi + 4V = 10 + 4V = 14V

- In Complete Negative Half Cycle Diode will be Forward Biased.
- Output Voltage will be +4V.
- Capacitor charges to Vm + 4V

BIASED POSITIVE CLAMPER (POSITIVE BIASED)





+ve Half Cycle

0 to +4V ▌Diode FB ▌

+4V to +10V ▌Diode RB ▌

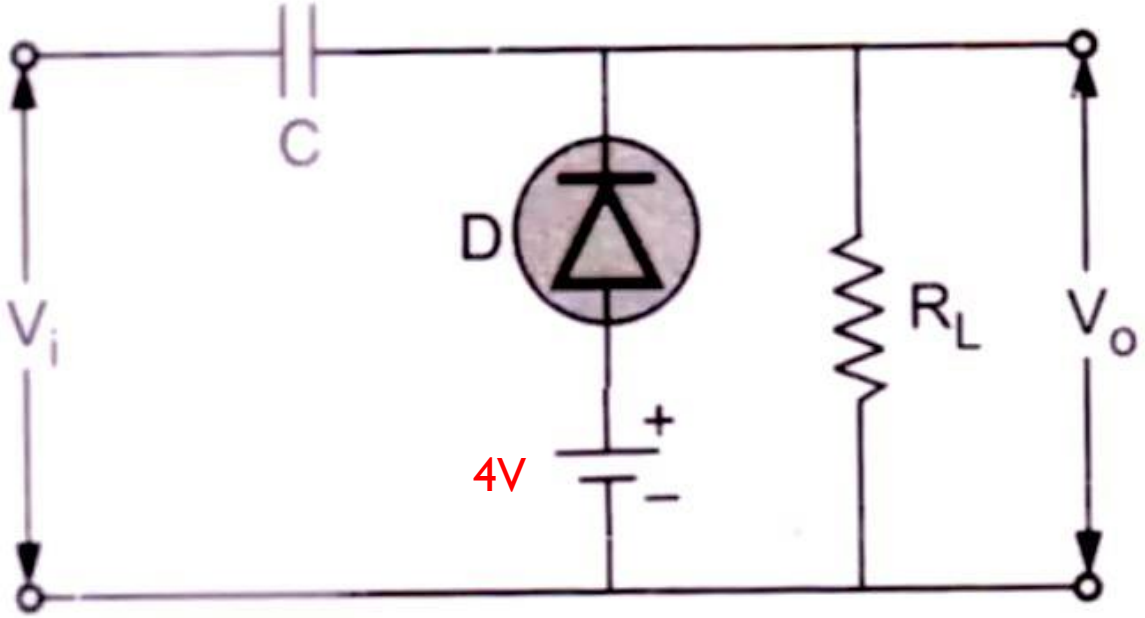
KVL:

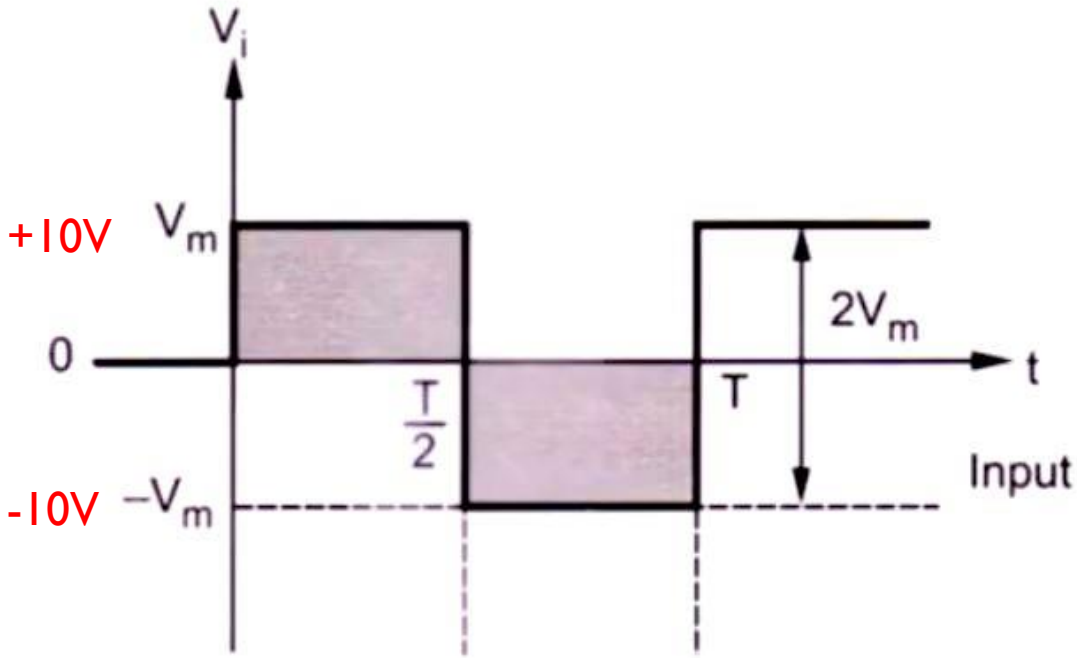
Vi + Vc – Vo = 0 ; Vo = Vi + Vc

Vo = Vm + Vm + 4V = 10 + 10V + 4V = 24V

- Diode FB till +4V, Diode RB from +4V to +10V
- When Diode RB, capacitor discharges already charged Vm + 4V.
- Output Voltage will be 2Vm + 4V = 24V

BIASED POSITIVE CLAMPER (POSITIVE BIASED)





+ve Half Cycle

Vo = Vi + Vc + Battery Voltage

Vo = Vm + Vm + (+4V)

Vo = 10 + 10 + 4 = 24V

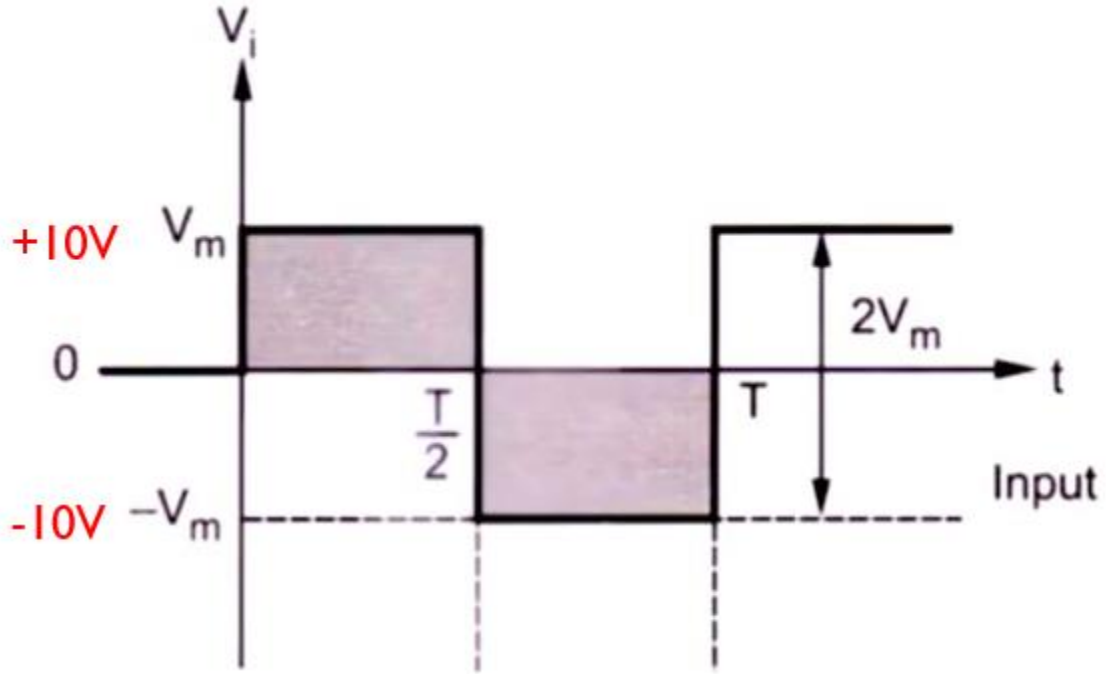
-ve Half Cycle

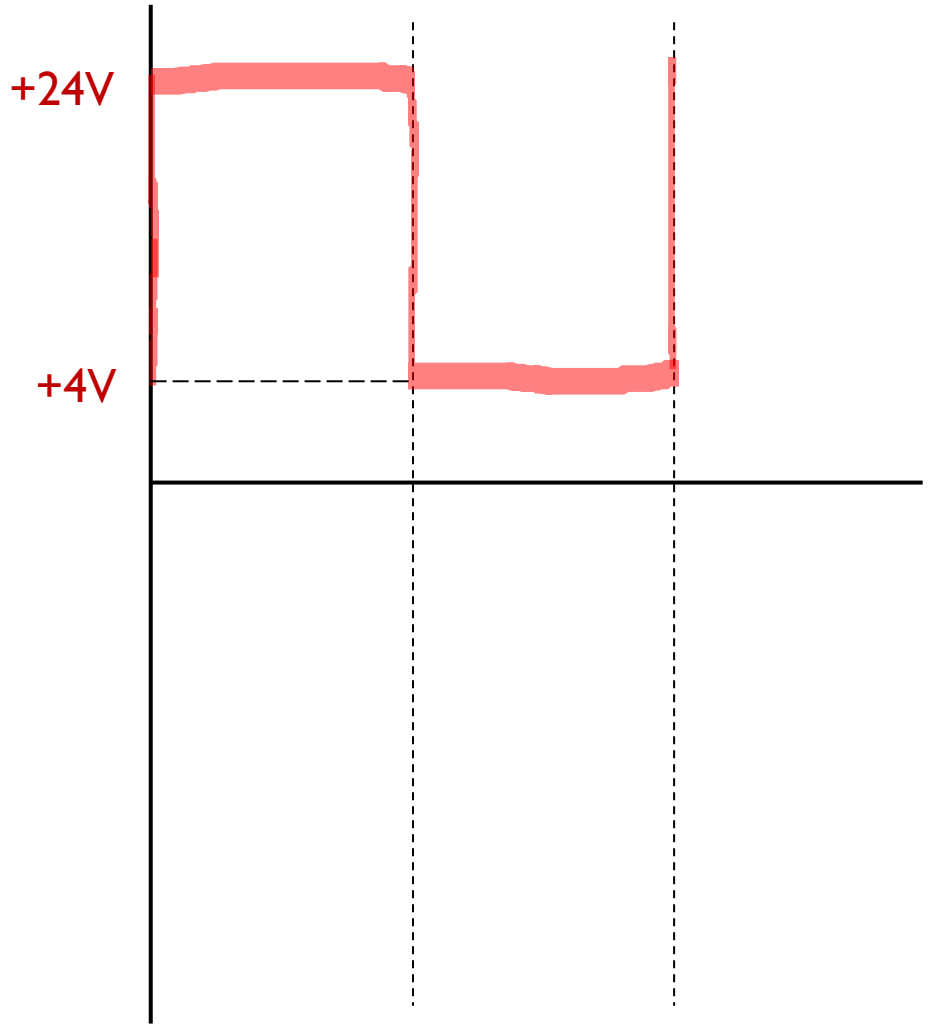
Vo = 0 + Battery Voltage

Vo = 0 + (+4V)

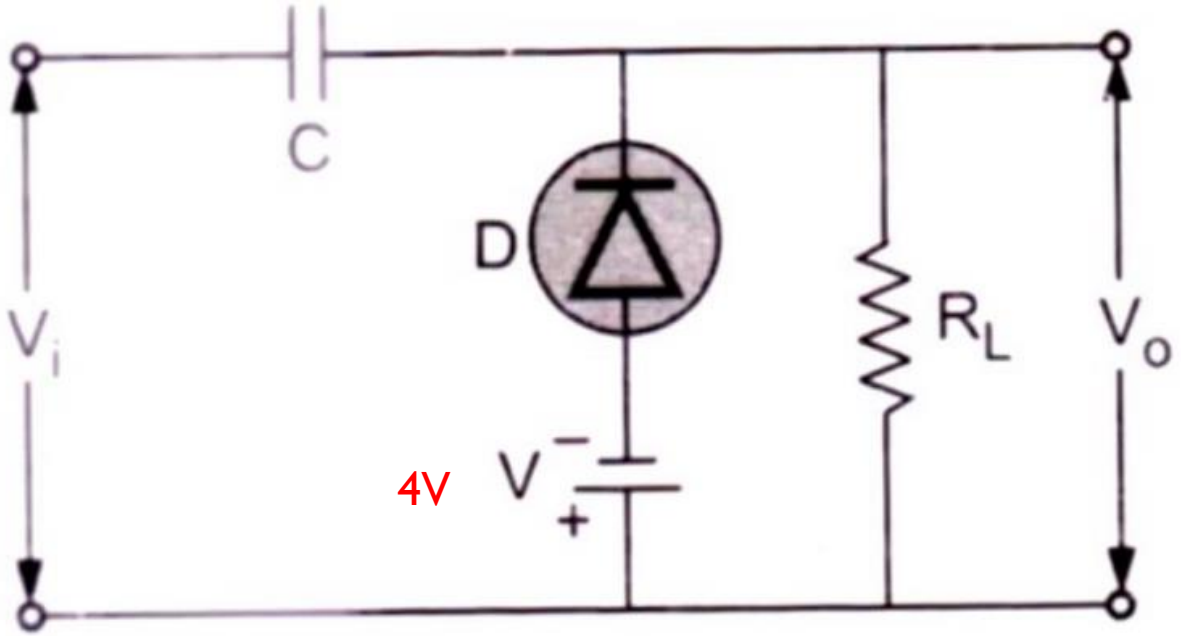
Vo = 0 + 4 = 4V

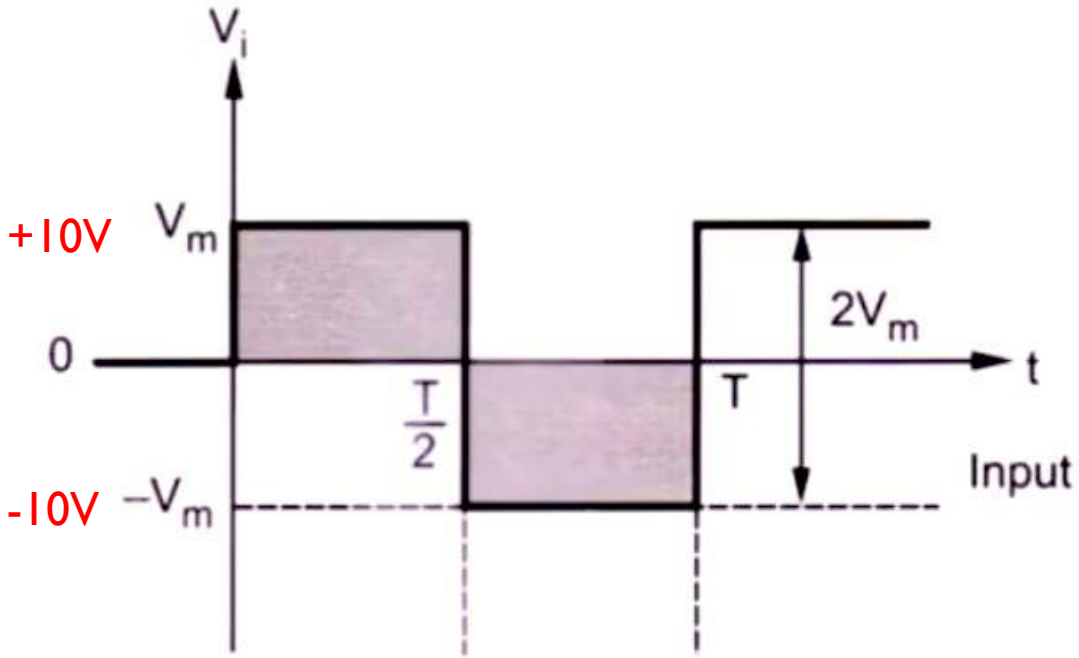
BIASED POSITIVE CLAMPER (POSITIVE BIASED)



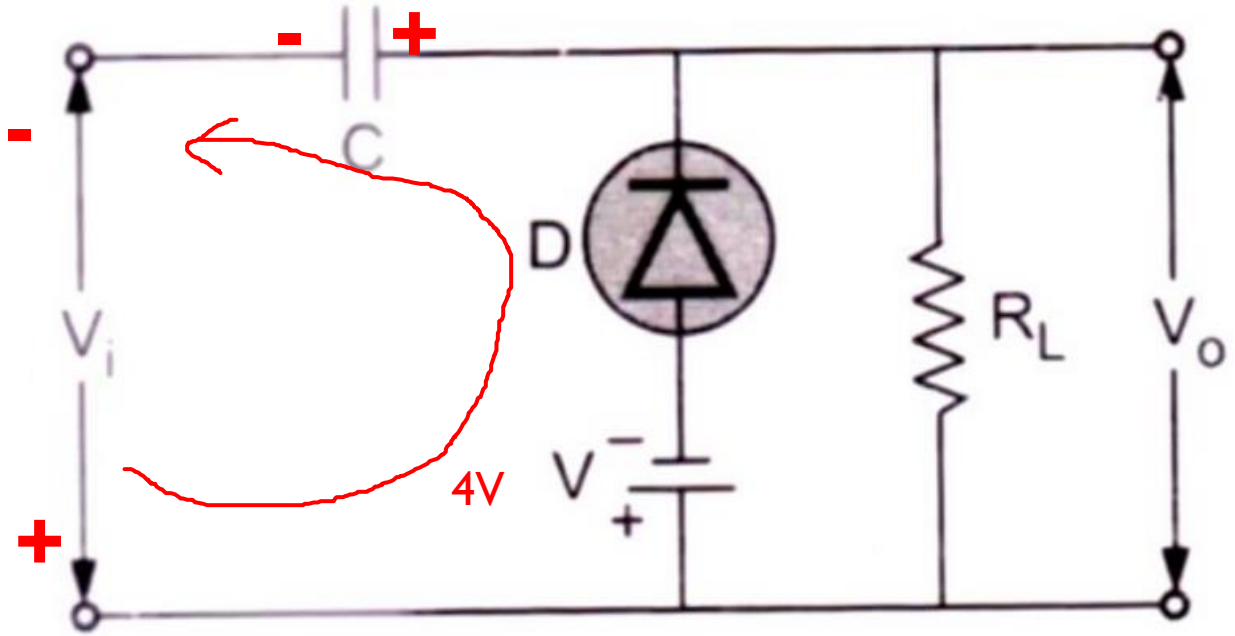


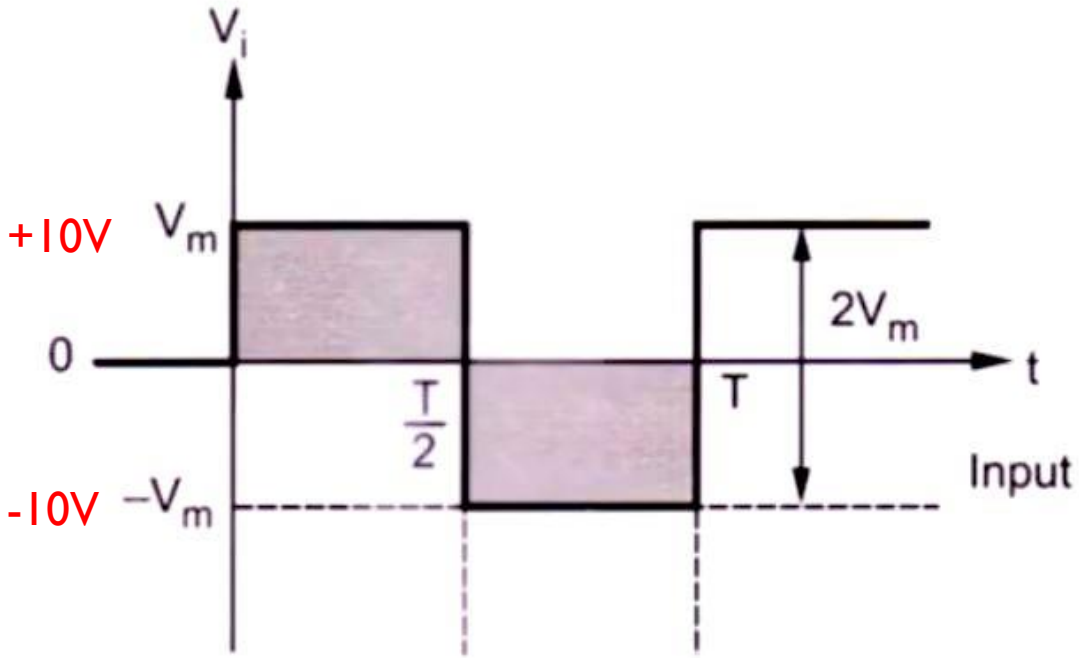
BIASED POSITIVE CLAMPER (NEGATIVE BIASED)





BIASED POSITIVE CLAMPER (NEGATIVE BIASED)





-ve Half Cycle

0 to -4V ▌ Diode RB ▌ Vo = -4V

-4V to -10V ▌ Diode FB ▌

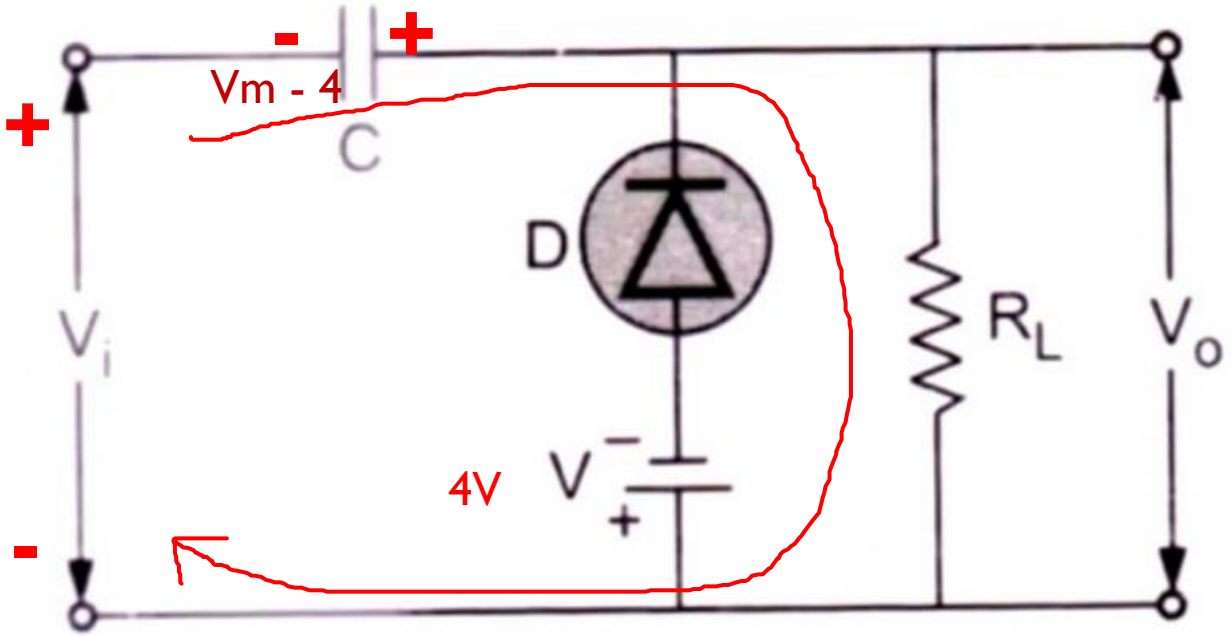
KVL:

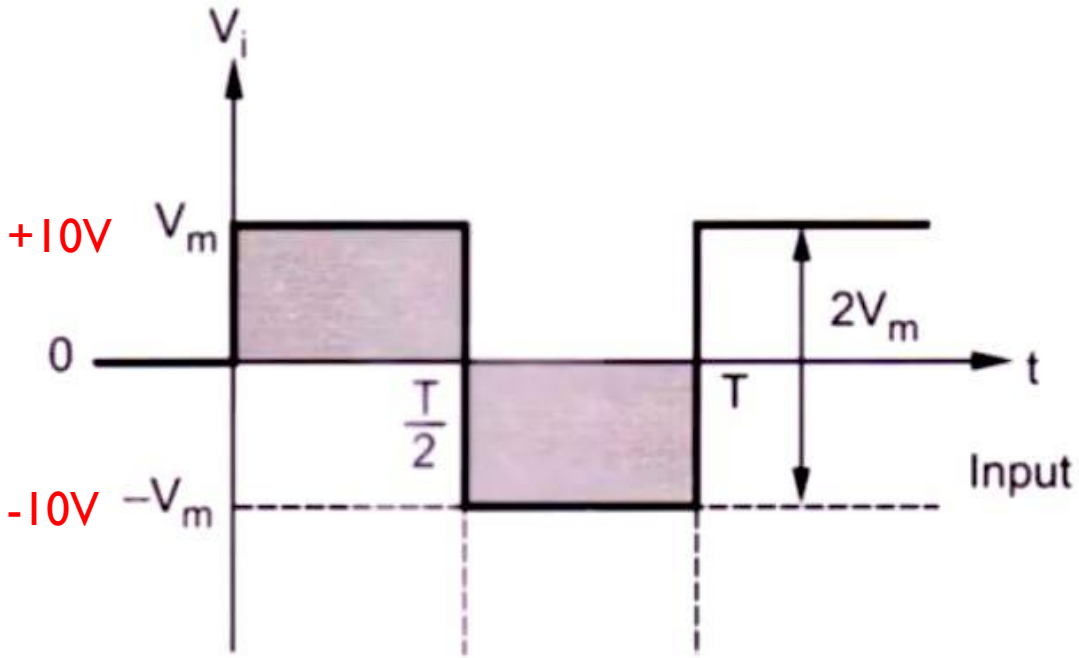
Vi - 4V – Vc = 0

Vc = Vi - 4V = 10 - 4V = 6V

- Diode RB till -4V, Diode FB from -4V to -10V
- When Diode FB, capacitor charges to Vm - 4V.
- Output Voltage will be -4V

BIASED POSITIVE CLAMPER (NEGATIVE BIASED)





+ve Half Cycle

0 to +10V ▌ Diode RB ▌

KVL:

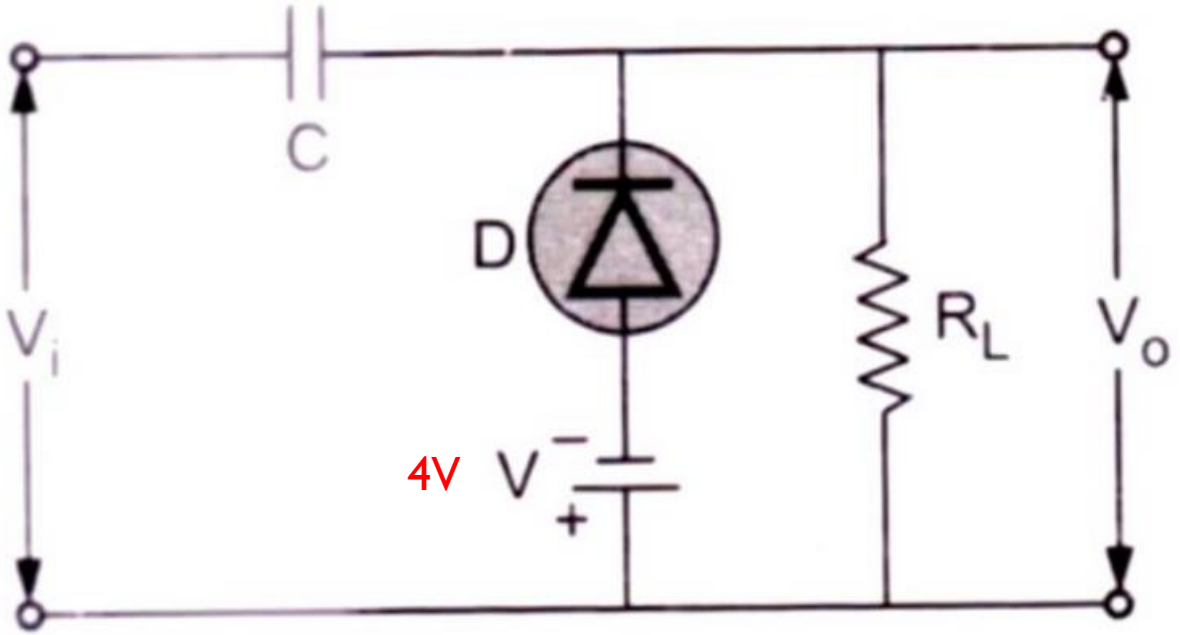
Vi + Vc – Vo = 0

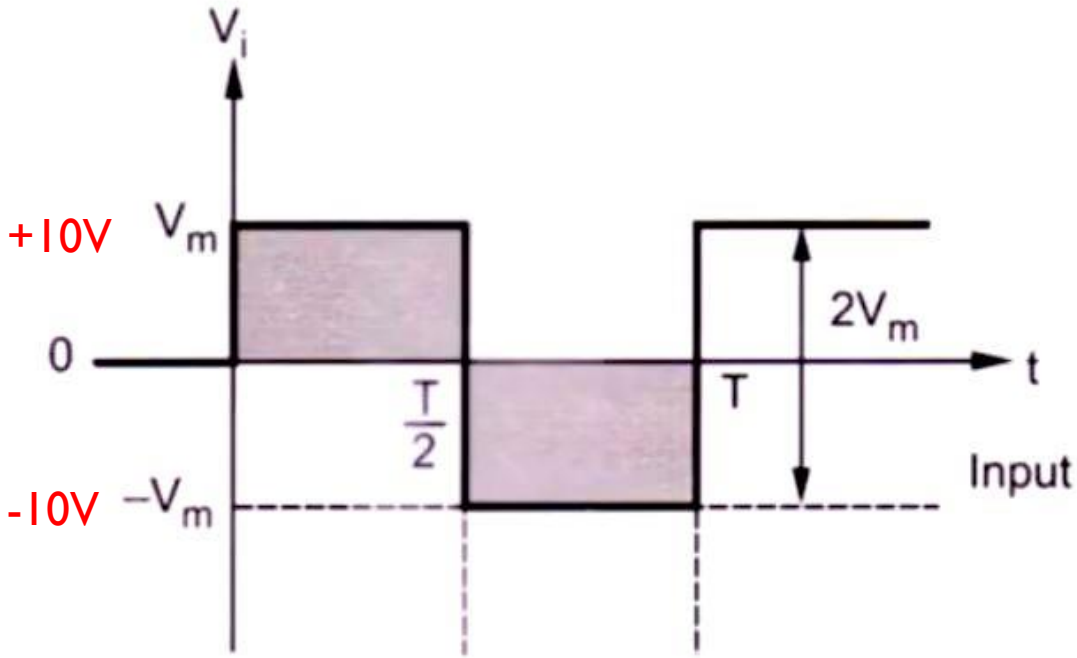
Vo = Vi + Vc

Vo = Vm + Vm – 4V = 10 + 10 – 4 = 16V

- In Complete Positive Half Cycle Diode will be Reverse Biased.
- When Diode RB, capacitor discharges already charged Vm - 4V.
- Output Voltage is 2Vm – 4V = 16V

BIASED POSITIVE CLAMPER (NEGATIVE BIASED)





+ve Half Cycle

Vo = Vi + Vc + Battery Voltage

Vo = Vm + Vm + (-4V)

Vo = 10 + 10 - 4 = 16V

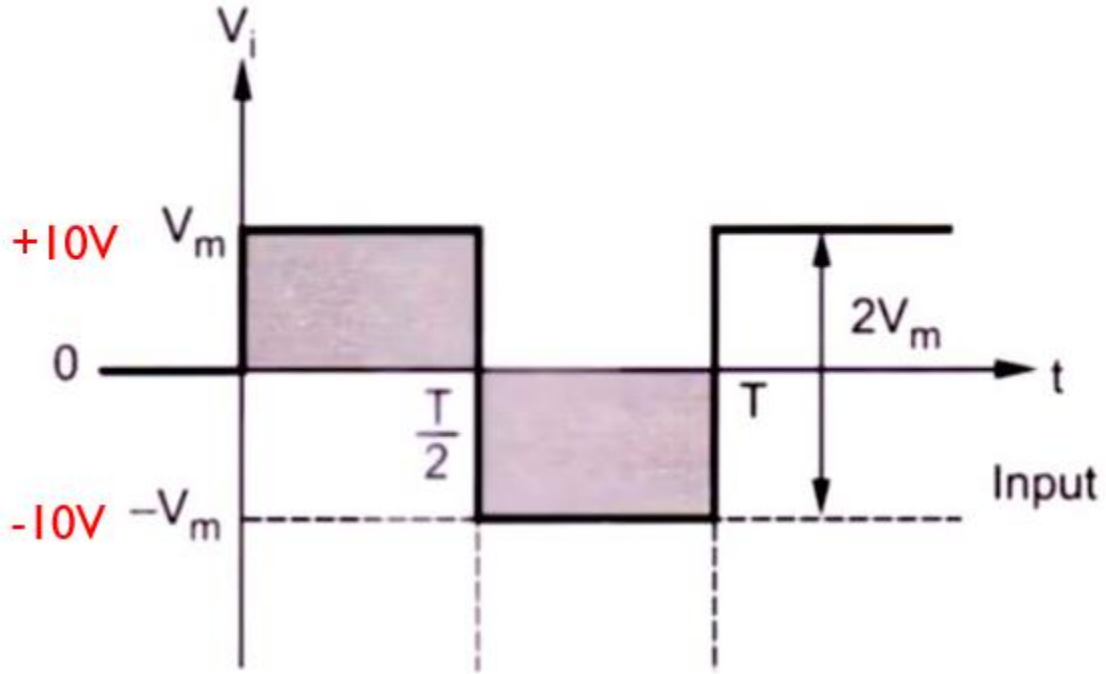
-ve Half Cycle

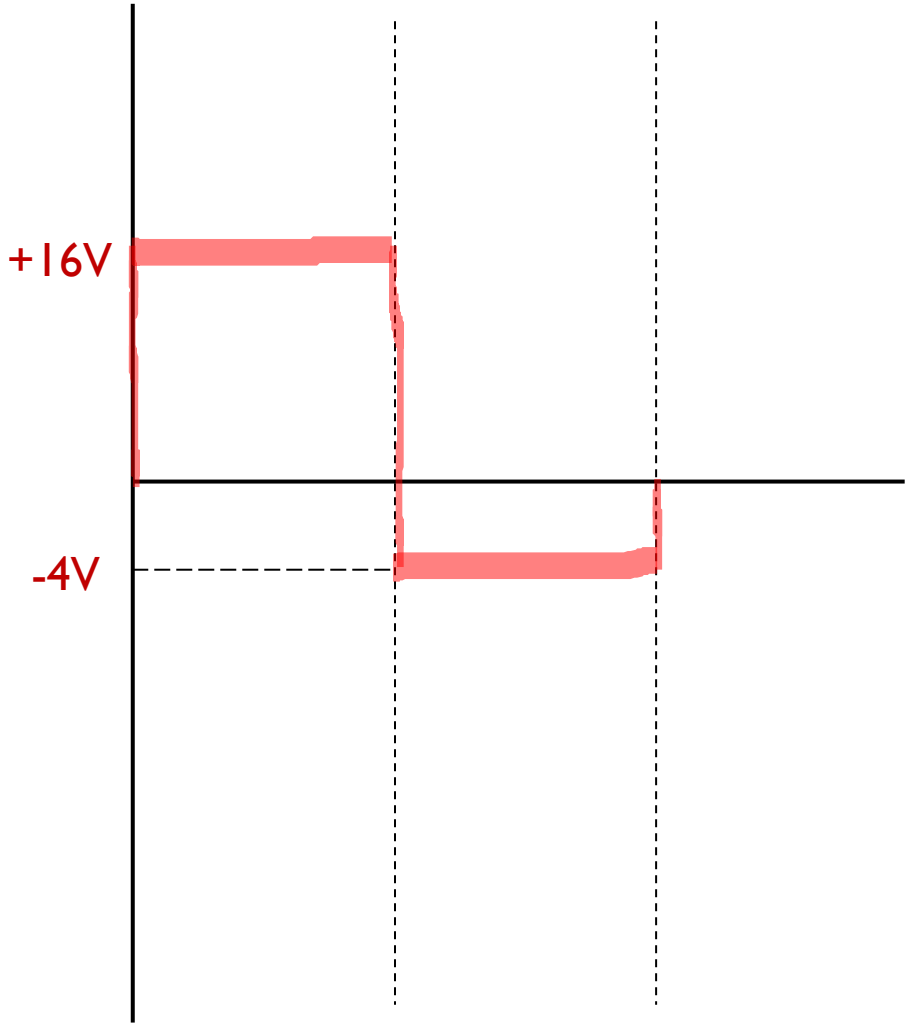
Vo = 0 + Battery Voltage

Vo = 0 + (-4V)

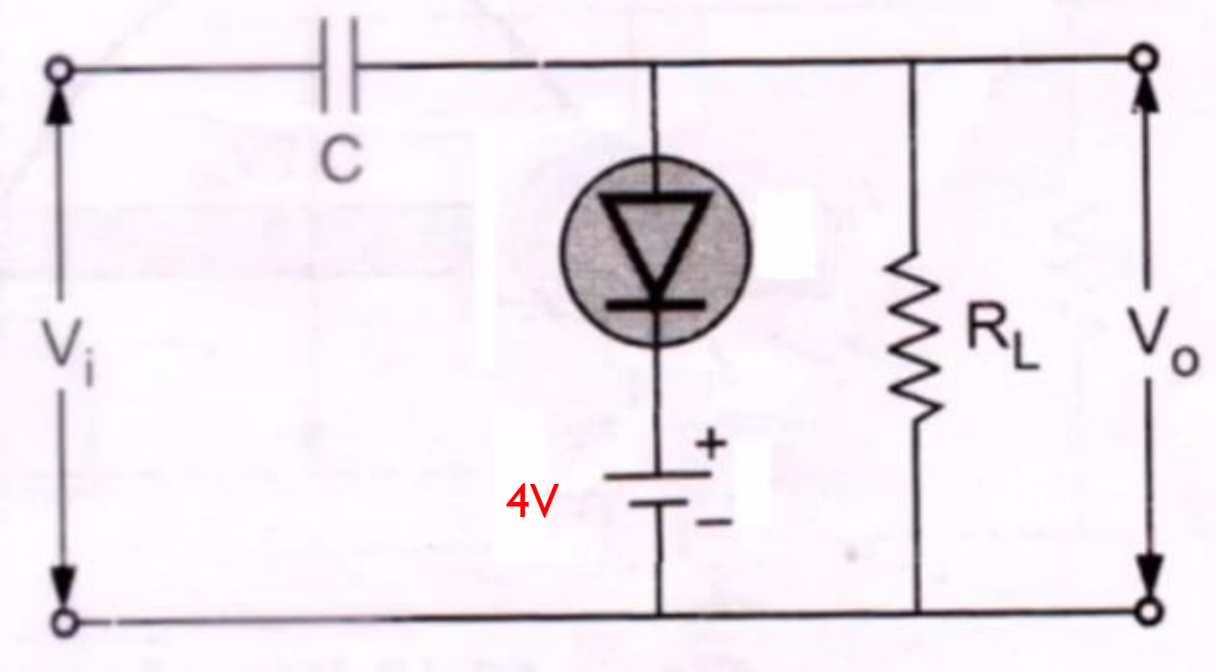
Vo = 0 - 4 = -4V

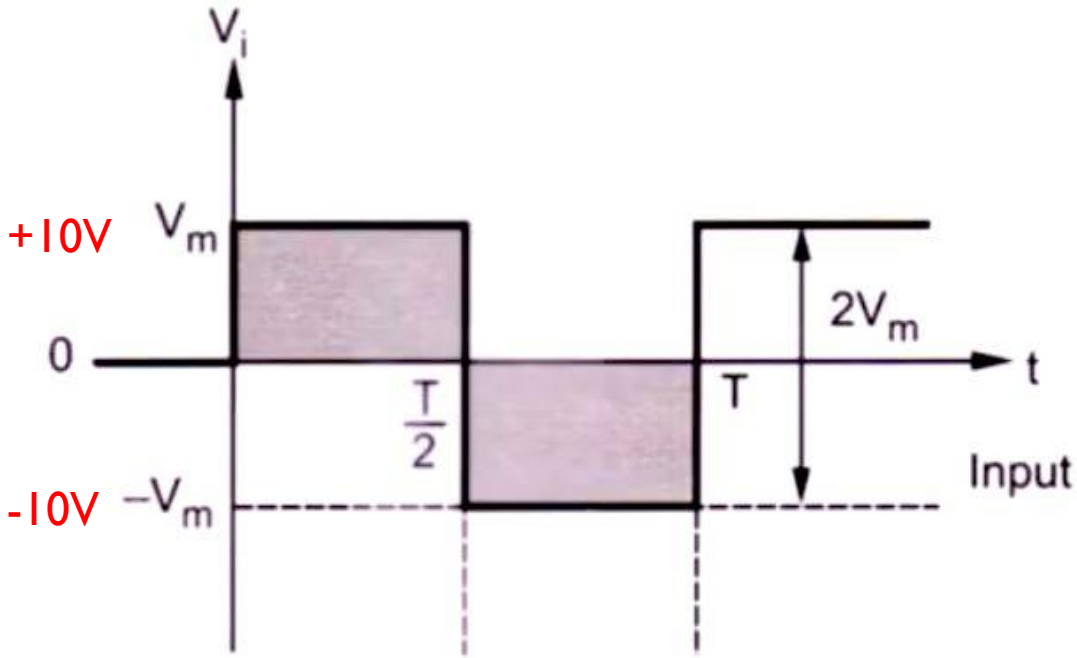
BIASED POSITIVE CLAMPER (NEGATIVE BIASED)





BIASED NEGATIVE CLAMPER (POSITIVE BIASED)





+ve Half Cycle

Vo = 0 + Battery Voltage

Vo = 0+ (+4V)

Vo = 0+ 4 = +4V

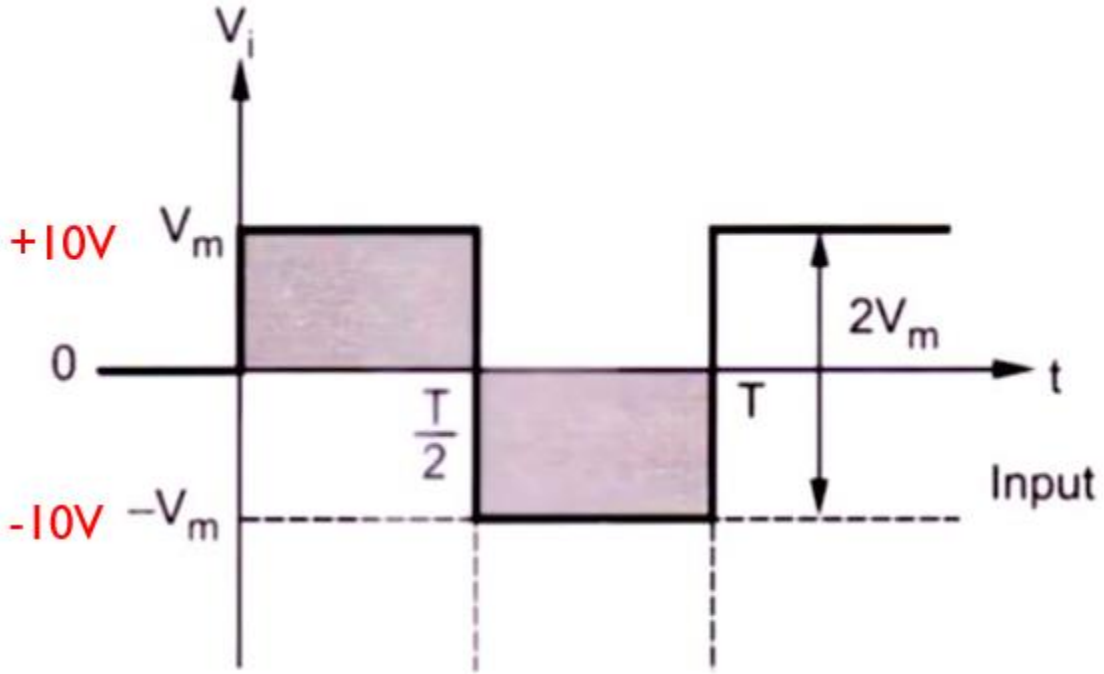
-ve Half Cycle

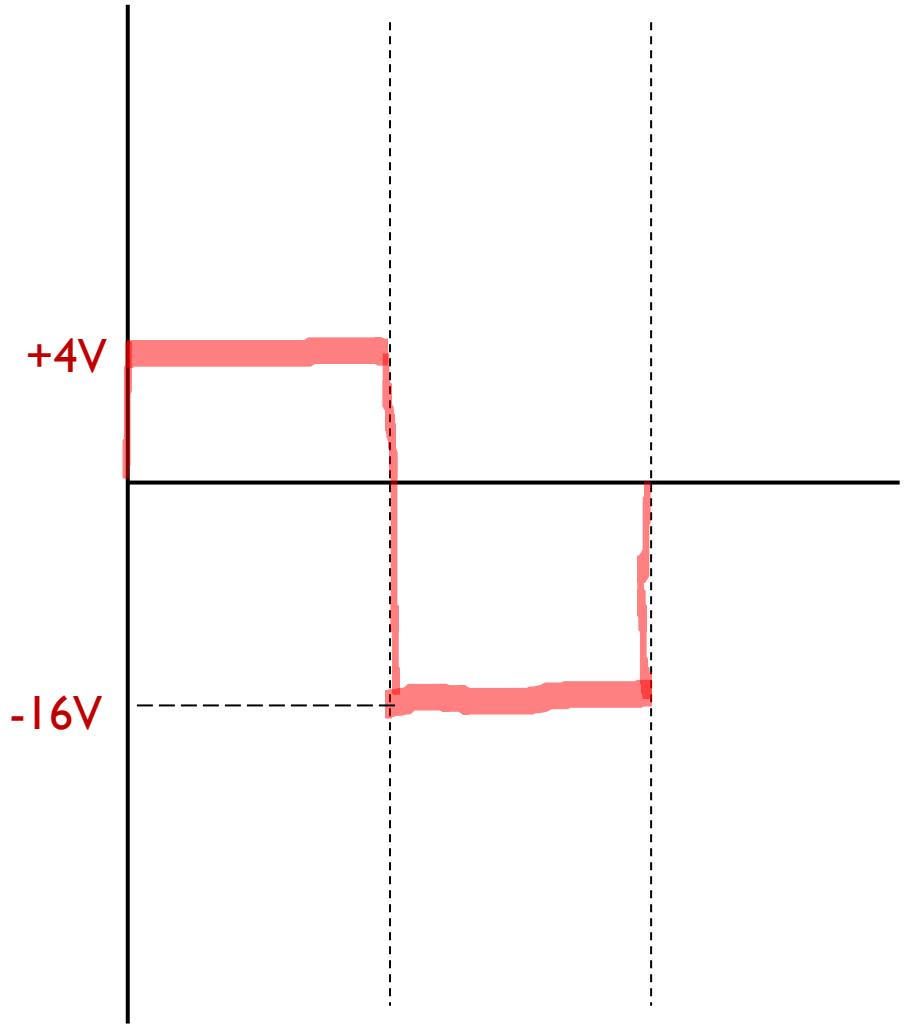
Vo = -Vi - Vc + Battery Voltage

Vo = -10 - 10 + (+4V)

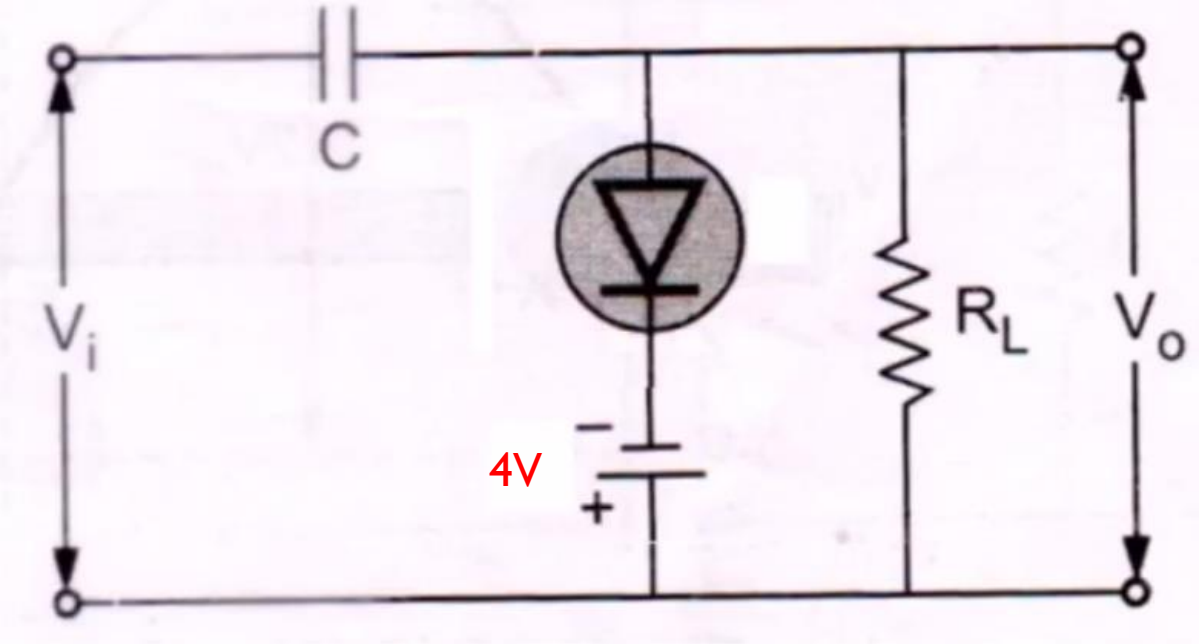
Vo = -20 + 4 = -16V

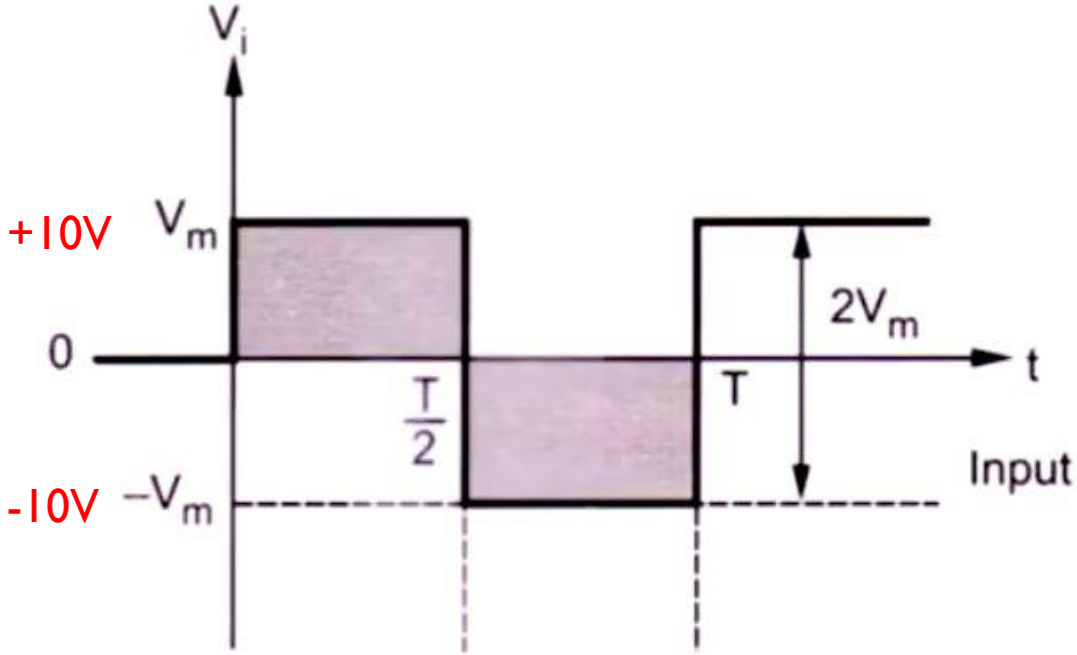
BIASED NEGATIVE CLAMPER (POSITIVE BIASED)





BIASED NEGATIVE CLAMPER (NEGATIVE BIASED)





+ve Half Cycle

Vo = 0 + Battery Voltage

Vo = 0 + (-4V)

Vo = 0 - 4 = -4V

-ve Half Cycle

Vo = -Vi - Vc + Battery Voltage

Vo = -10 - 10 + (-4V)

Vo = -20 - 4 = -24V

BIASED NEGATIVE CLAMPER (NEGATIVE BIASED)