TWO STAGE RC COUPLED AMPLIFIER

AIM:

To design, set up and study a two-stage RC coupled CE amplifier using BJT.

COMPONENTS REQUIRED:

Transistor, capacitors, resistors, breadboard, signal generator, dc power source, multimeter and CRO.

THEORY:

Multistage amplifiers are used in cascade to improve parameters such as voltage gain, current gain, input resistance and output resistance etc. for example, common emitter stages can be cascaded to increase the voltage gain. A two-stage amplifier provides an overall voltage gain of $A_1 A_2$ where A_1 and A_2 are the gains of first and second stages respectively. Since each stage provides a phase inversion, the final output signal is in phase with the input signal.

The input resistance of the second stage is in parallel with RC_1 of the first stage. The voltage gain of the first stage is

$$A_1 = \frac{RC_1 \parallel R_{12}}{re + Re}$$ where R_{12} is the input resistance of the second stage.

$$R_{12} = R_{12} \parallel R_{22} \parallel (1 + R_{PE}) re$$

The ac voltage gain of the second stage is

$$A_2 = \frac{R_{C_2} \| R_L}{r_e}$$

Care must be taken while selecting A_1 and A_2. If A_1 is large, the input to the second stage will become too high. This may put out the transistor of the second stage from active region. For example, if we need an overall voltage gain of 100, select $A_1 = 4$ and $A_2 = 25$. The gain of the first stage can be controlled by a negative feedback in series with the emitter. This is achieved by unbypassed resistor R_e.

DESIGN:

Output requirements : Midband voltage gain of the amplifier = 100

Selection of transistor : Select transistor BC107 because it has h_{fe} more than the required voltage gain.

Assume the gains $A_1 = 4$ and $A_2 = 25$ since $A = A_1 A_2$ and A_1 should be a lower value to avoid high input voltage to second stage. High input to second stage will lead to clipping of output waveform.

DC biasing conditions:

$V_{CC} = 12V$ $I_C = 2mA$

$V_{RC} = 40\%$ of $V_{CC} = 4.8V$

$V_{RE} = 10\%$ of $V_{CC} = 1.2V$

$V_{CE} = 50\%$ of $V_{CC} = 6V$

Design of R_{C1} and R_{C2} :

Take $R_{C1} = R_{C2} = R_C$

$V_{RC} = I_C \times R_C = 4.8V$

$R_C = 2.4k$ Use 2.2k std

Design of R_E :

$V_{RE} = I_E \times R_E$

R_E of first stage is split into $R_e + R_e'$

Because $I_E \simeq I_C$

$V_{RE} = I_C \times R_E = 1.2V$

from this we get.

$R_E = 600\Omega$ Select 680Ω (std)

Design of voltage divider R_1 and R_2 :

Take $R_{11} = R_{12} = R_1$ and $R_{21} = R_{22} = R_2$

from the data sheet of BC107 we get h_{fe} min = 100

$$I_B = \frac{I_C}{h_{fe}} = \frac{2mA}{100}$$

$$= 20\mu A$$

assume the current through $R_1 = 10 I_B$ and that through $R_2 = 9 I_B$ for the stability of potential divider bias current

$V_{R2} = V_{BE} + V_{RE}$

$V_{R2} = V_{BE} + V_E = 0.6 + 1.2 = 1.8V$

$V_{R2} = 9 I_B R_2 = 1.8V$

$$R_2 = \frac{1.8}{9 \times 20 \times 10^{-6}}$$

$= 10k$

$V_{R1} = V_{CC} - R_2 = 12 - 1.8 = 10.21V$

$V_{R1} = 10 I_B R_1 = 10.2V$

$R_1 = \frac{10.2}{10 \times 20 \times 10^{-6}} = 51k$ Select 47k

Design of Rc and Re':

Gain of first stage is given by the expression

$A_1 = \frac{Rc \| R_{in2}}{r_e + Re}$ where $Re = R_E - Re'$

$R_{in2} = R_1 \| R_2 \| (1 + R_{FE} r_e) = 1.1\Omega$

$r_e = \frac{25mV}{I_E} = \frac{25mV}{2mA} = 12.5\Omega$ at room temperature

Substituting the values of A, Rc, re and Rin2 we get

$Re = 173\Omega$ use 180Ω

$Re' = R_E - Re$

$= 680 - 180 = 500$ use 470Ω

Design of RL:

$A_2 = (Rc \| R_L)/r_e = 25$

Substituting values of A_2, Rc, re we get

$R_L = 363\Omega$ use 470Ω

Design of coupling capacitors CC_1, C_{C2} and CC_3:

To permit the lowest frequency f_L (say 100Hz) X_{C1} should be less than or equal to input resistance R_{in1}

As a rule of thumb.

$X_{C1} \leq R_{in1}/10$

Here $R_{in} = R_1 \| R_2 \| (1 + R_{FE} r_e) = 1.1k$

$X_{C1} \leq 110\Omega$

So $C_{C1} \geq \frac{1}{2\pi f_L \times 110} \geq 14\,\mu F$ Use 22μF (std)

Take $C_{C2} = C_{C3} = C_{C1} = 22\,\mu F$ because the input impedance of second stage is approximately same to that of first stage.

Design of bypass capacitor

To bypass the lowest frequency (say 100Hz) X_{CE} should be less than or equal to resistance R_E.

$$X_{CE} \leq \frac{R_E}{10}$$

Then $C_E \geq \frac{1}{2\pi \times 100 \times 68} = 23\,\mu F$. Use 33μF

PROCEDURE:

1) Test all components using multimeter. Set up circuit and verify dc bias conditions.
2) Apply a 100mV sinusoidal signal from the function generator to circuit input. Observe the input and output waveforms on the CRO screen simultaneously.
3) Keeping the input amplitude constant, vary the frequency from 0Hz to 1MHz. Measure the output amplitude corresponding to different frequencies and enter in table.
4) Plot the frequency response characteristics on the graph sheet with gain on Y axis and f on X axis. Mark f_L and f_H corresponding to 3dB down to the maximum gain.
5) Calculate bandwidth of amplifier using the expression $BW = f_H - f_L$

RESULT:

Designed two stage RC coupled amplifier using BJT and plotted the frequency response curve

Lower cut-off frequency f_L = 170Hz

Upper cut-off frequency f_H = 900×10^3 Hz

Bandwidth BW = $f_H - f_L$

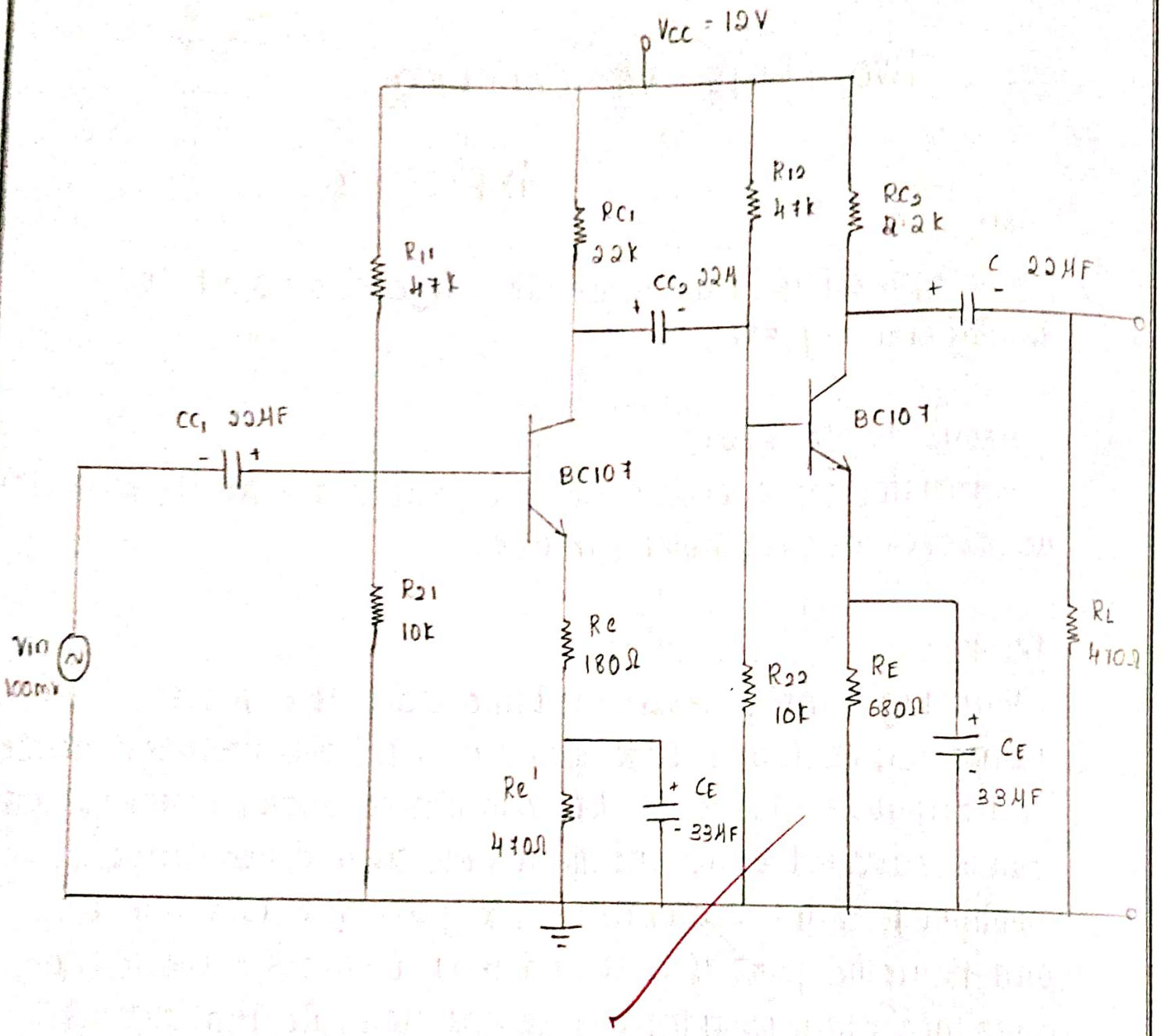
= $900 \times 10^3 - 170$

= 899830 Hz

= 899.83 kHz

27/7/22

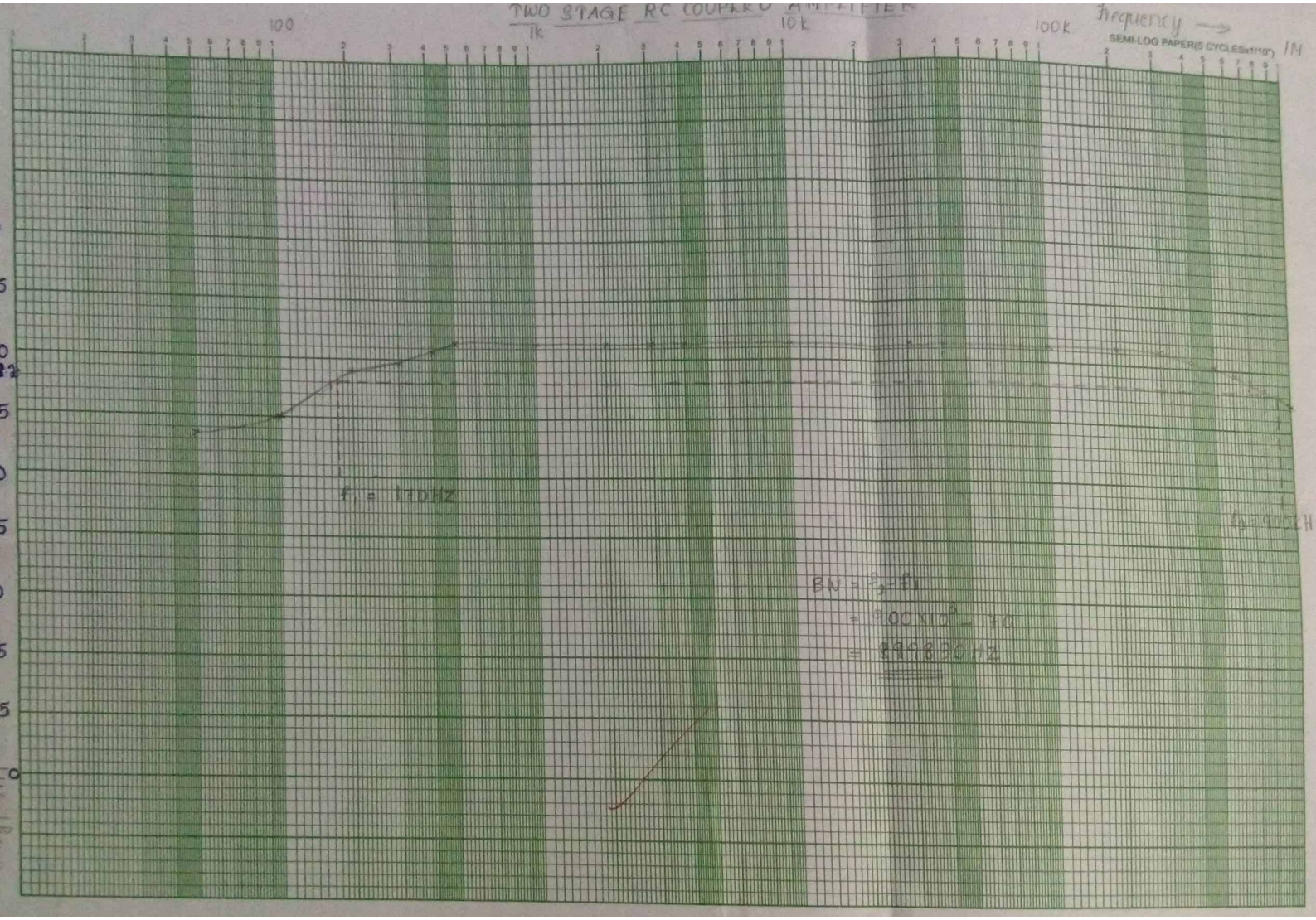
CIRCUIT DIAGRAM :



OBSERVATION:

V_i = 20mVpp

freq	V_o	V_o/V_i	$20\log(V_o/V_i)$	freq	V_o	V_o/V_i	$20\log(V_o/V_i)$
10 Hz	.680	34	30.69	9kHz	2.3	115	41.214
50 Hz	0.980	49	33.803	10kHz	2.3	115	41.214
100Hz	1.14	57	35.117	100kHz	2.3	115	41.214
200Hz	1.8	90	39.085	200kHz	2.3	115	41.214
300Hz	1.98	99	39.913	300kHz	2.3	115	41.214
400Hz	2.2	110	40.828	400kHz	2.24	112	40.984
500Hz	2.3	115	41.214	500kHz	2.10	105	40.424
700Hz	2.3	115	41.214	600kHz	1.98	99	39.913
900Hz	2.3	115	41.214	700kHz	1.88	94	39.462
1kHz	2.3	115	41.214	800kHz	1.74	87	38.790
2kHz	2.3	115	41.214	900kHz	1.62	81	38.1697
3kHz	2.3	115	41.214	1MHz	1.5	75	37.5012
4kHz	2.3	115	41.214	2MHz	1.1	55	34.807
5kHz	2.3	115	41.214				
6kHz	2.3	115	41.214				
7kHz	2.3	115	41.214				
8kHz	2.3	115	41.214				


TWO STAGE RC COUPLED AMPLIFIER
100
1k
10k
100k
Frequency →
SEMI-LOG PAPER(5 CYCLES x 1(10))
IN
f1 = 111Hz
BW = f2 - f1
= 100 x 10^3 - 111
= 99889 Hz