R/W Memory (RAM)

Two types :-

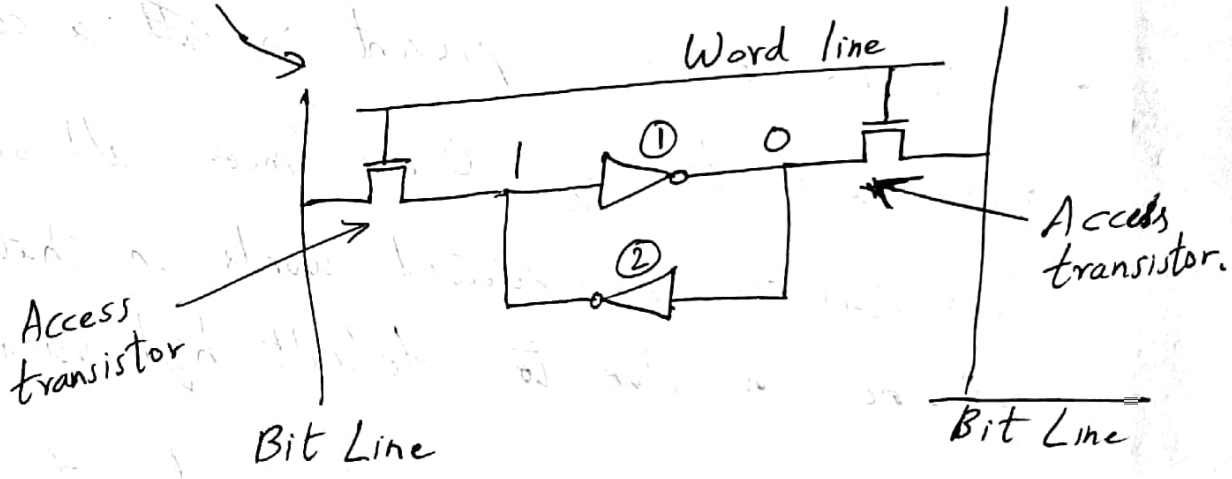
→ SRAM (Static RAM)

→ DRAM (Dynamic RAM)

SRAM

→ A normal CMOS SRAM cell requires 6 transistors.

Basic idea of SRAM cell

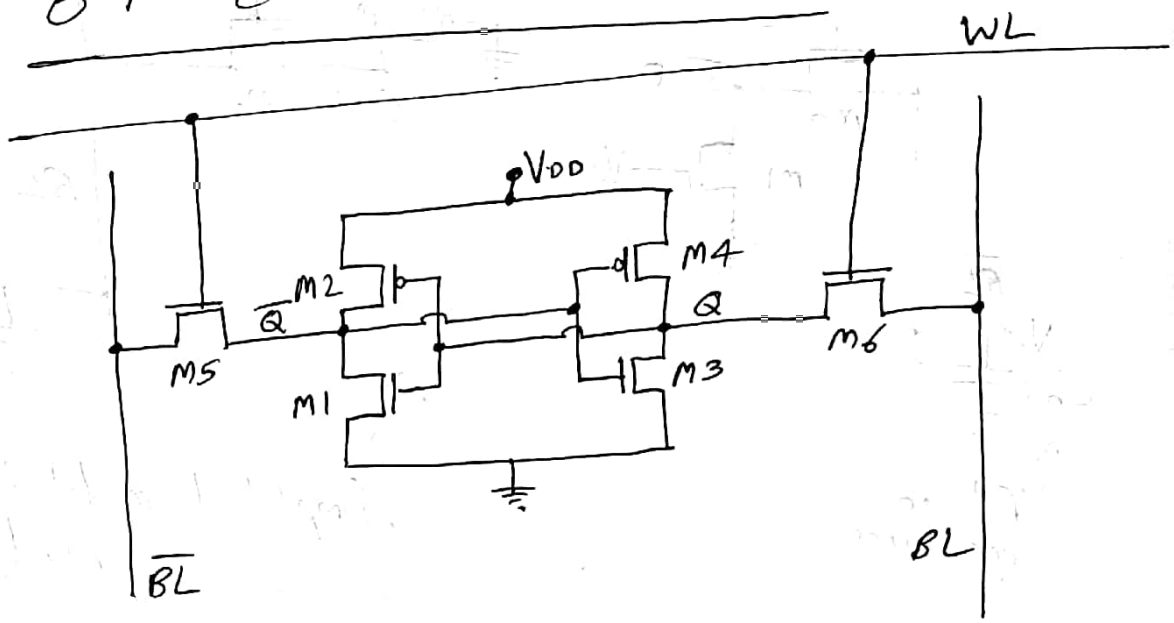


→ If a 1 is created in one side, then automatically, a 0 is generated at other side due to inverters.

→ If access transistors are off, then the cell holds the value.

→ During Read/Write operation, access transistors will be enabled & output/input will be available in bit lines.

6T CMOS SRAM cell



M1 & M2 → Inverter 1

M3 & M4 → Inverter 2

M5 & M6 → Access transistors.

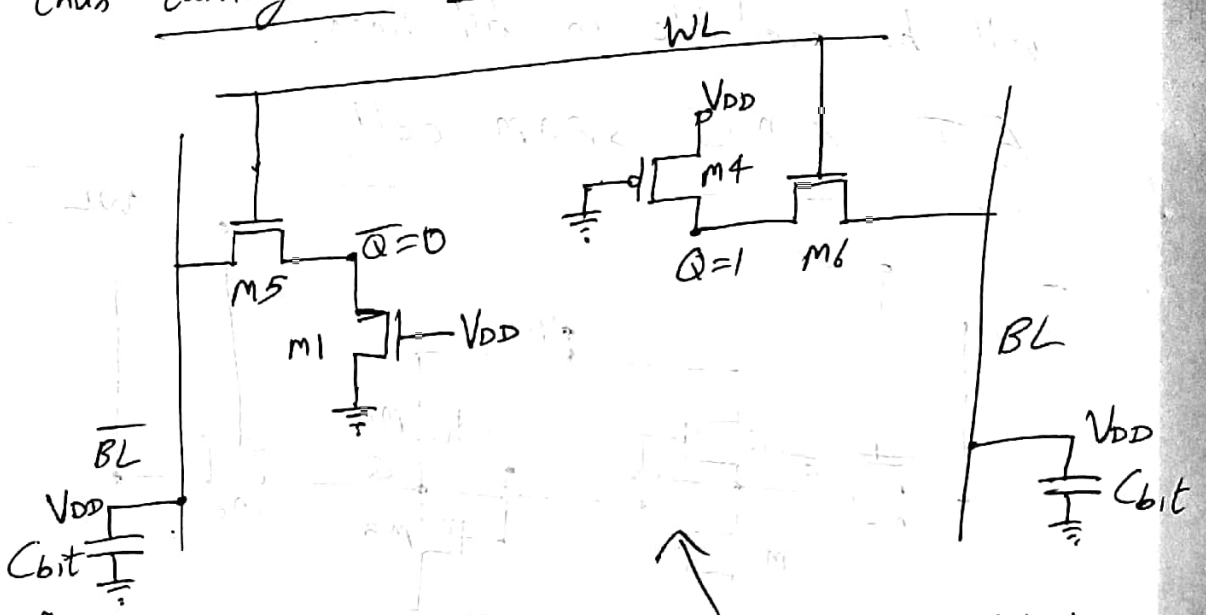
Read operation

→ Assume that $Q=1$ & $\bar{Q}=0$

→ Before starting read operation, BL & $\overline{BL}$ lines are precharged to V_{DD}.

→ As per Q & $\bar{Q}$ values, M1 = on, M2 = off.
M4 = on, M3 = off.

→ To initiate read operation, WL is made high thus turning on M5 & M6.



→ Since M5 & M1 are on, $\overline{BL}$ will discharge through them. So voltage at $\overline{BL}$ reduces.

→ Since Q=1 & BL=1, there is no current flow through M6. So BL voltage remains the same.

→ BL & $\overline{BL}$ are given to a comparator. Here, BL > $\overline{BL}$. So comparator gives output as 1, which is the value read from memory cell.

→ Instead, if the contents of cell was different, ie $Q=0$ & $\overline{Q}=1$, then upon initiating read operation, BL will discharge & $\overline{BL}$ remains the same. So $\overline{BL} > BL$ & output of comparator will be 0.

Transistor sizing constraint (Read)

→ When $\overline{BL}$ is precharged to V_{DD} & M5 is turned on, then voltage at $\overline{Q}$ will increase. If voltage at $\overline{Q}$ goes above V_{Tn} of M3, then M3 will turn on & contents of cell will change.

To prevent this issue from happening, resistance of M1 should be small compared to M5. ie ~~$(W/L)_{M1} > \left(\frac{W}{L}\right)_{M5}$~~

$$\text{ie } \frac{W_1}{L_1} > \frac{W_5}{L_5}$$

or cell ratio (CR) $= \dfrac{W_1/L_1}{W_5/L_5} > 1.2$

(Similar ratio between M6 & M3 also)

Write operation

→ Assume that $Q=1$ & $\bar{Q}=D$

→ No we want to make $Q=0$ & $\bar{Q}=1$.

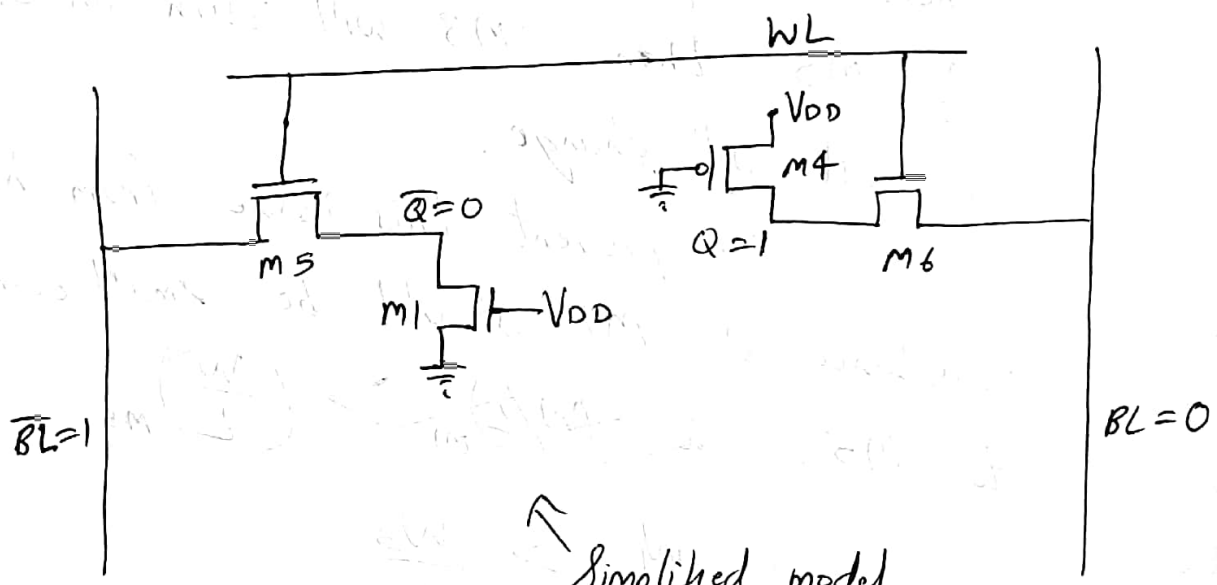
→ So $\bar{BL}$ is made 1 & BL is made 0 forcefully.

→ As per initial values of Q & $\bar{Q}$,

M1 = on, M2 = off

M4 = on, M3 = off.

→ Now WL is enabled, thus turning on M5 & M6



Simplified model during write

→ Since M4 & M6 are on, current will flow to BL & voltage at Q will reduce.

→ When voltage at Q goes below V_{Tn} of M1, M1 will turn off. Then voltage at $\bar{Q}$ will increase & thus contents of the cell will switch, thus making $Q=0$ & $\bar{Q}=1$.

Transistor sizing constraint (Write)

→ Since voltage at Q must be low to switch the value, resistance of M6 should be low compared to M4.

ie $$\frac{W_6}{L_6} > \frac{W_4}{L_4}$$

or Pullup Ratio (PR) $= \dfrac{W_4/L_4}{W_6/L_6} < 1.8$

(Similar ratio between M2 & M5 also)