

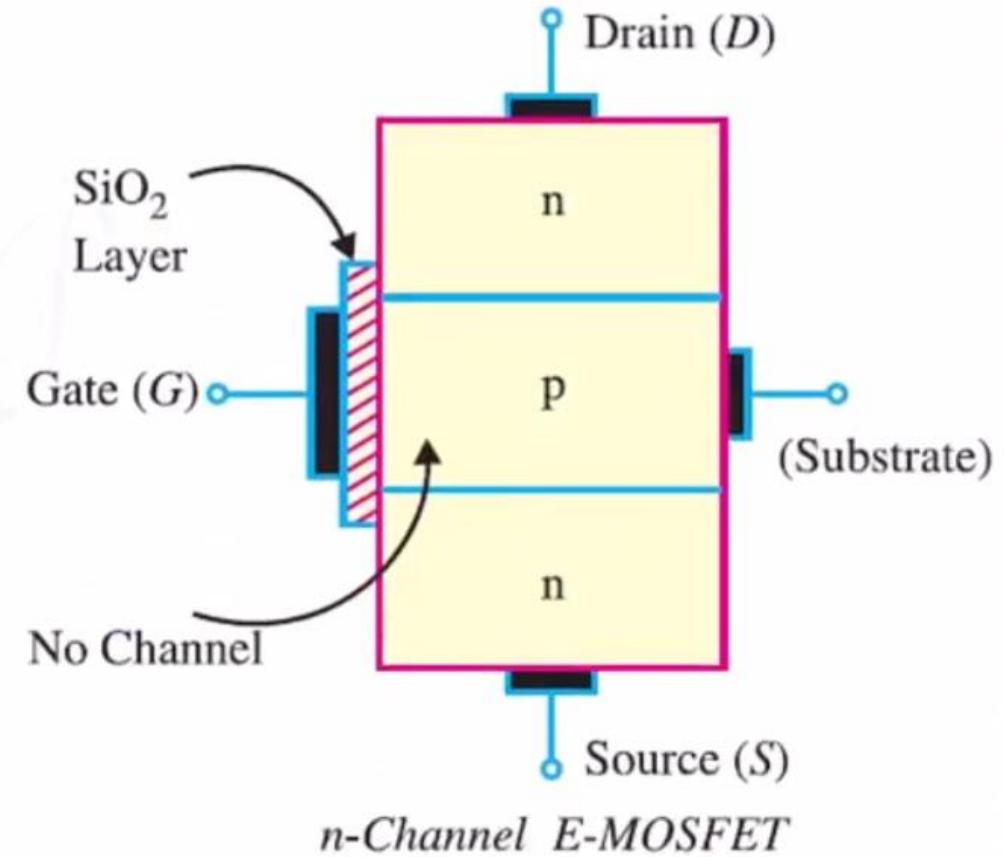
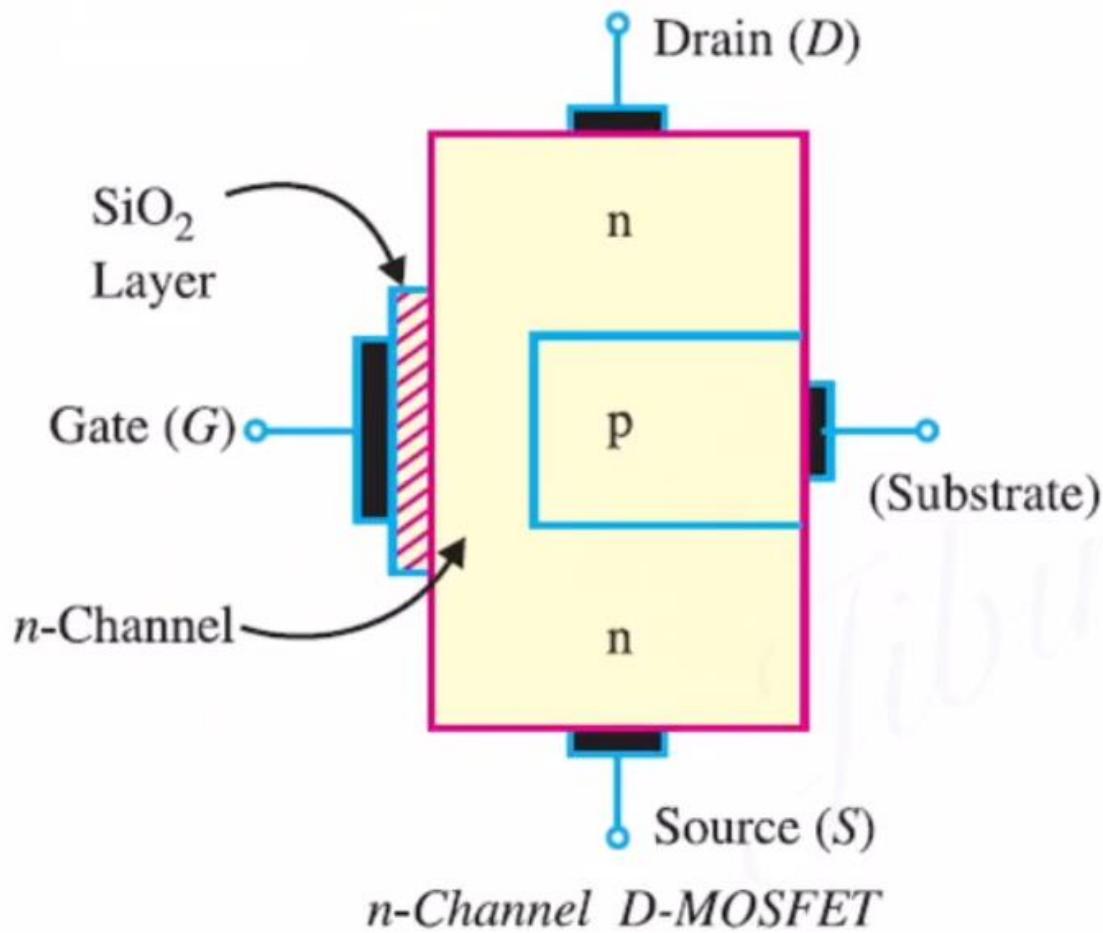
INTRODUCTION TO FET

- BJT is a Current Controlled Device. i.e., output characteristics of the device is controlled by input current and not by input voltage.
- FET is a Voltage Controlled Device. i.e., output characteristics of the device is controlled by input voltage and not by input current.
- Two types of FET (Field effect Transistors)
 - Junction Field effect Transistors (JFET)
 - Metal Oxide Semiconductor/Silicon Field effect Transistors (MOSFET)

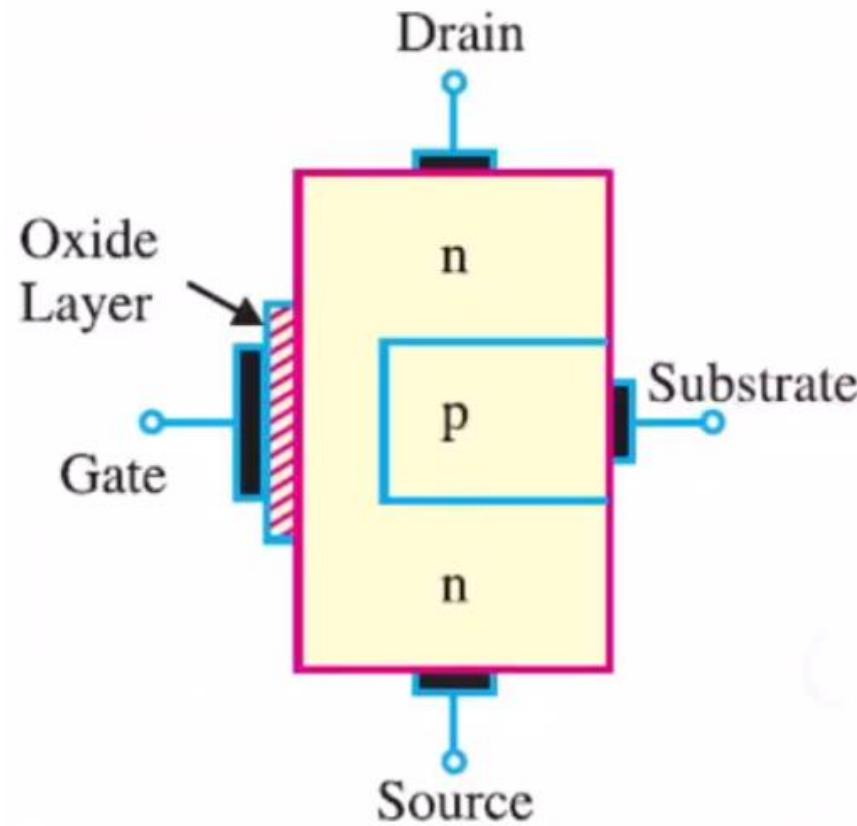
CLASSIFICATION OF MOSFET

- **DEPLETION TYPE MOSFET OR D-MOSFET**
- Operated in both depletion/enhancement mode.
- Sometimes called as depletion/enhancement MOSFET
- **ENHANCEMENT TYPE MOSFET OR E-MOSFET**
- Can operate in Enhancement mode only

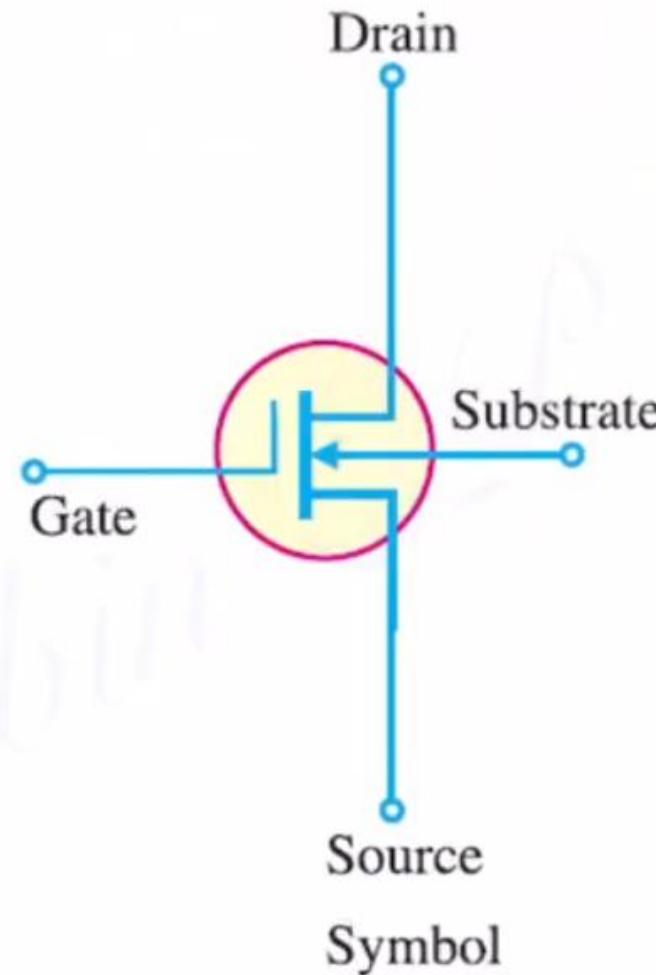
CONSTRUCTION OF MOSFET



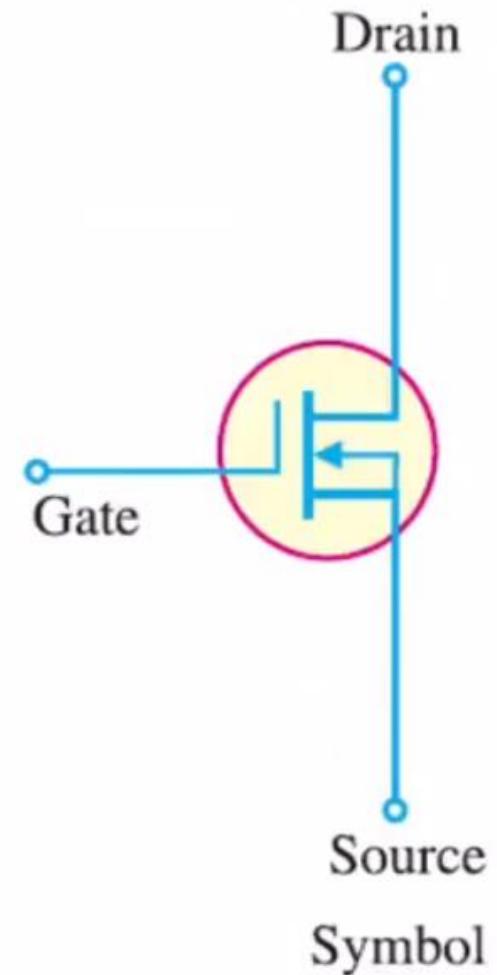
SYMBOL OF D-MOSFET (n-CHANNEL)



n-Channel D-MOSFET

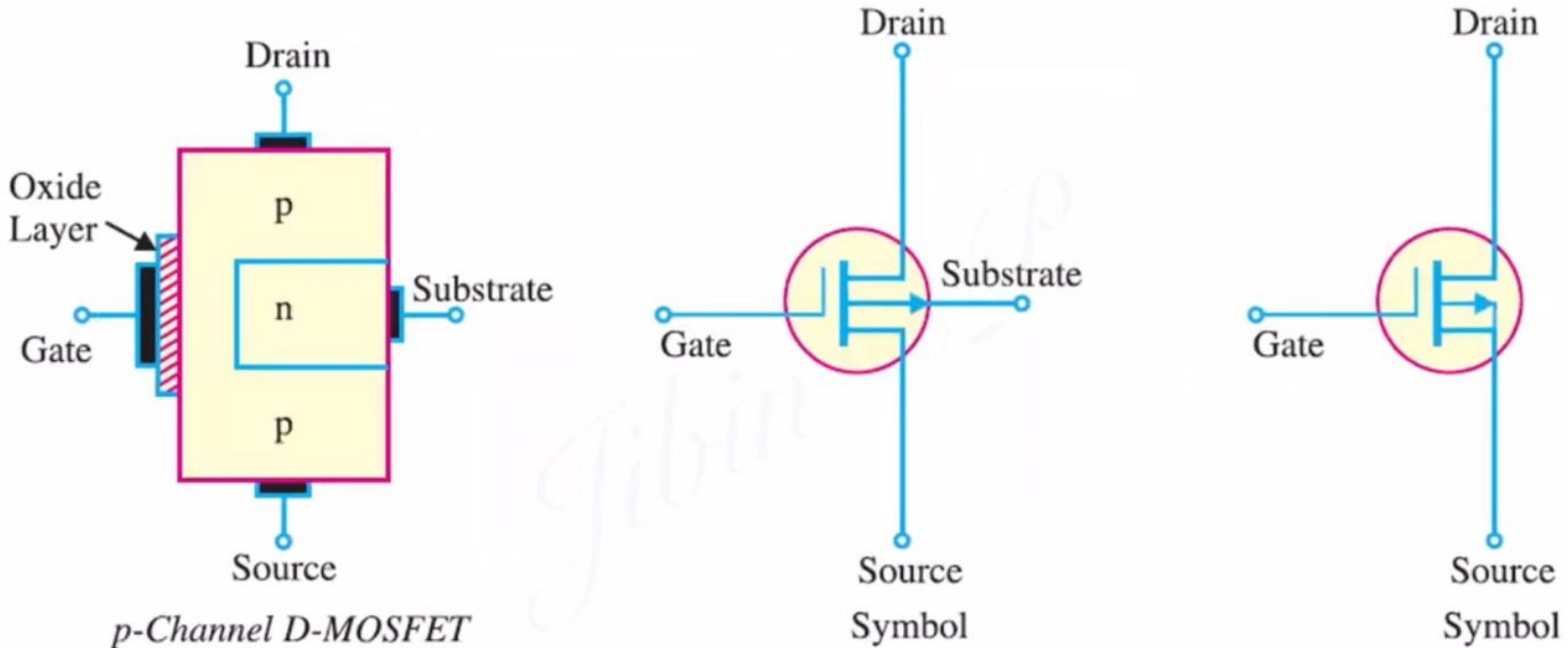


Symbol

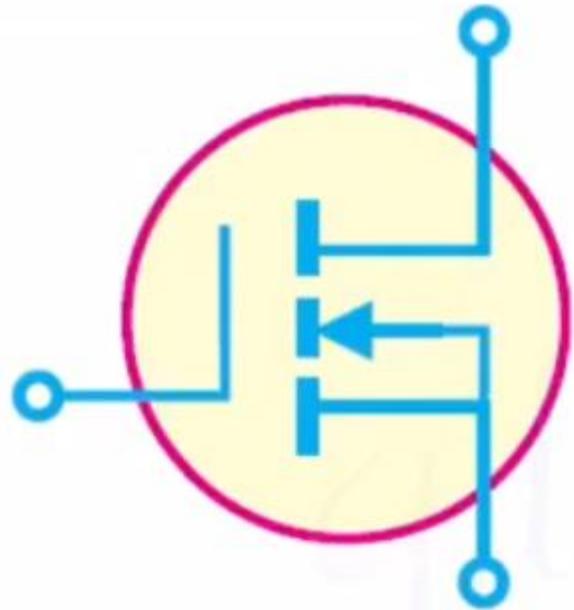


Symbol

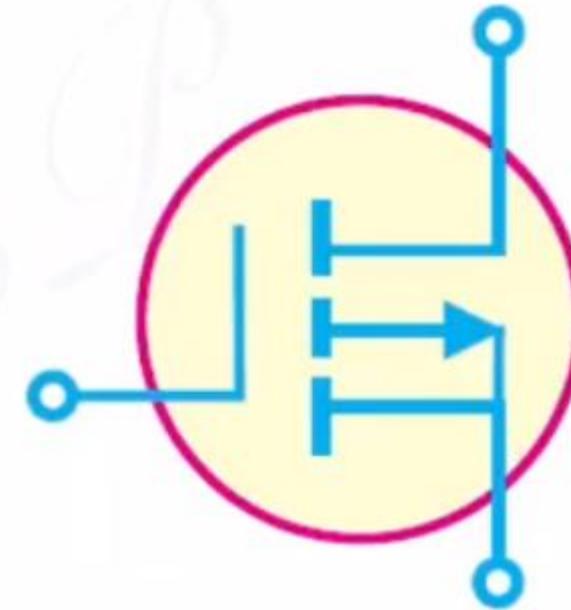
SYMBOL OF D-MOSFET (p-CHANNEL)



SYMBOL OF E-MOSFET



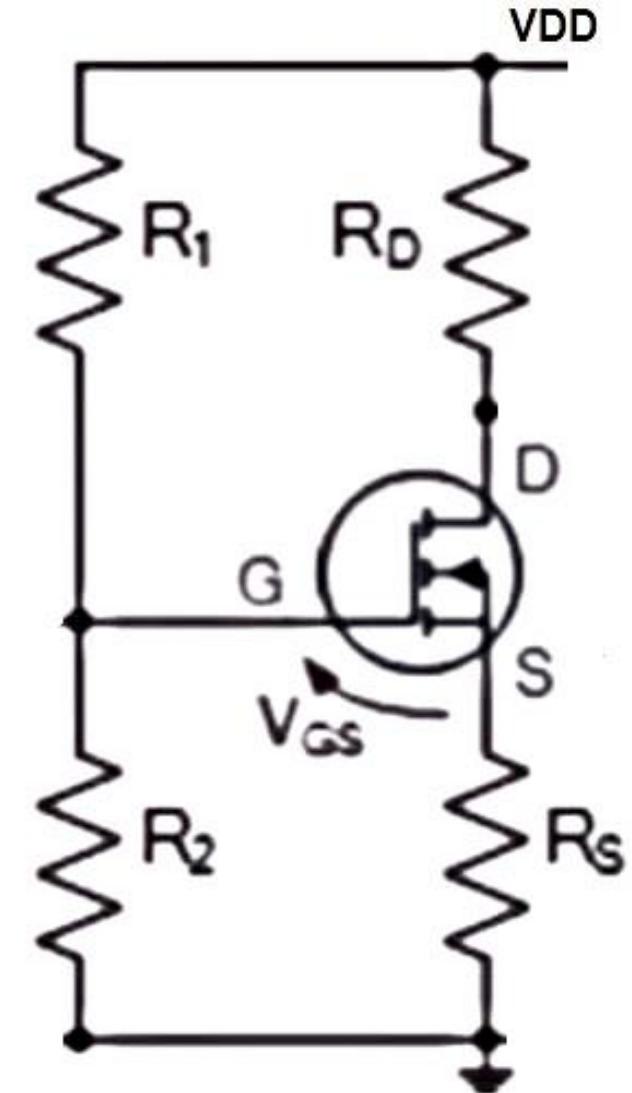
n-channel *E-MOSFET*



p-channel *E-MOSFET*

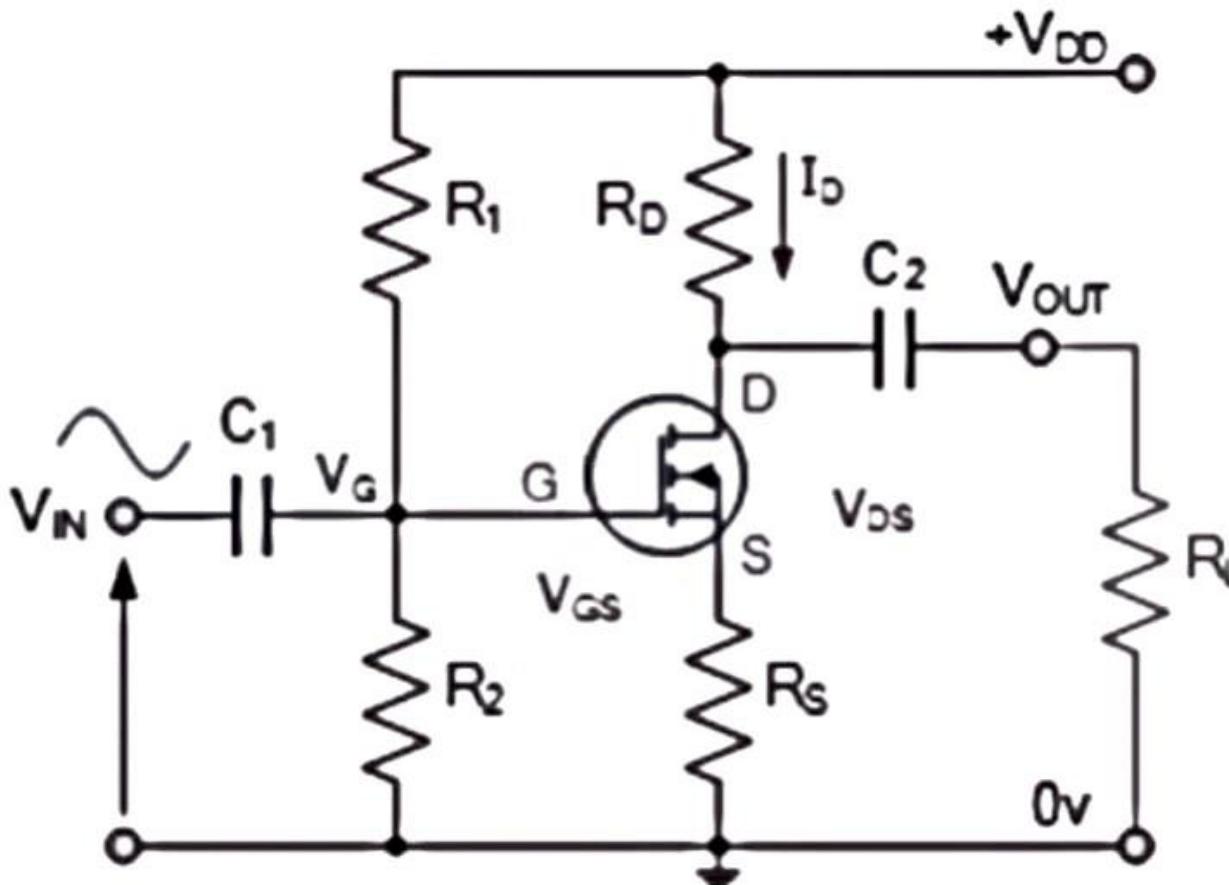
VOLTAGE DIVIDER BIAS IN MOSFET

- Most widely used method to provide biasing and stabilization to a MOSFET.
- Two resistances R₁ and R₂ connected across supply voltage VDD and provide biasing.
- Drain resistance R_D provide stabilization.
- Voltage divider formed by resistors R₁ and R₂



BASIC MOSFET AMPLIFIER

- Enhancement Mode Common Source MOSFET Amplifier with single supply at drain and generates the required voltage V_G using a resistor divider.

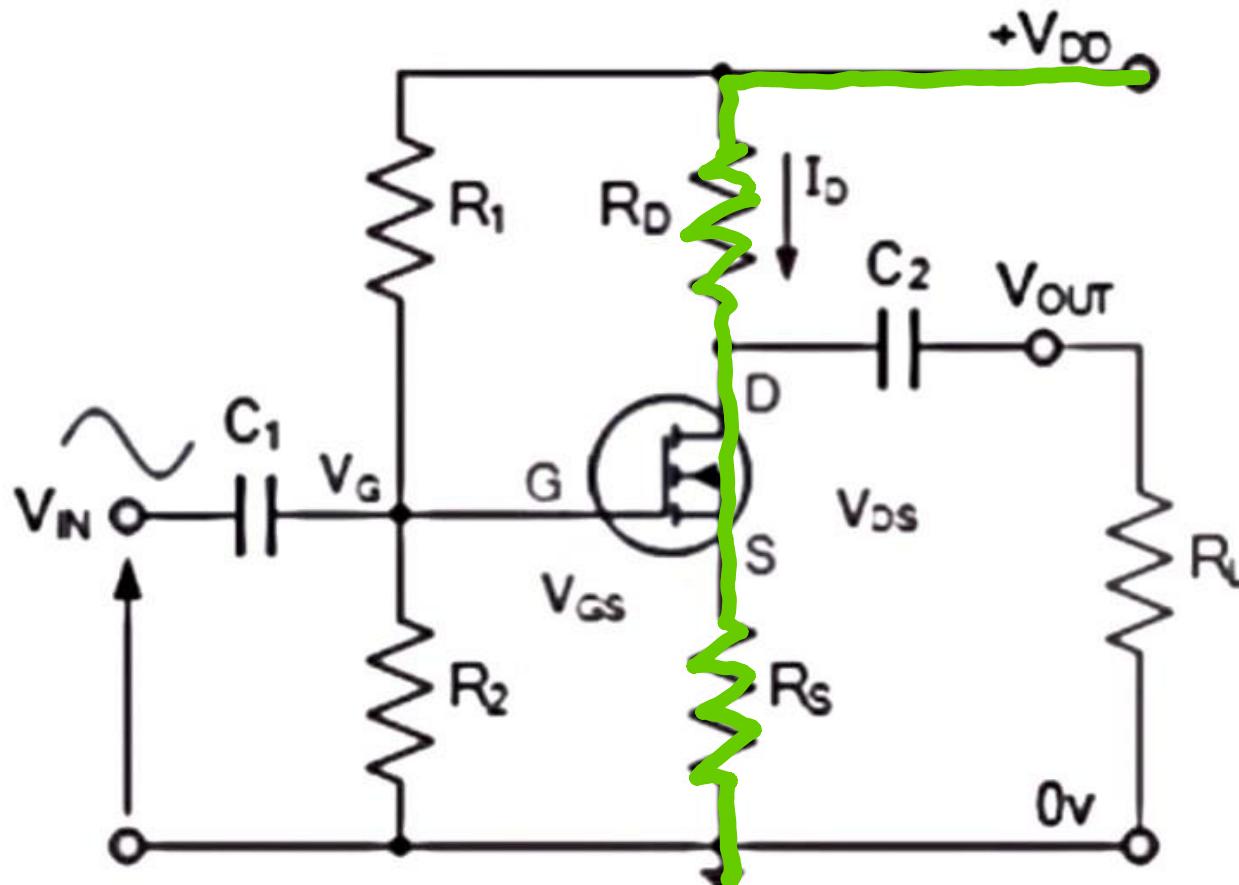


$$V_{GS} = V_G - V_S$$

$$V_{DS} = V_D - V_S$$

BASIC MOSFET AMPLIFIER ANALYSIS

- CALCULATION OF V_{DD} AND R_D



$$V_{DD} = I_D R_D + V_{DS} + I_s R_S$$

$$I_s \cong I_D$$

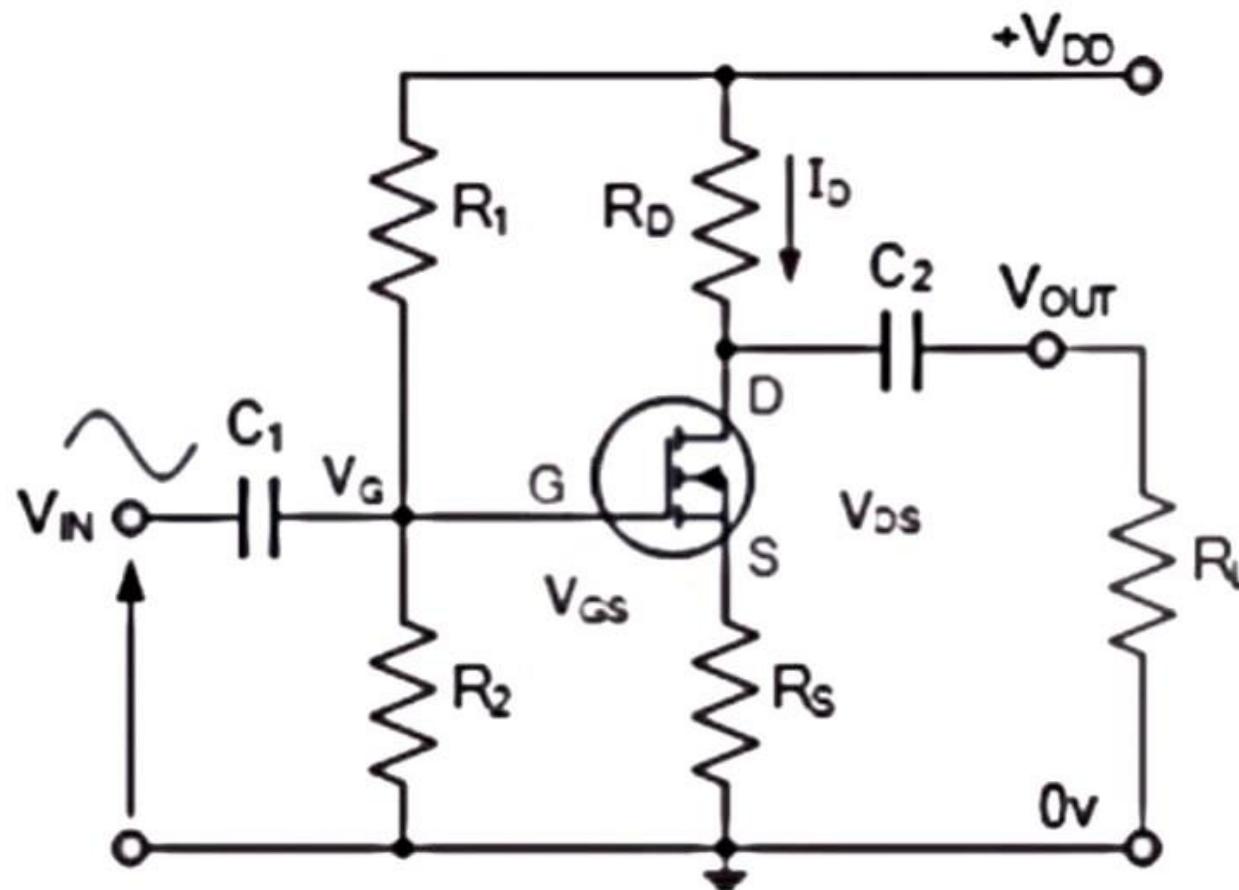
$$V_{DD} = I_D R_D + V_{DS} + I_D R_S$$

$$V_{DD} = I_D (R_D + R_S) + V_{DS}$$

1

BASIC MOSFET AMPLIFIER ANALYSIS

- CALCULATION OF V_{DD} AND R_D



$$V_{DD} = I_D (R_D + R_S) + V_{DS}$$

$$R_D + R_S = \frac{V_{DD} - V_{DS}}{I_D}$$

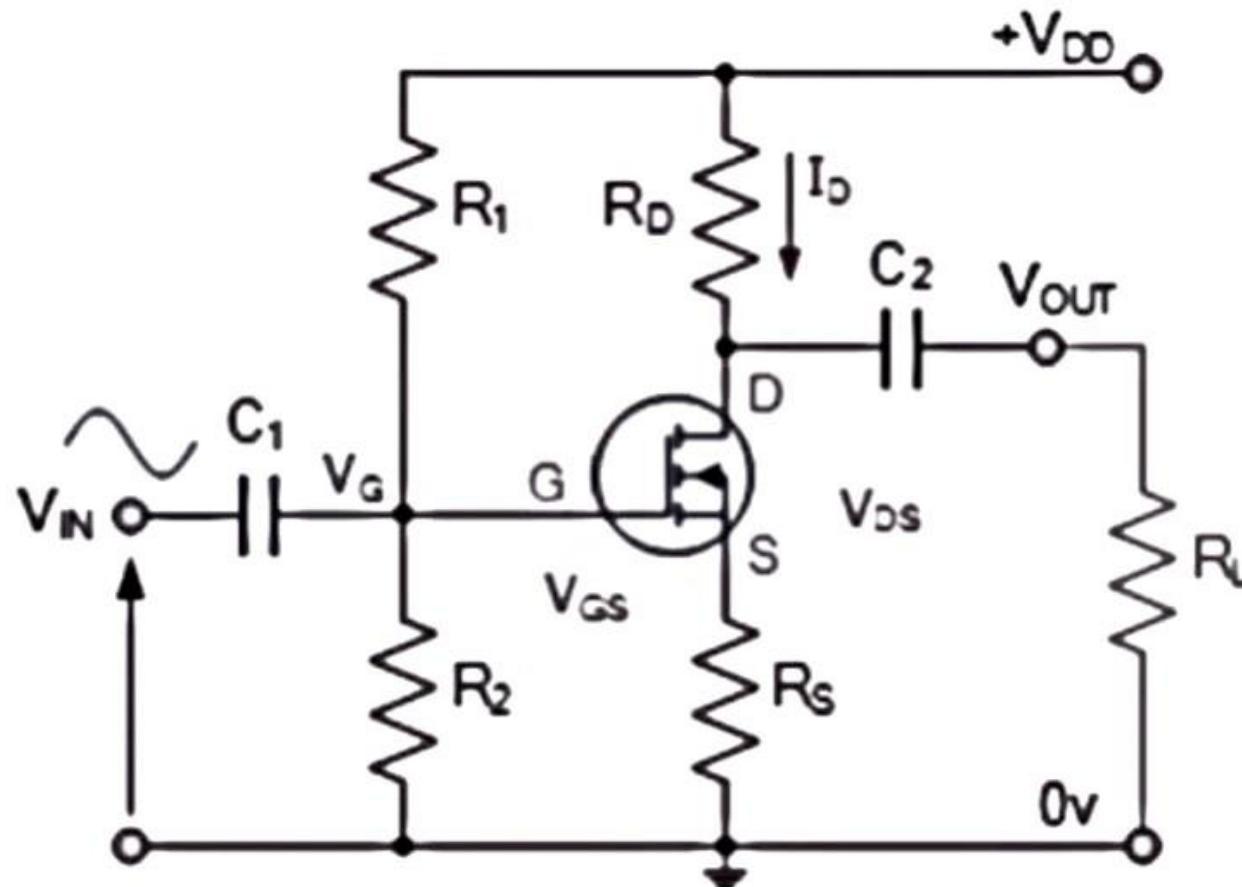
$$R_D = \frac{V_{DD} - V_{DS}}{I_D} - R_S \rightarrow ②$$

$$R_S = \frac{V_S}{I_D} \quad (I_D \approx I_s)$$

$$R_D = \frac{V_{DD} - V_{DS}}{I_D} - \frac{V_S}{I_D}$$

BASIC MOSFET AMPLIFIER ANALYSIS

- CALCULATION OF V_{DD} AND R_D



$$R_D = \frac{V_{DD} - V_{DS}}{I_D} - \frac{V_S}{I_D}$$

$$R_D = \frac{V_{DD} - (V_{DS} + V_S)}{I_D} \rightarrow ③$$

$$V_{DS} = V_D - V_S$$

$$V_D = V_{DS} + V_S \rightarrow ④$$

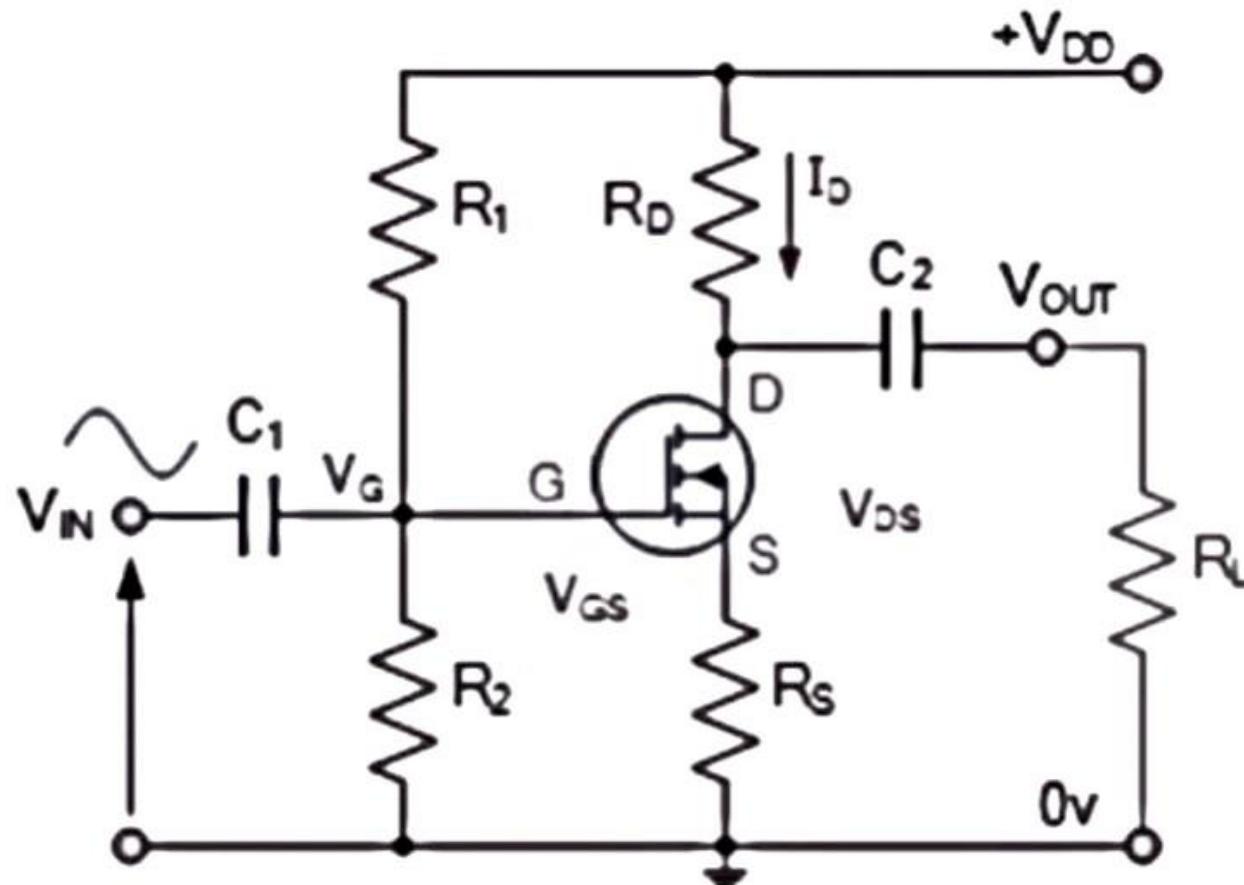
Substituting ④ in ③

$$R_D = \frac{V_{DD} - V_D}{I_D} \rightarrow ⑤$$

BASIC MOSFET AMPLIFIER ANALYSIS

- CALCULATION OF V_{GS} AND V_G

$$V_{GS} = V_G - V_S \rightarrow 6$$



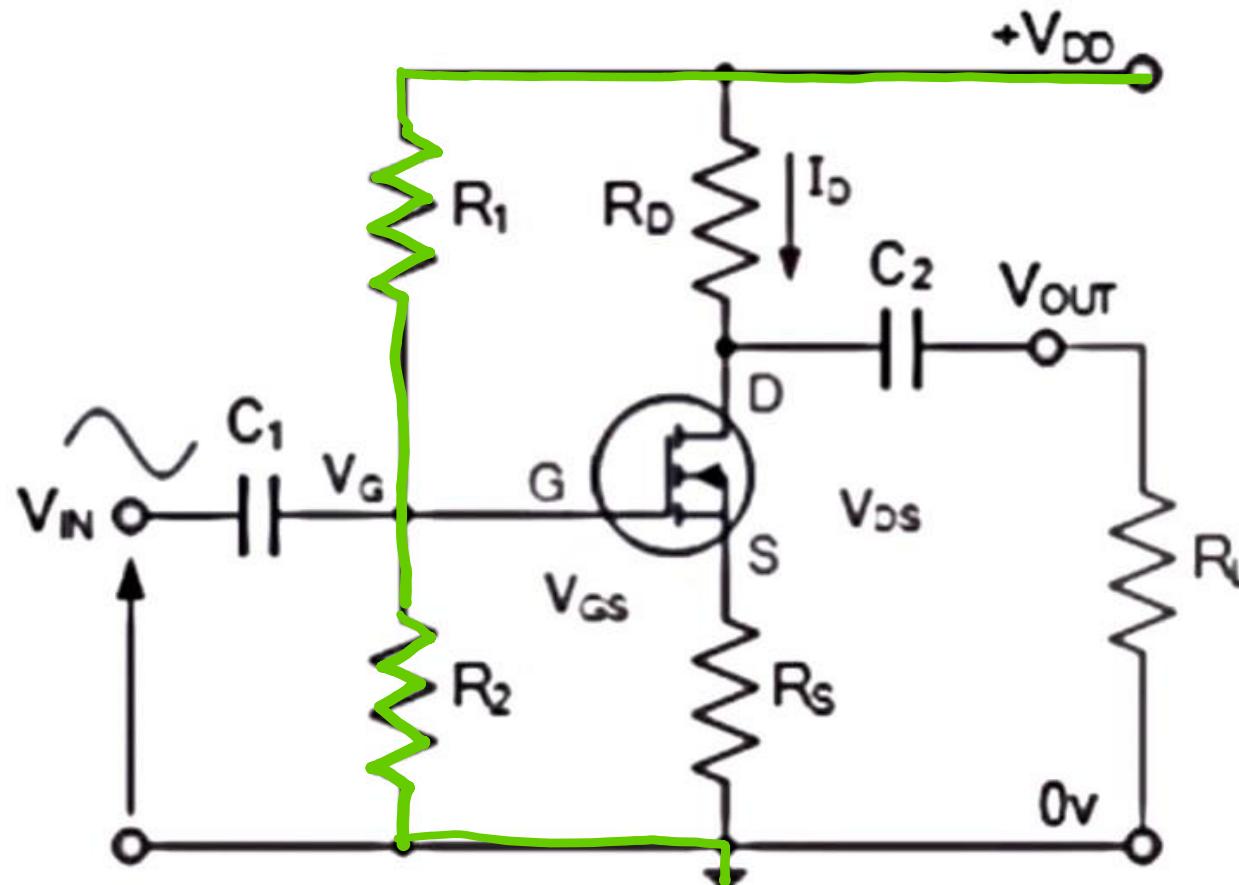
$$V_{GS} = V_G - I_S R_S$$

$$I_D \approx I_S$$

$$V_{GS} = V_G - I_D R_S \rightarrow 7$$

BASIC MOSFET AMPLIFIER ANALYSIS

- CALCULATION OF V_{GS} AND V_G



$$V_G = \frac{V_{DD} \times R_2}{R_1 + R_2}$$

$$V_G = V_{DD} \cdot \left(\frac{R_2}{R_1 + R_2} \right)$$

8

BIASING OF DEPLETION MODE MOSFET

- For a MOSFET to work an amplifier, have to bias properly.
- In depletion mode MOSFET, it requires a negative voltage at Gate.
- Three types of biasing techniques,
 - Fixed bias
 - Source Self bias
 - Voltage Divider bias

FIXED BIAS IN MOSFET

- 2 Power supplies are used.
- A fixed voltage is applied at Gate terminal of MOSFET.
- A negative power supply is applied at gate terminal.

$$V_G = -V_{GG}$$

$$V_S = 0$$

$$V_{GS} = V_G - V_S$$

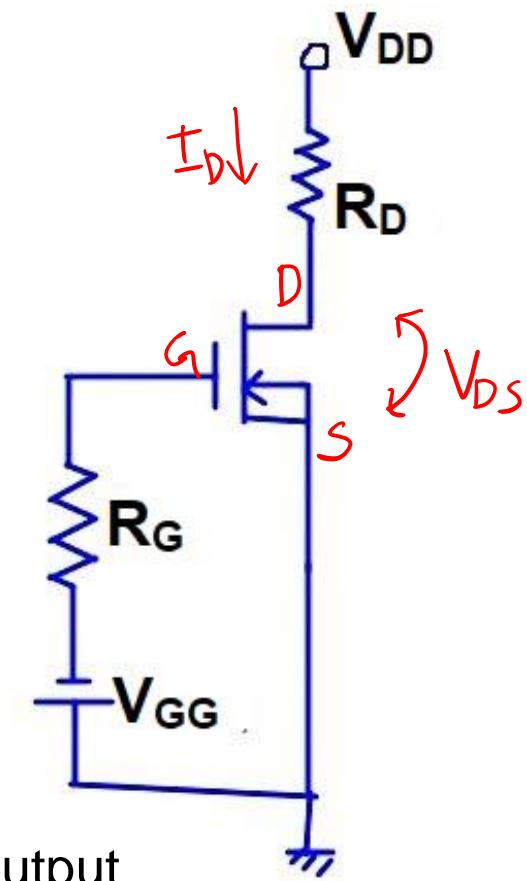
$$V_{GS} = -V_{GG}$$

FROM DRAIN LOOP

$$V_{DD} = I_D R_D + V_{DS}$$

$$V_{DS} = V_{DD} - I_D R_D$$

- In mosfet q-point is a function of input and output voltages, i.e. V_{GS} and V_{DS}
- DISADVANTAGE of fixed bias is it is using 2 power supplies.



SOURCE SELF BIAS IN MOSFET

- Not required 2 power supplies.
- Using single power supply the required negative voltage at gate with respect to source can be ensured by using a Resistor in source lead.

$$V_G = 0 \quad I_s \approx I_D$$

$$V_S = I_s R_S = I_D R_S$$

$$\begin{aligned} V_{GS} &= V_G - V_S \\ &= 0 - I_D R_S \end{aligned}$$

$$V_{GS} = -I_D R_S$$

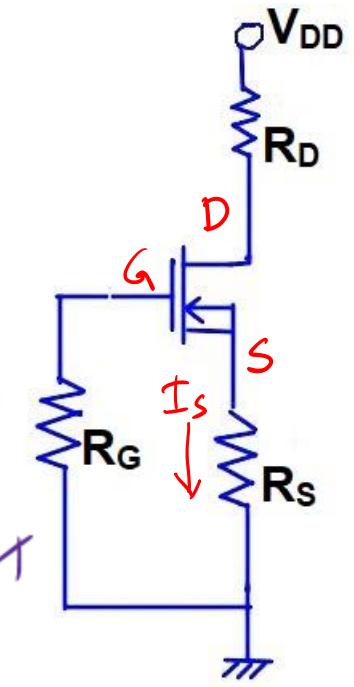
IN DRAIN Loop

$$V_{DD} = I_D R_D + V_{DS} + I_D R_S$$

VALUE OF I_D for Depletion MOSFET

$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_P} \right)^2$$

SHOCKLEY EQN



VOLTAGE DIVIDER BIAS IN MOSFET

- Most widely used method to provide biasing and stabilization to a MOSFET.
- Two resistances R_{G1} and R_{G2} connected across supply voltage V_{DD} and provide biasing.
- Drain resistance R_D provide stabilization.
- Voltage divider formed by resistors R_{G1} and R_{G2}

GATE VOLTAGE,

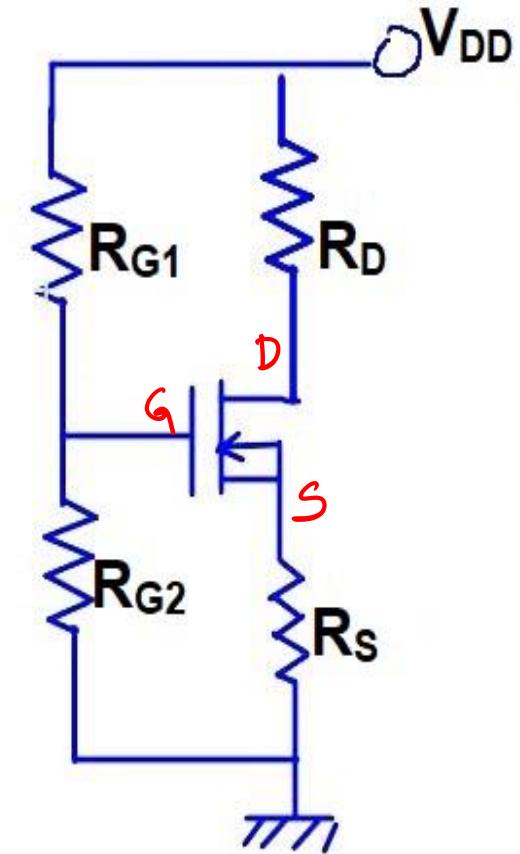
$$V_G = \frac{V_{DD} \times R_{G2}}{R_{G1} + R_{G2}}$$

$$V_S = I_S R_S \approx I_D R_S$$

$$V_{GS} = V_G - V_S$$

$$V_{GS} = \frac{V_{DD} \times R_{G2}}{R_{G1} + R_{G2}} - I_D R_S$$

- To ensure Negative V_{GS} , select R_{G1} and R_{G2} in such a way that V_G is less than V_S .



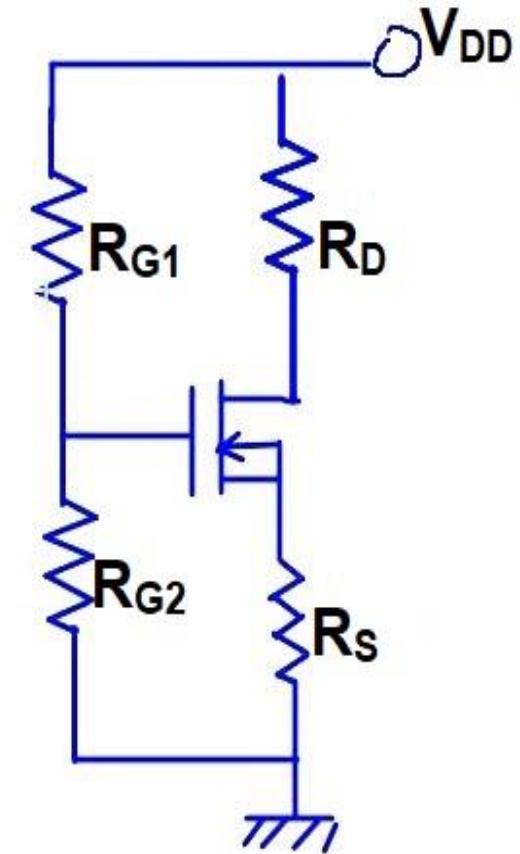
VOLTAGE DIVIDER BIAS IN MOSFET

FROM DRAIN LOOP,

$$V_{DD} = I_D R_D + V_{DS} + I_D R_S$$

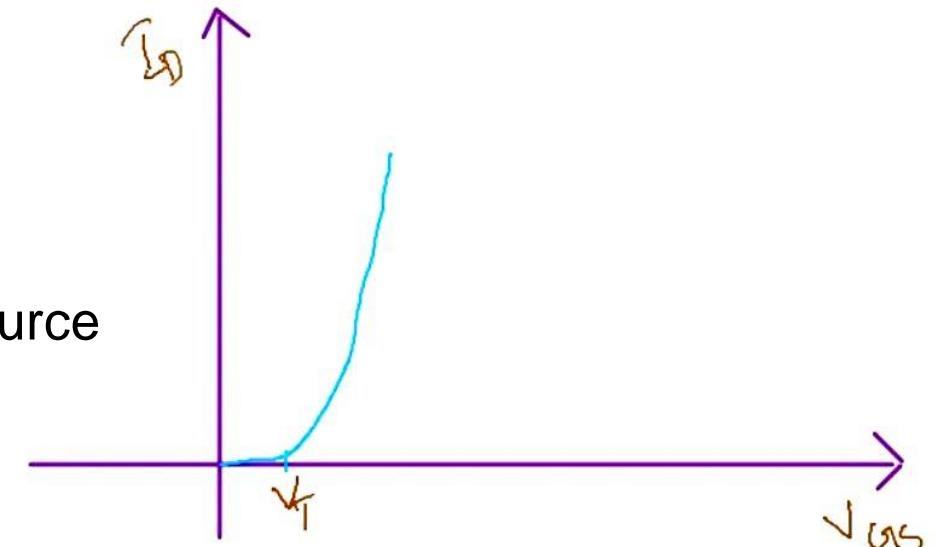
$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_P} \right)^2$$

$$V_{DS} = V_{DD} - I_D (R_D + R_S)$$



BIASING OF ENHANCEMENT MODE MOSFET

- In depletion mode MOSFET, already a channel will be there, but in Enhancement mode MOSFET channel to be induced.
- Conduction takes place in Enhancement mode MOSFET after channel formation.
- Channel will be formed when the input voltage applied is greater than threshold voltage.
- Depletion mode MOSFET normally in ON condition, Enhancement mode MOSFET normally in OFF condition.
- Enhancement mode MOSFET requires a Positive voltage at the gate.
- Enhancement mode MOSFET conducts when Gate to Source voltage (V_{GS}) exceeds threshold voltage (V_T)



BIASING OF ENHANCEMENT MODE MOSFET

- 3 biasing methods used
 - VOLTAGE DIVIDER BIAS
 - DRAIN TO GATE BIAS
 - MODIFIED DRAIN TO GATE BIAS

VOLTAGE DIVIDER BIAS IN E- MOSFET

- Most widely used method to provide biasing and stabilization to a MOSFET.
- Two resistances R_{G1} and R_{G2} connected across supply voltage V_{DD} and provide biasing.
- Drain resistance R_D provide stabilization.
- Voltage divider formed by resistors R_{G1} and R_{G2}

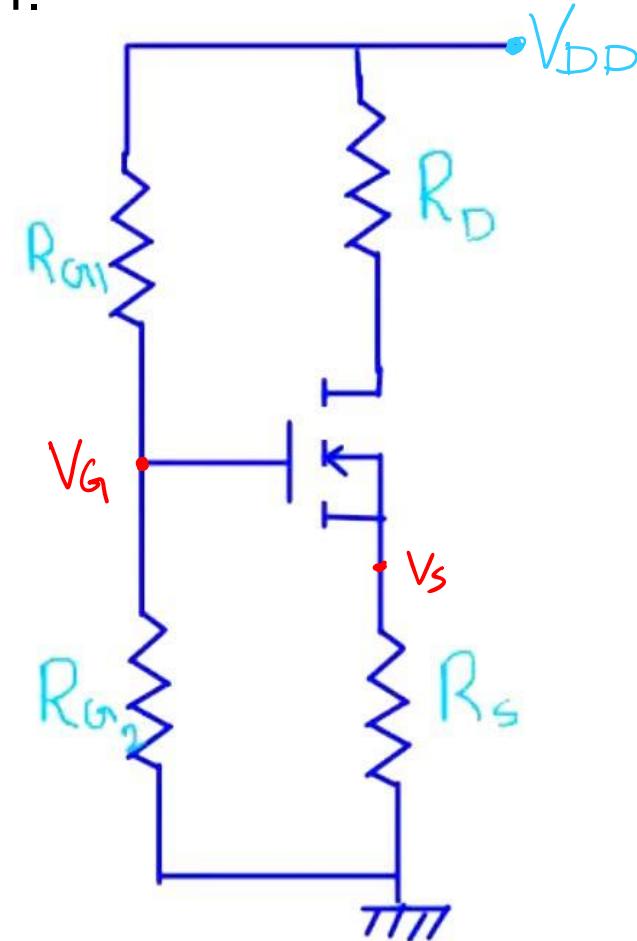
$$V_G = \frac{V_{DD} \times R_{G2}}{R_{G1} + R_{G2}}$$

$$V_S = I_D R_S$$

$$V_{GS} = V_G - V_S$$

$$V_{GS} = \frac{V_{DD} \times R_{G2}}{R_{G1} + R_{G2}} - I_D R_S$$

To ensure V_{GS} a POSITIVE value, select R_{G1} and R_{G2} in such a way that V_G is more than V_S



VOLTAGE DIVIDER BIAS IN E- MOSFET

CONSIDERING DRAIN Loop

$$V_{DD} = I_D R_D + V_{DS} + I_D R_S$$

$$V_{DS} = V_{DD} - I_D(R_D + R_S)$$

FOR E-MOSFET

$$I_D = K (V_{GS} - V_T)^2$$

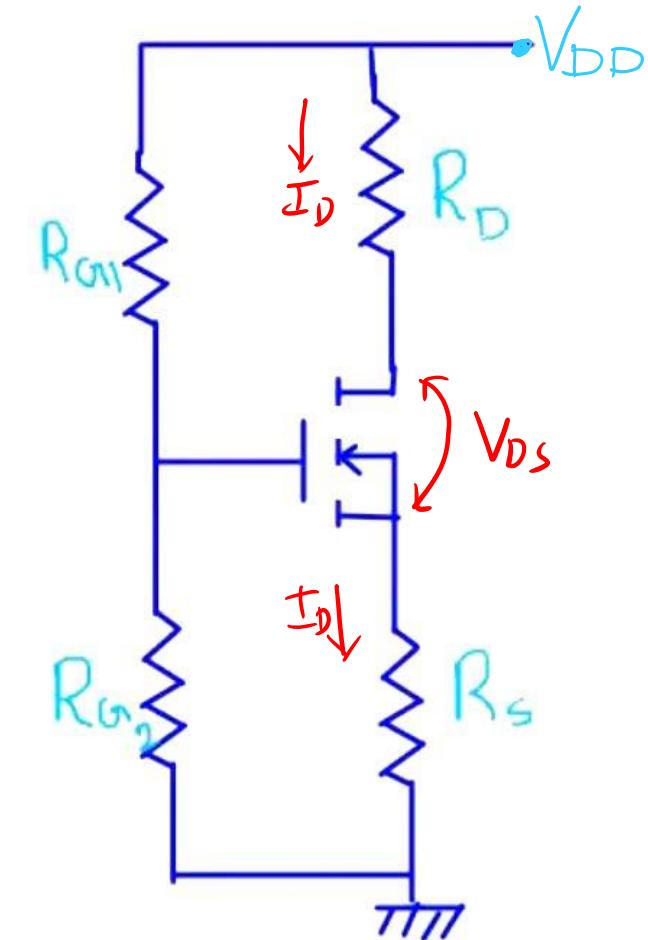
$$K = k_n' (W/L)$$

$$K = \mu_n C_{ox} (W/L)$$

(W/L) - width to length ratio

μ_n - mobility

C_{ox} - Oxide Capacitance



DRAIN TO GATE BIAS IN E- MOSFET

- Simple biasing technique used in E-MOSFET
- Biasing provide from Drain to Gate
- Gate is isolated here, so Gate current is Zero.

$$\text{So, } V_D = V_G$$

$$V_S = 0$$

$$V_{DS} = V_D - V_S = V_D$$

$$V_{GS} = V_G - V_S = V_G$$

$$V_{GS} = V_{DS}$$

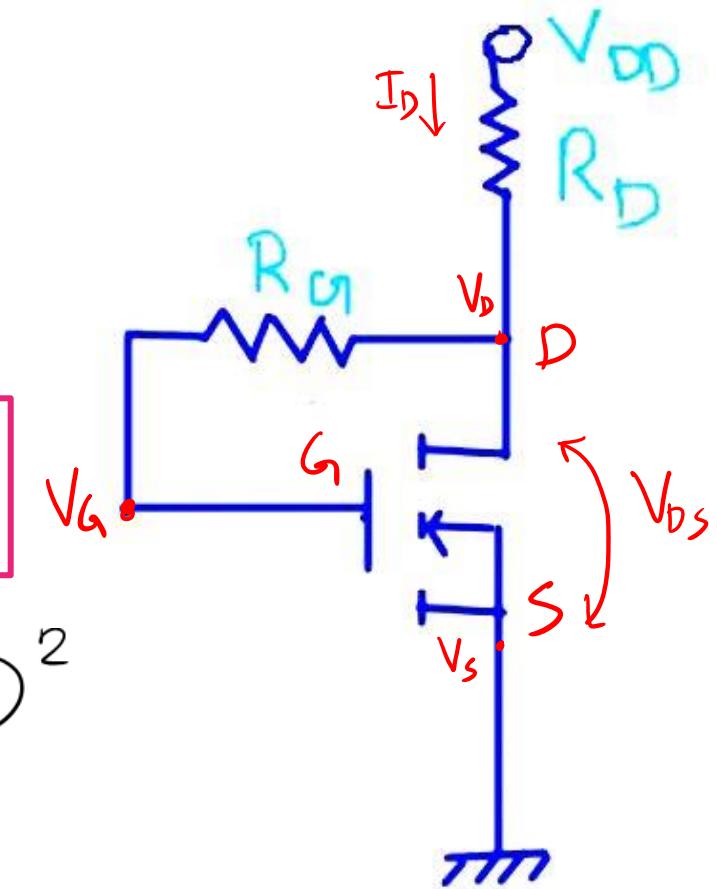
DRAIN LOOP

$$V_{DD} = I_D R_D + V_{DS}$$

$$V_{DS} = V_{DD} - I_D R_D$$

$$I_D = K(V_{GS} - V_t)^2$$

$$K = \mu_n C_{ox} (W/L)$$



MODIFIED DRAIN TO GATE BIAS IN E- MOSFET

- In some conditions VGS and VDS will be different, not equal
- So difficult to use Drain to Gate bias, so the circuit is modified by adding a resistance in gate

By Voltage Division rule

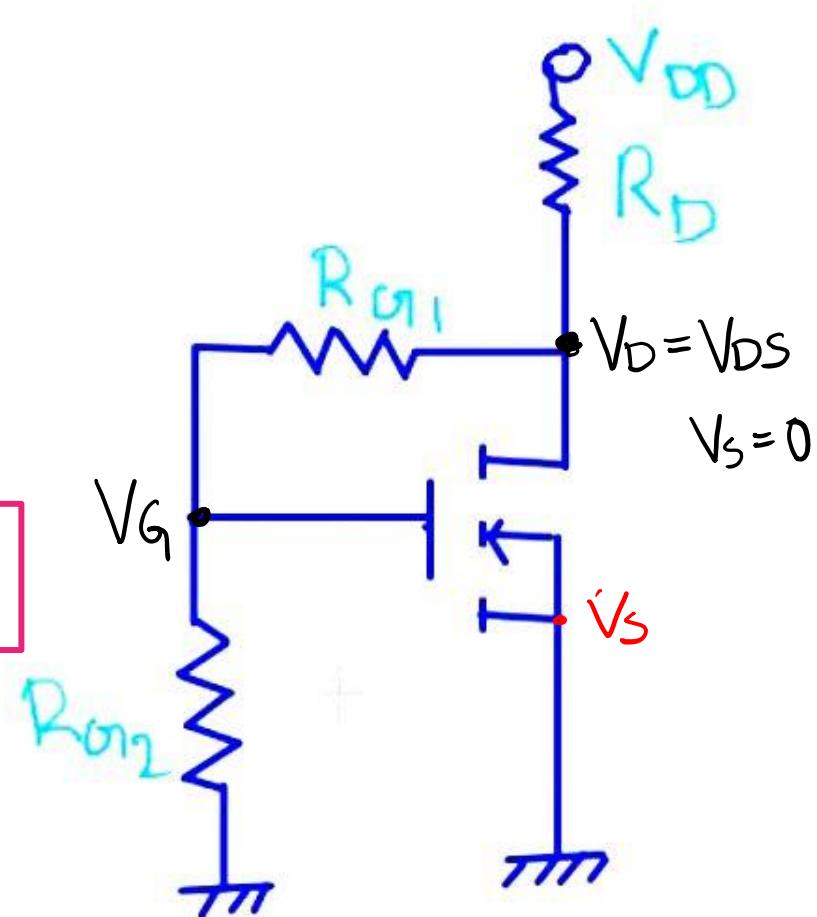
$$V_G = \frac{V_{DS} \times R_{G2}}{R_{G1} + R_{G2}} \quad V_S = 0$$

$$V_{GS} = \frac{V_{DS} \times R_{G2}}{R_{G1} + R_{G2}}$$

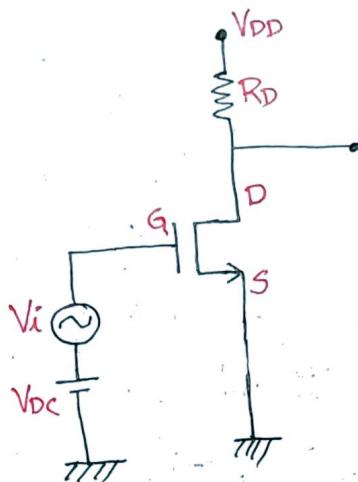
DRAIN LOOP $V_{DS} = V_D - V_S$
 $V_S = 0$

$$V_{DD} = I_D R_D + V_{DS}$$

$$V_{DS} = V_{DD} - I_D R_D$$



MOSFET SMALL SIGNAL MODEL



- Fig shows an n-channel enhancement MOSFET
- Common source n-channel enhancement MOSFET input applied between Gate and source terminal output taken across Drain and source terminal
- At Gate terminal, an AC input V_i is given along with a DC Voltage V_{DC} .
- DC input is given to providing biasing to the MOSFET, so that the MOSFET will work as a linear amplifier, if the biasing is fixed at Q-point in the saturation region.
- So the MOSFET here is biased at certain DC voltage V_{DC} , so that MOSFET operating point is fixed in saturation region, so that MOSFET works as a linear Amplifier.

The equation for drain current in saturation region is

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_t)^2$$

→ ①

μ_n - mobility

C_{ox} - Oxide Capacitance

$\frac{W}{L}$ - Width by length ratio

V_{GS} - Gate source voltage

V_t - threshold voltage

The Gate source voltage from fig is summation of V_i and V_{DC}

$$V_{GS} = V_i + V_{DC} \rightarrow ②$$

Substituting ② in ①

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_i + V_{DC} - V_t)^2$$

Here we can see

$I_D \propto V_i^2$ → relationship between drain current and input voltage is NOT LINEAR

- To make linear relationship between I_D and V_i , approximate V_i is very small (small signal approximation)

- So $I_D \propto V_i$, when V_i is taken very small value

so from equation can write $\Rightarrow V_i \ll (V_{DC} - V_t)$

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_i + (V_{DC} - V_t))^2$$

$$(a+b)^2 = a^2 + 2ab + b^2$$

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_i^2 + 2V_i(V_{DC} - V_t) + (V_{DC} - V_t)^2)$$

- V_i taken very small
so V_i^2 term can be neglected from Eqn.:

$$I_D = \frac{1}{2} \mu n C_{ox} \frac{W}{L} (2 V_i (V_{DC} - V_t)) + \frac{1}{2} \mu n C_{ox} \frac{W}{L} (V_{DC} - V_t)^2$$

$$I_D = \underbrace{\mu n C_{ox} \frac{W}{L} (V_{DC} - V_t) V_i}_{\text{Transconductance } (g_m)} + \underbrace{\frac{1}{2} \mu n C_{ox} \frac{W}{L} (V_{DC} - V_t)^2}_{\text{DC Component}}$$

$$I_D = I_{D0} + g_m V_i$$

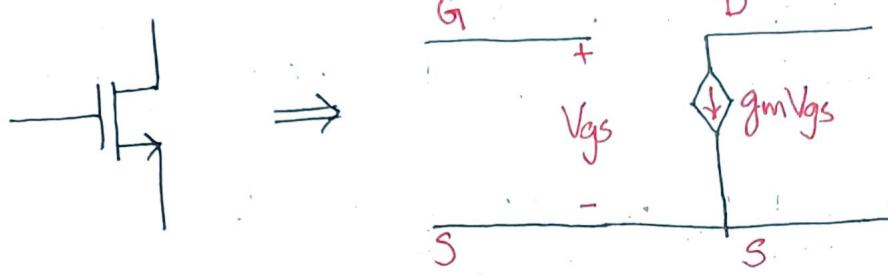
- if DC Analysis is made
AC component is not considered
- AC Analysis is made
DC component is not considered

- Also, $\boxed{I_D \propto V_i}$, as we have taken
Small Signal Approximation
the change in drain current I_D , is linearly proportional to input AC signal V_i , in that case MOSFET can be replaced by its
SMALL SIGNAL MODEL

I_{D0} - DC Drain Current

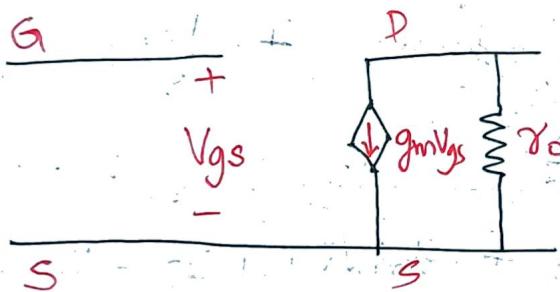
$g_m V_i$ - change in Drain current due to AC i/p signal

$g_m = \mu n C_{ox} \frac{W}{L} (V_{DC} - V_t)$



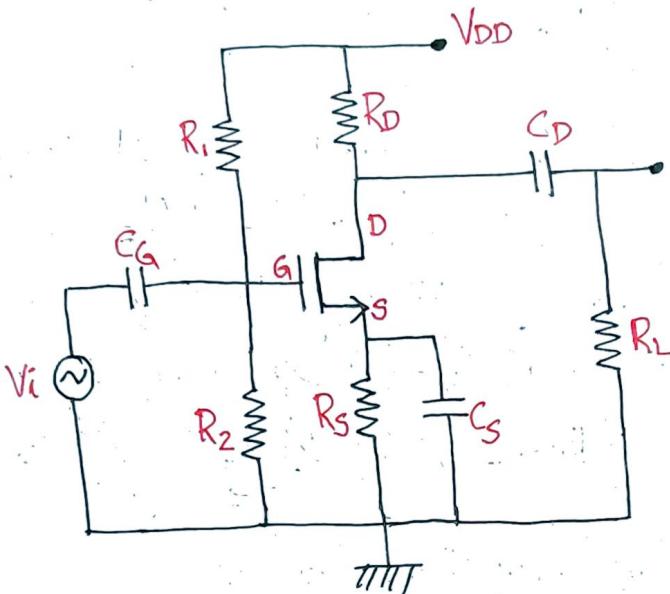
- Small signal model with out considering channel length modulation, λ

$$\text{Drain current } i_D = gm V_{gs}$$



- if channel length modulation, λ is considered
resistance r_0 is added in drain source terminal.

SMALL SIGNAL ANALYSIS OF CS AMPLIFIER



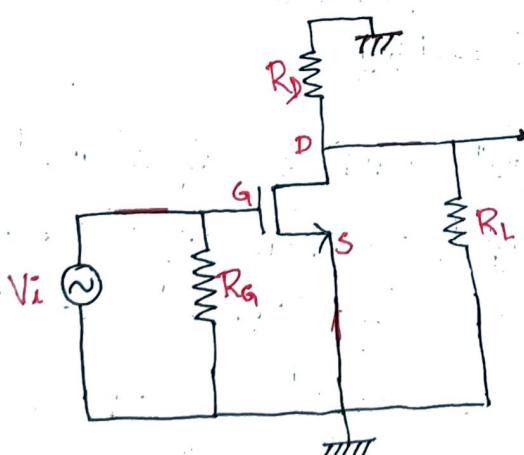
- Fig shows n-channel Enhancement Common Source Amplifier with voltage divider circuit.
- It is called CS Amplifier because, a small input (V_i) applied between gate and source terminal and output taken across Drain and source terminal. So, Source terminal common to input and output.
- C_G is the input coupling capacitor at gate
- C_D is the output coupling capacitor at drain
- C_S is the bypass capacitor at the source
- R_S is the source resistance, R_D is the drain resistance and R_L is the load resistance
- R_1 and R_2 is the voltage divider resistors which provides biasing to the Amplifier.

- IN case of DC Analysis, will take AC if as Zero, as well as all the coupling and bypass capacitors are open circuited.
- IN case of AC low frequency/mid frequency analysis, will make all DC Voltage supplies as ground and coupling and bypass capacitors shorted. (short circuited), inter electrode capacitors also act as open circuited.

⇒ Steps in Small Signal Analysis

- ① Draw AC Equivalent Circuit
- ② Replace MOSFET by its Small Signal model
- ③ Analysis

AC EQUIVALENT CIRCUIT



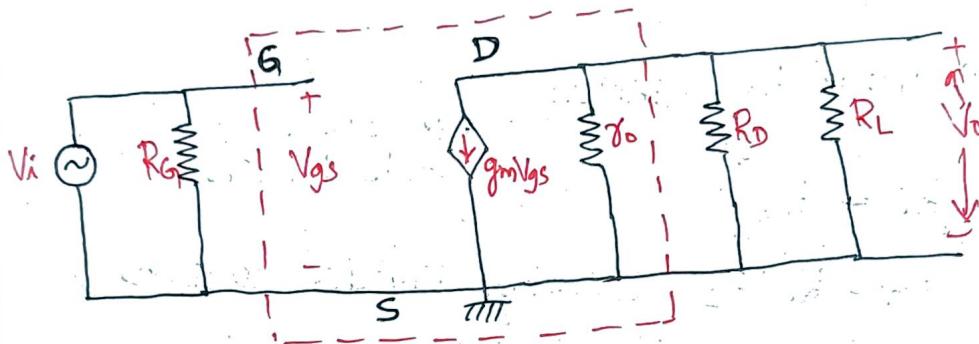
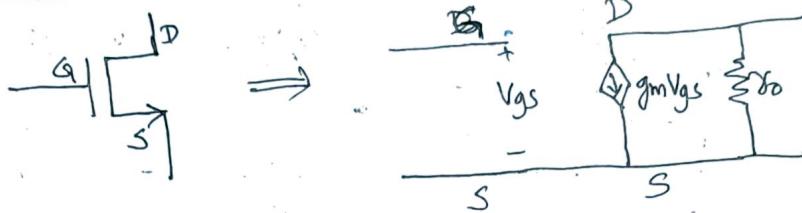
DC Supply → Ground
Coupling Cap } → Short
By pass cap }

$$R_G = (R_1 || R_2)$$

- Effect of R_G is neglected as C_G is short circuited.

② REPLACE AC EQUIVALENT MOS TRANSISTOR

TO SMALL SIGNAL MODEL

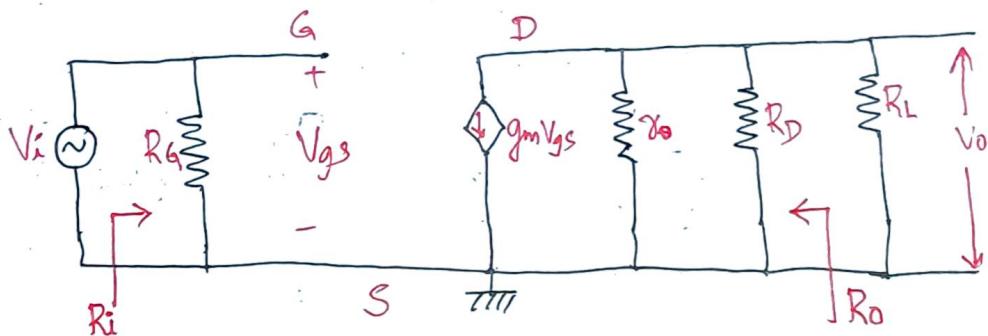


- R_G is the voltage divider resistor at Gate, $R_G = R_{RR}(R_1 || R_2)$
- R_D drain resistor, R_D and Load resistor R_L in the ~~drain~~ Output side.

③ ANALYSIS OF SMALL SIGNAL MODEL

Parameters to determine

- ① INPUT RESISTANCE
- ② OUTPUT RESISTANCE
- ③ VOLTAGE GAIN



① INPUT RESISTANCE

$$R_i = R_G$$

• resistance b/w i/p & Gate Terminal.

$$R_G = R_1 \parallel R_2 \quad (\text{Voltage Divider resistors})$$

$$R_i^o = (R_1 \parallel R_2)$$

② OUTPUT RESISTANCE

• resistance b/w output & Drain terminal

$$R_o = R_D \parallel \gamma_o$$

③ VOLTAGE GAIN

$$\text{From circuit, } V_i = V_{gs} \rightarrow ①$$

$$\text{From output side, } V_o = R_{eq} \times i_D \rightarrow ②$$

$$i_D = g_m V_{gs} \xrightarrow{③}, R_{eq} = (\gamma_o \parallel R_D \parallel R_L) \rightarrow ④$$

current direction is opposite, so a negative sign for direction of current flow.

Substituting ④ and ③ in ②

$$V_o = -g_m V_{gs} (\gamma_D \parallel R_D \parallel R_L) \rightarrow ⑤$$

$$V_i = V_{gs}$$

the voltage gain, $A_v = \frac{V_o}{V_i}$

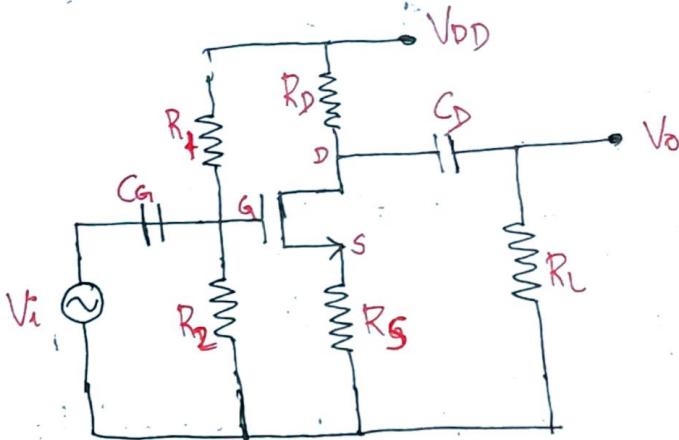
Substituting V_o and V_i

$$A_v = \frac{V_o}{V_i} = \frac{-g_m V_{gs} (\gamma_{D\parallel} \parallel R_D \parallel R_L)}{V_{gs}}$$

$$A_v = -g_m (\gamma_{D\parallel} \parallel R_D \parallel R_L)$$

SMALL SIGNAL ANALYSIS OF CS AMPLIFIER

WITHOUT BYPASS CAPACITOR

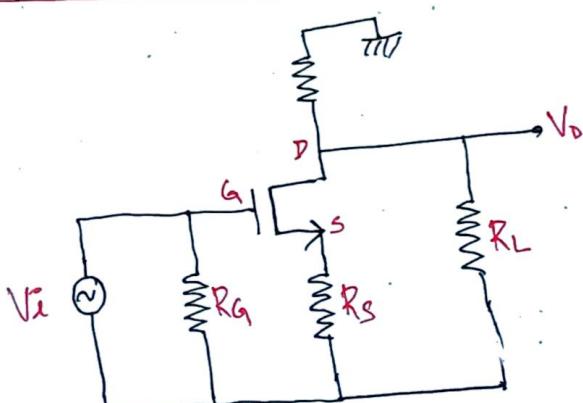


- Here Bypass capacitor C_S is not present in Source terminal
- As C_S is not present the effect of R_S to be taken in the Analysis.

→ STEPS IN SMALL SIGNAL ANALYSIS

- ① Draw AC Equivalent ckt
- ② Replace MOSFET by its small signal model
- ③ Analysis

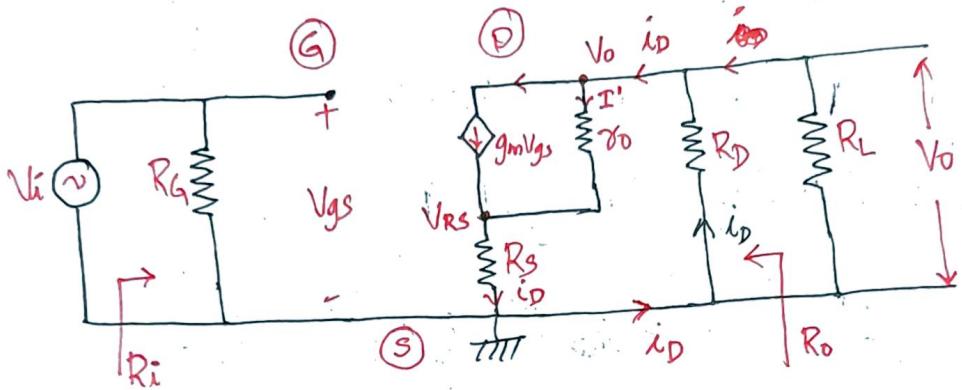
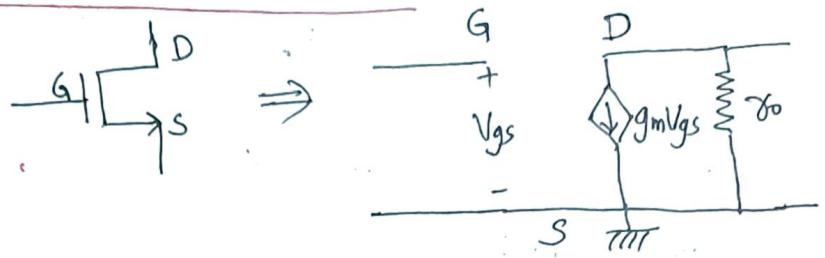
AC EQUIVALENT CKT



DC Supply \rightarrow Ground
Coupling Cap \rightarrow Short

$$R_G = (R_1 \parallel R_2)$$

② REPLACE AC EQUIVALENT MOS TRANSISTOR
TO SMALL SIGNAL MODEL



① INPUT RESISTANCE

Input resistance, $R_i = R_G$

$$R_G = R_1 \parallel R_2$$

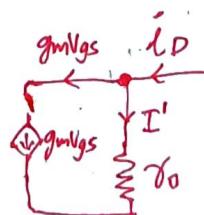
$$R_i = R_G = (R_1 \parallel R_2)$$

② VOLTAGE GAIN

$$A_v = \frac{V_o}{V_i}$$

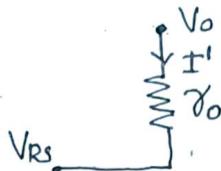
current direction is opposite

$$V_o = -i_D R_D \rightarrow ①$$



From Fig, $i_D = g_m V_{gs} + I' \rightarrow ②$

To find I'



$$I' \gamma_0 = V_o - V_{RS} \rightarrow ③$$

$$V_{RS} = i_D R_S \rightarrow ④$$



$$\text{From } ② \Rightarrow V_o = -i_D R_D$$

substituting ④ and ② in ③

$$I' \gamma_0 = -i_D R_D - i_D R_S$$

$$I' \gamma_0 = -i_D (R_D + R_S)$$

$$I' = \frac{-i_D (R_D + R_S)}{\gamma_0} \rightarrow ⑤$$

substitute eqn ⑤ in ②

$$\text{eqn } ② \Rightarrow i_D = g_m V_{GS} + I'$$

$$i_D = g_m V_{GS} - \frac{i_D (R_D + R_S)}{\gamma_0} \rightarrow ⑥$$

We know,

$$V_{GS} = V_g - V_s$$

$$V_{GS} = V_i - i_D R_S \rightarrow ⑦$$

Sub ⑦ in ⑥

$$i_D = g_m (V_i - i_D R_S) - \frac{i_D (R_D + R_S)}{\gamma_0}$$

$$i_D = g_m V_i - g_m i_D R_S - i_D \frac{(R_S + R_D)}{\infty}$$

$$g_m V_i = i_D \left(1 + g_m R_S + \left(\frac{R_S + R_D}{\infty} \right) \right)$$

$$i_D = \frac{g_m V_i}{1 + g_m R_S + \left(\frac{R_D + R_S}{\infty} \right)}$$

→ ⑧

we know

$$V_o = -i_D \cdot R_D \rightarrow ①$$

substitute ⑧ in ①

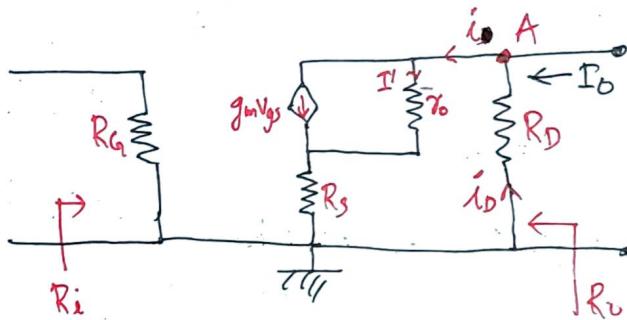
$$V_o = - \frac{g_m V_i}{1 + g_m R_S + \left(\frac{R_D + R_S}{\infty} \right)} \times R_D$$

$$A_V = \frac{V_o}{V_i} = \frac{-g_m R_D}{1 + g_m R_S + \left(\frac{R_D + R_S}{\infty} \right)} \rightarrow ②$$

$$A_V = \frac{-g_m R_D}{1 + g_m R_S + \left(\frac{R_D + R_S}{\infty} \right)}$$

③ OUTPUT RESISTANCE

For determining $\%/\text{p}$ res, set $V_i = 0$



$$R_o = \frac{V_o}{I_o} \rightarrow ⑩$$

$$V_o = -i_D R_D$$

$$V_{gs} = V_g - V_s = V_i - i_D R_s \Rightarrow ⑪$$

$$V_{gs} = -i_D R_s \rightarrow ⑪$$

From node A

$$I_o + i_D = i \rightarrow ⑫$$

$$\text{where as, } i = g_m V_{gs} + I'$$

$$I_o + i_D = I' + g_m V_{gs}$$

$$\text{from } ⑤ \Rightarrow I' = -i_D \frac{(R_D + R_s)}{\gamma_0}$$

$$\begin{aligned} I_o &= -i_D - i_D \frac{(R_D + R_s)}{\gamma_0} + g_m V_{gs} \\ &= -i_D - i_D \frac{(R_D + R_s)}{\gamma_0} + g_m (-i_D R_s) \end{aligned}$$



$$I_o = -i_D \left(\frac{R_D + R_S}{\gamma_0} + g_m R_S + 1 \right)$$

→ (13)

We know, $R_o = \frac{V_o}{I_o}$

$$V_o = -i_D R_D$$

$$R_o = \frac{-i_D R_D}{-i_D \left(\frac{R_D + R_S}{\gamma_0} + g_m R_S + 1 \right)}$$

$$R_o = \frac{R_D}{\frac{R_D + R_S}{\gamma_0} + g_m R_S + 1}$$

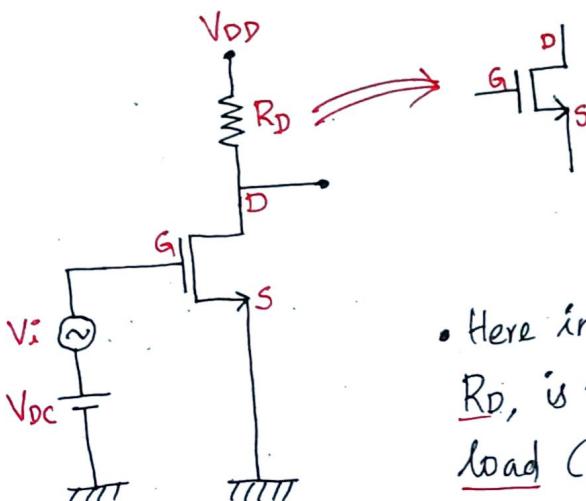
MOSFET AMPLIFIER WITH ACTIVE LOAD

- what is an Active load? and why it is commonly used in Amplifier circuits.

⇒ Active loads are commonly used in Integrated Circuits where Size and Power consumption are major concern.

eg: In case of an IC, if a resistor is there, it requires more space. Instead of that if an active components like MOSFET or MOSFET Circuits are used it requires less space and less power consumption.

⇒ Active component or Active devices used instead of a resistor is known as ACTIVE LOAD



• Here in this fig, the resistor R_D , is replaced by Active load (MOSFET)

• So this, MOSFET act as ACTIVE LOAD

- For a Common Source Amplifier, the gain,

$$A_V = -g_m (\gamma_0 \| R_D)$$

if channel length modulation is neglected (~~is neglected~~)

$$A_V = -g_m R_D$$

So to Increase gain

① \Rightarrow Increase R_D

② \Rightarrow Increase g_m (transconductance)

\Rightarrow If we are Increasing value of R_D ,

We cannot increase the value of R_D indefinitely,
as it is increased, the voltage across R_D increases,
so the available voltage at the drain reduces.

So it is not a stable option.

\Rightarrow Increasing value of g_m

we know

$$I_D = \frac{1}{2} \mu_n C_{ox} (V_{GS} - V_t) \frac{W}{L} \rightarrow ①$$

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}} \left(\frac{\text{change in } I_D}{\text{change in } V_{GS}} \right)$$

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = \frac{1}{2} \times \mu_n C_{ox} 2 (V_{GS} - V_t) \left(\frac{W}{L} \right)$$

$$g_m = \mu_n C_{ox} \left(\frac{W}{L} \right) (V_{GS} - V_t) \rightarrow ②$$

$$\text{From Eqn ①} \Rightarrow I_D = \frac{1}{2} \mu n C_{ox} (V_{GS} - V_t) \left(\frac{W}{L} \right)^2$$

$$(V_{GS} - V_t) = \sqrt{\frac{2 I_D}{\mu n C_{ox} \left(\frac{W}{L} \right)}}$$

$$g_m = \mu n C_{ox} \left(\frac{W}{L} \right) (V_{GS} - V_t) = \mu n C_{ox} \left(\frac{W}{L} \right) \sqrt{\frac{2 I_D}{\mu n C_{ox} \left(\frac{W}{L} \right)}}$$

$$g_m = \sqrt{2 I_D \mu n C_{ox} \left(\frac{W}{L} \right)}$$

→ ③

$$\text{From ①} \Rightarrow I_D = \frac{1}{2} \mu n C_{ox} \left(\frac{W}{L} \right) (V_{GS} - V_t)^2$$

$$\text{From ②} \Rightarrow g_m = \mu n C_{ox} \left(\frac{W}{L} \right) (V_{GS} - V_t)$$

$$\frac{\textcircled{2}}{\textcircled{1}} = \frac{g_m}{I_D} = \frac{2}{(V_{GS} - V_t)}$$

$$g_m = \frac{2 I_D}{V_{GS} - V_t}$$

→ ④

$$\Rightarrow \text{From } \textcircled{4} \quad g_m = \frac{2 I_D}{(V_{GS} - V_t)}$$

$(V_{GS} - V_t) \Rightarrow$ overdrive voltage

- So to Increase g_m , I_D can Increase, but if I_D is increased, the power con dissipation will be increased, also due to rise in I_D the voltage

drop across R_D increase, which reduces available drain voltage

⇒ So not a suitable solution by increasing I_D

• ⇒ from ③ ⇒ $g_m = \sqrt{2 \mu n C_o (\frac{W}{L})} I_D$

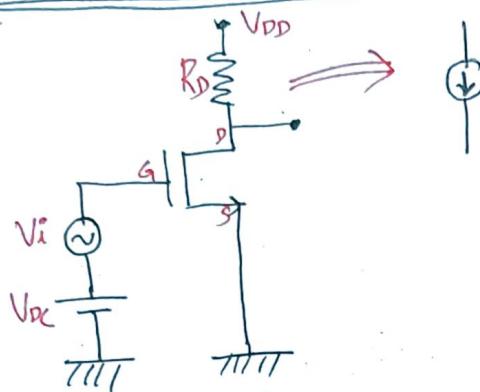
if Increase $(\frac{W}{L})$ ratio, g_m can be Increased

but Increasing $(\frac{W}{L})$ ratio make transistors consuming more space.

⇒ So not a suitable solution by Increasing $(\frac{W}{L})$ ratio

⇒ Possible way is to replace resistor (R_D) by a current source and current source act as ACTIVE LOAD.

• COMMON SOURCE AMPLIFIER WITH CURRENT SOURCE LOAD



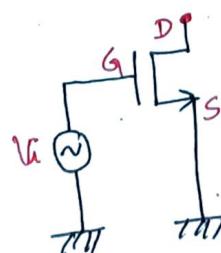
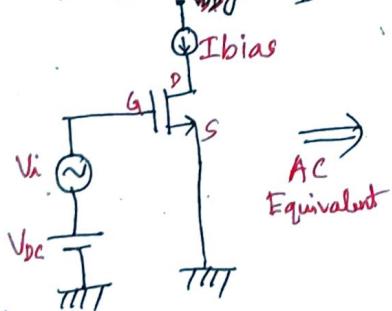
- Here the resistor (RD) will be replaced by an ACTIVE LOAD, that is a CURRENT SOURCE.

⇒ If the current source is an IDEAL CURRENT SOURCE

the following advantages are there

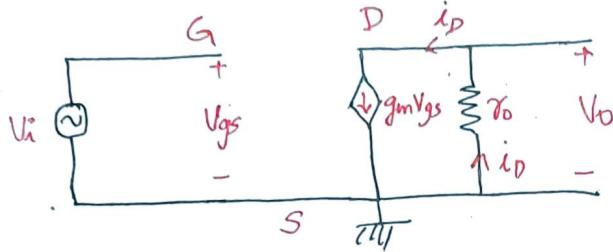
- Biasing current of the circuit is independent of temperature.
- During small signal Analysis, ideal current source is replaced by open circuit.
ie, the resistance become Infinity

$$\Rightarrow A_{v0} = \frac{V_{DD}}{I_{bias} R_D} \Rightarrow R_D \rightarrow \infty \Rightarrow A_{v0} \rightarrow \infty$$



- Open circuited the Ideal current source

- Small signal model (considering channel length modulation)



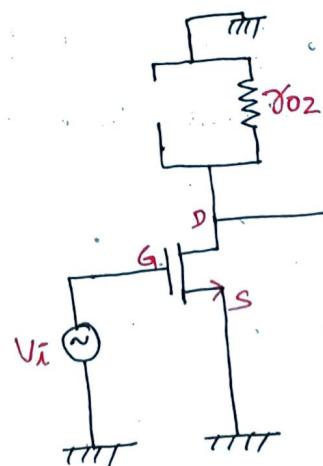
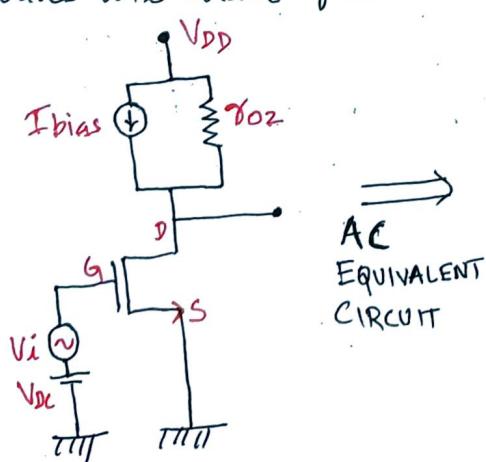
$$V_i = V_{gs}$$

$$V_o = -i_D r_D = -gmV_{gs} r_D$$

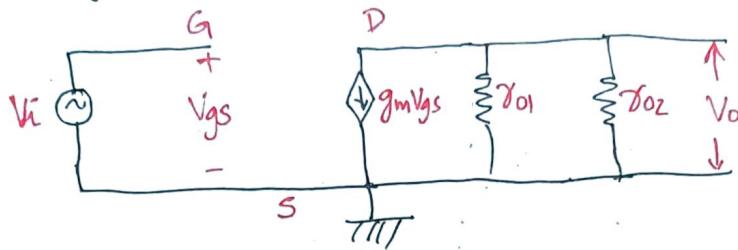
$$A_v = \frac{V_o}{V_i} = -\frac{gmV_{gs}r_D}{V_{gs}}$$

$$\boxed{A_v = -gm r_D}$$

- So there is significant improvement in gain here and this gain is called INTRINSIC GAIN
 \Rightarrow It is the maximum obtainable gain for a Common Source Amplifier. It is obtained when current source used is Ideal current source.
- if we are using actual current source, the current source will have finite output resistance



- Small signal model for the ckt



r_{o1} - output resistance of MOSFET
due to channel length modulation

r_{o2} - output resistance of current source

So here

$$V_i = V_{gs}$$

$$V_o = -i_D (r_{o1} \parallel r_{o2})$$

$$i_D = g_m V_{gs}$$

$$V_o = -g_m V_{gs} (r_{o1} \parallel r_{o2})$$

$$A_v = \frac{V_o}{V_i} = \frac{-g_m V_{gs} (r_{o1} \parallel r_{o2})}{V_{gs}}$$

$$A_v = -g_m (r_{o1} \parallel r_{o2})$$

- Gain is less than Intrinsic voltage gain, but greater than obtained by using drain resistance.

- How to make current source using MOSFET?

- MOSFET can be used as current source in Saturation region.

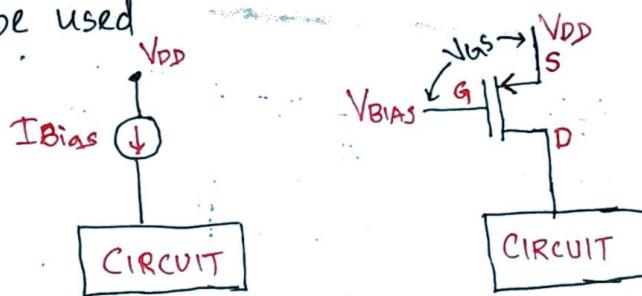
In saturation region,

$$I_D = \frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L} \right) (V_{GS} - V_t)^2$$

$$I_D = k (V_{GS} - V_t)^2$$

⇒ if we are using fixed value of V_{GS} , I_D can make constant, so that can make MOSFET work as a current source

⇒ If MOSFET is used as current source between power supply and circuit, P-type MOSFET can be used

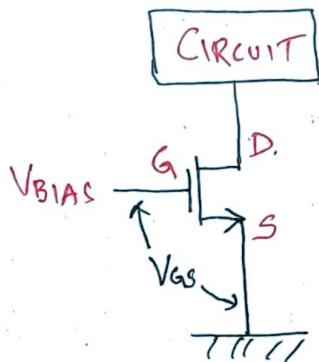
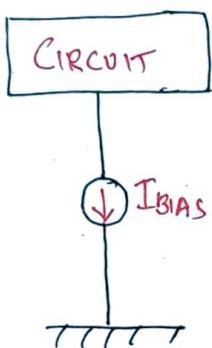


- Source terminal connected to V_{DD}
- fixed voltage applied at Gate
- Drain terminal remaining circuit is connected

• MOSFET to work in Saturation region, so

$$V_{SD} \geq V_{GS} - V_t$$

→ if MOSFET used as current source between circuit and ground, we can use n-type MOSFET



- Drain connected to ckt.
- fixed bias given at Gate.
- source is grounded.
- To operate MOSFET in saturation region,

$$V_{DS} \geq V_{GS} - V_t$$

Fig-1

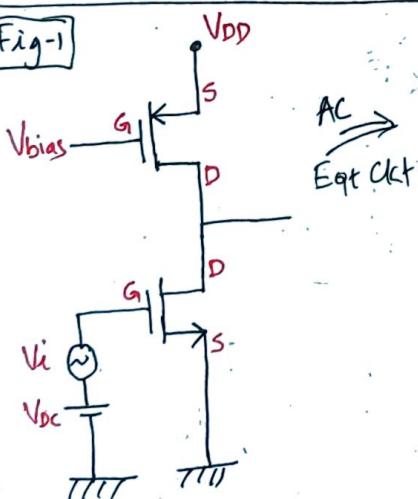
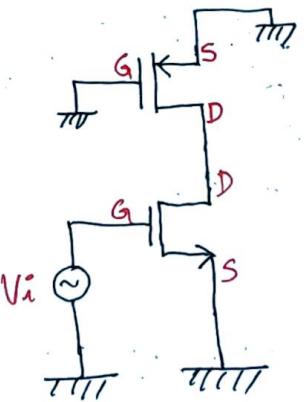
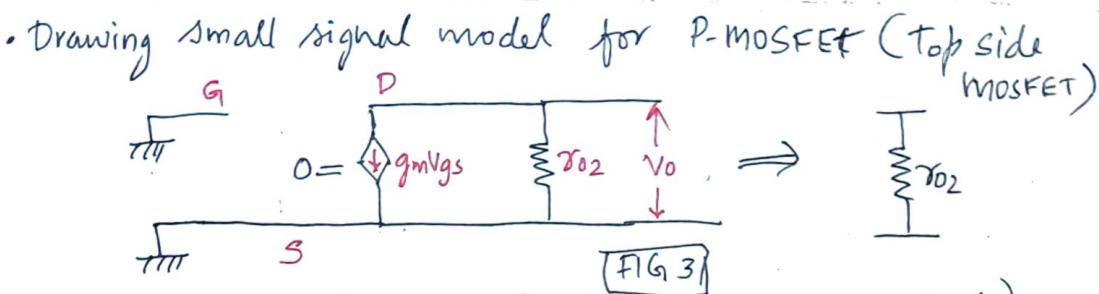


FIG 2



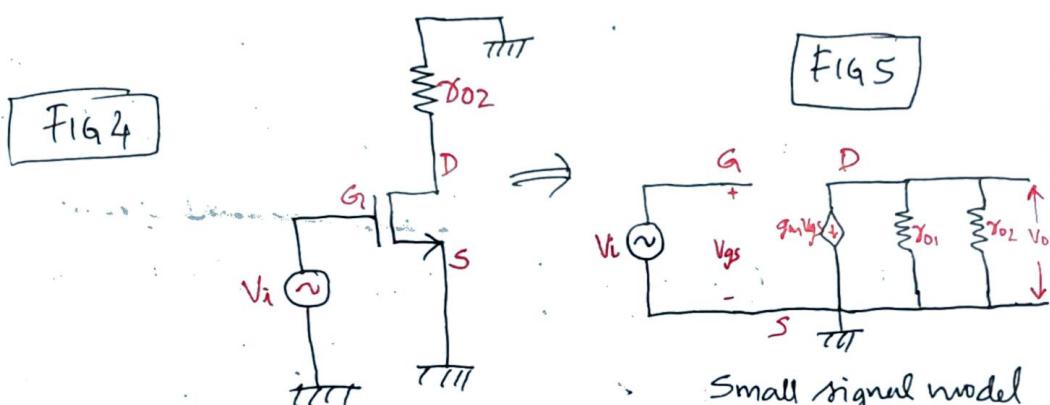
- In the fig, current source replaced by a p-mos.
- While drawing AC equivalent ckt, DC sources replace as ground.



• Here gate is grounded, source also grounded
 $V_{GS} = V_G - V_S = 0$, so $i_D = gmV_{GS} = 0$

so equivalent small signal ckt consist only a resistance (r_{D2}) [r_{D2} - $\frac{1}{gm}$ is 0/p resistance of P-MOSFET]

so figure 2 can redrawn as



Small signal model
 $|r_{D2}|$ - 0/p res of n-mos

- P-mos replaced on a resistance r_{D2} .
- The small signal model of fig 4 is drawn in fig 5. From that

fig 4: $V_i = V_{GS}$, $V_o = -i_D (r_{D1} \parallel r_{D2})$

$$i_D = gmV_{GS}$$

$$AV = \frac{V_o}{V_i} = -\frac{gmV_{GS}(r_{D1} \parallel r_{D2})}{V_{GS}}$$

$$AV = -gm(r_{D1} \parallel r_{D2})$$

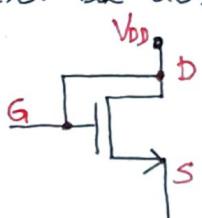
- This gain is less than Intrinsic voltage gain due to finite load resistance. if $r_{D1} = r_{D2} = r_D$, $AV = -\frac{gm r_D}{2}$

Voltage gain is half of Intrinsic gain, if $r_{D1} = r_{D2}$

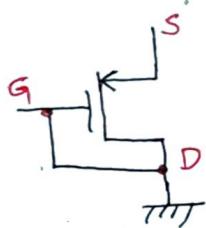
COMMON SOURCE STAGE WITH DIODE CONNECTED LOAD

- CS stage with a diode connected load is an Active load. Active loads are used in IC to reduce power consumption and also size.

- In a N-MOSFET, if Gate and drain terminals are shorted and connected to DC supply, it will ~~be~~ act as a diode connected load



- In a P-MOSFET, if Gate and drain terminals are shorted and connected to the ground, it will act as a diode connected load.



CS stage with Diode connected load using N-MOS

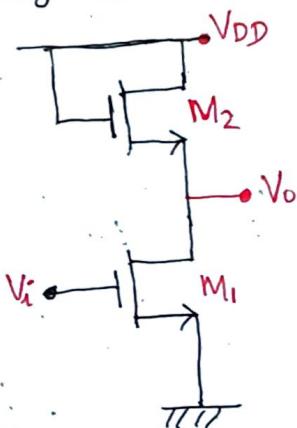


FIG-1

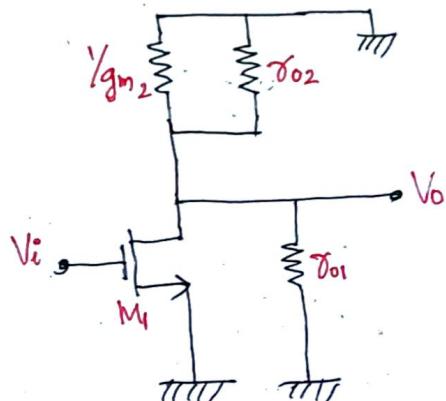


FIG-2

Fig-1 shows a CS stage with a Diode connected load with n-MOS, where input applied at MOSFET-1 and MOSFET-2 taken as a diode connected load

Fig-2 is the equivalent small signal circuit with diode connected load, where g_{m2} is the transconductance of and γ_{o2} is the output resistance of diode connected load, and γ_{o1} is the output resistance of MOSFET-1

⇒ Gain of the stage,

$$A_V = -g_{m1} \left(\frac{1}{g_{m2}} \parallel \gamma_{o1} \parallel \gamma_{o2} \right)$$

output resistance,

$$R_o = \left(\frac{1}{g_{m2}} \parallel \gamma_{o2} \parallel \gamma_{o1} \right)^{-1}$$

g_{m1} = G. Transconductance of MOSFET-1 where input is applied.

g_{m2} = Transconductance of MOSFET-2
diode connected load

γ_{o1} = O/p resistance of MOSFET-1

γ_{o2} = O/p resistance of MOSFET-2

- if we are neglecting channel length modulation

$$\gamma = 0, \therefore \gamma_{o1} = \gamma_{o2} = 0$$

$$A_V = -\frac{g_{m1}}{g_{m2}}$$

$$g_{m1} = \sqrt{2} \mu_n C_{ox} (W/L)_1 I_D$$

$$g_{m2} = \sqrt{2} \mu_n C_{ox} (W/L)_2 I_D$$

$$A_V = \sqrt{\frac{(W/L)_1}{(W/L)_2}}$$

- Gain depends on width to length ratio.
Gain is depending on dimensions of M₁ and M₂
and not depending of process parameter
M_n and C_{ox} and drain current I_D

- This diode connected topology exhibits Moderate gain due to relatively low Impedance of diode connected load.

- Diode connected load not considered in Common Emitter BJT because

$$A_V = -g_{m_1} \cdot \frac{1}{g_{m_2}}$$

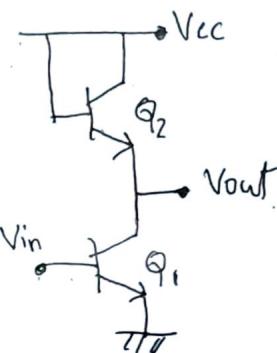
$$g_{m_1} = \frac{I_{C_1}}{V_T} \quad g_{m_2} = \frac{I_{C_2}}{V_T}$$

$$A_V = -\frac{I_{C_1}}{I_{C_2}}$$

$$I_{G_1} \approx I_{C_2}$$

$A_V \approx -1$

∴ It provides unity voltage gain only.



- The Transconductance of MOSFET depends on device dimension but in BJT it is not dependent on device dimension.

CS Stage with Diode connected PMOS device

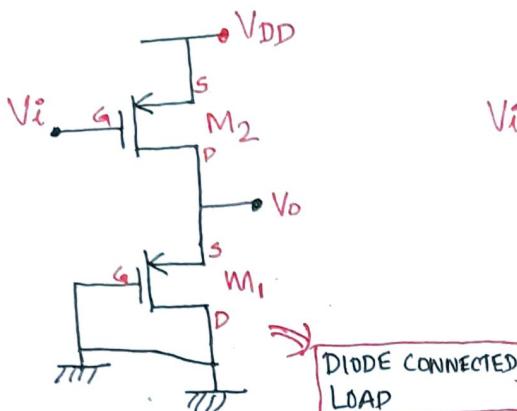


FIG-1

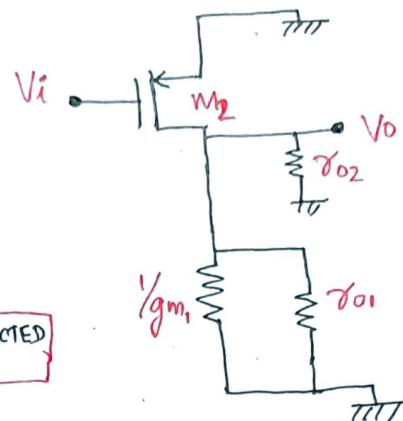


FIG-2

- Fig-1 shows CS stage with a diode connected load using P-mos, where input applied at MOSFET-2 and MOSFET-1 act as diode connected load.
- Fig-2 is the equivalent small signal circuit with diode connected load, where g_m is the transconductance and Ro_1 is the output resistance of diode connected load and Ro_2 is the O/p resistance of MOSFET-1 where input is applied.

Gain of the stage,

$$A_V = -g_{m2} \left(\frac{1}{g_{m1}} \parallel \text{Ro}_1 \parallel \text{Ro}_2 \right)$$

Output resistance,

$$\text{Ro} = \frac{1}{g_{m1}} \parallel \text{Ro}_1 \parallel \text{Ro}_2$$

g_{m1} - transconductance of diode connected load

g_{m2} - " MOSFET-2 where input is applied

Ro_1 - O/p resistance of diode connected load

Ro_2 - " MOSFET-2 where i/p is applied.