ECT 301

LINEAR INTEGRATED CIRCUITS

ASSIGNMENT

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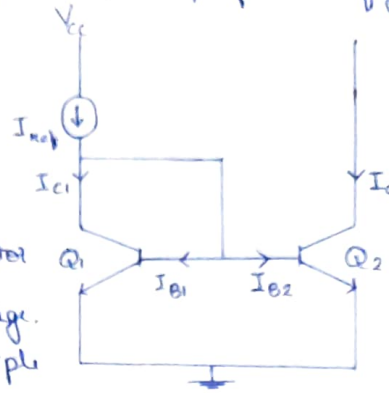
Class : S4 ECE-B

Q: a) Explain the concept of current mirror in differential amplifier configuration using BJT

Ans The current source used in differential amplifier is an integral part of the circuit. These circuits make use of the fact that when the transistor operates in the active region, collector current is relatively independent of collector voltage.

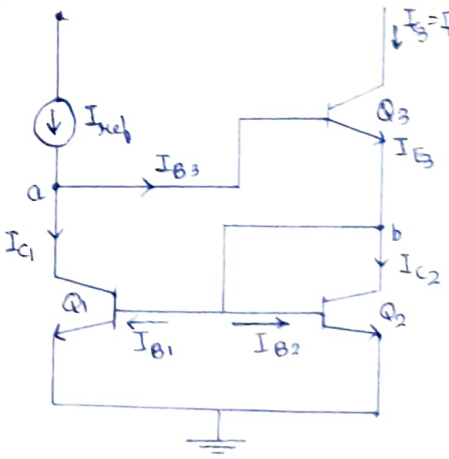


Most current sources work on the principle of current mirror. The circuit consists of two identical transistors Q_1 & Q_2, with their bases and emitters connected. Hence the two transistors have same V_{BE}, $V_{BE1} = V_{BE2}$. The collector of Q_1 is shorted to its base, so $V_{CB} = 0$. Hence it is a diode connected transistor.

When a current I_{C_1} is forced to pass through collector of Q_1, V_{BE} becomes high and since $V_{CB} = 0$, Q_1 operates in the active region. $\because$ $V_{BE1} = V_{BE2}$, Q_2 will also be in the active region, and $I_{C1} = I_{C2}$ Thus current flowing through left part of the circuit produces a mirror image of the current in the right side. The mirror effect is valid only for large β.

b) Explain Wilson and Widlar current mirrors.

The Wilson current mirror is designed to achieve much higher output resistance than the simple current mirror. Also the effect of β on output current is reduced.



At node b:

$$I_{E3} = I_{C2} + I_{B1} + I_{B2}$$

but $I_{B1} = I_{B2} = I_B$

$$\Rightarrow I_{E3} = I_{C2} + 2I_B$$

$$= I_{C_2} + 2\frac{I_{C_2}}{\beta}$$

$$\Rightarrow I_{E_3} = I_{C_2}\left(1 + \frac{2}{\beta}\right)$$

$$I_{C_3} = \alpha I_3 = \alpha \cdot I_{C_2}\left(1 + \frac{2}{\beta}\right) \quad \because \alpha = \frac{\beta}{1+\beta}$$

$$\Rightarrow I_{C_3} = I_{C_2}\left(1 + \frac{2}{\beta}\right)\left(\frac{\beta}{1+\beta}\right)$$

$$I_{C2} = I_{C3}\left[\frac{1}{\left(1+\frac{2}{\beta}\right)\left(\frac{\beta}{1+\beta}\right)}\right] = I_{C3}\left(\frac{\beta+1}{\beta+2}\right)$$

At node a: $I_{ref} = I_{C1} + I_{B3}$

$$I_{C1} = I_{ref} - I_{B3}$$
$$= I_{ref} - \frac{I_{C3}}{\beta}$$

$\because$ Q_1 & Q_2 form a current mirror, $I_{C1} = I_{C2}$.

Or equating:

$$I_{C3}\left[\frac{1}{\left(1+\frac{2}{\beta}\right)\left(\frac{\beta}{1+\beta}\right)}\right] = I_{ref} - \frac{I_{C3}}{\beta}$$

$$\Rightarrow I_{C3} = I_{ref}\left[1 - \frac{2}{\beta^2+2\beta+2}\right]$$

Hence the output current I_{C3} differs from I_{ref} by a factor. $2/\beta^2+2\beta+2$ i.e dependent.

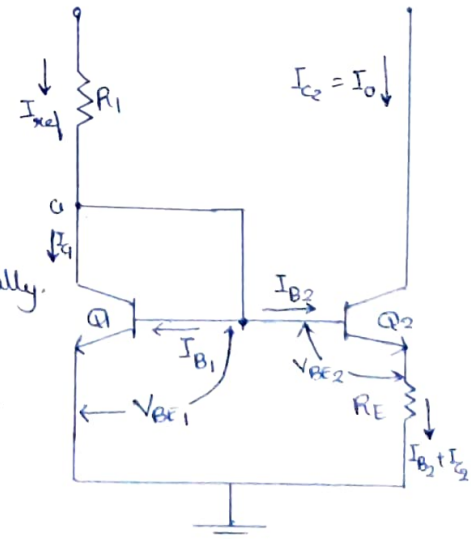
For wilson current mirror, output resistance will be:

$R_o = \frac{\beta}{2}\frac{V_A}{I_{C3}}$, i.e it is $\beta/2$ times larger than output resistance of simple current mirror circuit.

Widlar current mirror:

The basic current mirror has a limitation whenever we need a low value current source, the value of the resistance R1 required is sufficiently high and cannot be fabricated economically.

In widlar current mirror, the current differs from basic current mirror only in the resistance R_E, that is included in the emitter lead of Q_2.



It can be seen that due to R_E, the base emitter voltage V_{BE_2} is less than V_{BE_1}. $\therefore$ I_o is smaller than I_{C1}.

$$V_{BE_2} < V_{BE1} \qquad I_o < I_C$$

We know $I_{C1} = \alpha I_E e^{V_{BE1}/V_T}$

$$I_{C_2} = \alpha I_E e^{V_{BE_2}/V_T}$$

$$\therefore \frac{I_{C_1}}{I_{C_2}} = e^{(V_{BE_1} - V_{BE_2})/V_T}$$

Taking natural logarithm on both sides

$$V_{BE_1} - V_{BE_2} = V_T \ln\left(\frac{I_{C_1}}{I_{C_2}}\right) \quad \text{---} (1)$$

Applying KVL for emitter base loop

$$V_{BE_1} = V_{BE_2} + (I_{B_2} + I_{C_2}) R_E$$

$$\Rightarrow V_{BE_1} - V_{BE_2} = \left(\frac{1}{\beta} + 1\right) I_{C_2} R_E$$

$$(1) \Rightarrow \left(\frac{1}{\beta} + 1\right) I_{C_2} R_E = V_T \ln\left(\frac{I_{C_1}}{I_{C_2}}\right)$$

$$\Rightarrow R_E = \frac{V_T}{\left(\frac{1}{\beta} + 1\right) I_{C_2}} \ln\left(\frac{I_{C_1}}{I_{C_2}}\right)$$

Applying KCL at collector point of Q_1 (node a)

$$I_{ref} = I_{C_1} + I_{B_1} + I_{B_2} = I_{C_1} + \frac{I_{C_1}}{\beta} + \frac{I_{C_2}}{\beta}$$

$$= I_{C_1}\left(1 + \frac{1}{\beta}\right) + \frac{I_{C_2}}{\beta}$$

In case of wilder current source, $I_{C_2} << I_{C_1}$ Hence I_{C_2}/β can be neglected.

$$\therefore I_{ref} \cong I_{C_1}\left(1 + \frac{1}{\beta}\right)$$

$$I_{C_1} = \frac{\beta}{1+\beta} \cdot I_{ref} \quad \text{where } I_{ref} = \frac{V_{CC} - V_{BE}}{R_1}$$

For $\beta >> 1$, $I_{C_1} \cong I_{ref}$.

c) What are the advantages and limitations of Wilson and Wilder current mirrors?

ans Wilson current mirror:

Advantages: Wilson current mirror is less dependent of β, hence it is less dependent on transistor parameters.

It provides a high o/p impedance which improves the efficiency of current mirror.

Limitations : It has higher compliance voltage compared to basic mirror circuit.
It creates noise across output.

Wilder current mirror :

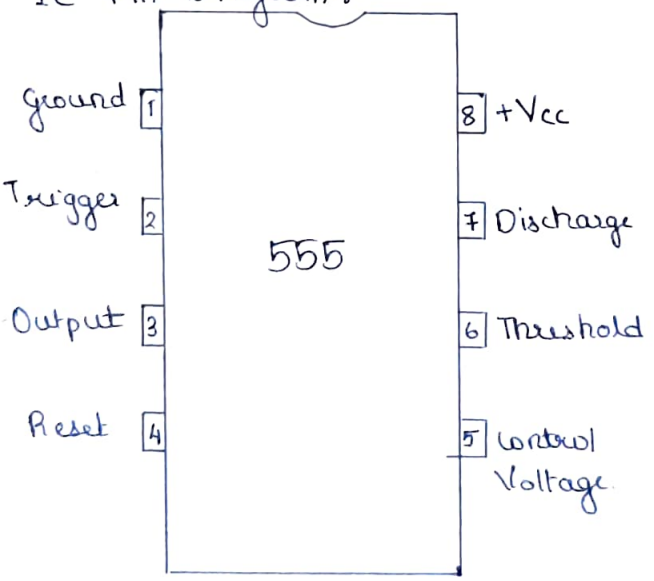
Advantages : It incorporates an emitter degeneration resistor for only the o/p transistor, enabling the current source to generate low current using only moderate resistor values.

Limitations :- It is much less accurate

2) What is 555 timer IC? Explain with pin diagram and functional diagram.

Ans The 555 timer IC is an integrated circuit used in a variety of timer, delay, pulse generation and oscillator generations. Derivatives provide two (556) or four (558) timing circuit in one package. The design was first used bipolar junction transistors.

555 timer IC Pin Diagram :



1) Ground : Ground reference voltage, low level (0V)
2) Trigger : The OUT pin goes high and a timming interval starts when this input falls below 1/2 of CTRL voltage (which is typically 1/3 Vcc). Out is high as long as the trigger is low.

3) OUT : The output is driven to approximately 1.7V below $+V_{cc}$ or to GND

4) RESET : A timing interval may be reset by driving this input to GND but the timing does not begin again until RESET rises above approx 0.7 V. Overrides TRIG which overrides threshold.

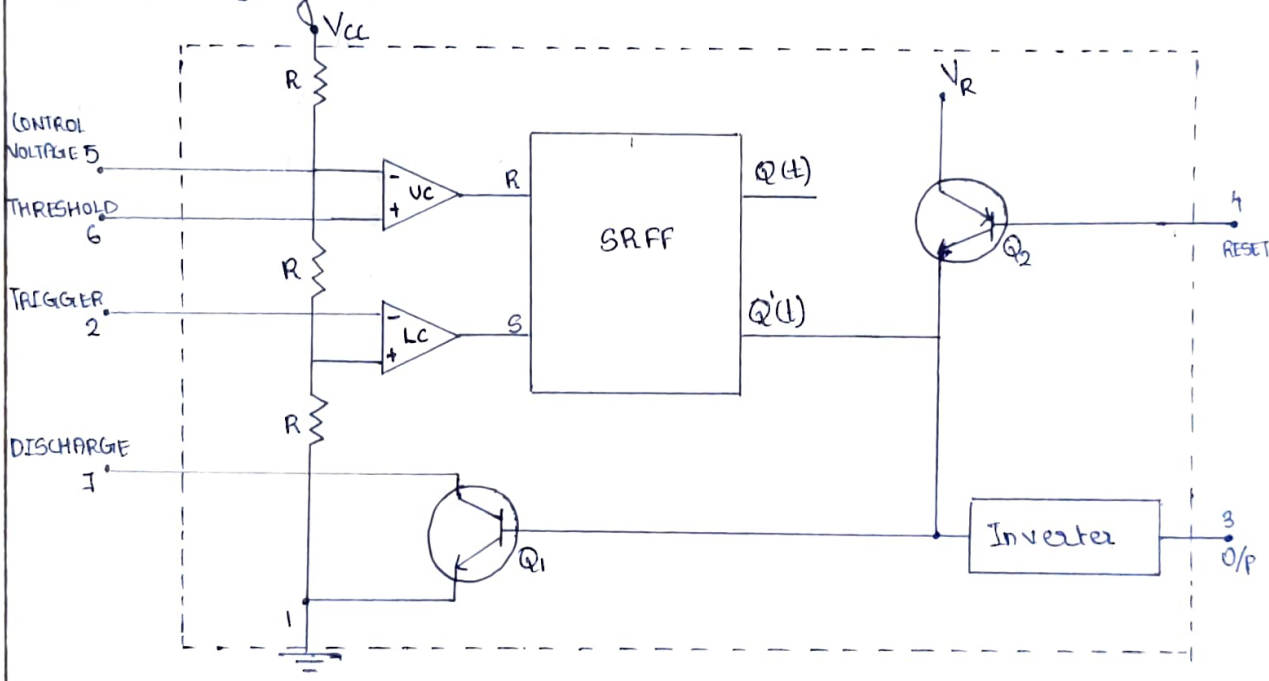
5) CTRL : Provides "control" access to the internal voltage divider (by default 2/3 V_{cc}).

6) THR : The timing (OUT high) interval ends when the voltage at the threshold is greater than that at CTRL (2/3 V_{cc} if CTRL is open)

7) DIS : Open collector output which may discharge a capacitor between intervals. In phase with output.

8) V_{cc} : Positive supply voltage, which is usually between 3 & 15 V depending on the variation.

Functional Diagram :



It consists of a voltage divider network, two comparator, one SR flip-flop, two transistors and an inverter.

1) Voltage divider network : It consists of three resistors (5kΩ) that are connected in series between supply voltage and ground.

2) Comparator : 555 IC has two comparators ; an Upper comparator (UC) and a lower comparator (LC). It compares the two inputs that are applied to it and produces an output.

3) SR Flip-flop : The SR flip flop operates with either positive clock transitions or negative clock transitions.

The outputs Q(t) and Q(t)' are complement to each other.

State table of SR FF:

S	R	Q(t+1)
0	0	Q(t)
0	1	0
1	0	1
1	1	-

Transistors and Inverter: The FD of 555 timer IC consists of one npn transistor and one pnp transistor. The npn transistor will be turned ON if its V_{BE} is positive and greater than cut in voltage.

- The pnp transistor is used as buffer inorder to isolate the reset input from SR flipflop & npn transistor.
- The inverter used in functional diagram of 555 timer IC not only performs the inverting action but also amplifies the power level.