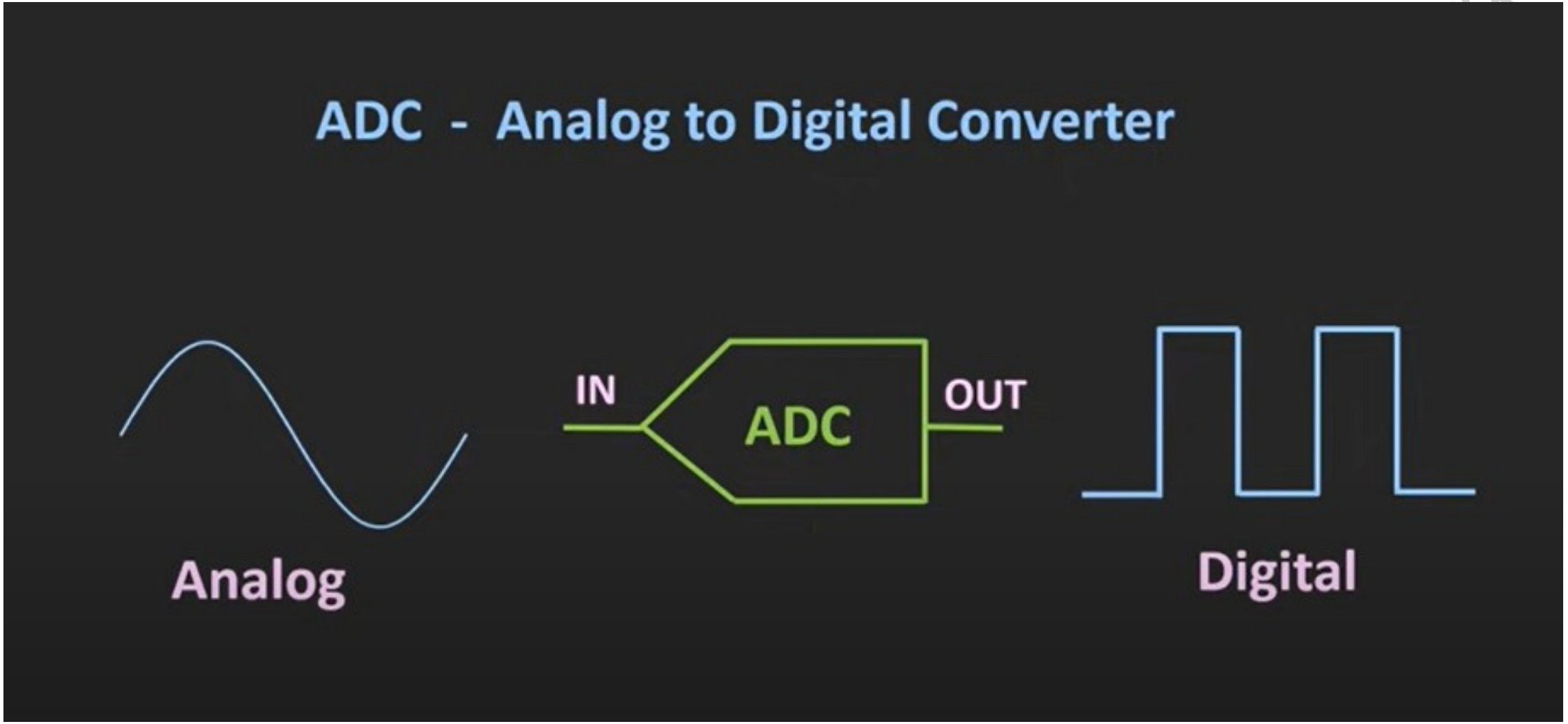
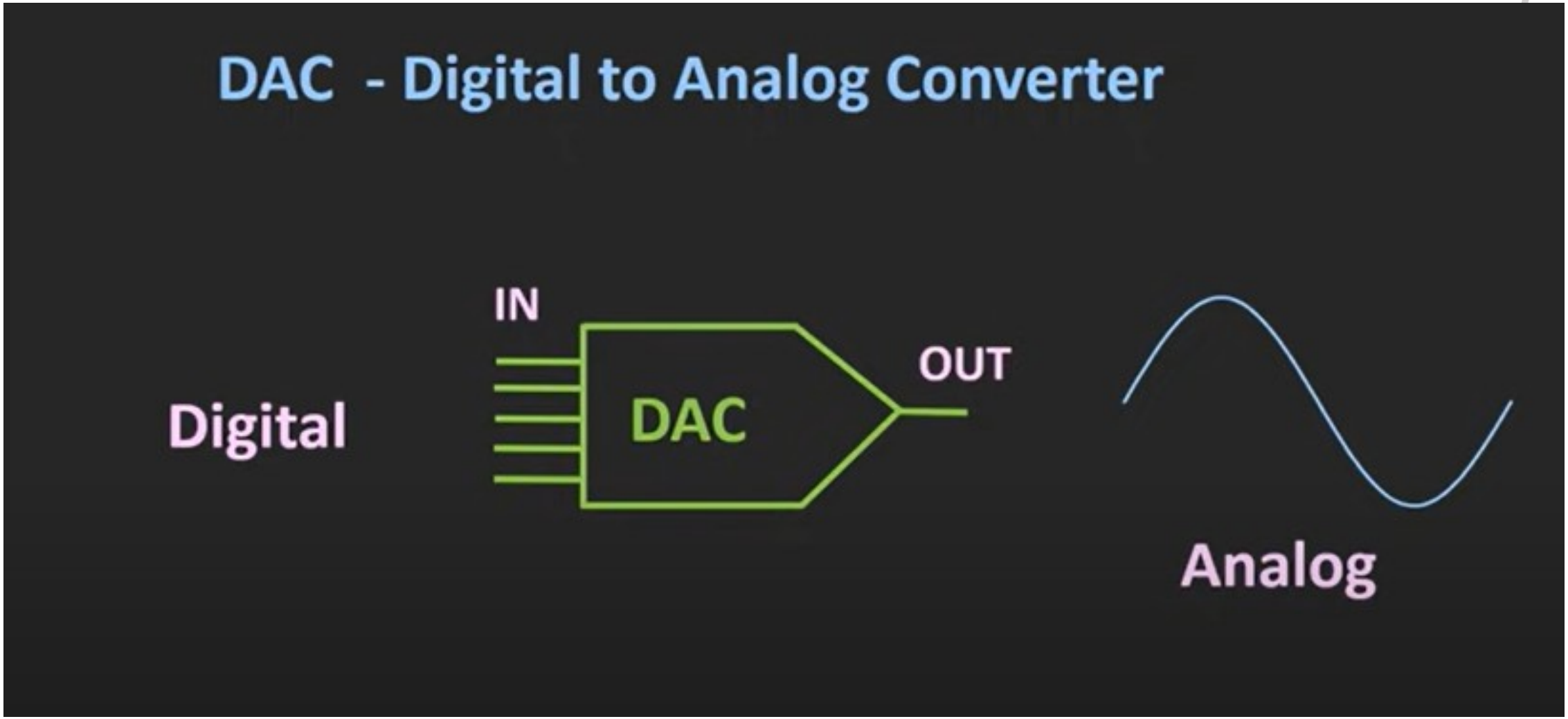
DATA CONVERTERS


ADC - Analog to Digital Converter
IN
ADC
OUT
Analog
Digital

DAC - Digital to Analog Converter



Why we use ADC and DAC ?

Susceptible to Noise

Analog Signal → Difficult to Process in Analog Domain

Difficult to Store in Analog Domain

Less Susceptible to Noise

Digital Signal → Easy to Process in Digital Domain

Easy to Store in Digtial Domain

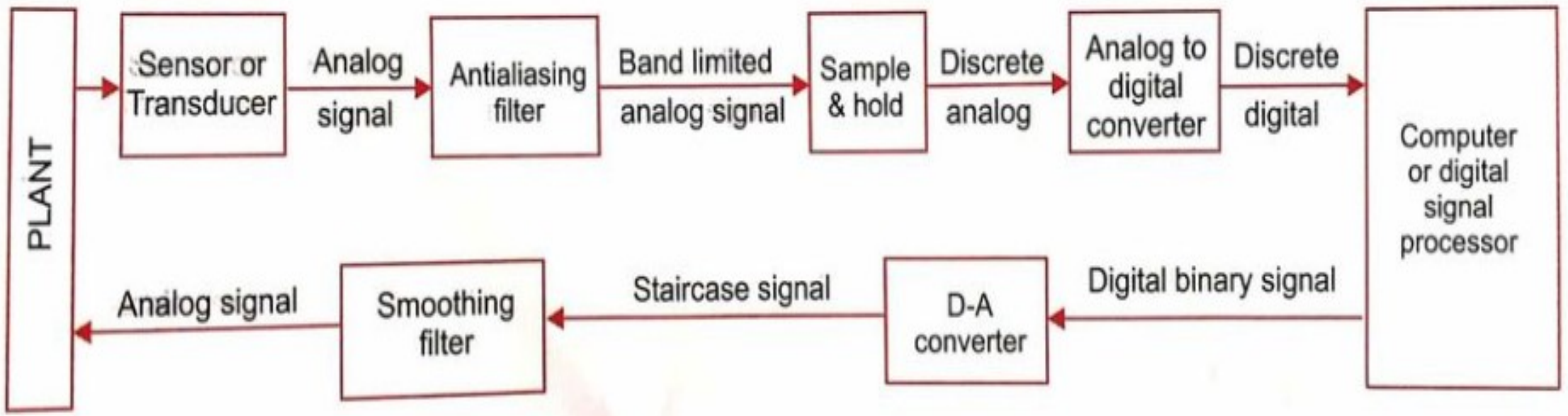


Fig. 10.1 Circuit showing application of A/D and D/A converter

DAC

BASIC DAC TECHNIQUES

- i/p is a n-bit binary word D
- It is combined with a ref voltage V_R to give an analog o/p s/g.
- o/p of DAC can be either V or I.

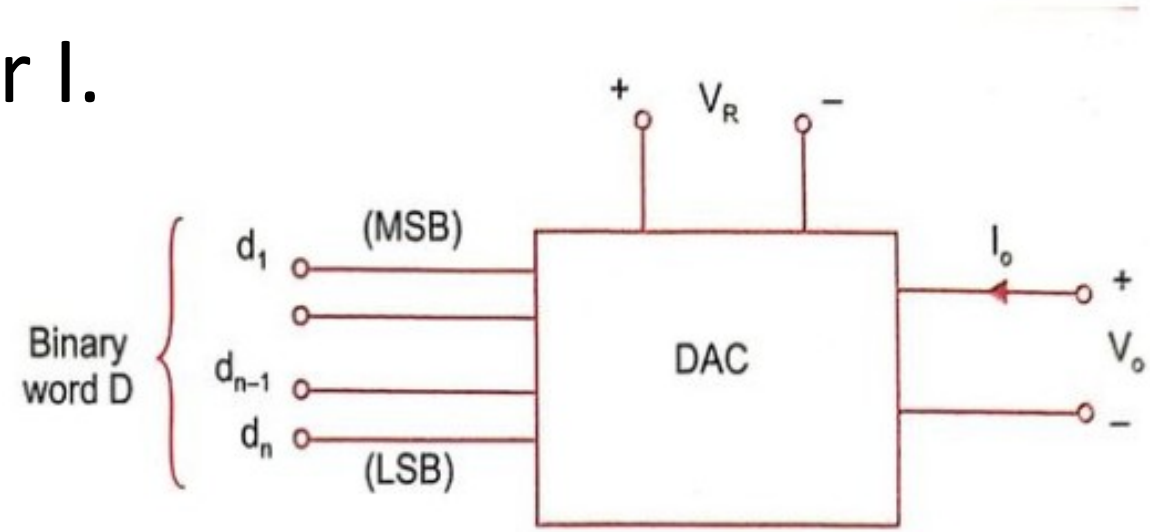


Fig. 10.2 Schematic of a DAC

- For a voltage o/p DAC, DAC is mathematically described as

$$V_0 = KV_{FS}\,(d_1 2^{-1} + d_2 2^{-2} + \ldots + d_n 2^{-n}) \qquad \text{------(1)}$$

Where V_0 =o/p V

V_{FS} = full scale o/p V (max V a DAC can produce when all i/ps are '1').

K = scaling factor (usually adjusted to 1)

$d_1, d_2, \ldots, d_n$ = n bit binary fractional word with decimal pt located at left

- d_1= most significant bit (MSB) with a weight of $V_{FS} / 2$.
- d_n= least significant bit (LSB) with a weight of $V_{FS} / 2^n$.

DAC Specifications

1.Resolution :

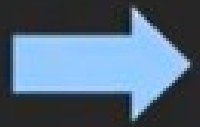
- Resolution of a converter is the smallest change in voltage which may be produced at the o/p (or i/p) of converter.
- Simply, resolution is the value of LSB.
- Resolution (in volts) = = 1 LSB increment

- It is defined as the number of different analog output voltage levels that can be provided by a DAC.
- Or alternatively resolution is defined as the ratio of a change in output voltage resulting for a change of 1 LSB at the digital input.

Resolution : No. of Bits (n)

3 bit DAC

V_{ref} - 5 V



$$\text{Resolution} = \frac{V_{ref}}{2^n}$$

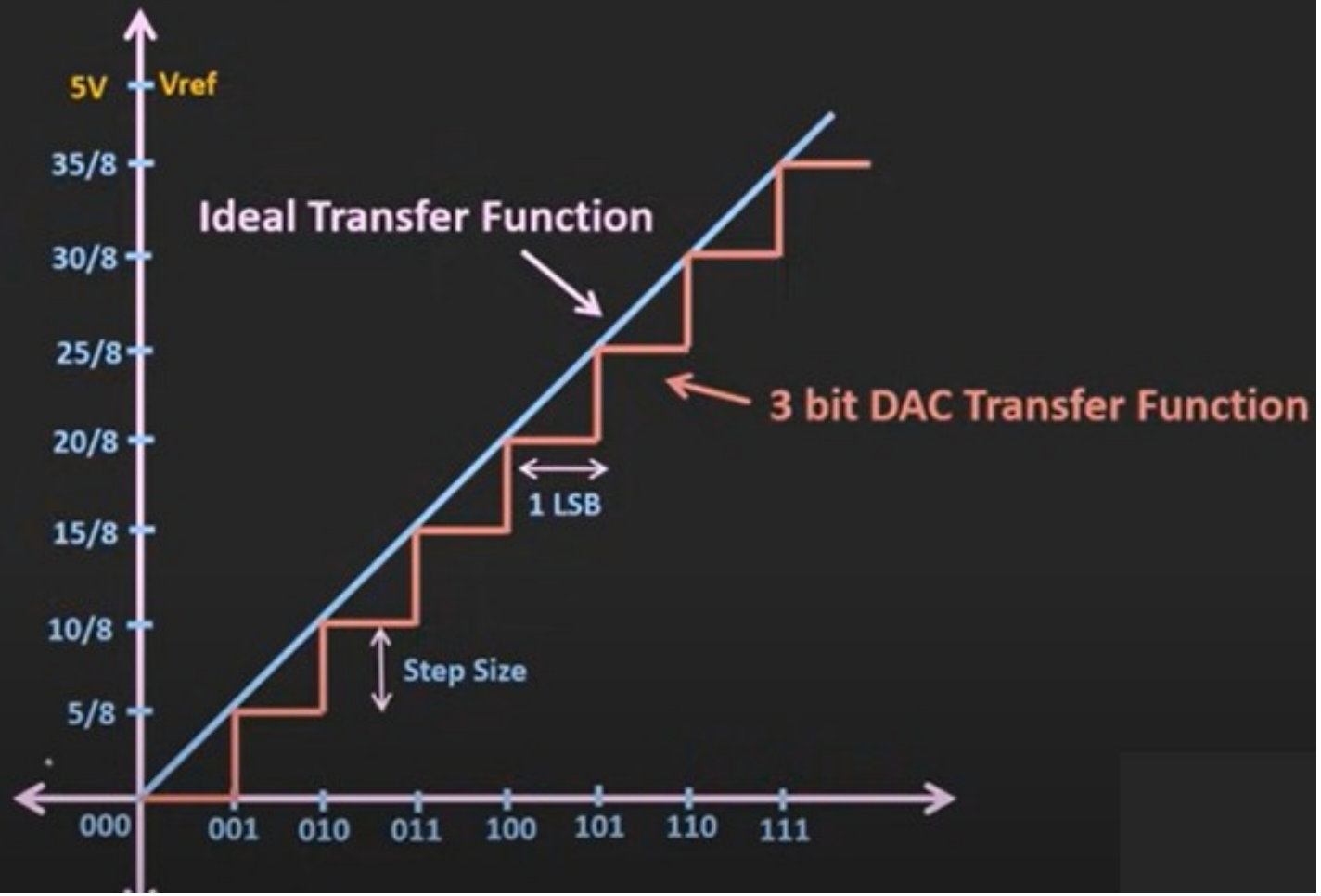
Digital to Analog converter

3 bit DAC

V_{ref} - 5 V

Resolution = 0.625V

LSB = 0.625 V



Digital to Analog converter

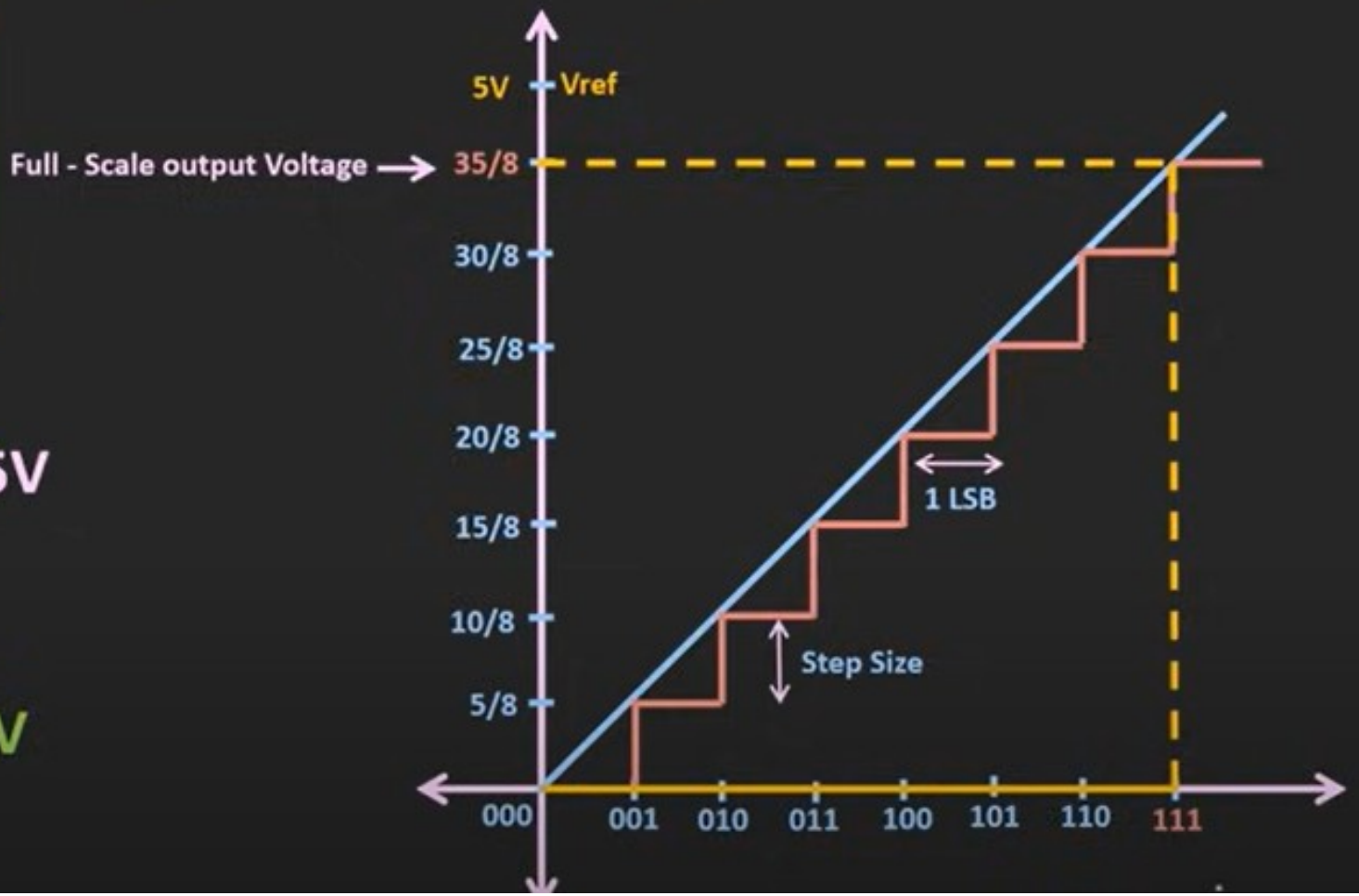
3 bit DAC

V_{ref} - 5 V

Resolution = 0.625V

LSB = 0.625 V

Step size = 0.625V



$$V_{FS} = \frac{(2^{n} - 1) \times V_{ref}}{2^{n}}$$

$$\text{Resolution} = \text{LSB} = \text{Step Size} = \frac{V_{ref}}{2^{n}} = \frac{V_{FS}}{(2^{n} - 1)}$$

$$V_{FS} = V_{ref} - 1\ \text{LSB}$$

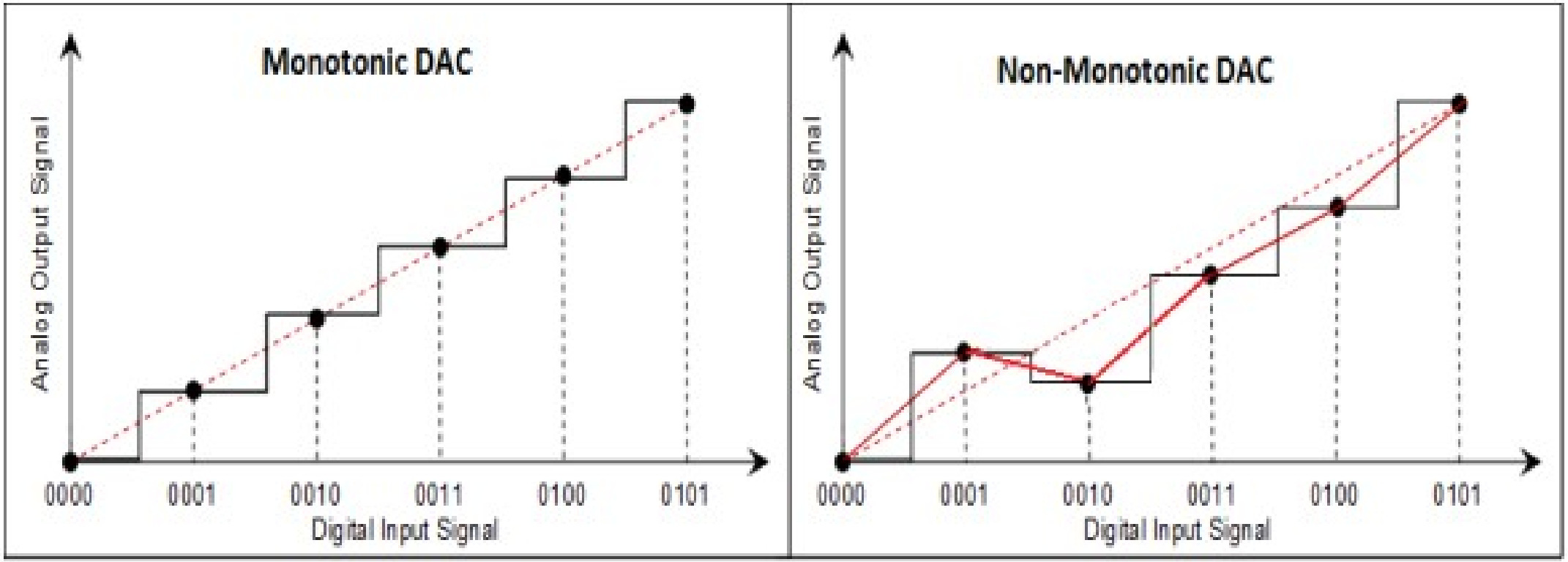
2. Accuracy

- Absolute accuracy is the maximum deviation between the actual converter output and the ideal converter output.
- The ideal converter is the one which does not suffer from any problem.
- Whereas, the actual converter output deviates due to the drift in component values, mismatches, aging, noise and other sources of errors.

- Normally, the data sheet of a D/A converter specifies the relative accuracy rather than absolute accuracy.
- The relative accuracy is the maximum deviation after the gain and offset errors have been removed.

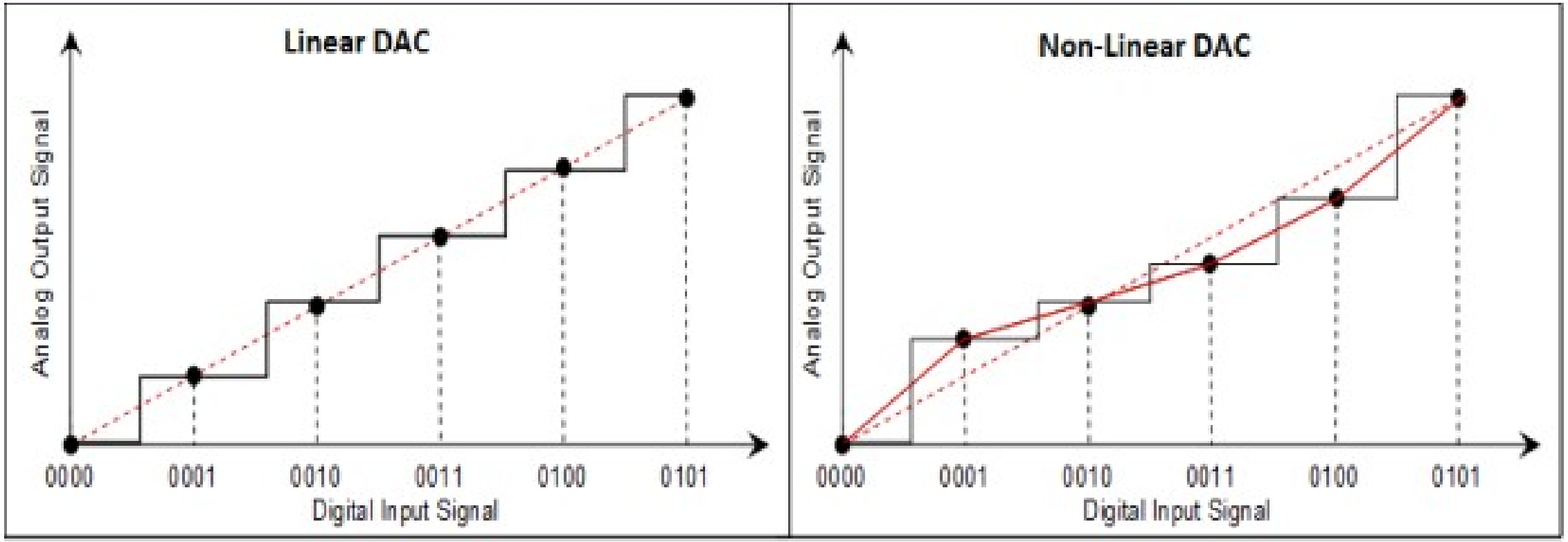
3. Monotonicity

- A Digital to Analog converter is said to be monotonic if the analog output increases for an increase in the digital input.
- ie staircase o/p shud haver no downward step as binary i/p is incremented.


Monotonic DAC
Analog Output Signal
0000
0001
0010
0011
0100
0101
Digital Input Signal
Non-Monotonic DAC
Analog Output Signal
0000
0001
0010
0011
0100
0101
Digital Input Signal

4. Linearity

- The difference between the desired analog output and the actual output over the full range of expected values.
- The linearity of a DAC is also defined as the precision or exactness with which the digital input is converted into analog output.
- An ideal DAC produces equal increments or step sizes at output for every change in equal increments of binary input.


Linear DAC
Analog Output Signal
0000
0001
0010
0011
0100
0101
Digital Input Signal
Non-Linear DAC
Analog Output Signal
0000
0001
0010
0011
0100
0101
Digital Input Signal

5. Settling time

- Time required for the output signal to settle within +/- (1/2) LSB of its final value after a given change in input scale.
- The settling time is limited by slew rate of output amplifier.
- Ideally, an instantaneous change in analog voltage would occur when a new binary word enters into the DAC.

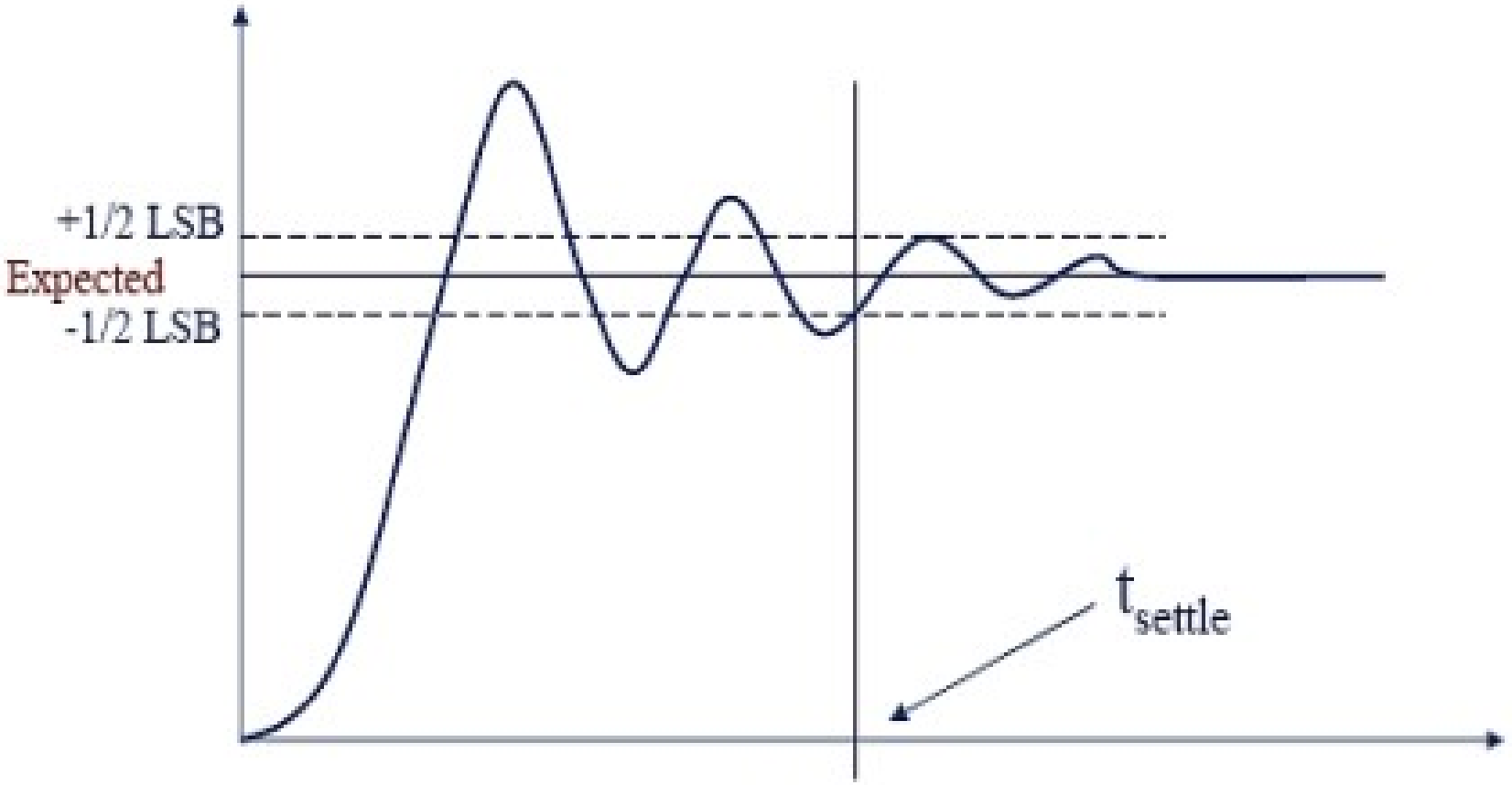


Figure 2-9 Settling Time

6. Conversion Time

- It is the time taken for the D/A converter to produce the analog output for the given binary input signal.
- It depends on the response time of switches and the output of the Amplifier.
- D/A converters speed can be defined by this parameter.
- It is also called as setting time.

7. Stability/ Temperature sensitivity

- The ability of a DAC to produce a stable output all the time is called as Stability.
- The performance of a converter changes with drift in temperature, aging and power supply variations.
- So all the parameters such as offset, gain, linearity error & monotonicity may change from the values specified in the datasheet.
- Temperature sensitivity defines the stability of a D/A converter.

8. Speed

- Rate of conversion of a single digital input to its analog equivalent.
- Conversion rate depends on clock speed of input signal and settling time of converter.
- When the input changes rapidly, the DAC conversion speed must be high.

9.Dynamic range:

- This is a measurement of the difference between the largest and smallest signals the DAC can reproduce.
- This is usually related to DAC resolution and noise floor.

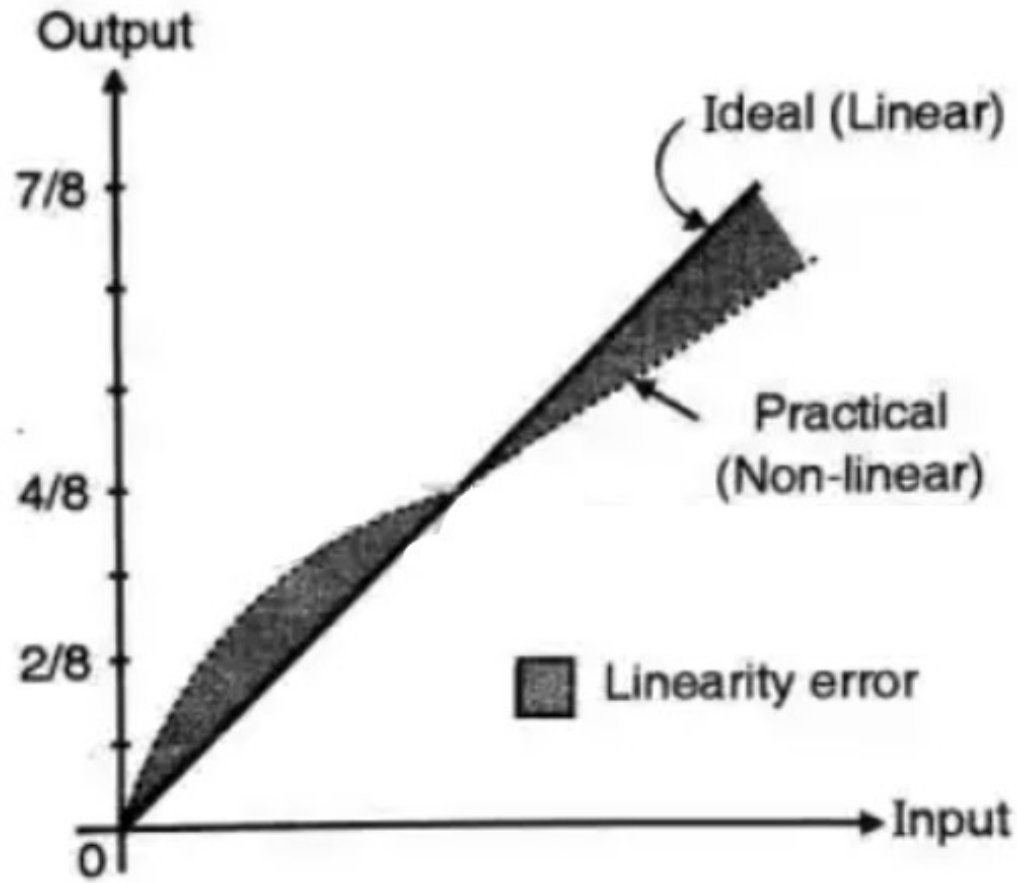
Sources of errors in DAC

1. Quantization error

- The full scale range of analog i/p V is quantized for conversion to a finite no.of steps.
- The error introduced in this process of quantization.
- Generally, quantization error is specified as ½ LSB.

2.Linearity Error:

- This is defined as the amount by which the actual output of a DAC differs from the ideal straight-line transfer characteristics.
- This error is introduced due to the error in the current source resistance values.



Linearity error in transfer characteristics of D/A converter

3. Offset Error:

- When all the digital inputs are 0, the analog output also is expected to be 0. But practically it does not happen.
- As shown in the figure, some non-zero analog output voltage is present even for a zero digital input. This is called an offset error.
- Thus the offset error is defined as the non-zero level analog output when all the digital inputs are 0. The offset error is due to the offset voltages of Op-Amps and leakage currents in the switches.

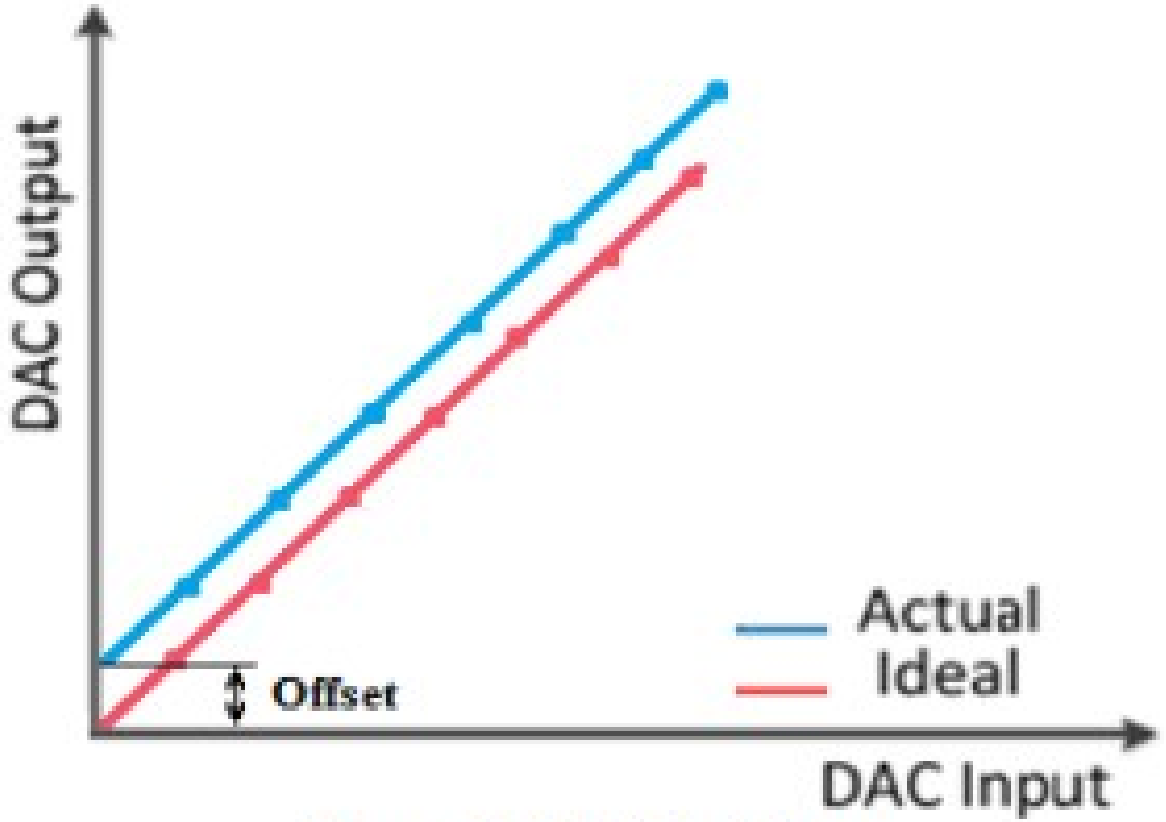


Figure 2-10 Offset Error

4.Gain Error:

- In a DAC we use a current-to-voltage converter. The gain of this converter determines the analog output voltage of the DAC.
- The gain error is defined as the difference between the calculated gain and the practically obtained gain of the I to V converter.
- This error exists due to the error in the feedback resistor value.

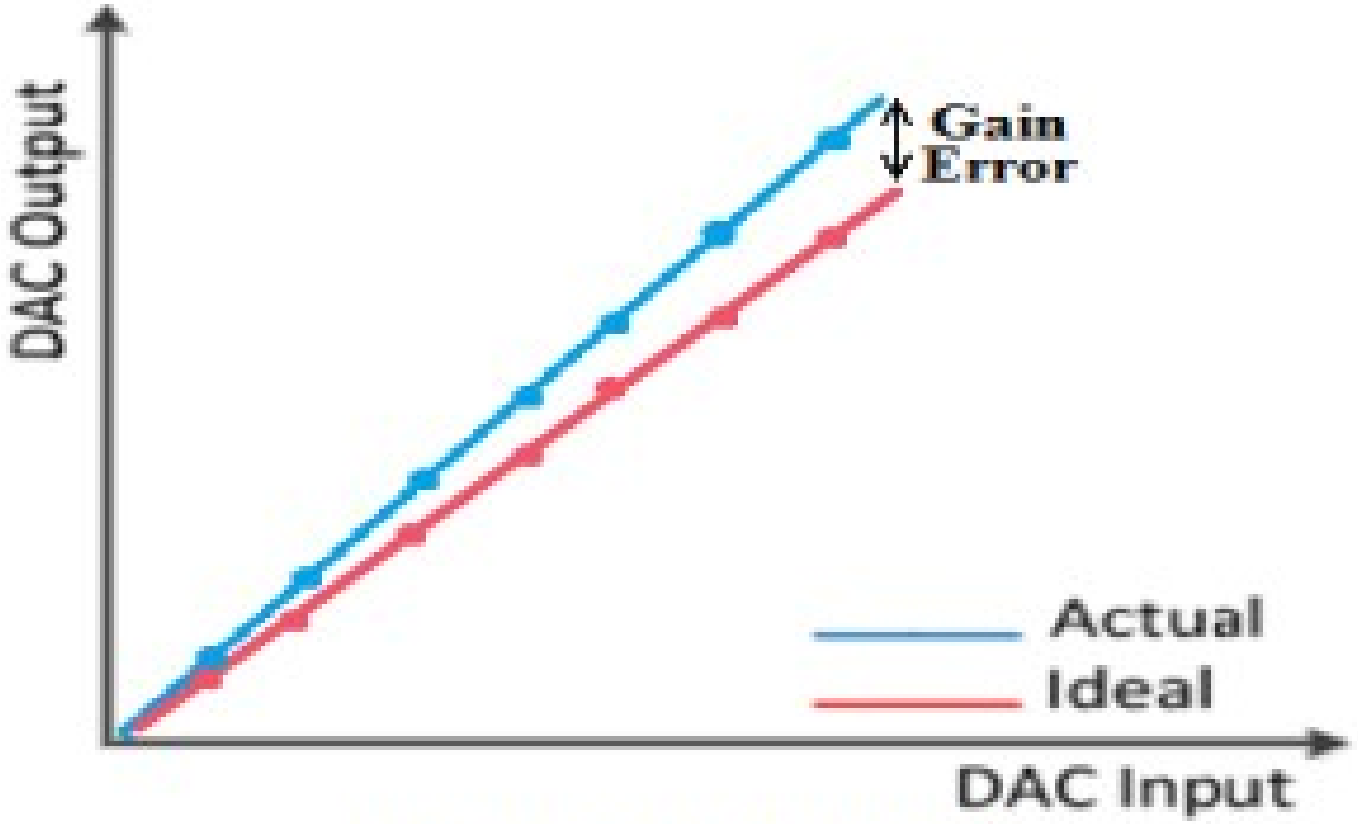
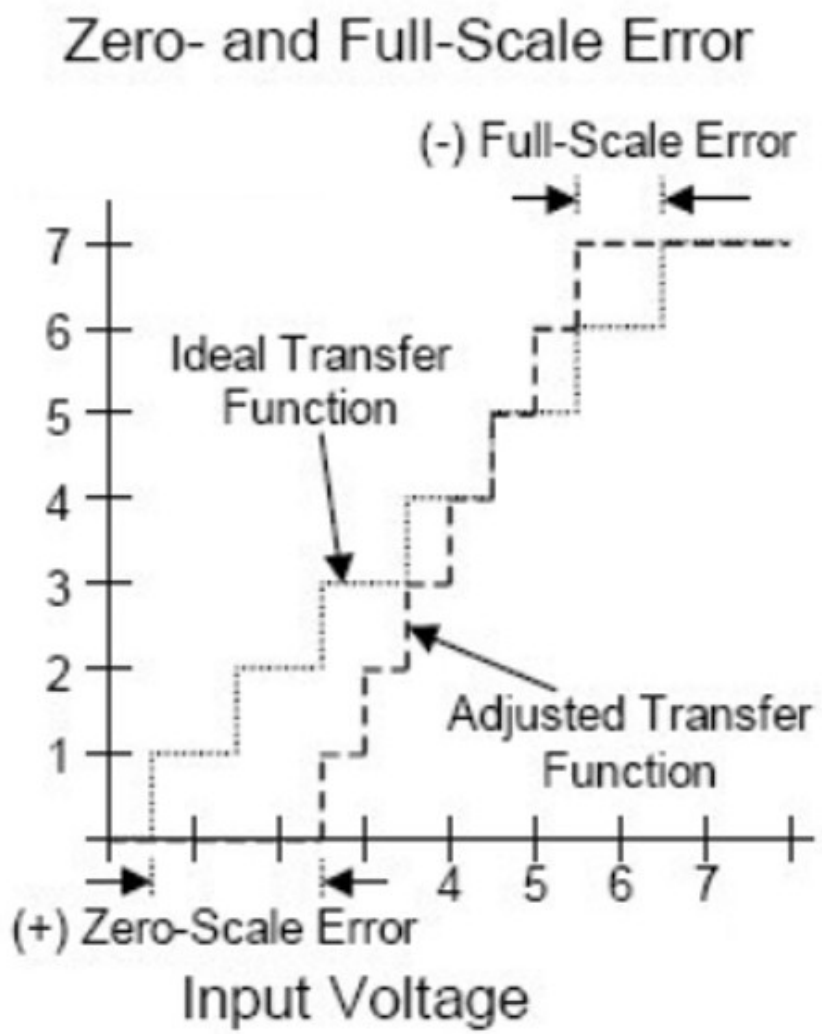


Figure 2-11 Gain Error

5. Full scale error

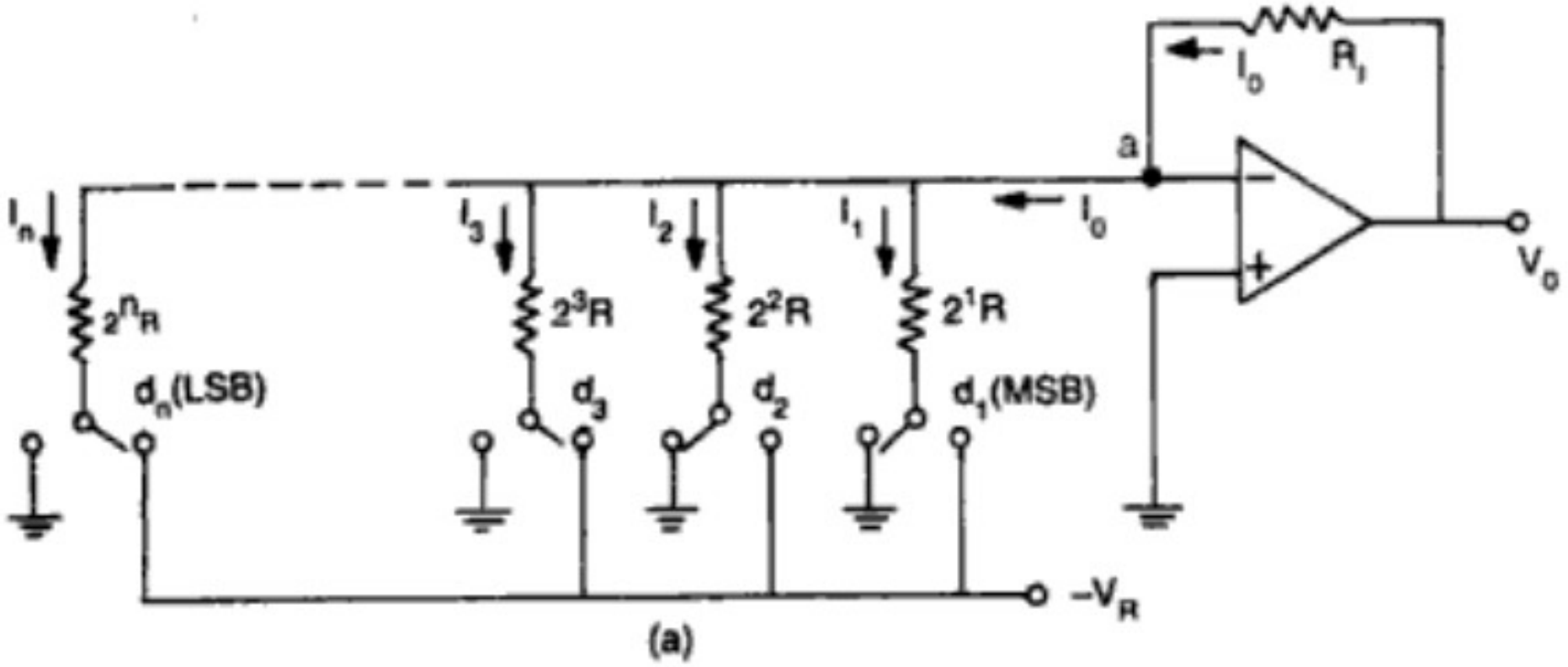
Diff btw actual last transition V and ideal last transition Voltage.



- There are various ways to implement eqn(1). But here we are using following resistive techniques

1. **Weighted resistor DAC**
2. **R-2R ladder**

1. Weighted resistor DAC



(a)

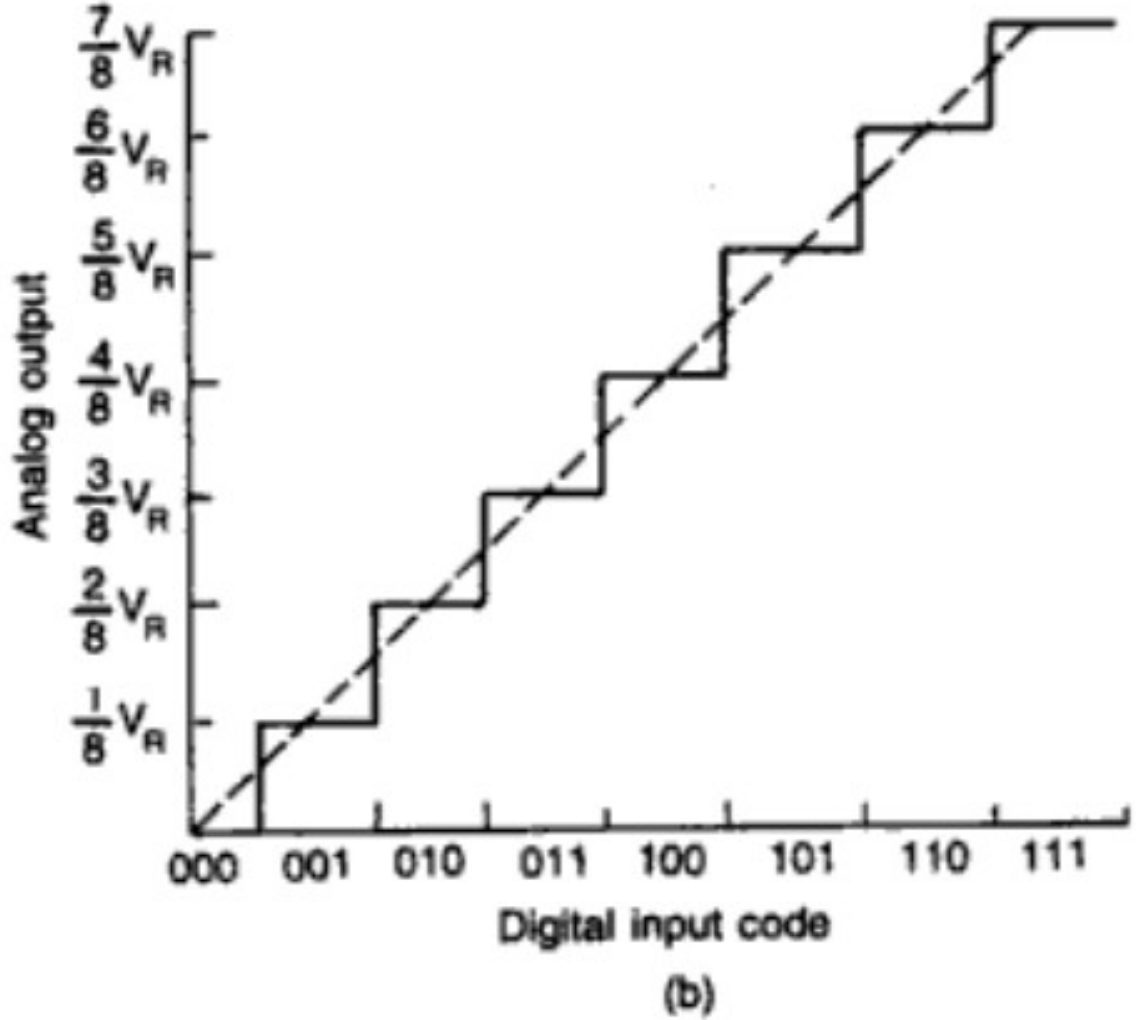


Fig. 10.3 (a) A simple weighted resistor DAC (b) Transfer characteristics of a 3-bit DAC

- type of DAC that converts a digital input signal into an equivalent analog output signal by using a network of binary weighted resistors.
- Inverting summing ampr is used
- $-V_R$ is connected as i/p thru a switch
- Switches are controlled by n bit digital i/p
- ‘n’ no. of switches are used.
- MSB d_1
- LSB d_n

- When n=1, corresponding switch will be connected to ref voltage
- When n=0, it will be connected to grnd.

Expression for o/p current & voltage.

$$I_0 = I_1 + I_2 + \ldots + I_n$$

$$= \frac{V_R}{2R} d_1 + \frac{V_R}{2^2 R} d_2 + \ldots + \frac{V_R}{2^n R} d_n$$

$$= \frac{V_R}{R} (d_1 2^{-1} + d_2 2^{-2} + \ldots + d_n 2^{-n})$$

- Output Voltage

$V_0 = I_0 R_f$

$\mathbf{V_0 = V_R\ (d_1 2^{-1} + d_2 2^{-2} + \ldots + d_n 2^{-n})}$ **----------(2)**

Comparing (1) &(2)

If R_f =R, then K=1 and V_{FS} =V_R

- Ckt uses a –ve ref V . Hence analog o/p V is therefore +ve staircase.
- Polarity of ref V is chosen in accordance with the type of switch used.
- Eg: for TTL compatible switches, ref V shud be +5V and o/p will be –ve.
- Accuracy and stability of DAC depends on accuracy of resistors and the tracking of each other with the temperature.

Disadvantages of binary weighted DAC

- Wide range of resistor values are required.

The accuracy and stability of this type DAC depends on the accuracy of the resistors used.

For better resolution, i/p binary length has to be increased which inturn increases range of resistance values.

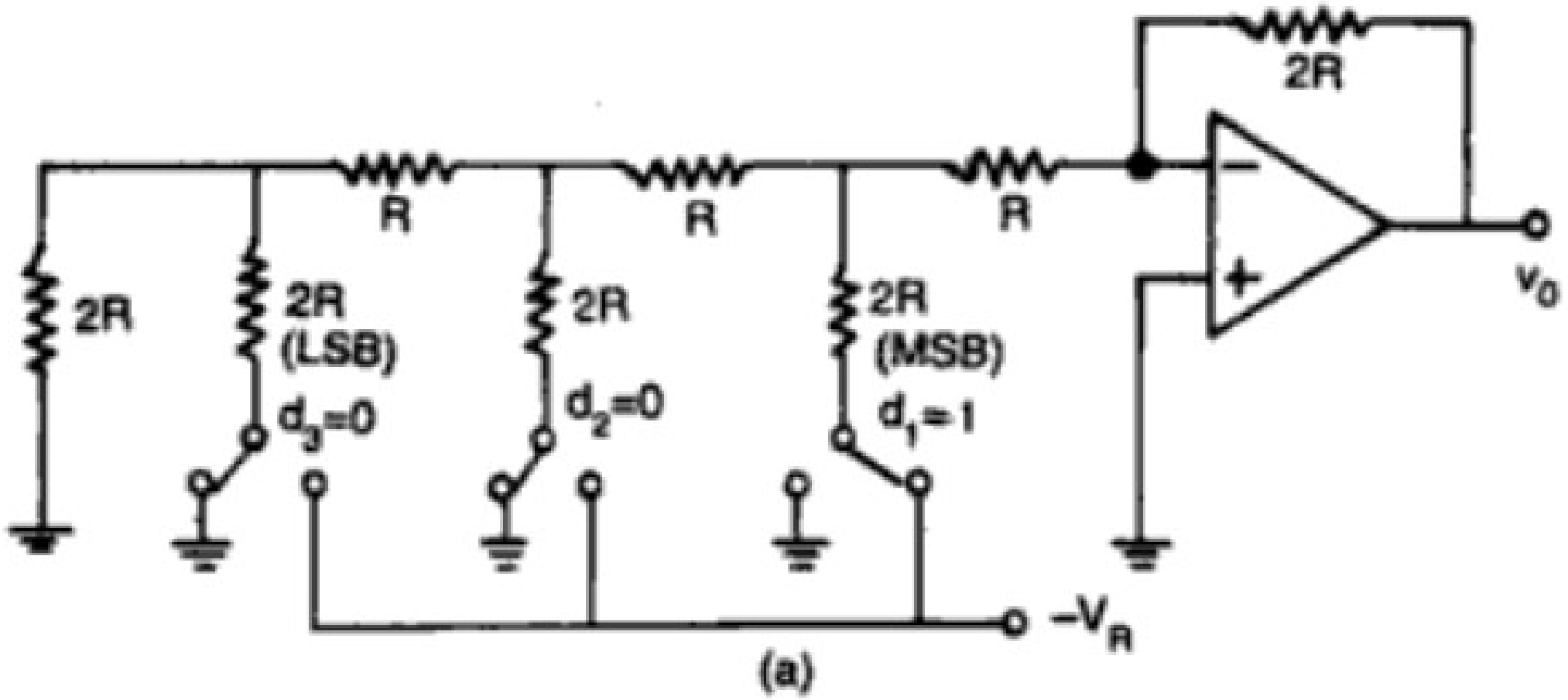
- Value of largest res depends on ‘n’ and value of smallest res cannot be < 2.5 Kohm to avoid loading effect.

- Can be expensive. So usually limited to 8 bit resolution.
- Switches are in series with resistors. So their ON res must be vey low and they shud have 0 offset Voltage.
- At higher resolutions, binary weighted resistor DACs consume high power.

2. R-2R ladder type DAC

- Here only 2 values of res are required. R & 2R
- Typical values of R ranges from 2.5 Kohm to 10 Kohm.
- Consider a 3 bit R-2R ladder type DAC where switch position d_1, d_2 , d_3 corresponds to the binary word 100.

3 bit R-2R ladder type DAC



(a)

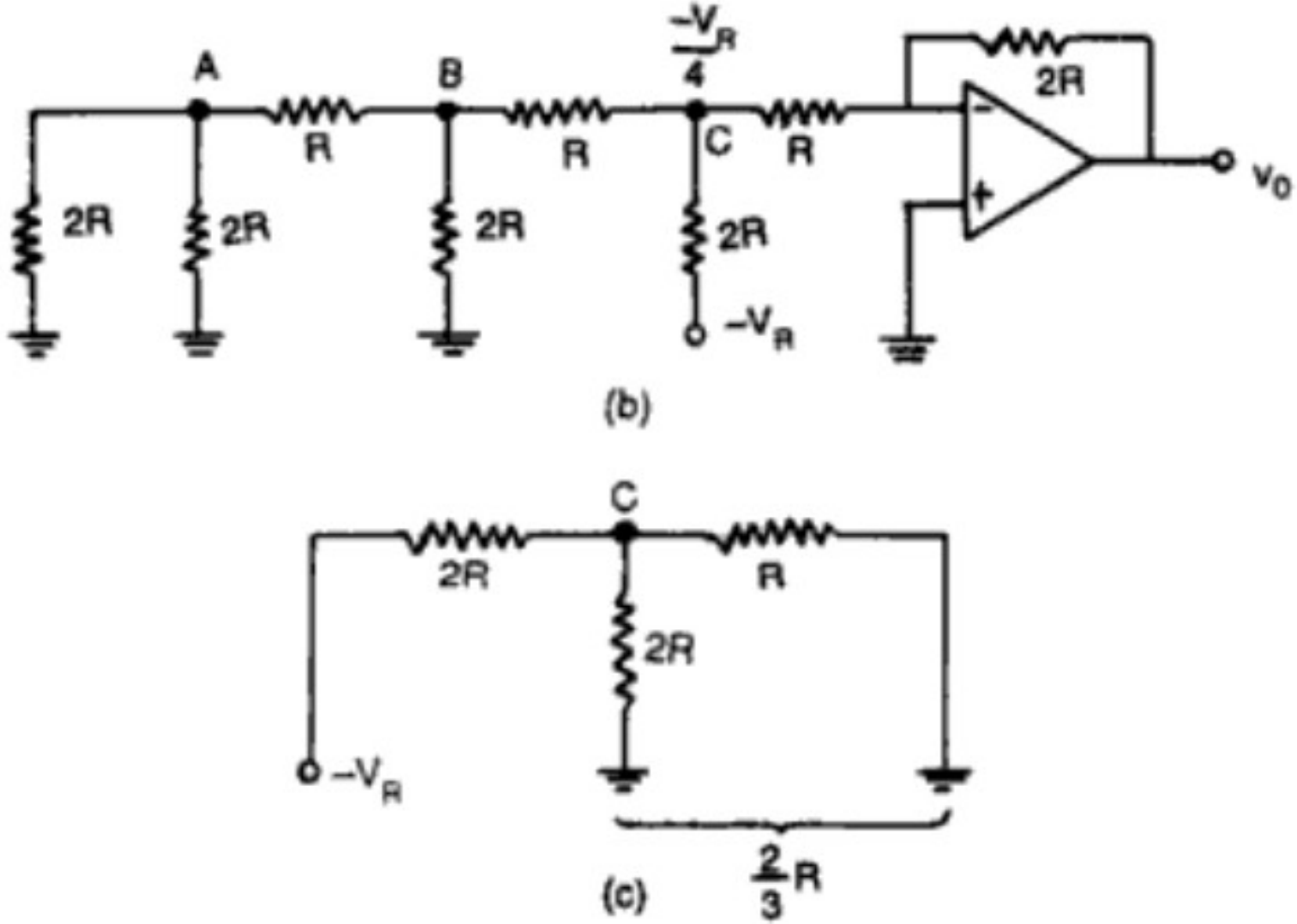


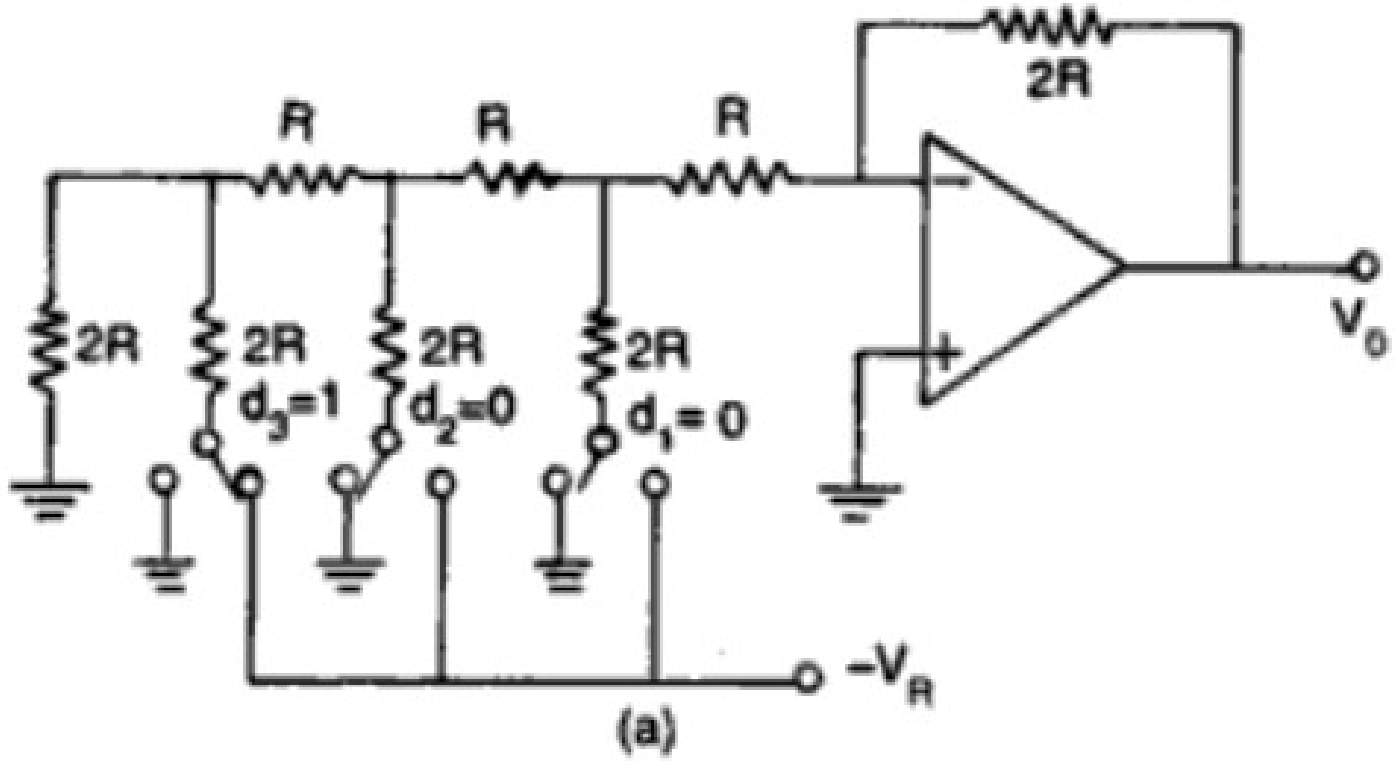
Fig. 10.5 (a) R-2R ladder DAC (b) Equivalent circuit of (a), (c) Equivalent circuit of (b)

- V at node C

Output voltage

V_0 =

- Consider a 3 bit R-2R ladder type DAC where switch position d_1, d_2 , d_3 corresponds to the binary word 001.



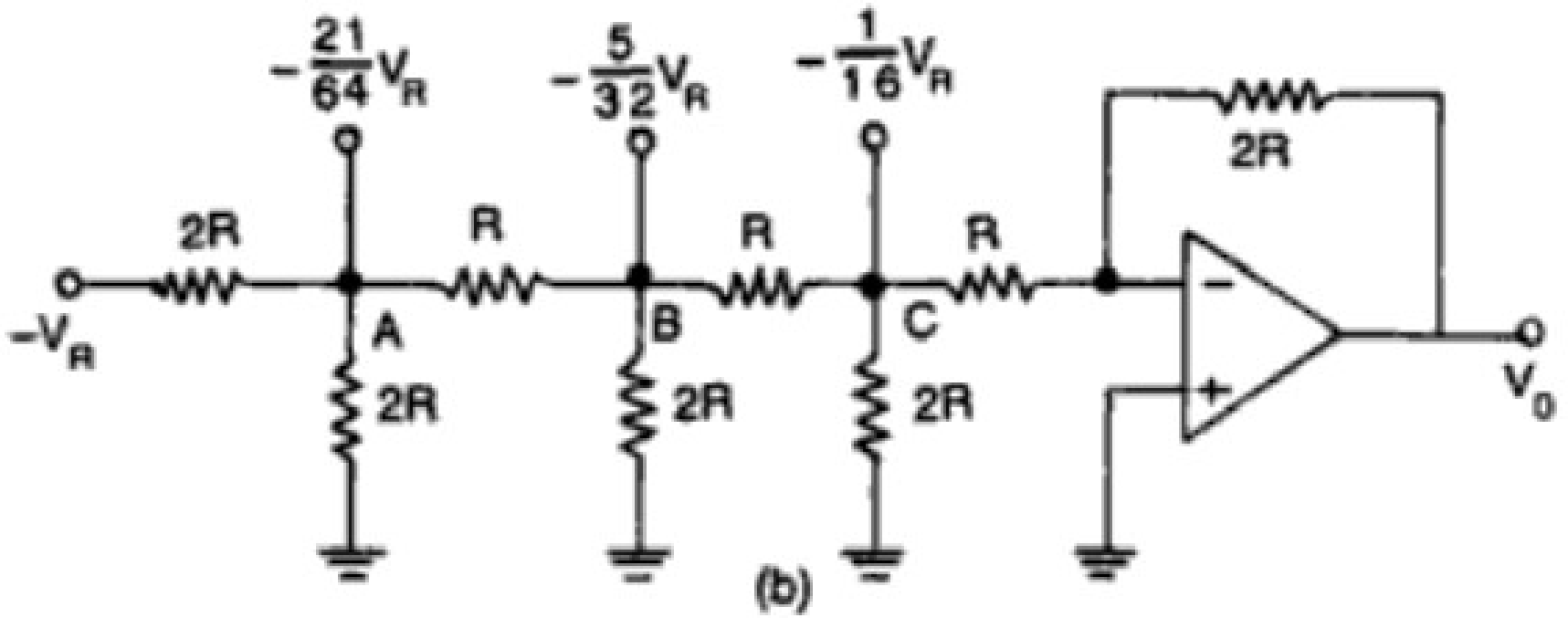


Fig. 10.6 (a) R-2R ladder DAC for switch positions 001 (b) Equivalent circuit

- V at node C

V_c

Output voltage

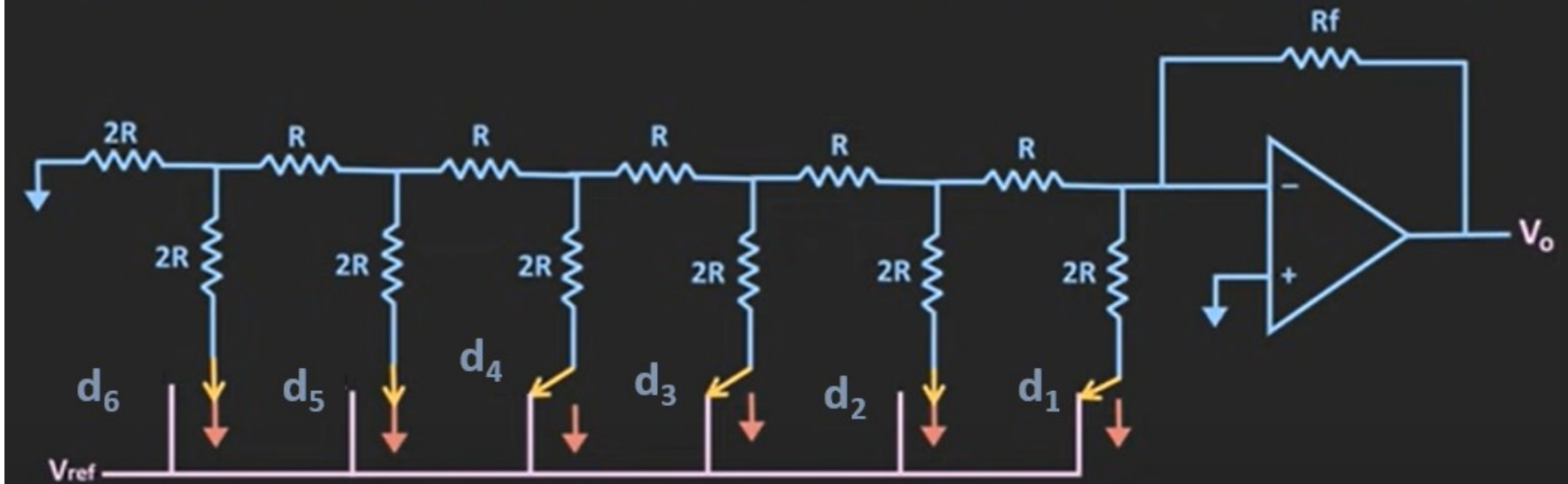
V_0 =

R-2R ladder DAC

d_1	d_2	d_3	
1	0	0	$\frac{V_R}{2}$
0	1	0	$\frac{V_R}{4}$
0	0	1	$\frac{V_R}{8}$
1	1	1	$\frac{V_R}{8} + \frac{V_R}{4} + \frac{V_R}{2} = \frac{7\,V_R}{8}$

Example

For the given DAC find the full scale output voltage if Rf = 2 kΩ and R = 1 kΩ. Also find the output voltage when the input is 101100. Assume Vref = 5V



- FSO $=V_{FS}$ = -5 (2/1) {+ + + + + }

  = -9.843 V

- V_0 = -5* (2/1) {+ + } = - 10*11/16 = -6.875V

Example 10.2

Calculate the values of the LSB, MSB and full scale output for an 8-bit DAC for the 0 to 10 V range.

Solution

For 10 V range, $\text{LSB} = \frac{10\text{ V}}{256} = 39\text{ mV}$

and $\text{MSB} = \left(\frac{1}{2}\right)\text{full scale} = 5\text{ V}$

Full scale output = (Full scale voltage – 1 LSB)

= 10 V – 0.039 V = 9.961 V

Example 10.3

What output voltage would be produced by a D/A converter whose output range is 0 to 10 V and whose input binary number is

(i) 10 (for a 2-bit D/A converter)
(ii) 0110 (for a 4-bit DAC)
(iii) 10111100 (for a 8-bit DAC)

Solution

(i) $V_o = 10\,\text{V}\left(1\times\frac{1}{2}+0\times\frac{1}{4}\right)=5\,\text{V}$

(ii) $V_o = 10\,\text{V}\left(0\times\frac{1}{2}+1\times\frac{1}{2^2}+1\times\frac{1}{2^3}+0\times\frac{1}{2^4}\right)$

$= 10\left(\frac{1}{4}+\frac{1}{8}\right)=3.75\,\text{V}$

(iii) $V_o = 10\,\text{V}\,(1 \times 1/2 + 0 \times 1/2^2 + 1 \times 1/2^3 + 1 \times 1/2^4 + 1 \times 1/2^5 + 1 \times 1/2^6 + 0 \times 1/2^7 + 0 \times 1/2^8)$

$= 10\,\text{V}\,(1/2 + 1/8 + 1/16 + 1/32 + 1/64) = 7.34\,\text{V}$