



Reg. No. :

Name :

Fourth Semester B.Tech. Degree Examination, June 2016

(2013 Scheme)

13.404 : DIGITAL SIGNAL PROCESSING (AT)

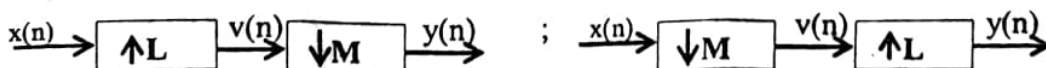
Time : 3 Hours

Max. Marks : 100

PART – A

Answer all questions. 2 Marks each.

- m1 1. What is meant by zero padding ? Why it is used ?
- m1 2. Compute IDFT of a sequence : $\{12, -4 + 4j, -4, -4 - 4j\}$.
- m3 3. For what kind of applications, the symmetrical impulse response of FIR filter is used ?
4. What are Gibbs oscillations ?
- m4 5. Determine the order of Butterworth filter for a given specifications : $\alpha_p = 1$ dB; $\alpha_s = 30$ dB; $\Omega_p = 200$ rad/sec., $\Omega_s = 600$ rad/sec.
- m5 6. How many number of additions, multiplications and memory locations are required to realize a system $H(z)$ having M zeros and N poles in direct form II realizations ?
- m6 7. Compare the fixed point and floating point arithmetic.
- m6 8. What is the steady state variance of the noise in the output due to the quantization of the input for the first order filter ?
- m6 9. State the identities of interpolator.
- m6 10. Under what condition the following systems will become identical ?



(10×2=20 Marks)

P.T.O.



PART - B

Answer **one** question from **each** Module.

Module - 1

11. a) Derive Radix-2 DIF-FFT algorithm using divide and conquer approach with necessary butterfly line diagram. Take $N = 8$. 15
- m1 ✓ b) State and prove the complex conjugate property of DFT. 5
12. a) An FIR digital filter has the unit impulse response sequence, $h(n) = \{2, 2, 1\}$.
m1 ✓ Determine the output sequence in the response to the input sequence
 $x(n) = \{3, 0, -2, 0, 2, 1, 0, -2, -1, 0\}$ using the overlap save convolution method. 12
- m1 ✓ b) Using efficient computation, perform DFT of sequence $x(n) = \{1, 4, 9, 16\}$. 4
- m2 ✓ c) Explain the use of FFT algorithm in correlation. 4

Module - 2

13. a) Explain the windows used in FIR filter design with necessary equations. 6
- m3 ✓ b) A low pass filter has the desired response as given below.
- m3 $H_d(e^{j\omega}) = e^{-j3\omega} ; 0 \leq |\omega| \leq \frac{\pi}{2}$
 $= 0 ; \frac{\pi}{2} < |\omega| \leq \pi$ 12
- Determine the filter coefficients $h(n)$ for $M = 7$ using frequency sampling technique.
- m3 ✓ c) What is the necessary and sufficient condition for linear phase characteristics in FIR filter ? 2
14. a) Determine the system function $H(z)$ of the lowest-order Chebychev digital filter that meets the following specifications : 12
- i) 1 - dB ripple in the pass band $0 \leq |\omega| \leq 0.3 \pi$
 ii) Atleast 60 dB attenuation in the stop band $0.35 \pi \leq |\omega| \leq \pi$. Use bilinear transformation.
- ✓ b) Derive mapping formula for impulse invariance technique in IIR filters. 8
- m4

**Module - 3**

15. a) A system is represented by a transfer function $H(z)$ is given by
- m5
$$H(z) = 3 + \frac{4z}{z - 1/2} - \frac{z}{z - 1/4}$$
- i) Does this $H(z)$ represent IIR or FIR filter ? 2
 - ii) Give a difference equation realization of this system using direct form - I. 4
 - iii) Draw the block diagram for direct form - II realization and give the governing equations for its implementation. 6
- b) Sketch the ladder structure for the system, 8
- $$H(z) = (1 - 0.5z^{-1} + 1.2z^{-2}) / (1 + 0.15z^{-1} - 0.64z^{-2})$$
- Also check the stability of the system.
16. a) The input to the system, $y(n) = 0.999y(n-1) + x(n)$ is applied to an ADC. 7
- m6 What is the power produced by the quantization noise at the output of the filter if the input is quantized to 8 bits and 16 bits.
- b) Explain the characteristics of limit cycle oscillations with respect to the system described by the difference equation $y(n) = 0.95y(n-1) + x(n)$ and also determine the dead band of the filter. 7
- m6 Explain the coefficient quantization error with an example. 6

Module - 4

17. a) What is the significance of multirate conversion in sub-band coding ? Derive the performance of analysis and synthesis filter in sub-band coding applications. 10
- m6 b) Explain the sampling rate conversion by a rational factor of I/D with suitable examples. 10
- m5 18. a) Explain the architecture of TMS320C6713 processor with a neat diagram. 12
- b) Draw the block diagram of FDM to TDM trans-multiplexer and explain. 8