PHASE LOCKED LOOP (PLL)

Phase Lock Loop Applications

Applications

Synchronization and Demodulation Circuits

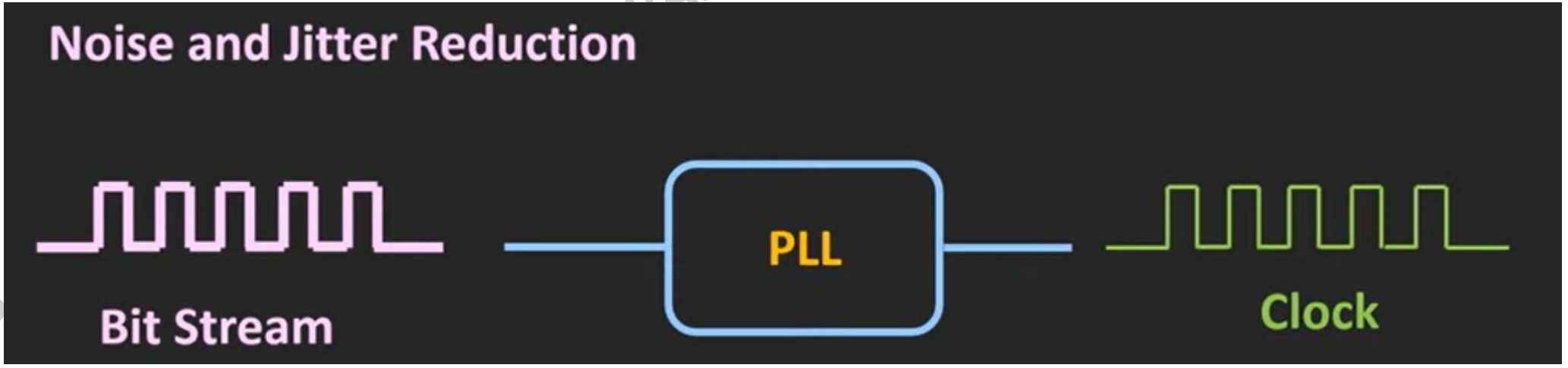
Clock Recovery

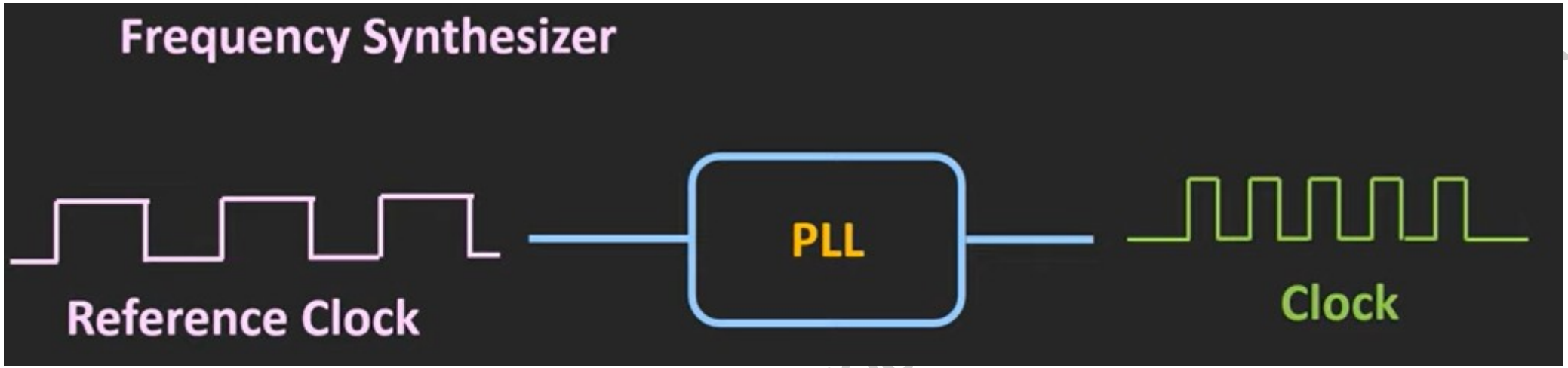
Noise and Jitter Reduction

Frequency Synthesizers

Microprocessors (Clock Multiplier and Clock Distribution)


Clock Recovery
PLL
Bit Stream
Clock

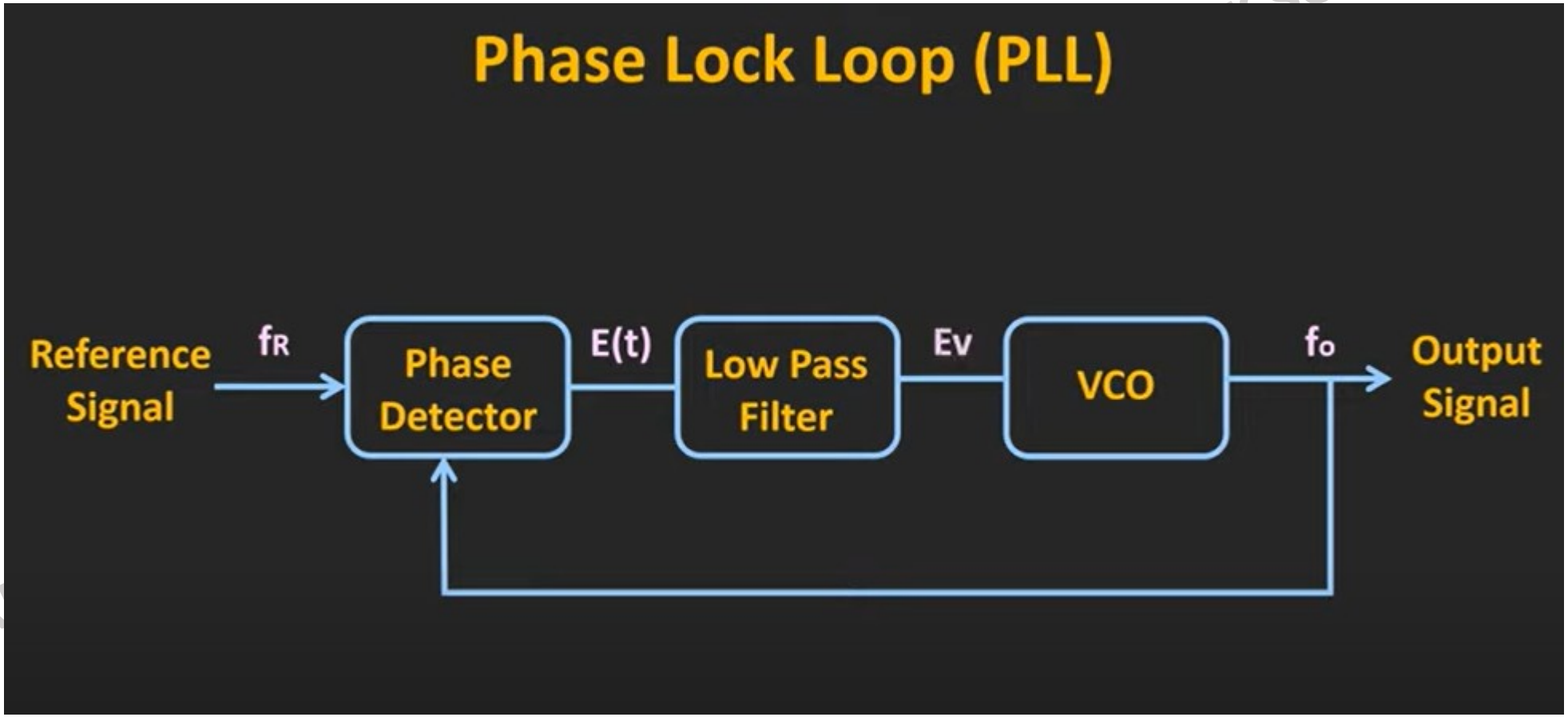

Noise and Jitter Reduction
PLL
Bit Stream
Clock



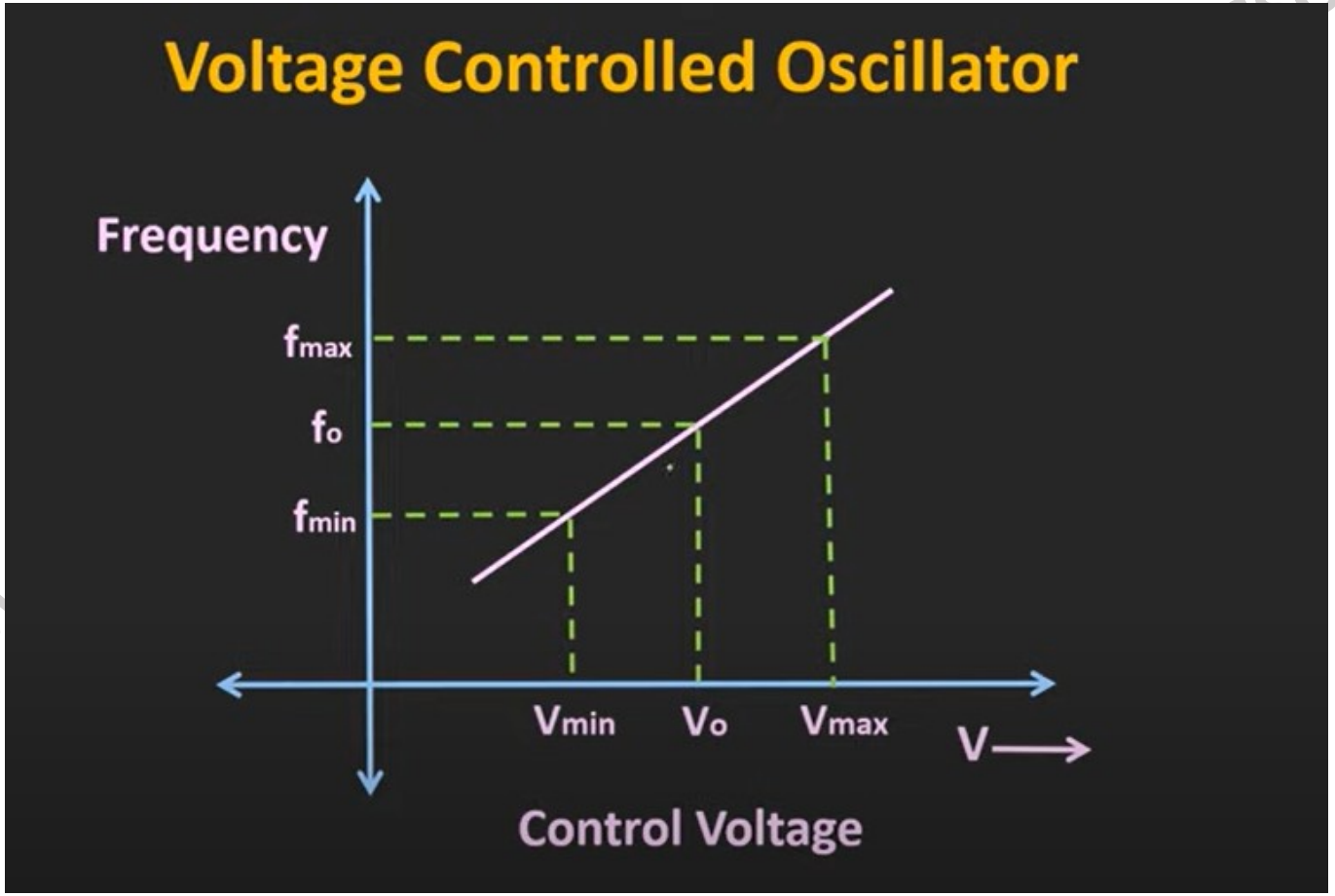
PLL

- It is a control s/m or control loop which maintains the same phase btw the i/p & o/p s/g.
- PLL synchronises o/p and i/p in phase as well as freq.
- PLL is a system that generates an output signal whose phase is related to its input.
- The two signals will have the same frequency and either no phase difference or a constant phase difference between them.

$f_0 = f_{in}$ & , we can say that loop is in the lock condition.



VCO : As the control V changes, freq of oscn also changes.



OPERATING PRINCIPLES:

- Whenever loop is jz turned ON, VCO runs at centre freq f_0 (free running freq).
- A **phase detector or comparator** compares the i/p or reference freq f_R with the f/b freq f_0 .
- o/p of phase detector is proportional to the phase difference btw f_R & f_0.
- The output V of a phase detector is a dc voltage and is called as error voltage.

- o/p of P.D. is applied to **LPF** which removes high freq noise and produce a DC level.
- Filter also helps in establishing dynamic chara of PLL ckt.
- This DC level is given as i/p to **VCO**.
- o/p freq of VCO is directly proportional to the i/p dc level.
- VCO freq is compared with i/p freq and adjusted until it is equal to the i/p freqs.

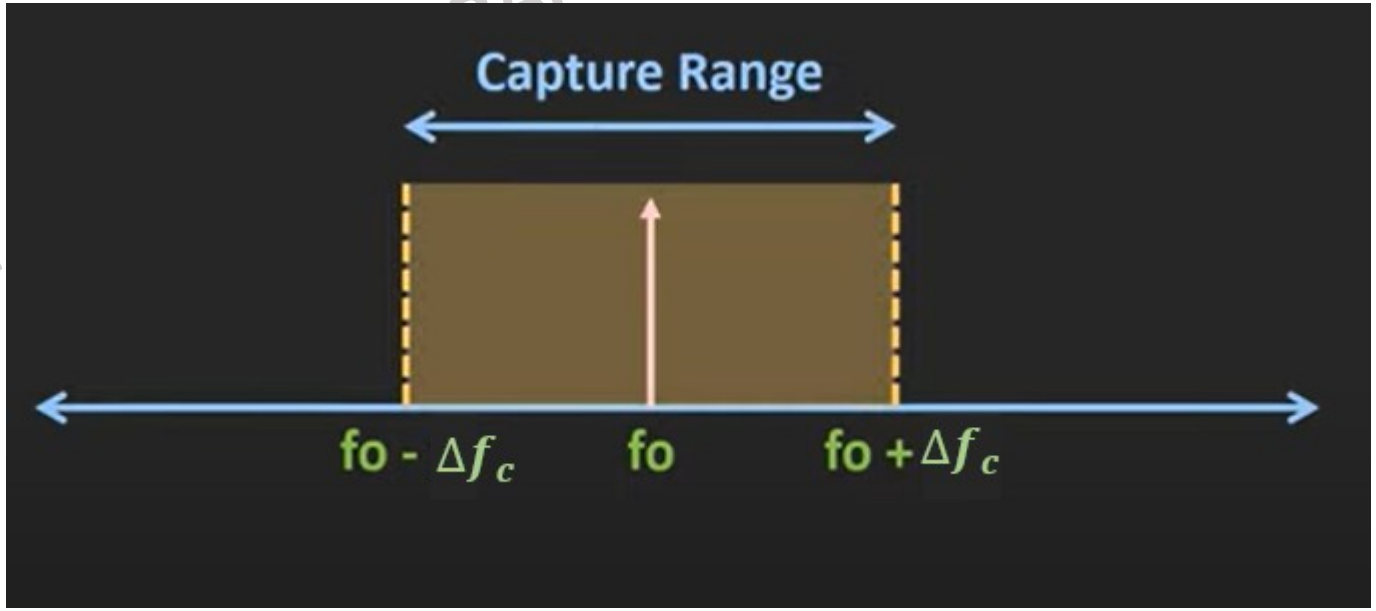
PLL goes thru 3 states:

- Free running
- Capture
- Phase lock

- Before the i/p is applied, PLL is in free running state.
- Once i/p freq is applied, VCO freq starts to change and PLL is said to be in capture mode.
- VCO freq continues to change until it equals the i/p freq and PLL is then in the phase locked state.
- When phase locked, the loop tracks any change in the i/p freq thru its repetitive action.

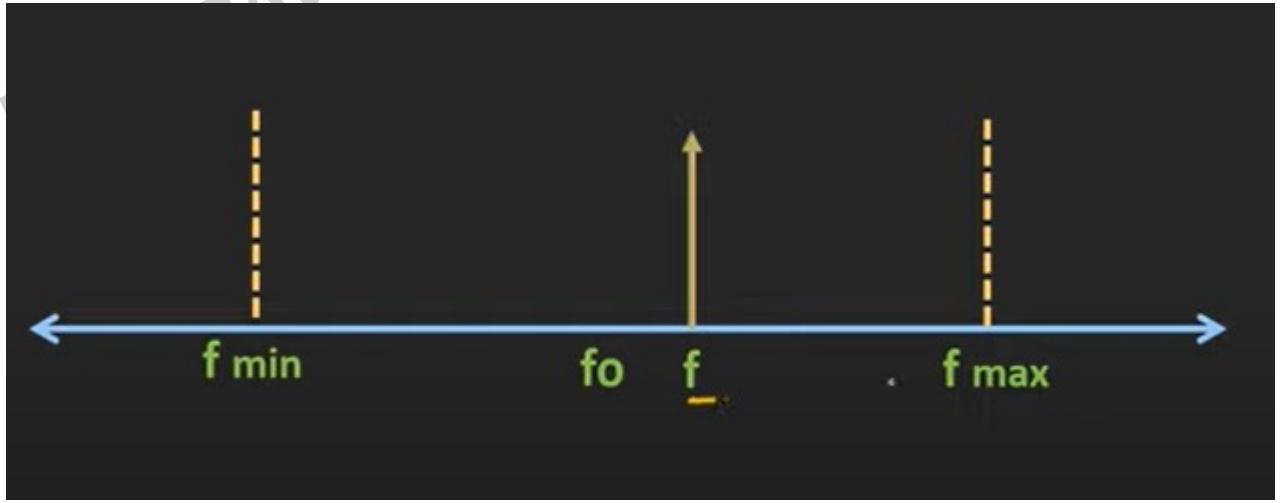
Capture Range:

- Range of i/p freqs around the VCO centre freq onto which the loop can lock when starting from the unlocked condition.

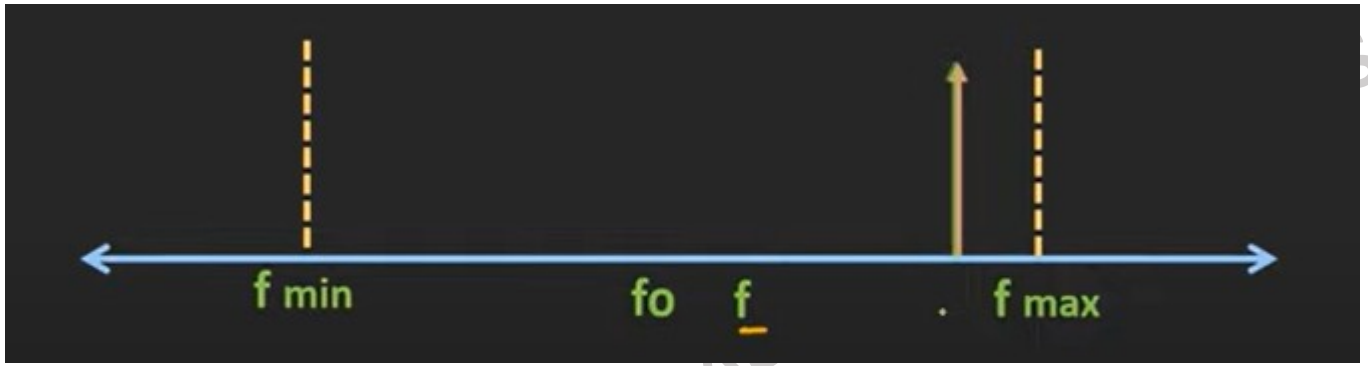


Lock (Tracking) Range:

- Range of i/p freqs over which the loop remain in the lock condition once it has captured the i/p s/g.
- Lets say VCO is already locked to i/p freq f.



- If i/p freq changes, then VCO will follow that freq if i/p freq is within the lock range.



- But if i/p freq goes out of lock range, VCO starts running at the free running freq.

- It wont be able to lock to the i/p freq until the i/p freq is within the capture range of PLL.

Pull in time: total time taken by PLL to establish lock. This depends on the initial phase and frequency difference between the two signals as well as on the overall loop gain and loop filter characteristics.

- **Capture range is symmetrically located with respect to the VCO free running freq**.
- PLL cannot acquire a s/g outside capture range, but once captured it will hold on till the s/g freq goes beyond lock in range.
- Inorder to increase the ability of lock in range, large capture range is required.
- But a large capture range will make PLL more susceptible to noise and undesirable signal.
- Hence a suitable compromise is often reached btw these 2 opposing requirements of the capture range.

- Many a times, BW of LPF is first set for a large value for initial acquisition of s/g, then once the s/g is captured, BW of LPF is reduced substantially.
- This will minimize interference of undesirable s/gs and noise.

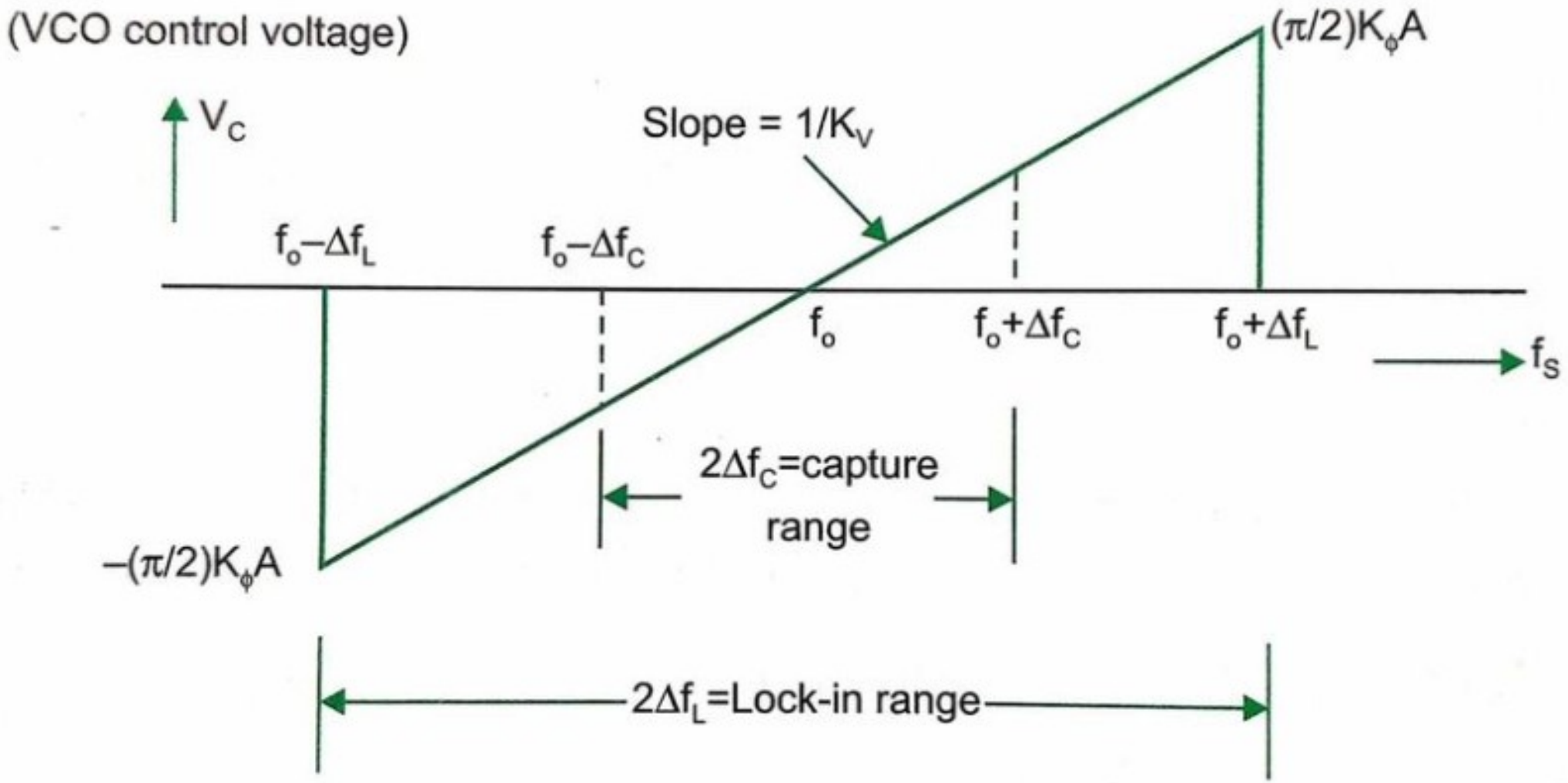


Fig. 9.11 PLL lock-in range and capture range

- Lock in range

$$= K_v K_\phi A\pi$$

$$= K_v K_\phi A(\pi/2)$$

- Capture range

K_v = voltage to freq transfer coefficient of VCO

K_ϕ = phase angle to voltage transfer coefficient of phase detector.

A = voltage gain of amplifier

$f_1 = 1/2\pi RC$

- Lets say at a given pt of time, 1 s/g has phase and other has phase
- Phase diff = -
- If phase difference is very small, then - = -

- 2nd term HF s/g eliminated using LPF.
- So jz by multiplying 2 s/gs, it is possible to generate phase diff btw them.

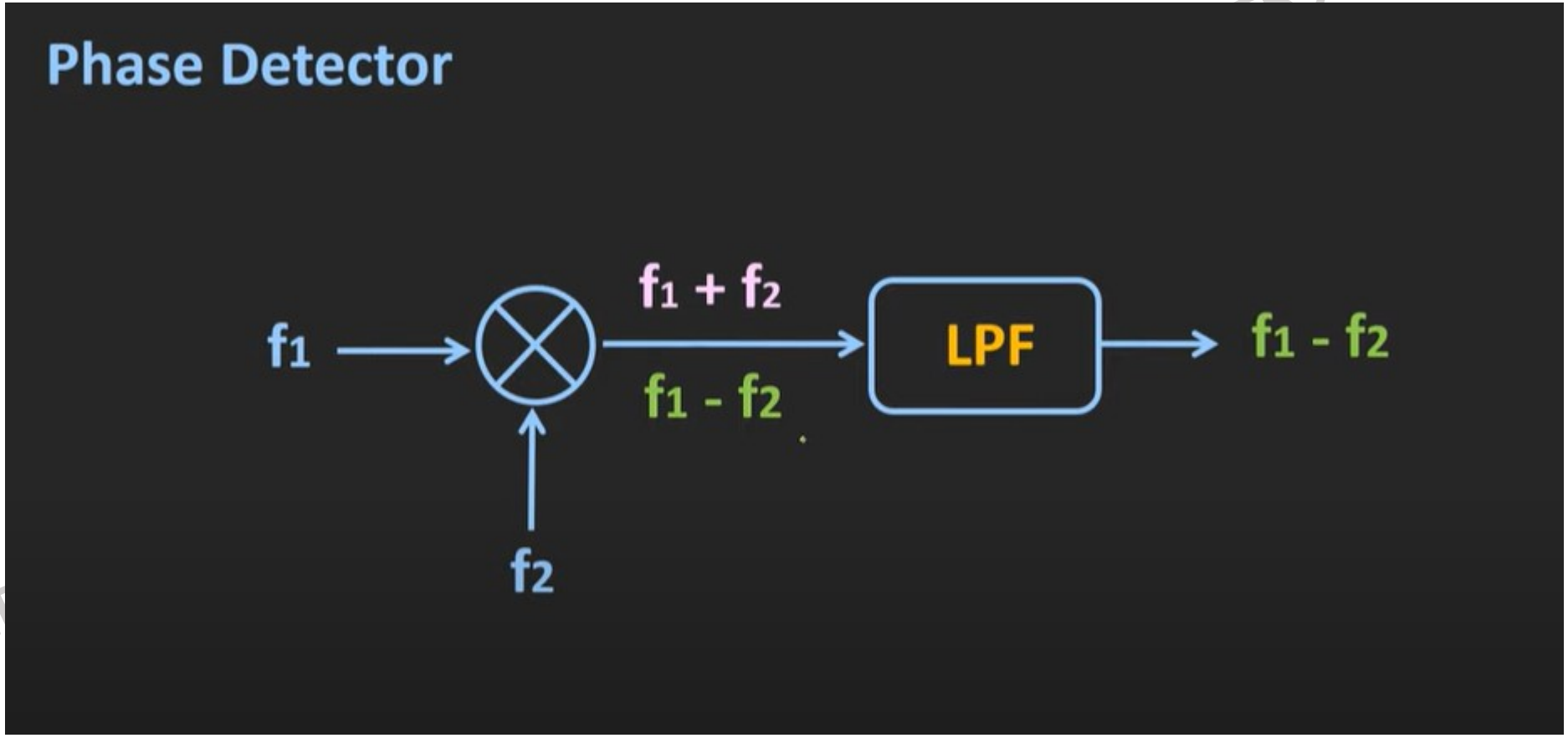
Phase Detector

$\alpha \quad \beta \Rightarrow$ Phase Difference $= \alpha - \beta \approx \sin(\alpha - \beta)$

$$\sin(\alpha - \beta) = \sin\alpha\cos\beta - \sin\beta\cos\alpha$$

$$\sin\alpha\cos\beta = \frac{\sin(\alpha - \beta)}{2} + \underbrace{\frac{\sin(\alpha + \beta)}{2}}_{\text{LPF}}$$

In freq domain



Types of phase detector used:

Phase Detector

RF Applications: Balanced Mixer

Digital Signals: XOR Gate

Phase Frequency Detector

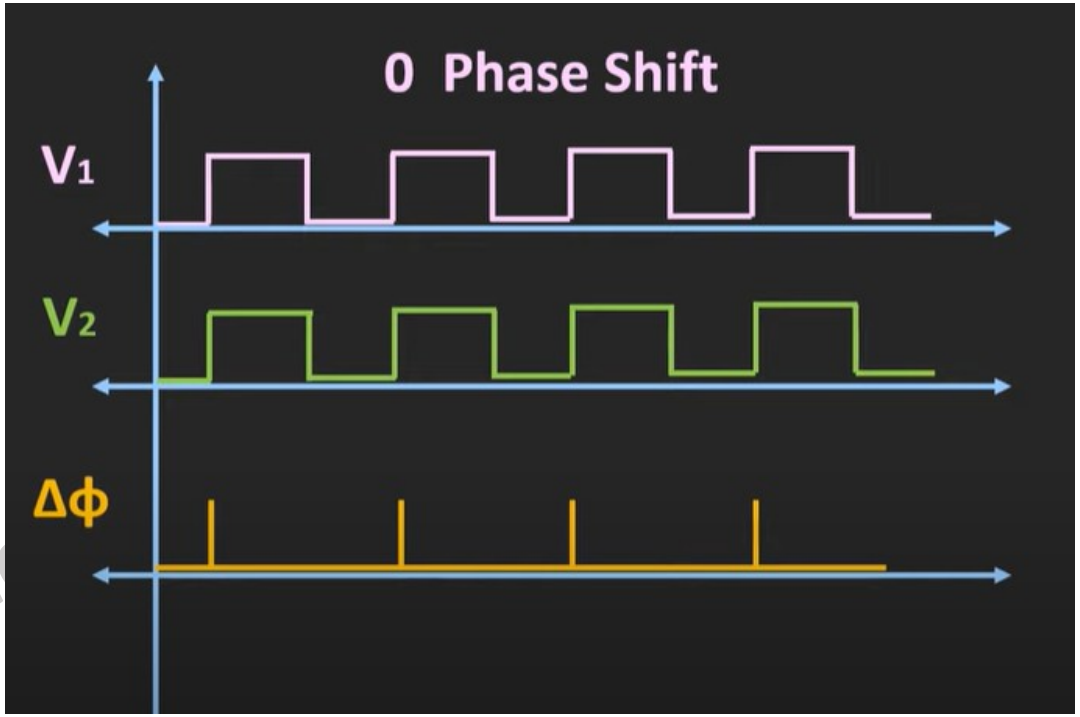
How XOR gate can be used as a phase detector?

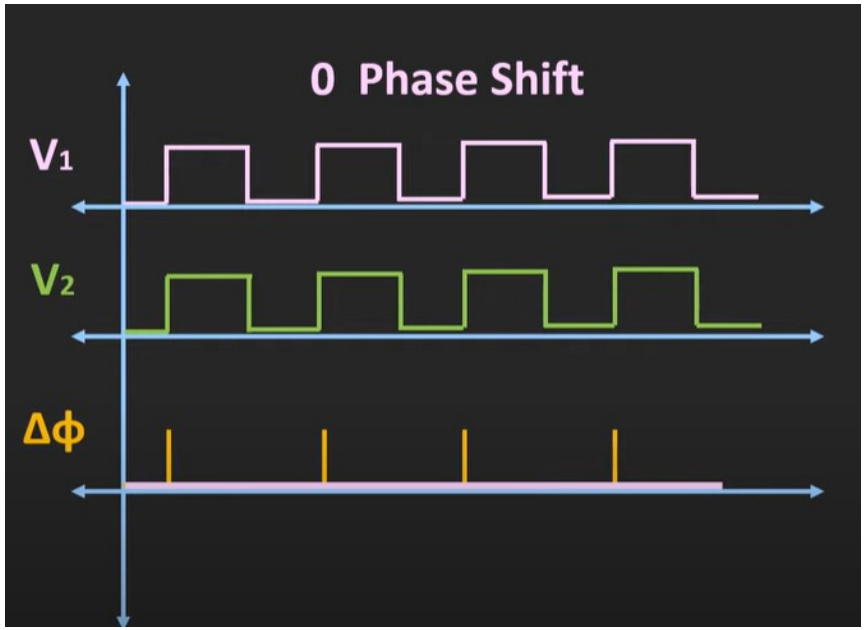
Phase Detector

XOR Gate

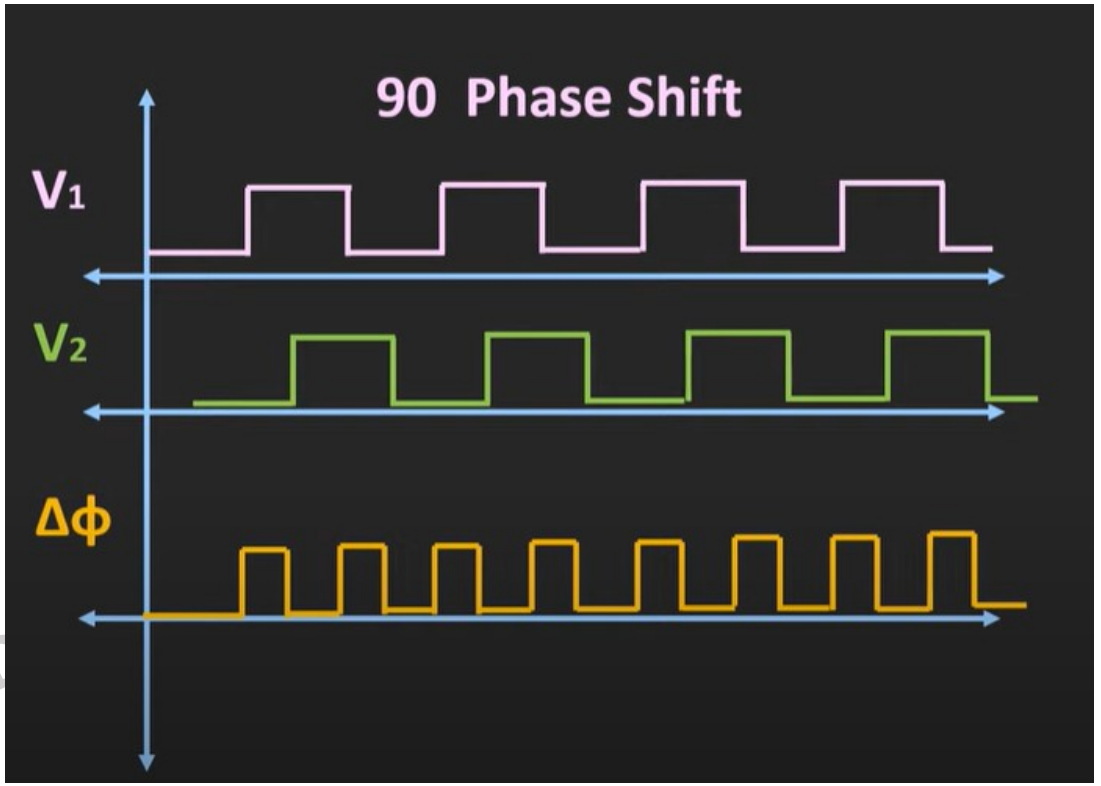
X	Y	Output
0	0	0
0	1	1
1	0	1
1	1	0

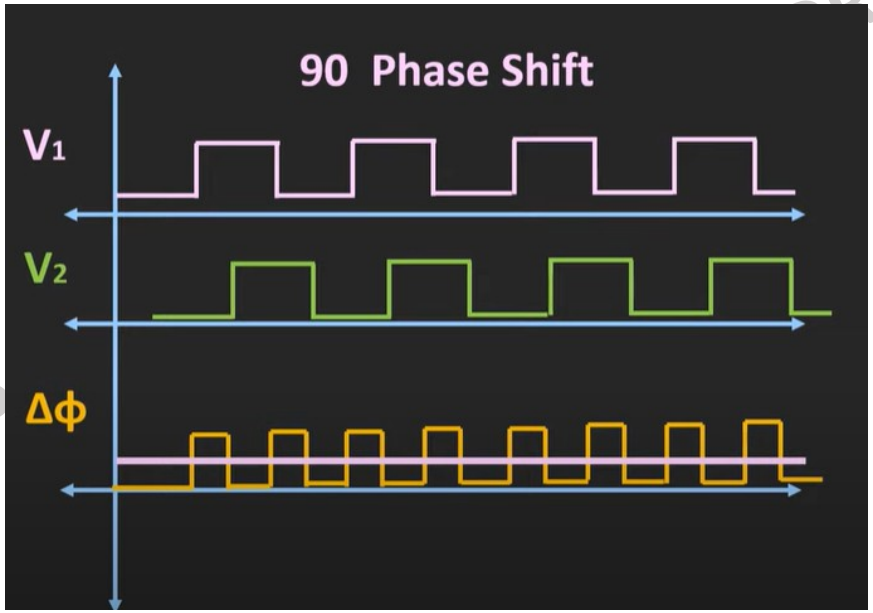
- Whenver 2 i/ps are different, o/p is high.
- When no phase shift btw 2 s/gs, ideally XOR o/p =0
- Practically there will be spikes at transition.
- Avg of phase difference s/g =0.



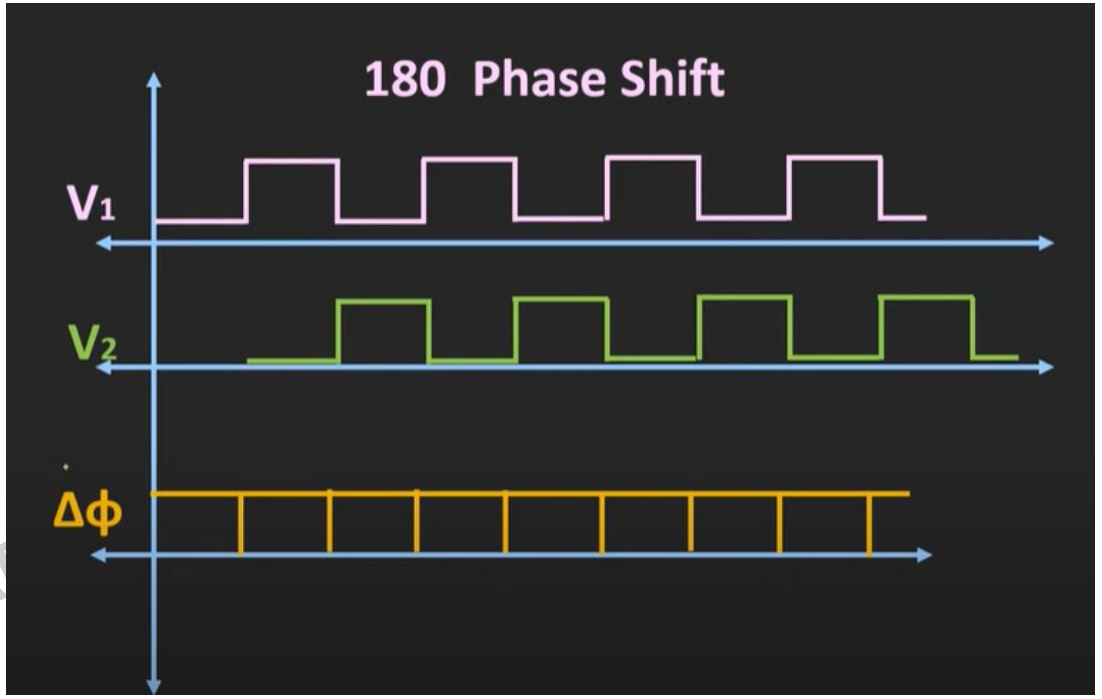


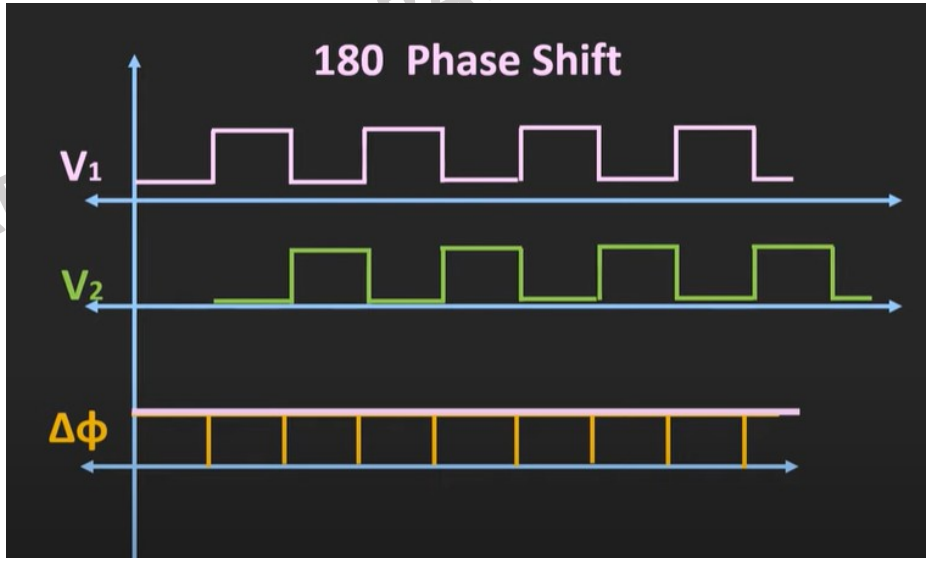
- When phase diff btw 2 s/gs =90 deg:
- If we take avg of phase diff s/g, we will get o/p V = half of the peak value.



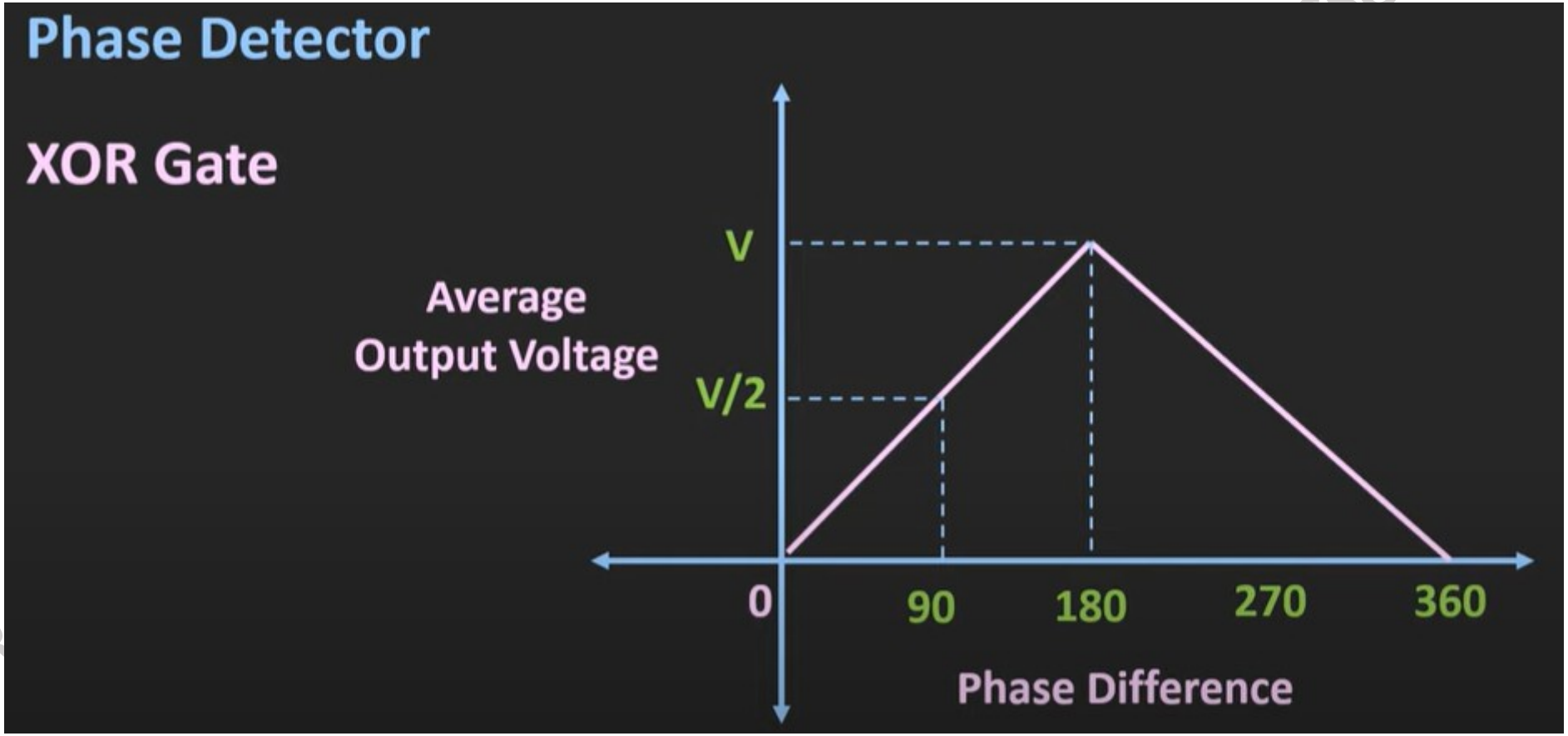


- When phase diff = 180, o/p will be max. and ideally high for all time.
- But practically, spikes at transition.
- Avg of this o/p w/f will give max value.





- That is , as phase difference btw 2 s/gs increases, avg value of o/p w/v will increase.

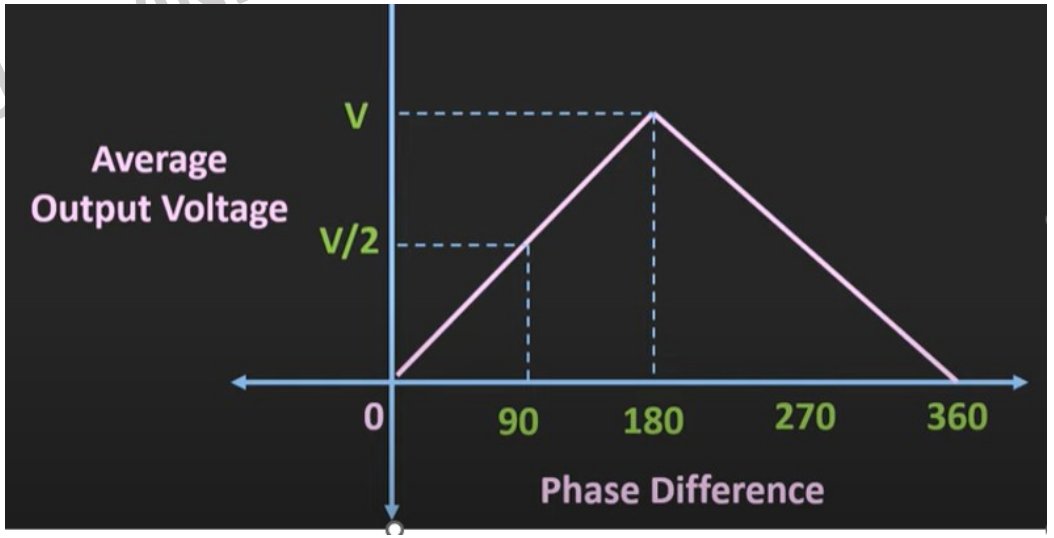


- Slope of curve = conversion gain of phase detector= k_ϕ

$$k_\phi =$$

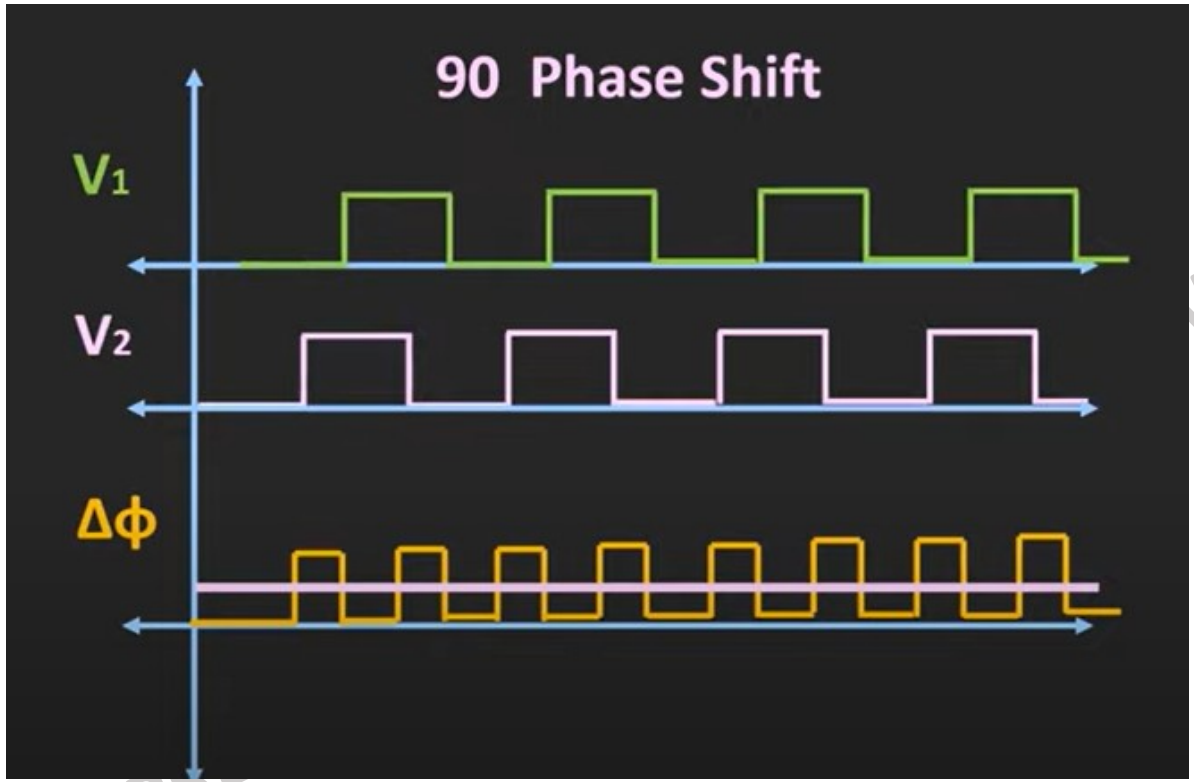
- If XOR gate uses a supply voltage V_{cc} =V= 5v, then

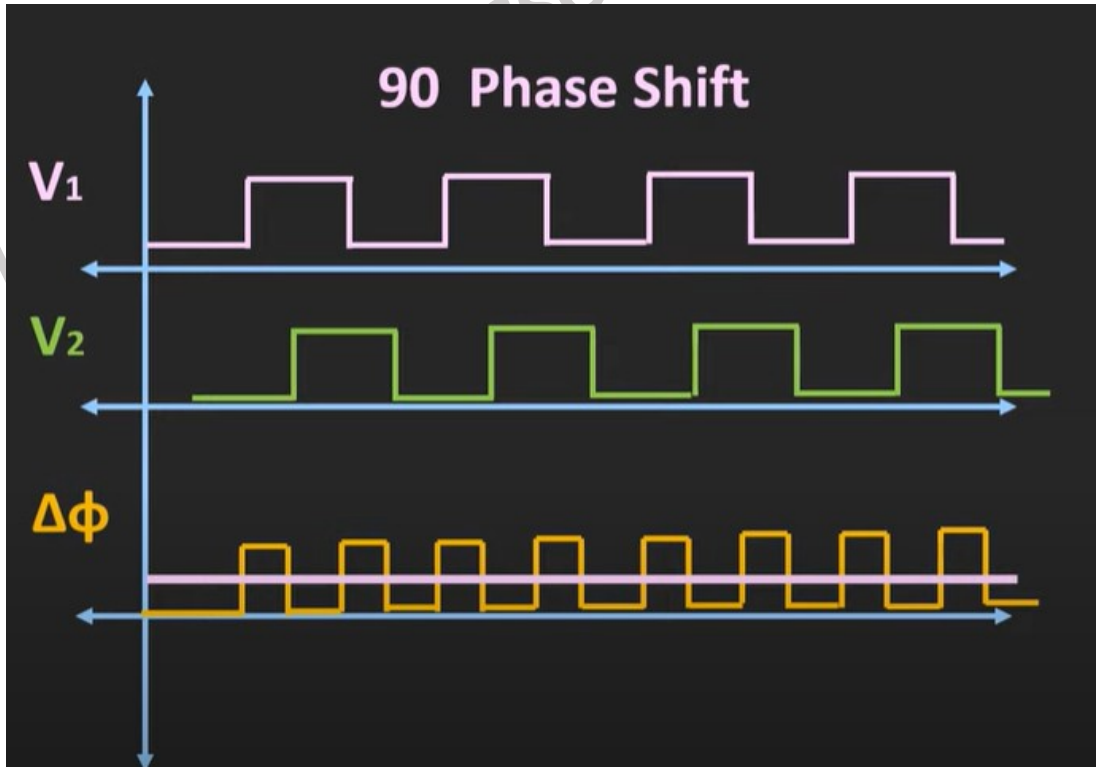
$$k_\phi = \quad = \quad = 1.59 \text{ V/rad}$$



- When phase diff btw 2 s/gs increases from 0 to 180, avg o/p V also increases linearly.
- So this is a linear phase detector.
- But it is linear only till 180.
- When p.d. increases from 180 to 360, avg o/p V starts decreasing.
- And it is also difficult to identify which s/g is leading/lagging.

- Irrespective of V1 lagging or leading V2, we get same o/p.





- For XOR gate to work as linear phase detector, both s/gs shud be square waves (must have approx. 50% duty cycle).

Edge triggered phase detector

- Preferred if i/p s/gs are pulse waveforms with < 50% duty cycle.
- Advs over XOR type of detector:

1. Dc o/p V is linear over 2π radians or 360 deg
2. Exhibits better capture, tracking and locking characteristics than XOR type.

- Uses a SR FF.
- SR FF is formed from a pair of cross coupled NOR gates.
- o/p of detector changes its logic state on +ve(leading) edge of i/ps.

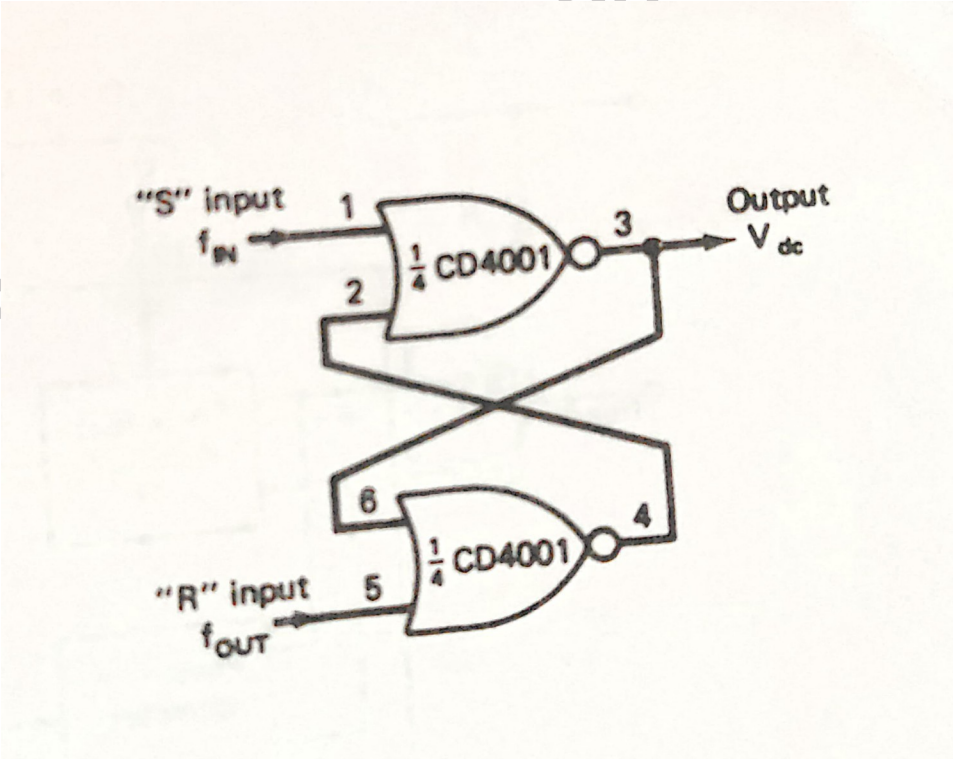
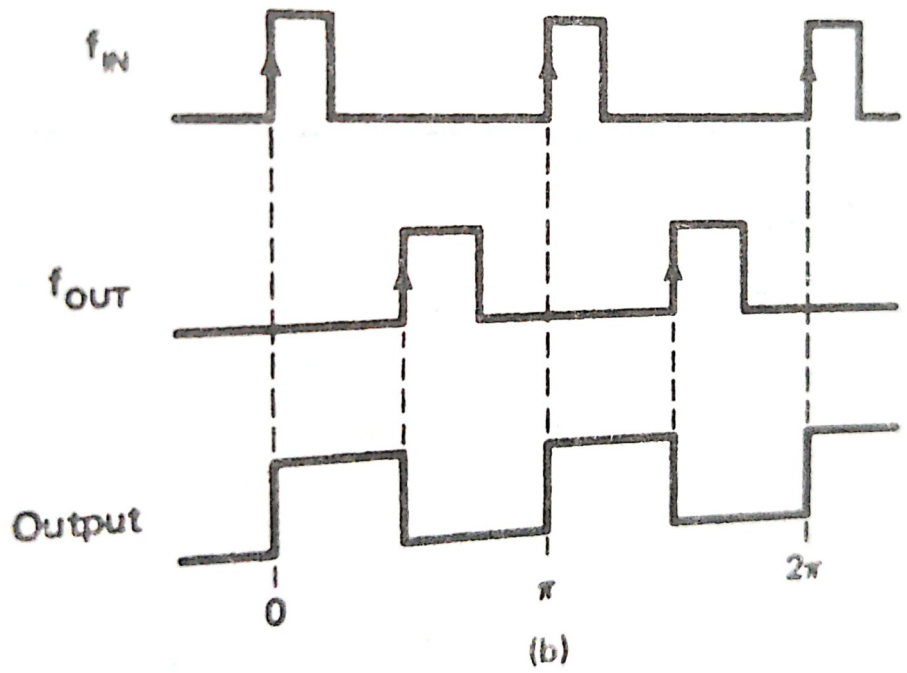
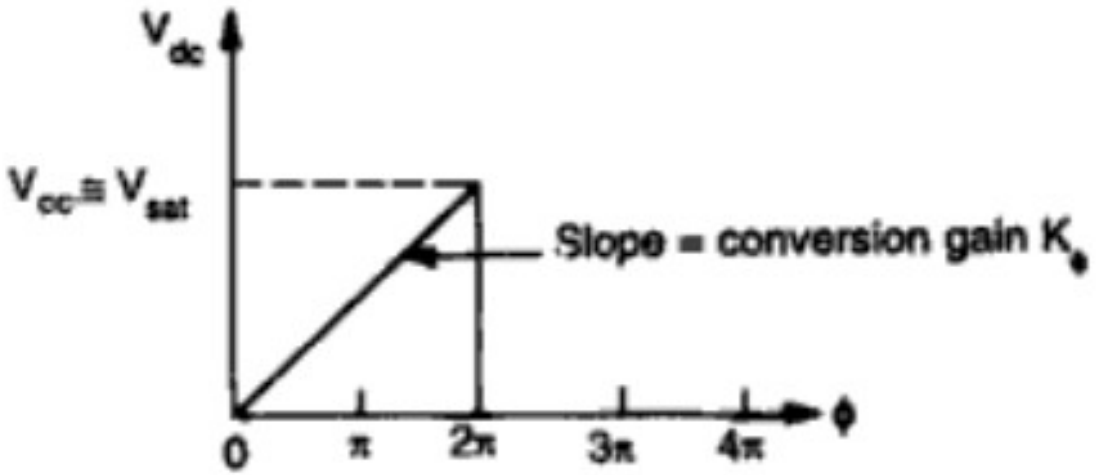


Fig : Edge triggered type of phase detector

a) NOR gate SR FF connection diagram
b) i/p & o/p w/f
c) DC o/p V vs p.d. btw f_{IN} and f_{OUT}



(b)



(c)

LOW PASS FILTER

- o/p of P.D. is applied to **LPF** which removes high freq noise and produce a DC level.
- Filter **controls the dynamic characteristics** of PLL ckt. These chara include capture and lock ranges, BW and transient response.
- If the filter BW is reduced, response time increases.
- But reducing BW of filter also reduces capture range of PLL.

- The charge on the filter capacitor gives a short time memory to the PLL.
- The loop filter used in PLL may be one of the 3 types shown in fig.

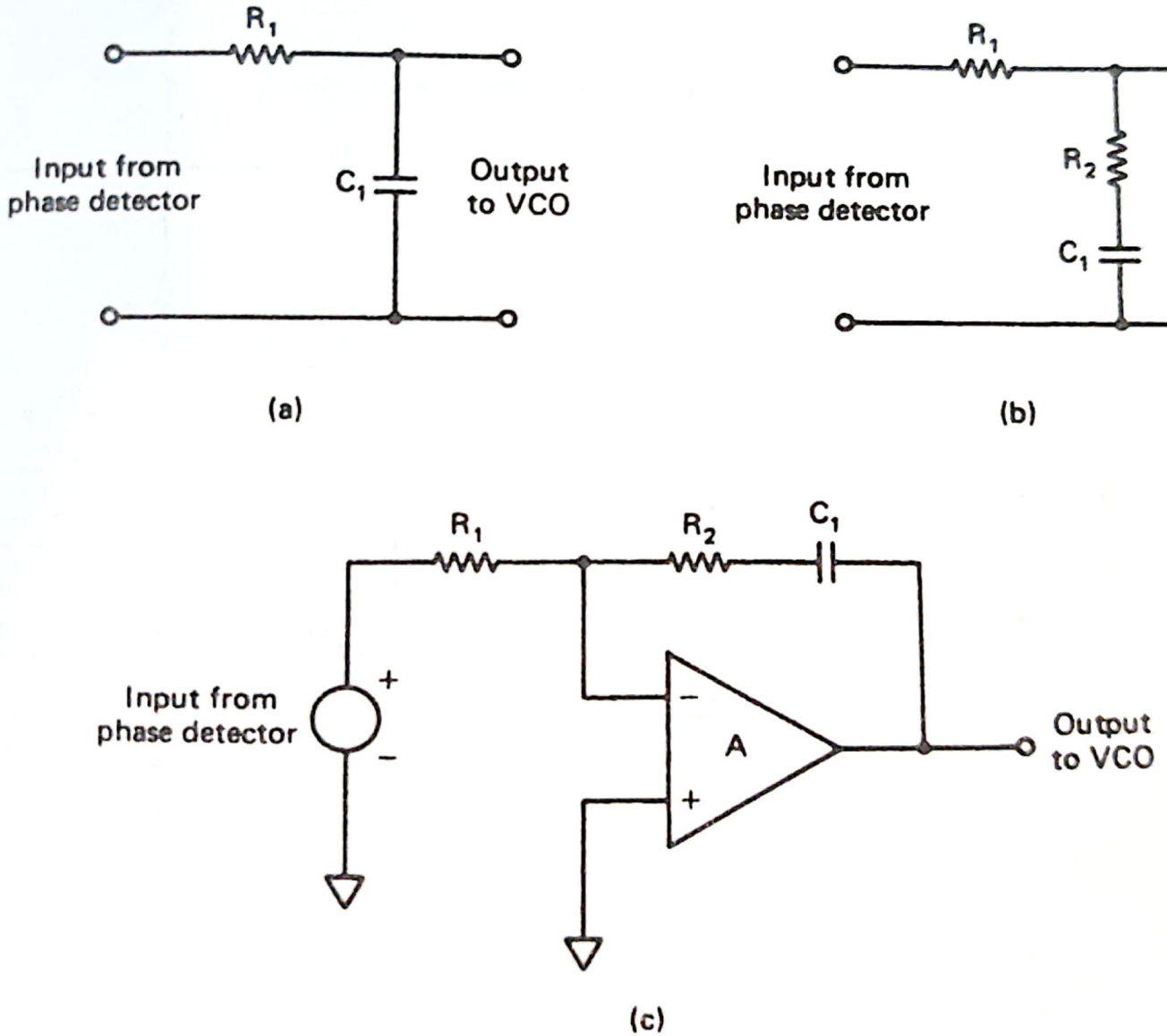


FIGURE 9–29 Low-pass filters. (a) and (b) Passive filters. (c) Active filter.

- With the passive filters, an amplifier is generally used for gain.
- Active filter includes gain.

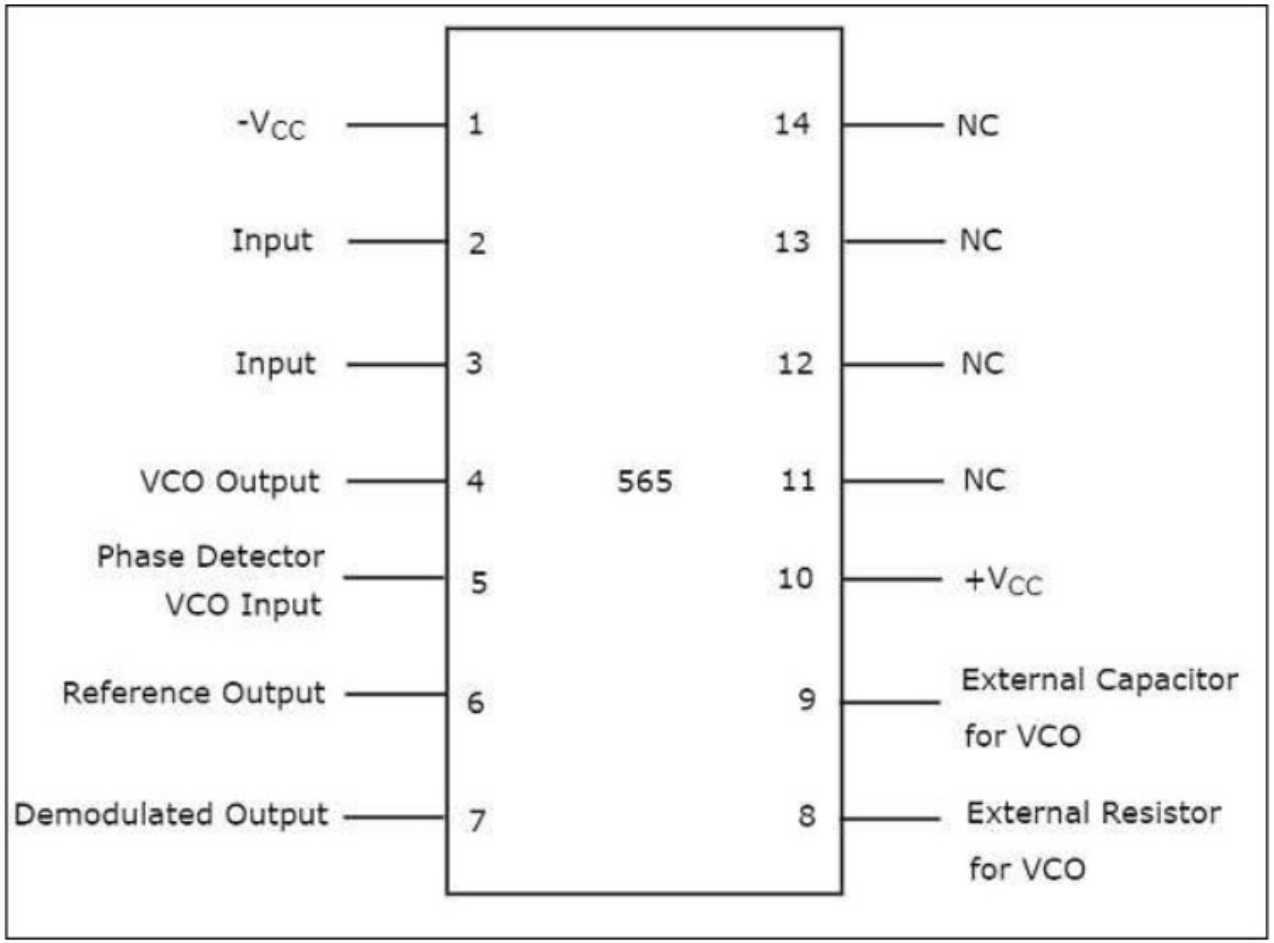
VCO

- Generates o/p freq that is directly proportional to its i/p V.

EXPLAIN VCO using block diagram and waveforms

IC PLL 565

- IC 565 is the most commonly used phase locked loop IC.
- It is a 14 pin Dual-In line Package (DIP).



- Out of 14 pins, only 10 pins (pin number 1 to 10) are utilized for the operation of PLL. So, the remaining 4 pins (pin number 11 to 14) are labelled with NC (No Connection).
- The **VCO** produces an output at pin number 4 of IC 565, when the pin numbers 2 and 3 are grounded.
- Mathematically, we can write the VCO output frequency,

Hz

- R_T is the external resistor that is connected to the pin number 8
- C_T is the external capacitor that is connected to the pin number 9
- Value btw 2 K & 20 K is recommended for R_T.
- VCO free running freq is adjusted with R_T & C_T to be at the centre of input freq range.
- **Pin numbers 4 and 5** are to be shorted with an external wire so that the output of VCO can be applied as one of the inputs of phase detector.

- IC 565 has an internal resistance of 3.6 Kohm.
- A capacitor, C has to be connected between pin numbers 7 and 10 in order to make a **low pass filter** with that internal resistance.

NE/SE565 PLL BLOCK DIAGRAM

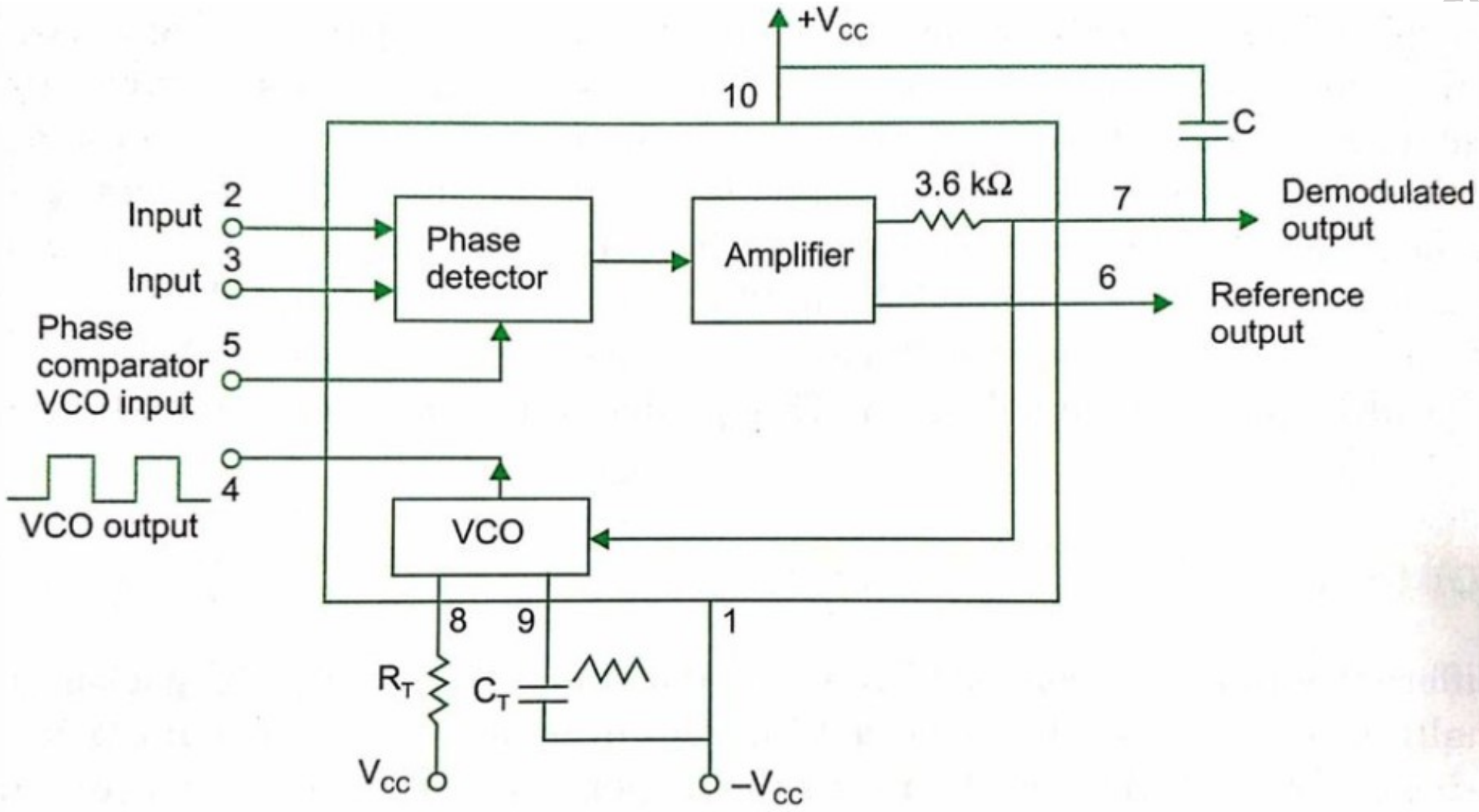


Fig. 9.9 (b) NE/SE565 PLL block diagram

Important electrical parameters of 565 PLL

Sr No.	CHARACTERISTIC	RANGE/VALUE
1	Operating frequency range	0.001Hz to 500KHz
2	Operating voltage range	±6 to ±12
3	Input level required for tracking	10mV rms minimum to 3Vp-p maximum
4	Input impedance	10kΩ typically
5	Output sink current	1mA typically
6	Output source current	10mA typically
7	Drift in VCO center frequency f_o with temperature	300 ppm/°C typically
8	Drift in VCO center frequency f_o with supply voltage	1.5% / V maximum
9	Triangular wave amplitude	Typically 2.4 V_{p-p} at ±6 supply voltage
10	Triangular wave amplitude	Typically 5.4 V_{p-p} at ±6 supply voltage
11	Bandwidth adjustment range	< ± 1 to to ± 60%

- For IC PLL 565,

K_v = where V = $+V_{cc} - (-V_{cc})$ and f_0 is VCO free running freq

$K_\phi = 1.4/\pi$

A = 1.4

- Lock in range $= K_v K_\phi A\pi$

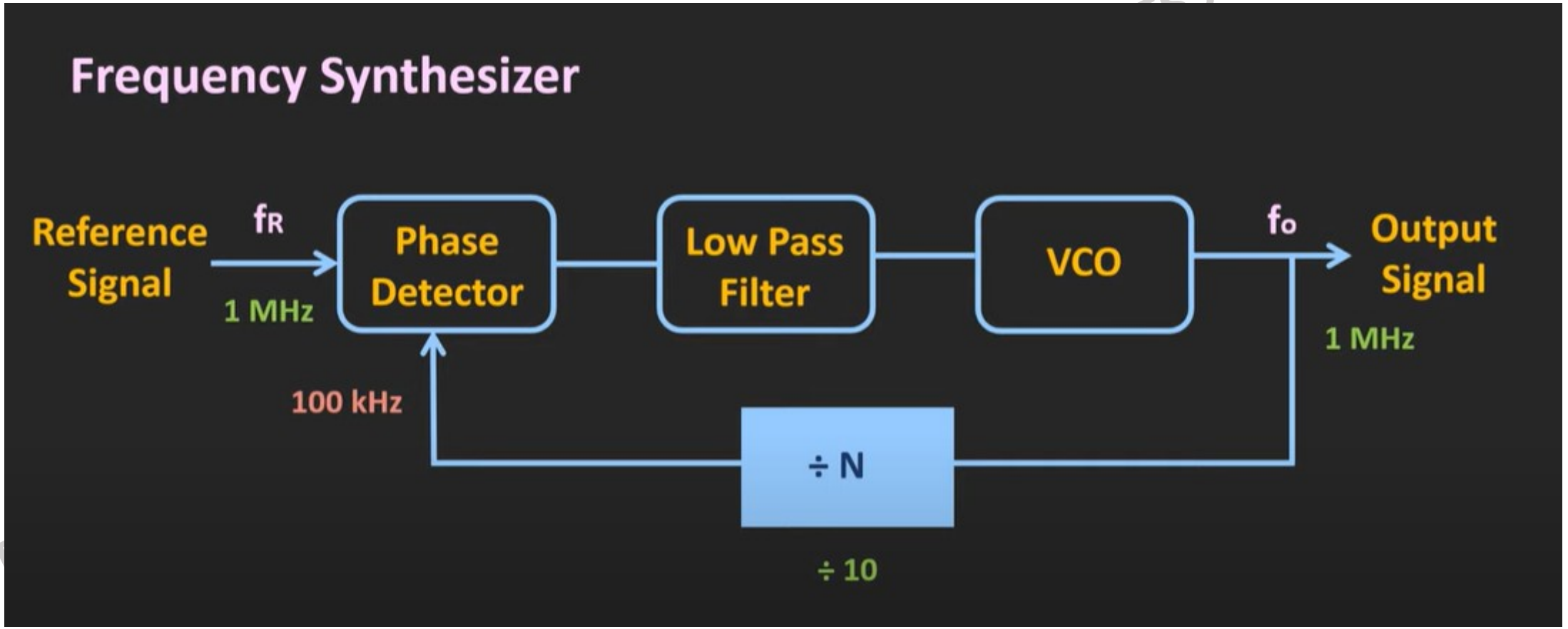
=

- For IC PLL 565, R= 3.6 k

$$f_1 = 1/2\pi RC$$

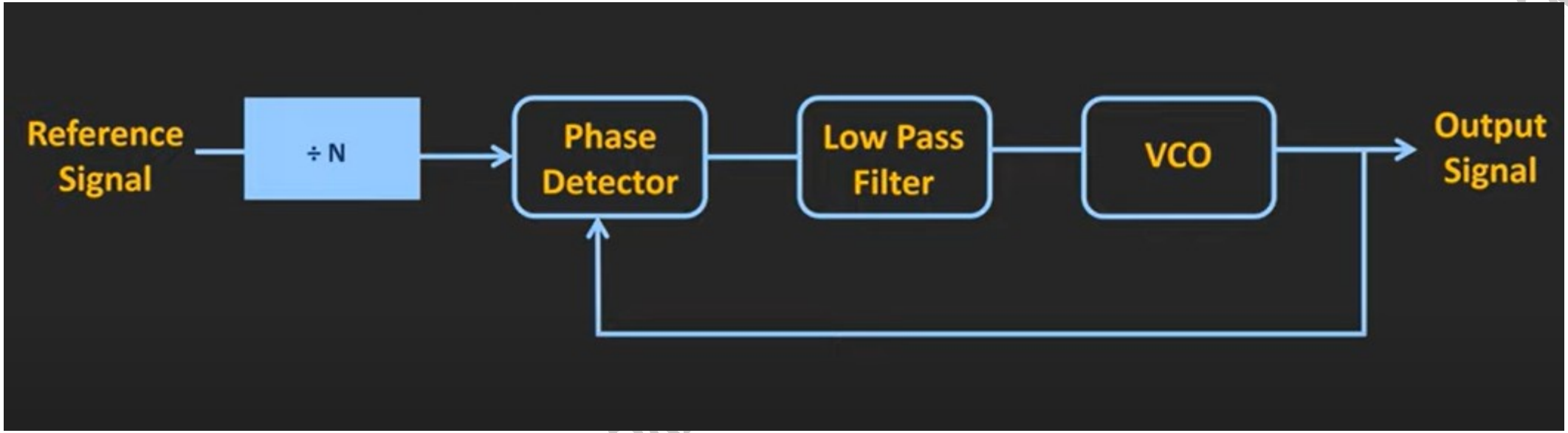
- Capture range

PLL APPLICATIONS



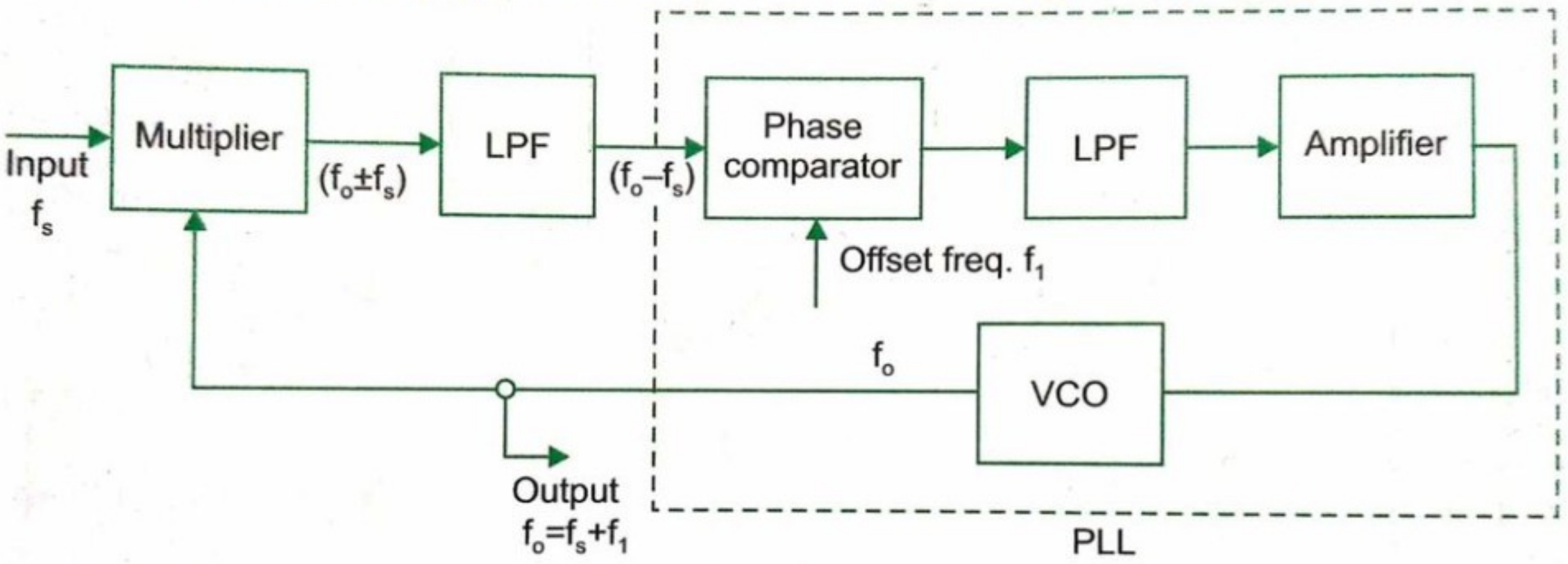
1. Freq synthesizer(freq multiplier & freq divider)

- Using Frequency divider (
- Lets say i/p freq =1MHz & VCO freq = 1MHz
- When we introduce divide by 10 counter in the f/b, o/p = 100KHz.
- Now PLL controls VCO in such a way that o/p of divider n/w = 1MHz
- That means VCO o/p should be = 10 MHz.
- That is o/p of PLL is 10 times the i/p freq. **(freq multiplier)** $\mathbf{f_0 = Nf_R}$



Here i/p freq is divided by a factor of N (freq divider) $f_0 = f_R/N$

2. Frequency translation

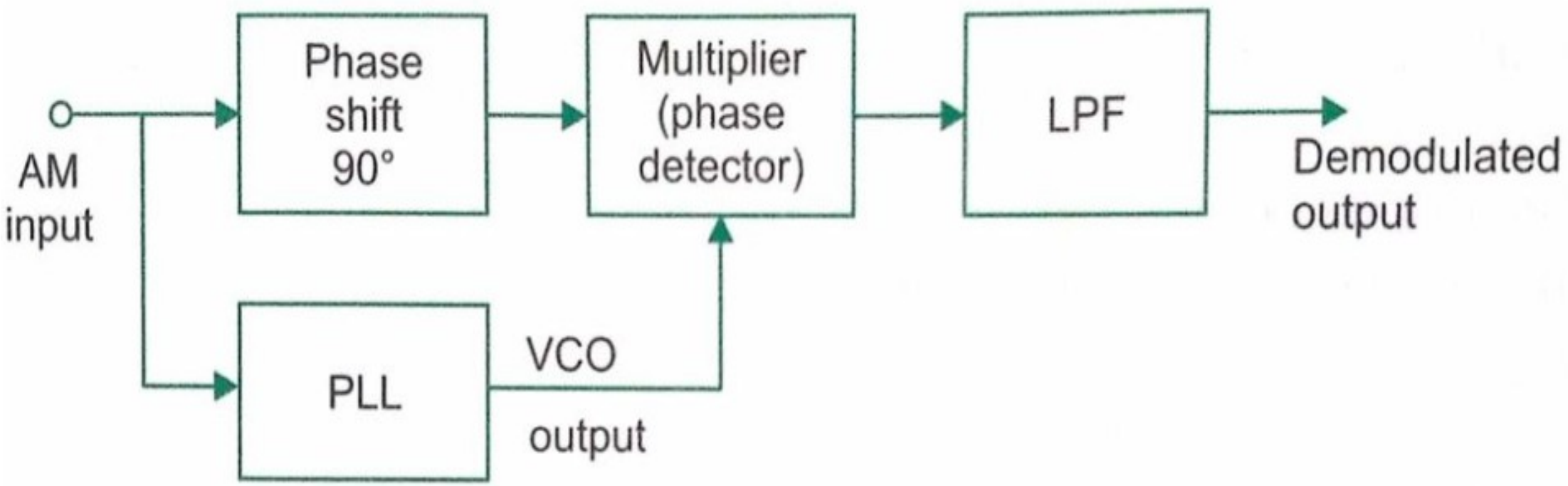


- Shifting the freq of an oscr by a small factor.
- Mixer (or multiplier) and a LPF is connected externally to PLL.
- s/g f_s which has to be shifted and o/p freq f_0 of VCO are applied as i/ps to mixer.
- o/p of LPF --- (f_0-f_s)
- Translation / offset freq f_1 ($f_1<<f_s$) is applied to phase comparator.
- When PLL is in lock state, $f_0-f_s = f_1$

$$f_0=f_s + f_1$$

- Thus it is possible to shift the incoming freq f_s by f_1

3. AM Detection



AM --- $f_s + f_c$

VCO --- $f_0 = f_c$

Demodulated o/p = $f_s + f_c - f_c = f_s$

- PLL is locked to the carrier freq of the incoming AM s/g.
- o/p of VCO which has the same freq of carrier but unmodulated is fed to the multiplier.
- Since VCO o/p is always 90^0 out of phase with incoming AM s/g under locked condition, AM i/p is also shifted in phase by 90^0 before being fed to multiplier.
- So both s/gs to multiplier are in same phase
- o/p of multiplier contains both sum & diff terms
- Demodulated o/p is obtained after filtering high freq components by LPF.

- Since PLL responds only to carrier freqs which are very close to VCO o/p, a PLL AM detector exhibits a high degree of selectivity and noise immunity which is not possible with a conventional peak detector type AM modulators.

4. FM Demodulation

- If PLL is locked to an FM s/g, the VCO tracks the instantaneous freq of i/p s/g.
- Filtered error V which controls VCO and maintains lock with i/p s/g is demodulated FM o/p.
- VCO transfer chara determine the linearity of demodulated o/p.
- Since VCO used in IC PLL is highly linear, it is possible to realize highly linear FM demodulators.

5. FSK demodulators

- In digital commn, binary data is transmitted by means of a carrier freq which is shifted btw 2 preset freqs.
- This type of data txn is called freq shift keying technique.

- As the s/g appears at i/p, loop locks to i/p freq and tracks it btw 2 freqs with a corresponding dc shift at the o/p.
- Filter removes carrier component.