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GOVT. COLLEGE OF ENGINEERING KANNUR

Department of Electronics and Communication Engineering

Third Semester Second Series Examination December- 2022
(2019 Scheme)

Course code: ECT203

Course Name: LOGIC CIRCUIT DESIGN

Max. Marks: 50
Duration: 1.5 Hours

PART A

Answer all questions. Each question Carries 3 marks

1. What is an encoder? What are the problems associated with an octal to binary encoder? (3)
2. What do you mean by characteristic table of a Flipflop? Write the *characteristic table of* SR Flipflop? (3)
3. Draw the circuit of an asynchronous decade up counter using JK Flipflops? (3)
4. What do you mean by noise immunity of a logic gate? How is it quantified? (3)
5. Define the specifications fan-in and fan-out of a logic gate? Illustrate its significance? (3)

PART B

Answer one question from each module

Module 3

6. What is a priority encoder? Design and realize a 4-input priority encoder with a valid output indicator? (7)

OR

7. Design and realize a full subtractor circuit? (7)

Module 4

8. a) Derive the characteristic equation of T Flipflop? (3)

   b) Explain the race-around in JK Flipflop? How is it solved? (3)

   c) How would you convert D flipflop to T flipflop. Illustrate? (5)

   d) Write a Verilog code to realize a D flipflop? (3)

OR

9. a) How many Flipflops are required to build a binary counter circuit to count from 0 to 1023? What is the frequency of the output of last Flipflop for an input clock frequency of 5Mhz? What is the modulus of the above counter? If the counter is initially at 0, what count will it hold after 2060 pulses? (4)

   b) Design and implement a mod-16 synchronous binary down counter using JK Flipflops and gates? (10)

Module 5

10. Draw the circuit diagram of a TTL inverter and explain? *(14)*

OR

11 a) Draw and explain the circuit diagram of a NMOS NOR gate? (7)

   b) Draw and explain the circuit diagram of a CMOS NAND gate? (7)