ARM Processor

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Instruction Set Architecture

- 0-Address Instruction format ---------- **ADD**
- 1-Address Instruction format ---------- **ADD A**
- 2-Address Instruction format ---------- **ADD A, B**
- 3-Address Instruction format ---------- **ADD A, B, C**
- 4-Address Instruction format ---------- **ADD A, B, C, nextaddr**

Addressing Modes and Instruction Types

Addressing Modes

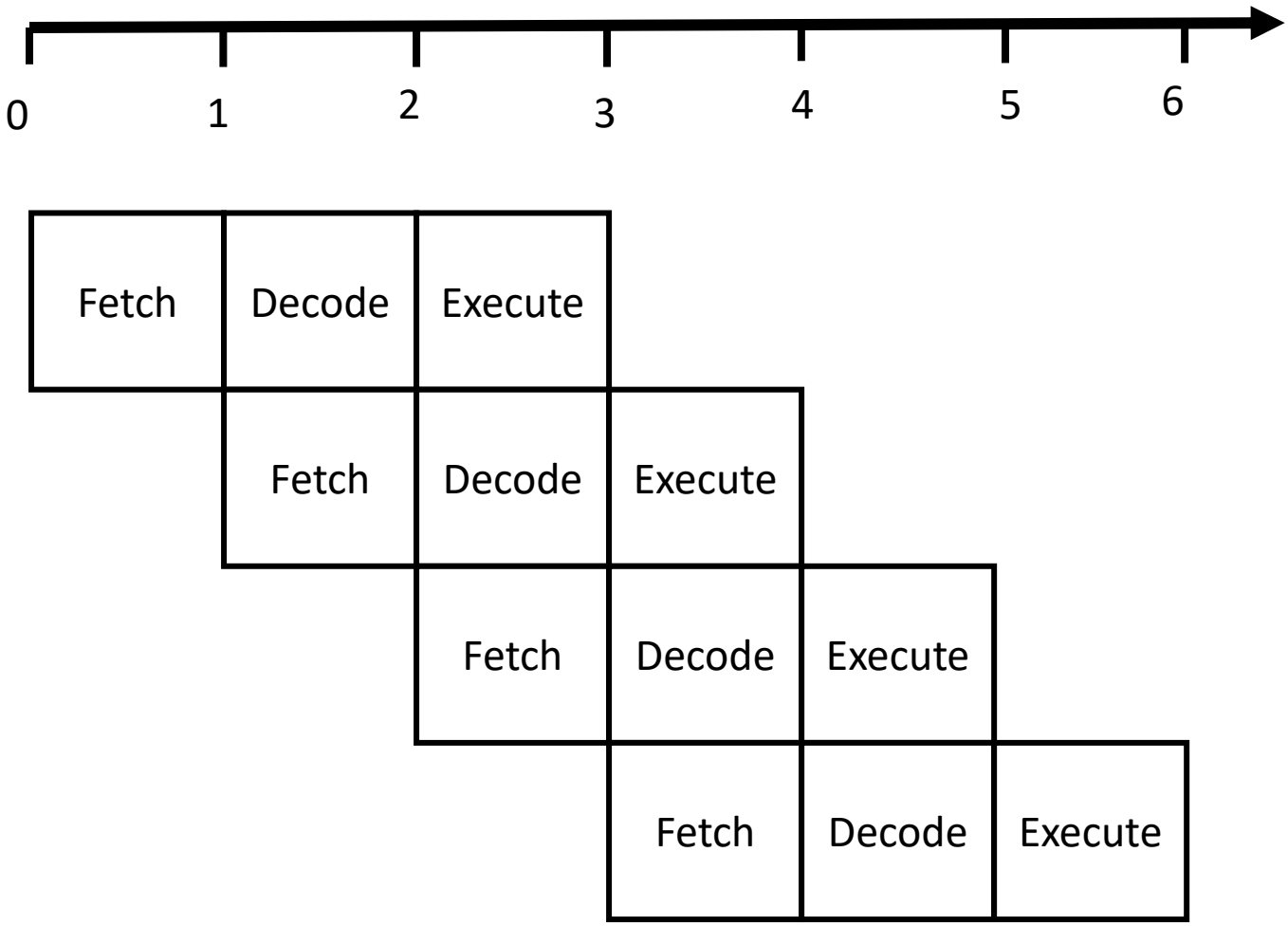
- Immediate
- Direct
- Indirect
- Register
- Register Indirect

Instruction Types

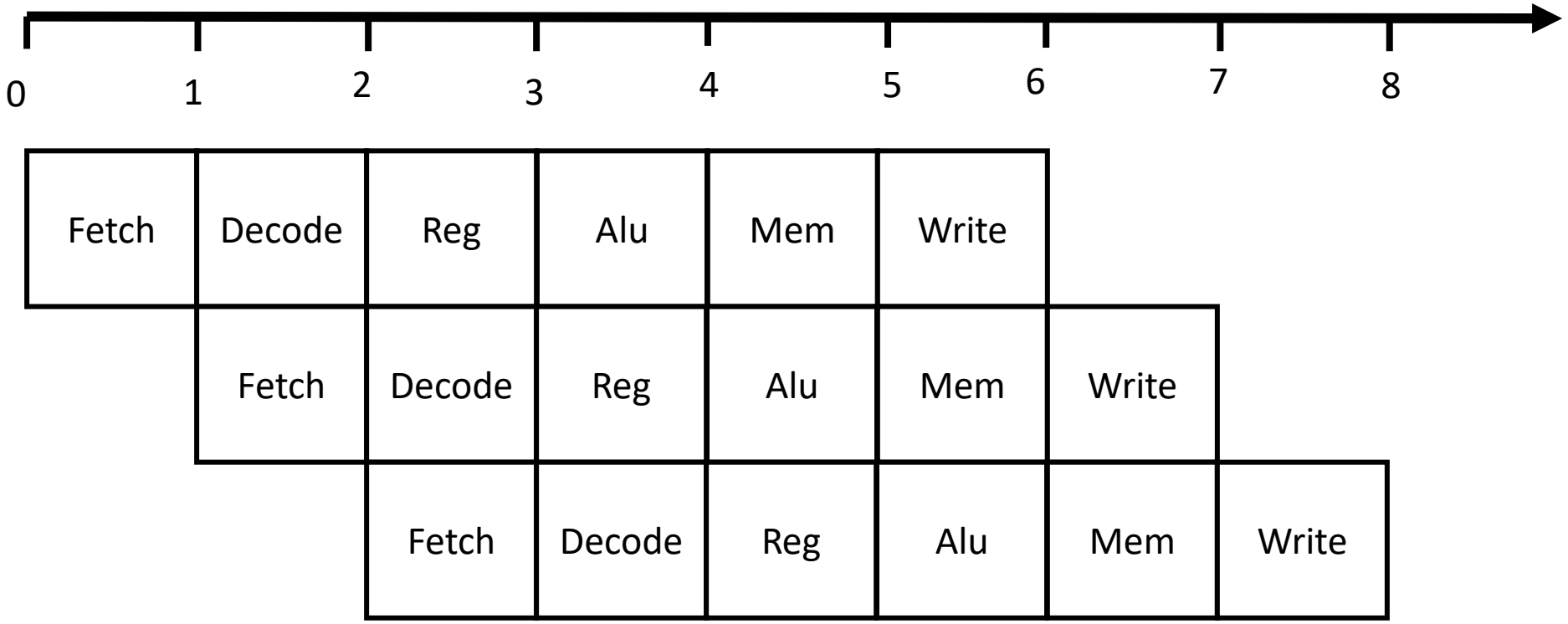
- Data movement Instructions
- Data processing Instructions
- Control flow Instructions
- Special Instructions

```
MOV A, #34
MOV R1, R2
MOV R1, [R2]
MOV A, [2001]
MOV A, @2001
```

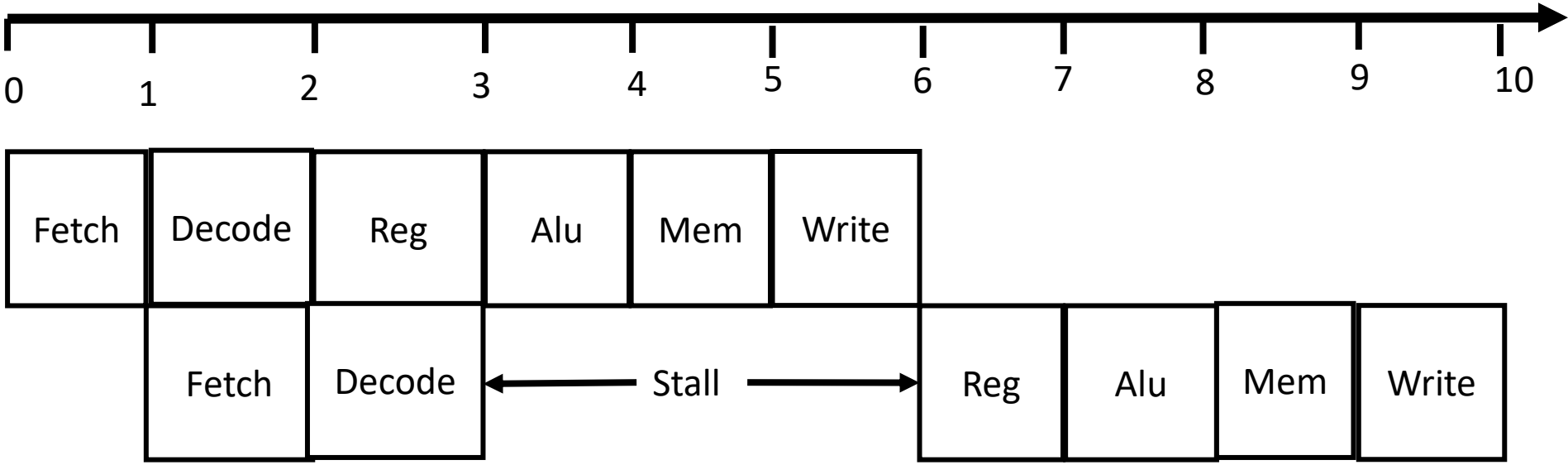
3 Stage Pipeline



6- Stage Pipeline



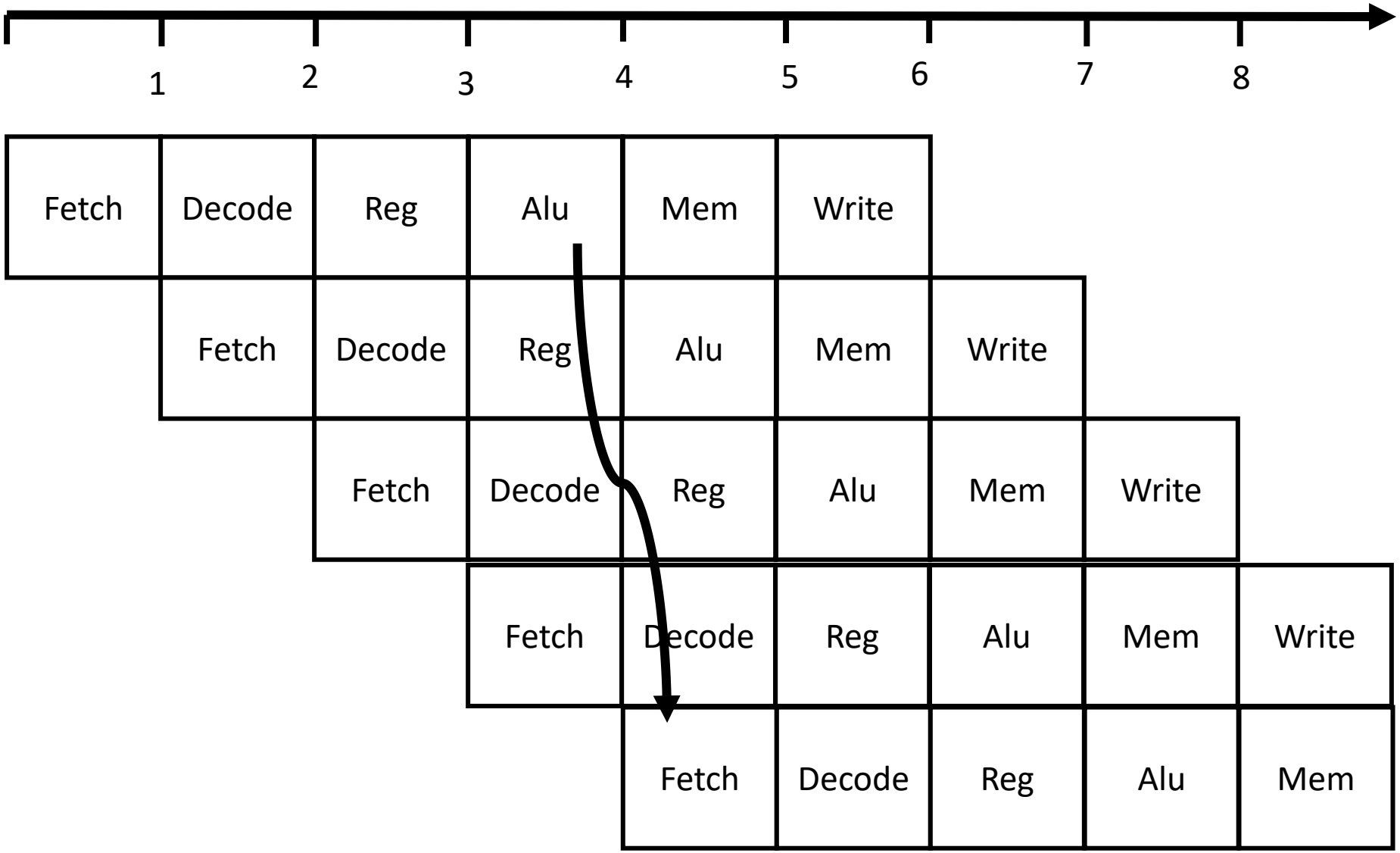
Read After Write Pipeline Hazard



Inst1: ADD A, B, C

Inst2: SUB D, A, B

Pipelined Branch Behavior



RISC Architecture

- A fixed (32-bit) instruction size with few formats
- A load-store architecture where instructions that process data operate only on registers
- A large register bank of thirty-two 32-bit registers
- Hardwired Instruction decode logic
- Pipelined Execution
- Single cycle Instructions

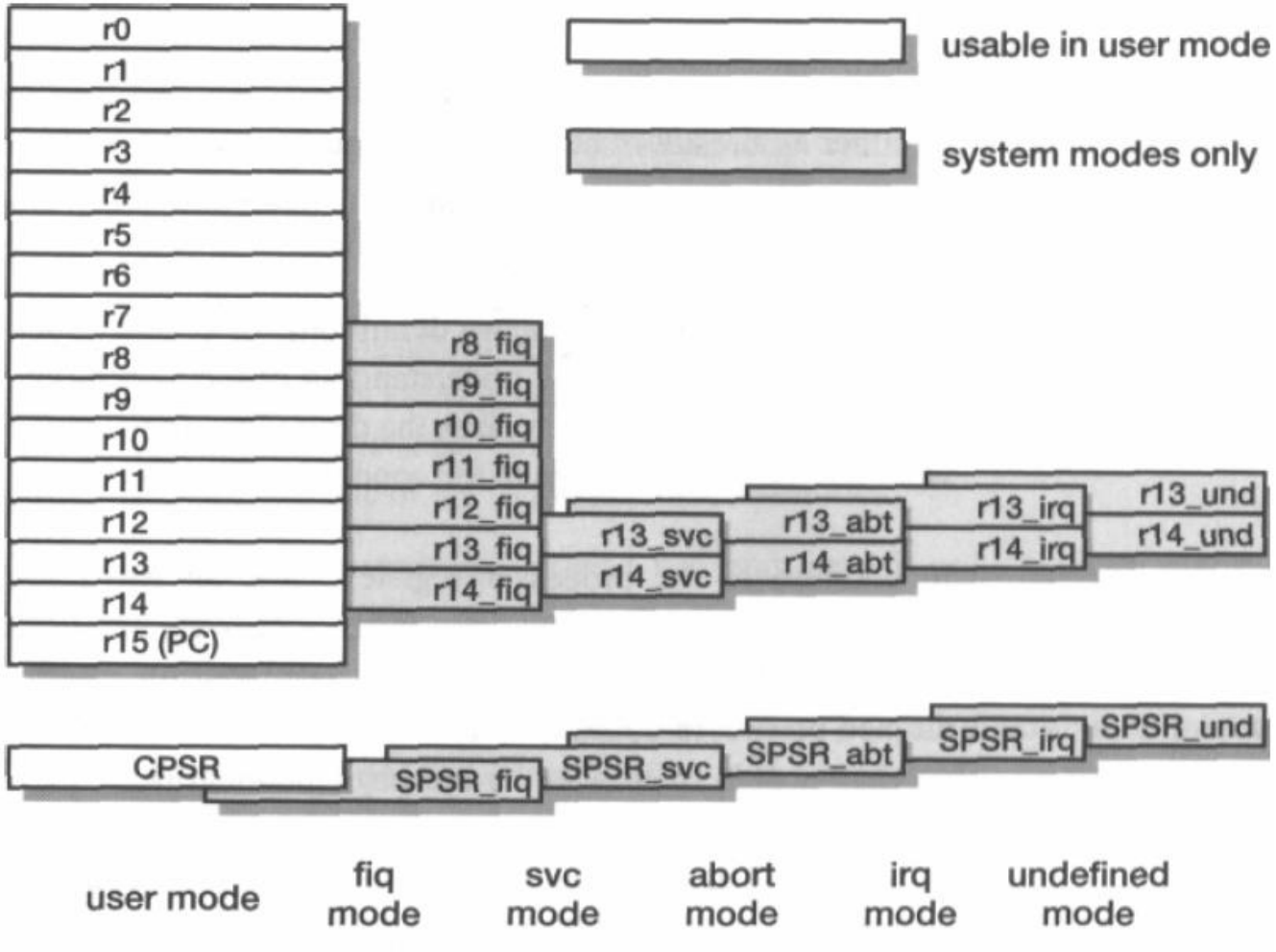
ARM Processor

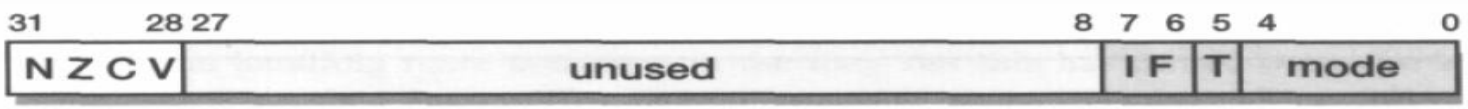
- a load-store architecture (Data processing instructions, data transfer instructions, control flow instructions)
- fixed-length 32-bit instructions;
- 3-address instruction formats.
- Register windows—Sixteen 32 bit registers. Shadow registers are used for exceptions
- Delayed branches --- Not used in ARM
- Single cycle instructions: Some are multi cycle instructions

ARM Architecture features

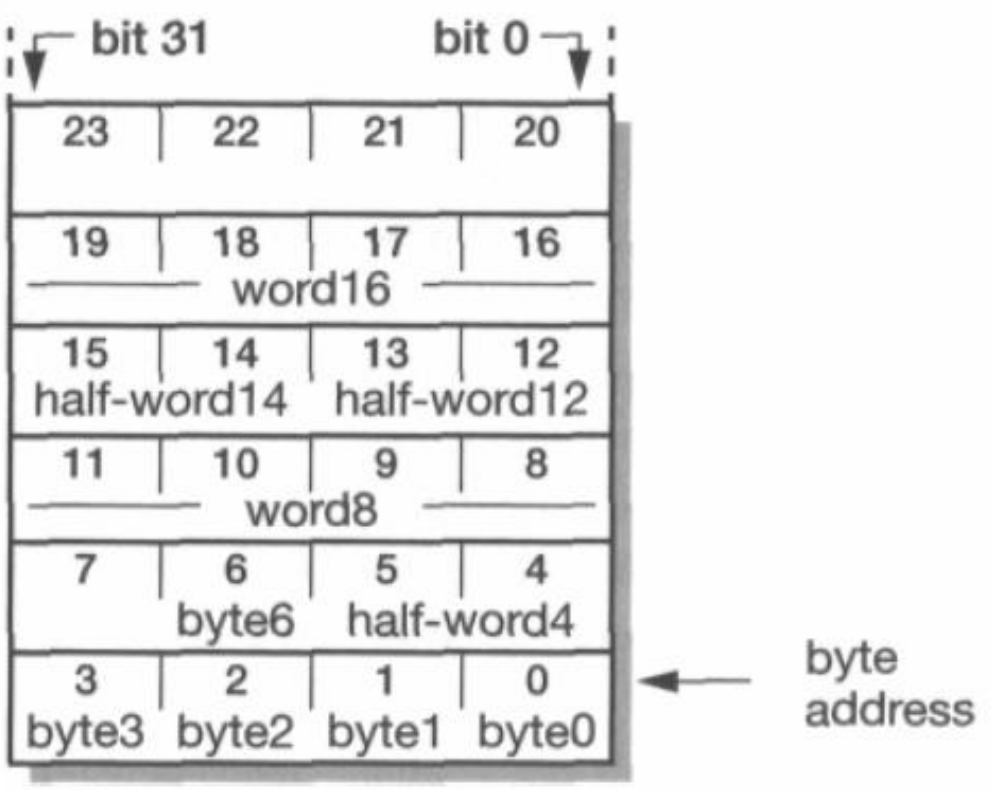
- conditional execution of every instruction;
- the inclusion of very powerful load and store multiple register instructions;
- the ability to perform a general shift operation and a general ALU operation in a single instruction that executes in a single clock cycle;
- open instruction set extension through the coprocessor instruction set, including adding new registers and data types to the programmer's model;
- a very dense 16-bit compressed representation of the instruction set in the Thumb architecture.

ARM Programmers Model





ARM Memory Organization



ARM Exceptions

- User
- FIQ
- IRQ
- Supervisor
- Abort
- Undefined
- System

Exceptions result in current PC stored in R14_exc and CPSR in SPSR_exc
R13_exc points the stack memory where register contents can be stored.

On return to user program, stack contents are restored before restoring PC and CPSR contents

ARM Development Tools