Embedded Systems

Dr. Sajesh Kumar U

Module 2 : Embedded system interfacing and peripherals (06 Hours)

- Communication devices

Serial Communication Standards and Devices - UART, HDLC and SPI. Serial Bus Protocols -I2C Bus, CAN Bus and USB Bus. Parallel communication standards ISA, PCI and PCI-X Bus.

- Memory

Memory devices and systems – ROM-Flash, EEPROM,RAM-SRAM, DRAM, Cache memory, memory mapping and addresses, memory management unit– DMA .

- I/O Device

Interrupts--Interrupt sources, recognizing an interrupt, ISR – Device drivers for handling ISR, Shared data problem, Interrupt latency.

COMPLEX SYSTEMS AND MICROPROCESSORS

CHARACTERISTICS, APPLICATIONS

CHALLENGES, QUALITY ATTRIBUTES

EMBEDDED SYSTEM DESIGN PROCESS

FORMALISMS FOR SYSTEM DESIGN

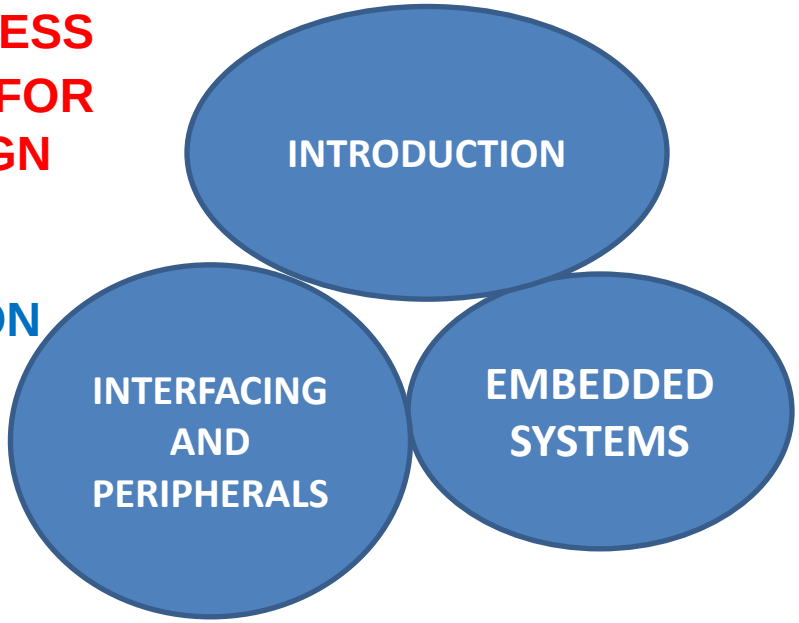
EDLC

COMMUNICATION DEVICES

MEMORY DEVICES

INPUT/OUTPUT DEVICES

INTERFACING

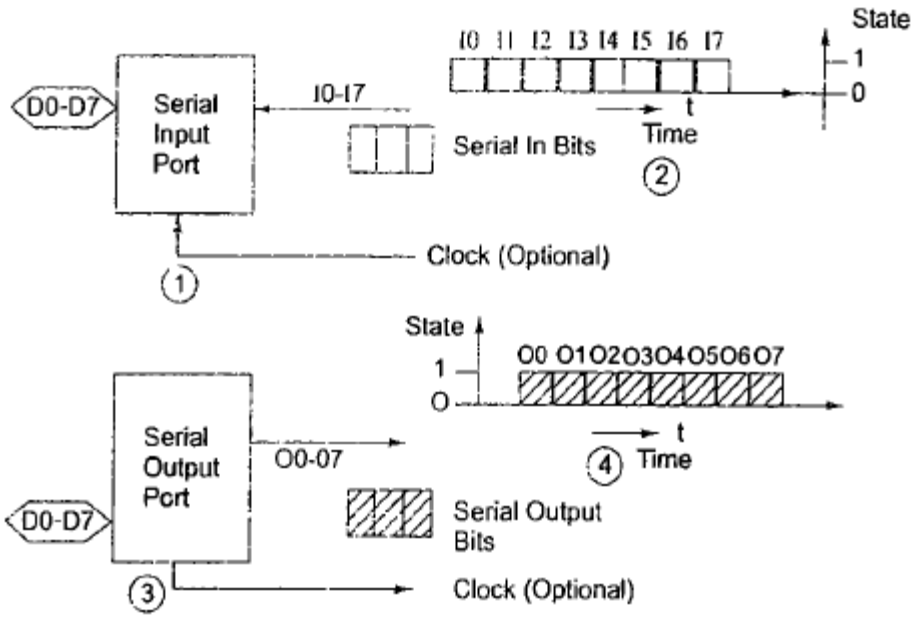


Serial and Parallel Port Communication

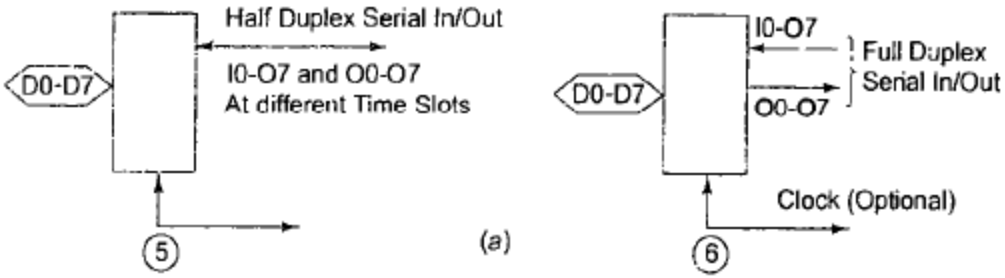
- Serial Communication: Over a given line or channel one bit can communicate
- Short or long range
- Parallel Communication: multiple bits can communicate over a set of parallel lines
- Short distance communication
- Wireless or mobile communication is serial communication

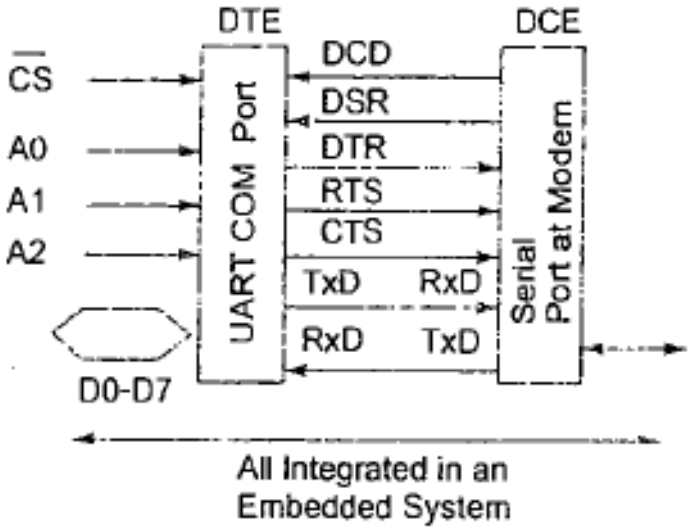
Communication Ports-Classification

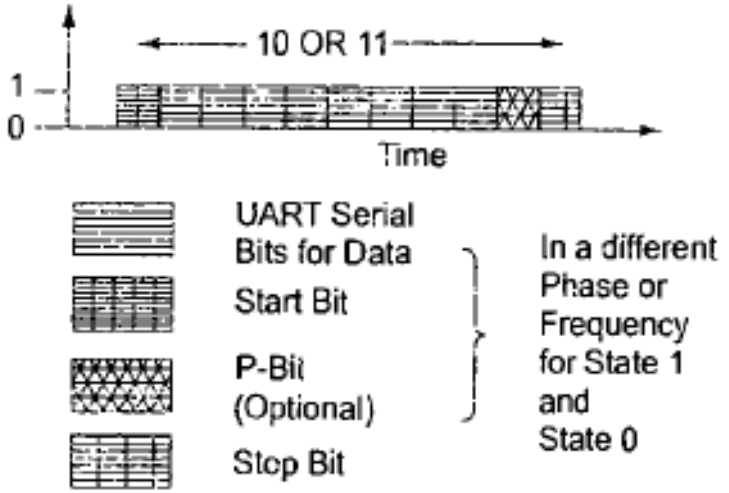
- Synchronous serial input
- Asynchronous serial input
- Synchronous serial output
- Asynchronous serial output
- Parallel port input
- Parallel port output



Half Duplex and Full Duplex

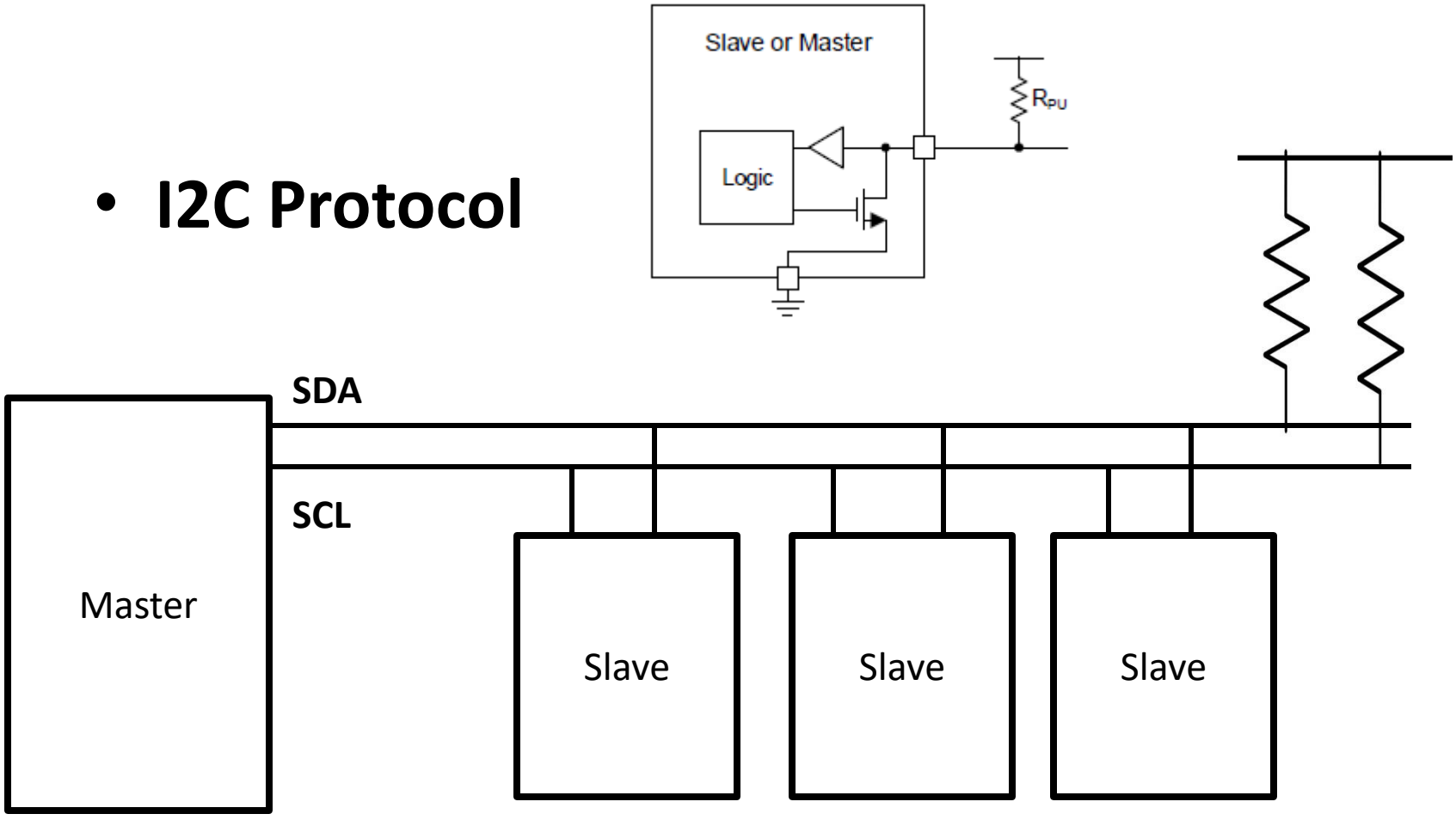




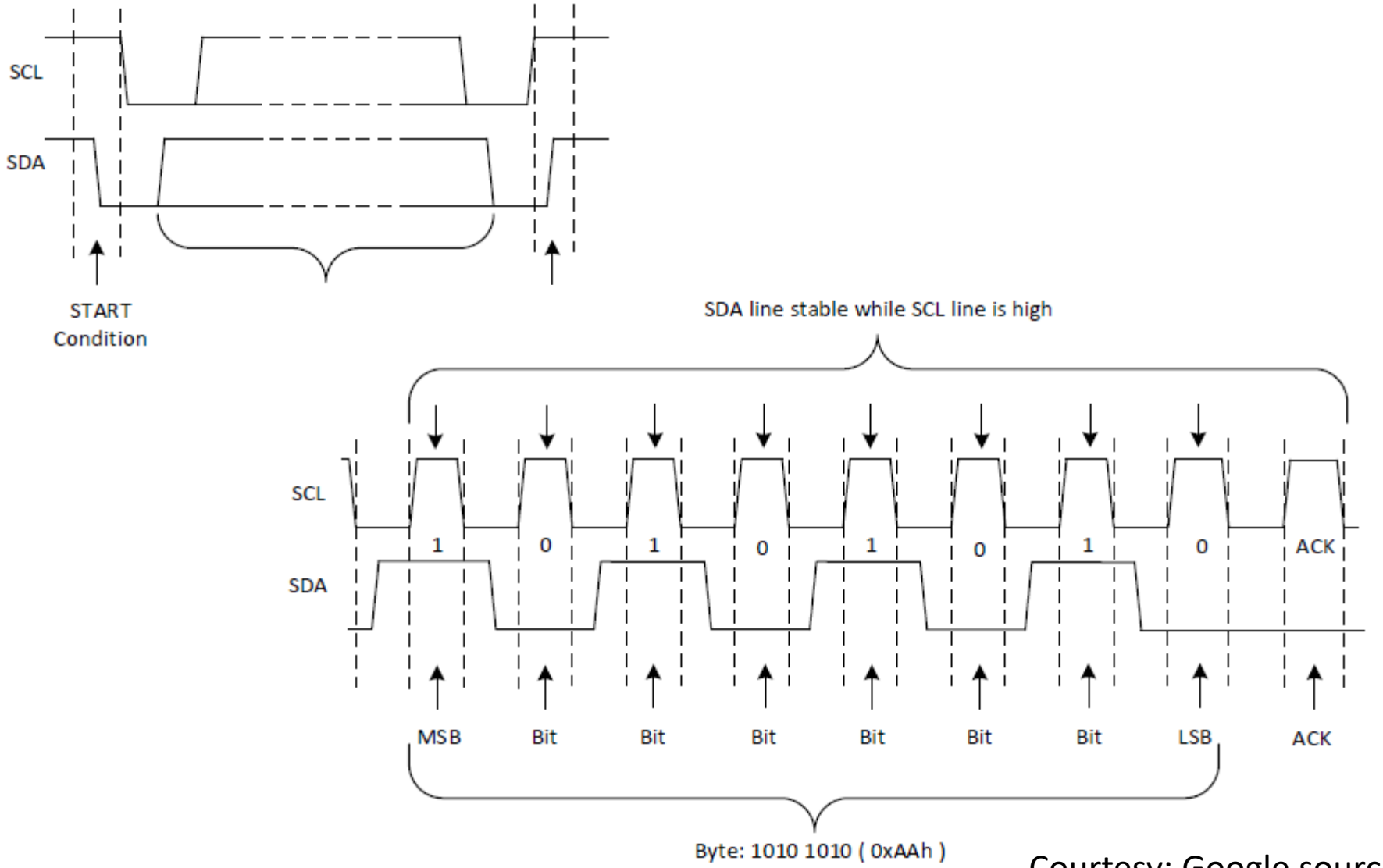


Communication Devices-I2C

- **I2C Protocol**

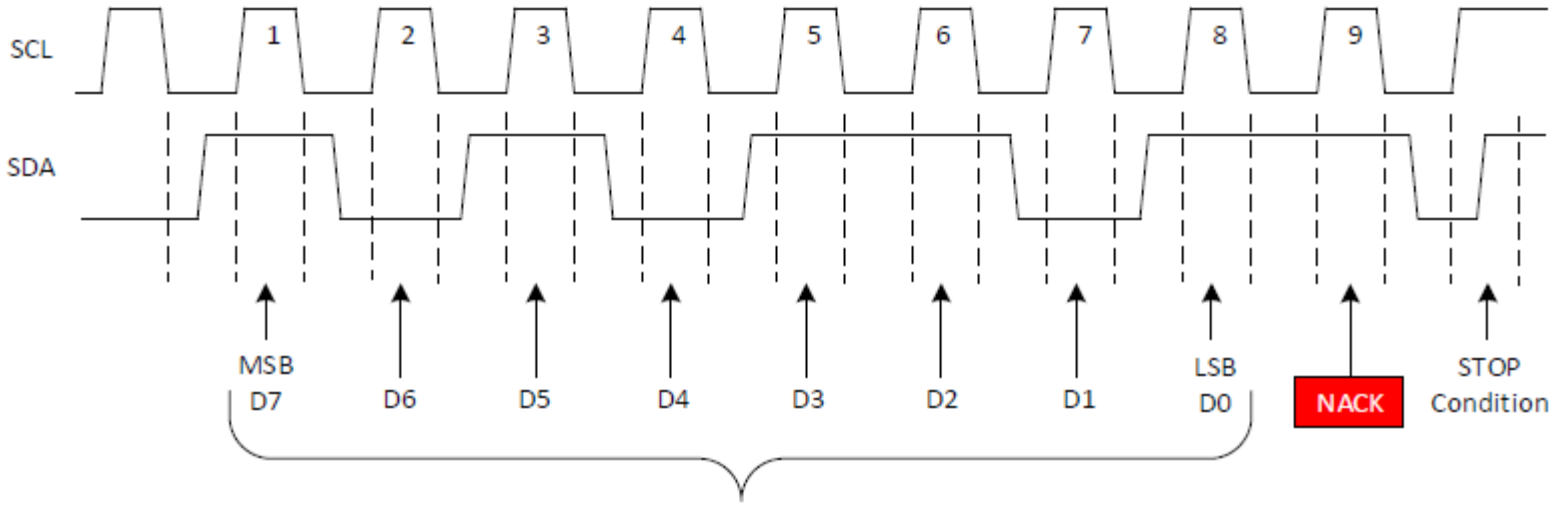


Data Transmission in I2C



Courtesy: Google sources

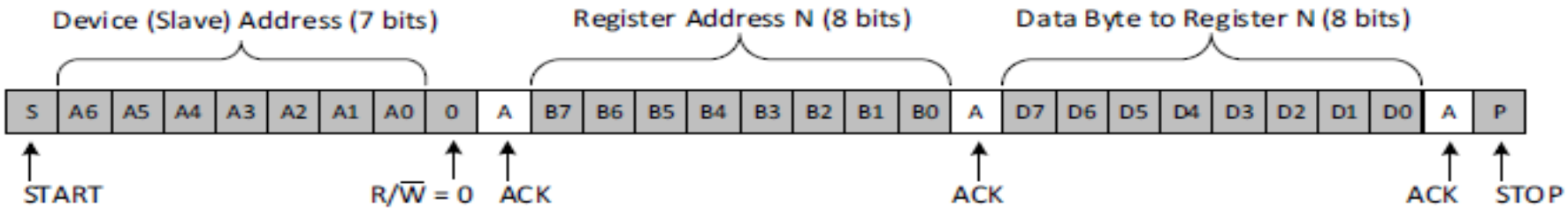
Data Transmission in I2C



Master Controls SDA Line

Slave Controls SDA Line

Write to One Register in a Device



Courtesy: Google sources

I2C Communication

- **Half-duplex Communication Protocol**
- **Synchronous Communication**
- **Can be configured in a multi-master configuration.**
- **Clock Stretching –** For slower slave devices
- **Arbitration** – The SDA and SCL are monitored by the masters. If the SDA is found low when it was supposed to be high it will be inferred that another master is active and hence it stops the transfer of data.
- **Serial transmission –** I2C uses serial transmission for transmission of data.
- **Used for low-speed communication**. 100kbps to 3.4mbps

I2C Communication

Advantages :

- Can be configured in multi-master mode.
- Complexity is reduced because it uses only 2 bi-directional lines
- Low Cost.
- ACK/NACK feature for error handling.

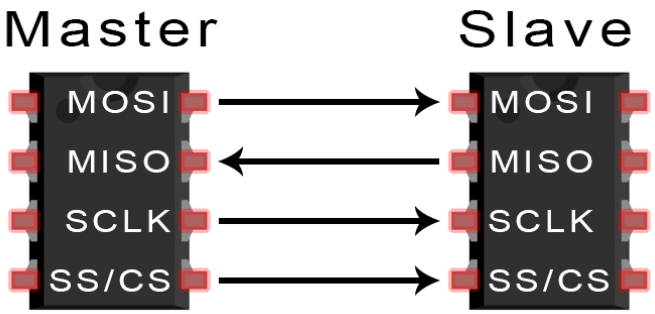
Limitations :

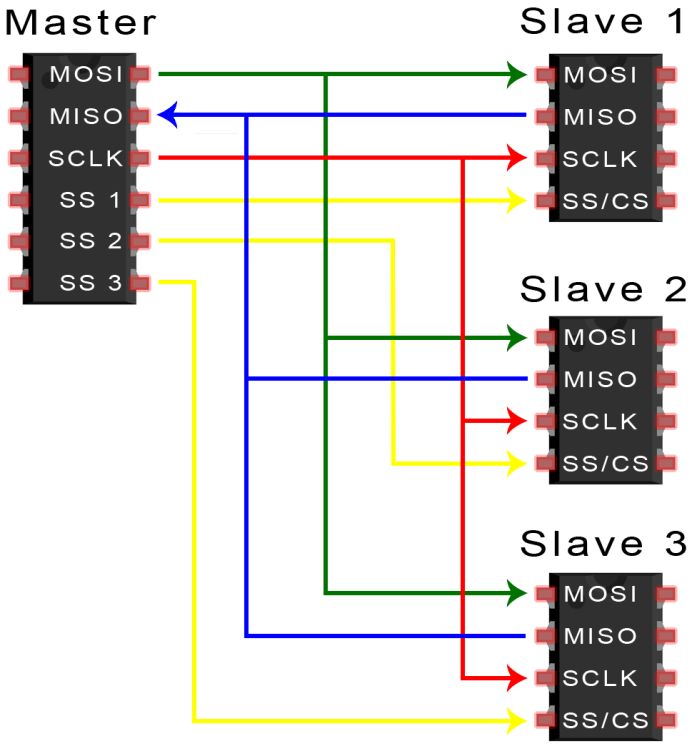
- Slower speed.
- Half-duplex communication is used in the I2C communication protocol.

SPI Communication

Serial Peripheral Interface

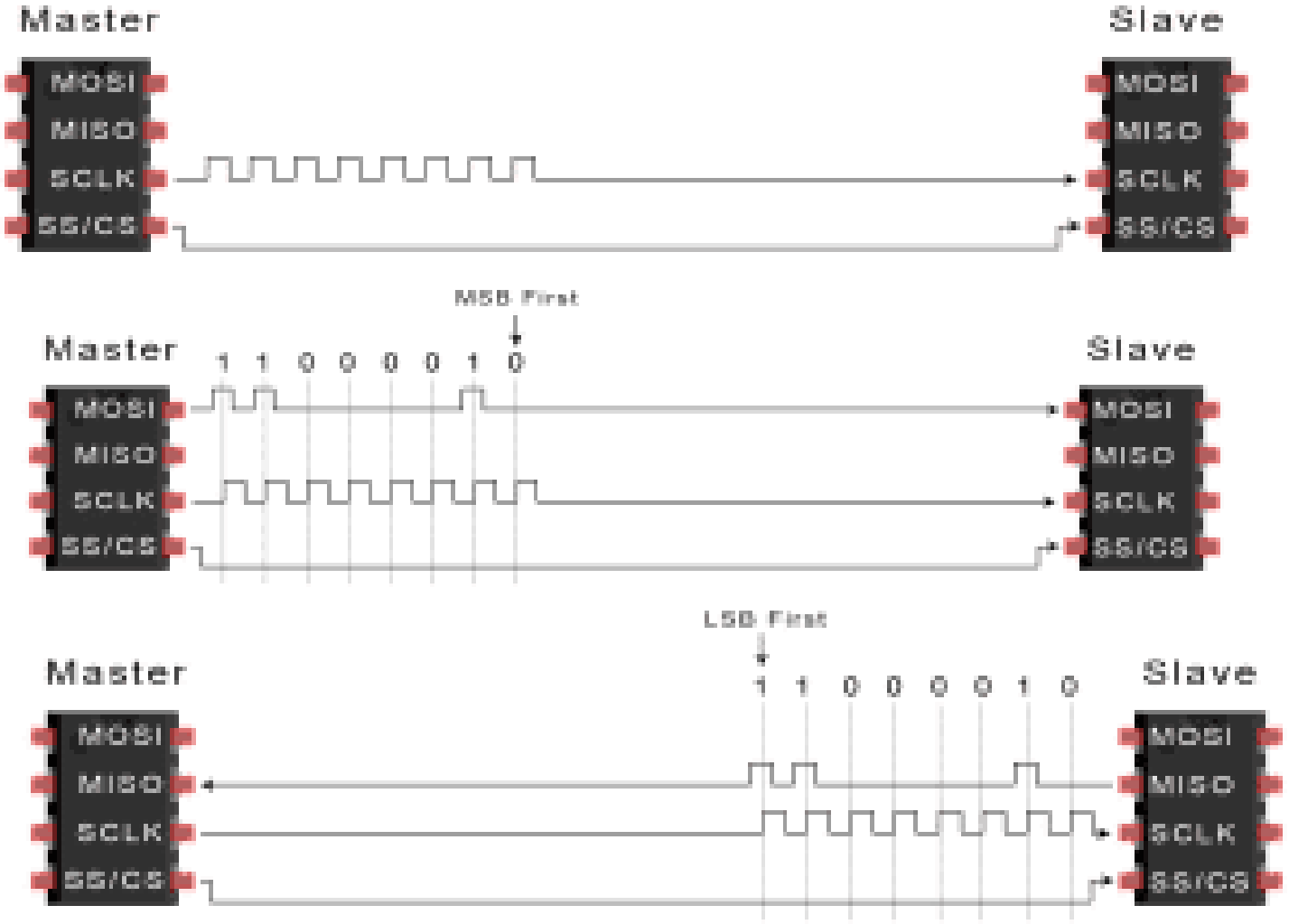
- MOSI: Master O/P slave I/P
- MISO: Master I/P slave O/P
- SCLK: Serial Clock
- SS: Slave Select





Courtesy: Google sources

SPI Communication



Courtesy: Google sources

SPI Communication

ADVANTAGES

- No start and stop bits, so the data can be streamed continuously without interruption
- No complicated slave addressing system like I2C
- Higher data transfer rate than I2C (20mbps)
- Separate MISO and MOSI lines, so data can be sent and received at the same time

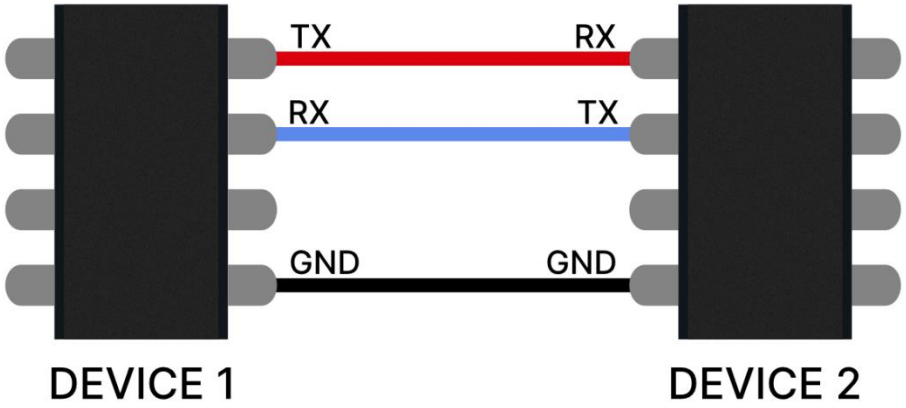
DISADVANTAGES

- Uses four wires (I2C and UARTs use two)
- No acknowledgement that the data has been successfully received (I2C has this)
- No form of error checking like the parity bit in UART
- Only allows for a single master

I2C vs SPI

Features	I2C	SPI
Number of wires	2(SDA,SCL)	4(MOSI, MISO, SCK,SS)
Communication type	Half Duplex	Full Duplex
Maximum number of devices	Limited by addressing scheme	Limited by number of select lines
Data transfer speed	Slower	Faster
Error handling	Improved as ACK/NACK feature	Not as robust
Cost	Less	More
Complexity	Simple	Complex
Multi master configuration	Yes	Yes
Synchronous Communication	Yes	Yes
Clock stretching	Yes	No
Arbitration	Yes	No

UART Communication



Courtesy: Google sources

Baud Rate

- Baud rate=number of bits/second
- For a UART frame with 1 start bit and 1 stop bit, the total bits/frame is 10 bits
- Baud rate of 9600bits/second means 960 frames/second are transmitted.
- Actual bytes transmitted/second is 960 bytes or 7680 bits

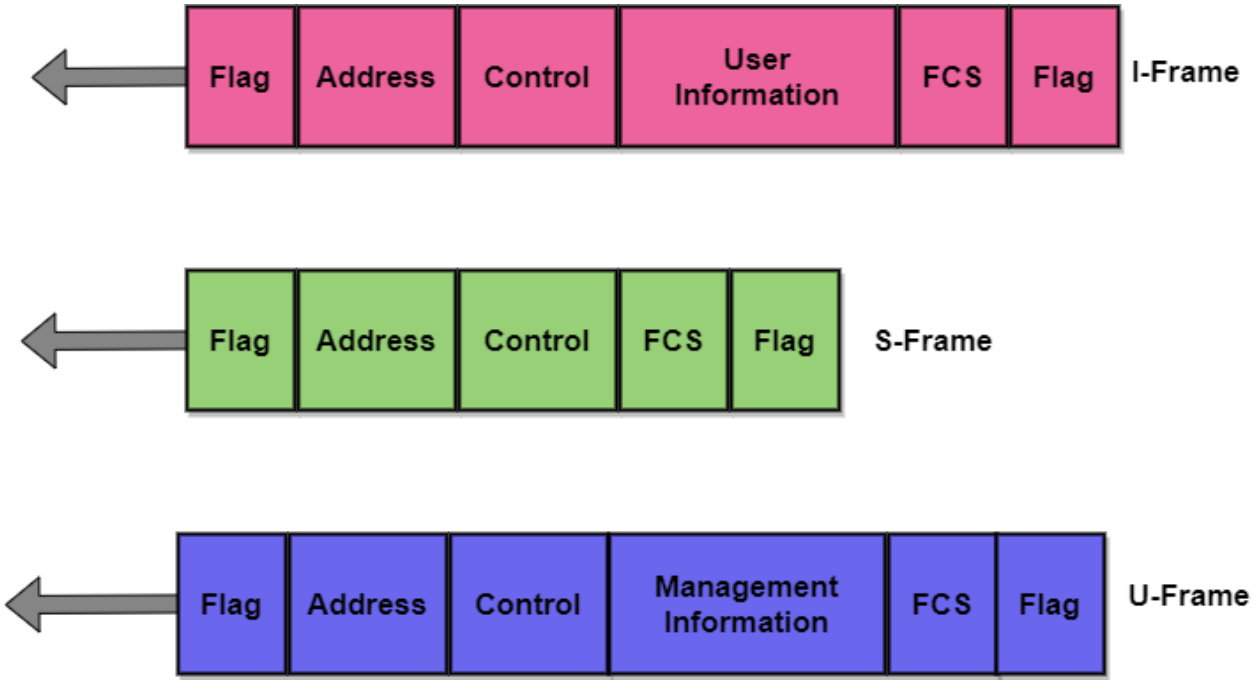
UART Communication

- **Advantages**
  - Uses only two wires
  - Clock signal is not necessary
  - Parity bit enables checking for errors
  - Costs less and is smaller than parallel communication
  - Supports the distance of about 15 meters
- **Disadvantages**
  - Data frame limited to a maximum of 9 bits
  - Doesn’t support multiple controllers and peripherals
  - Not suitable for higher data transmission rates
  - Data transfer speed lower than with parallel communication

HDLC Protocol

- **High Level Data Link Control**
- **Synchronous Serial Communication**
- **Full Duplex**

HDLC Protocol



- Flag is 01111110
- 8/16 bit address
- Information/supervisory/unnumbered frames
- Frame check sequence bits-16/32 bits

Courtesy: Google sources

HDLC Protocol

	1	2	3	4	5	6	7	8
I: Information	0	N (S)			P/F	N (R)		
S: Supervisory	1	0	S		P/F	N (R)		
U: Unnumbered	1	1	M		P/F	M		

N (S): Send Sequence Number
N (R): Receive Sequence Number
S: Supervisory Function Bits
M: Unnumbered Function Bits
P/F: Poll/Final Bit

Control Field Format

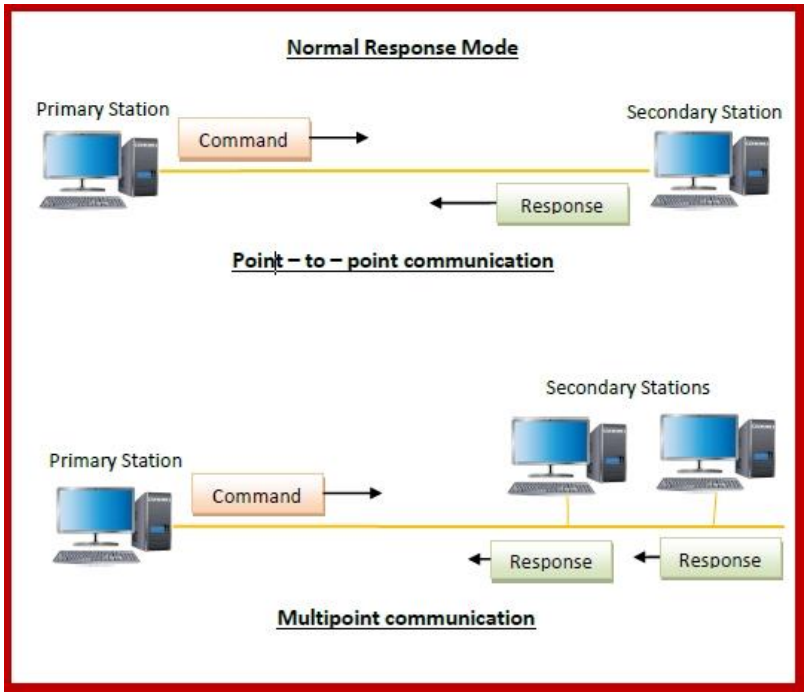
Supervisory, S=RR,RNR,REJ,SREJ

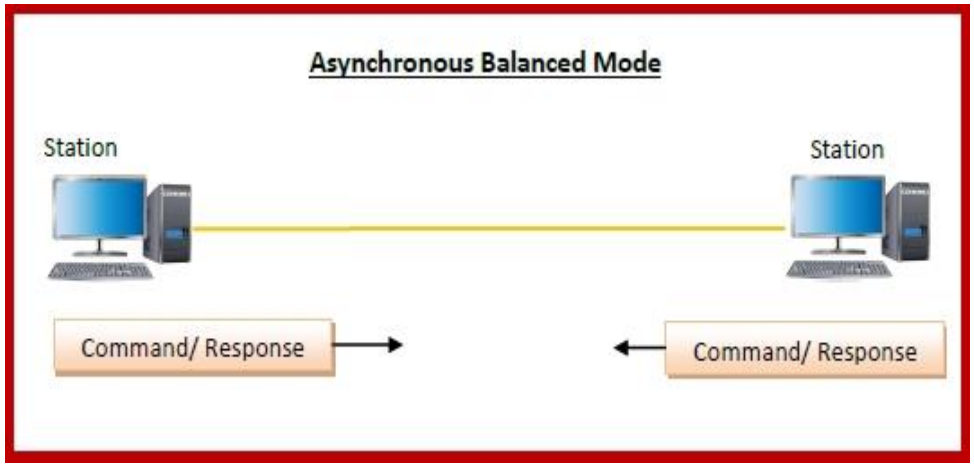
Unnumbered=Reset, Disconnect, Disconnect mode accepted, frame rejected, command rejected, unnumbered acknowledgement

Courtesy: Google sources

Modes of Communication in HDLC

- Primary station
- Secondary station
- Combined Station
- Balanced Communication
- Unbalanced Communication

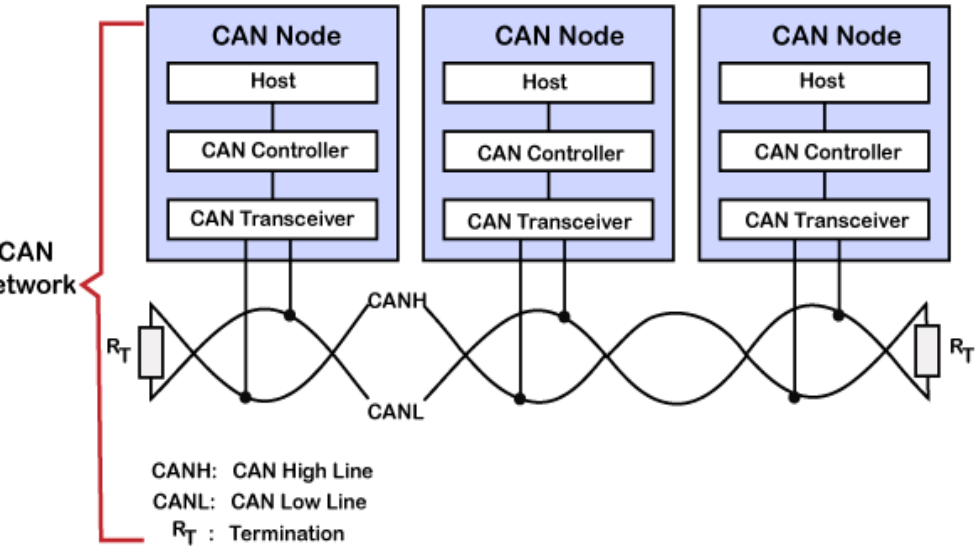


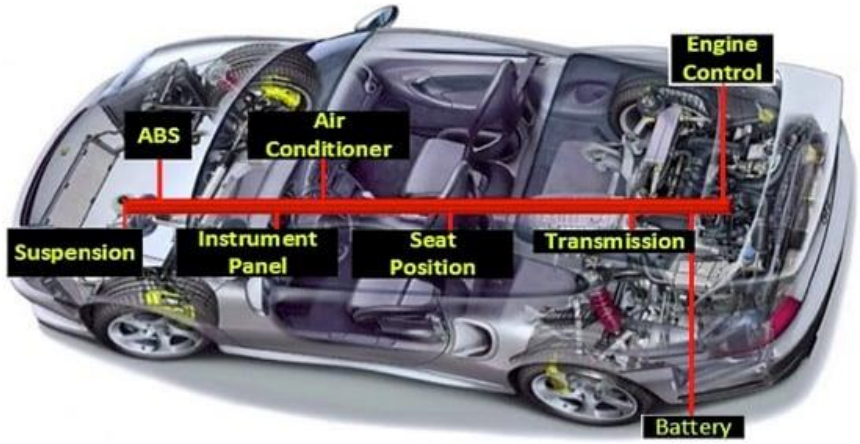


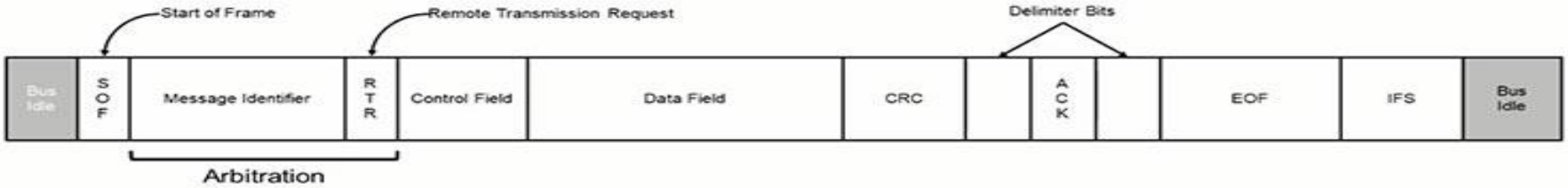
- Normal Response Mode
- Asynchronous Response Mode
- Asynchronous Balanced Mode

Courtesy: Google sources

Controller Area Network Protocol







Start of Frame – A dominant bit begins the frame and initiates arbitration

Message Identifier – 11-bit identifier used for arbitration priority

Remote Transmission Request – Indicates whether this is a data or request frame

Control Field – Specifies the length of the data to be transmitted

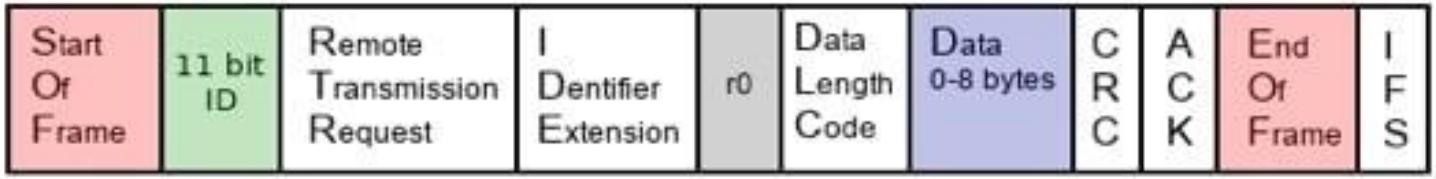
Data Field – Up to eight bytes of data

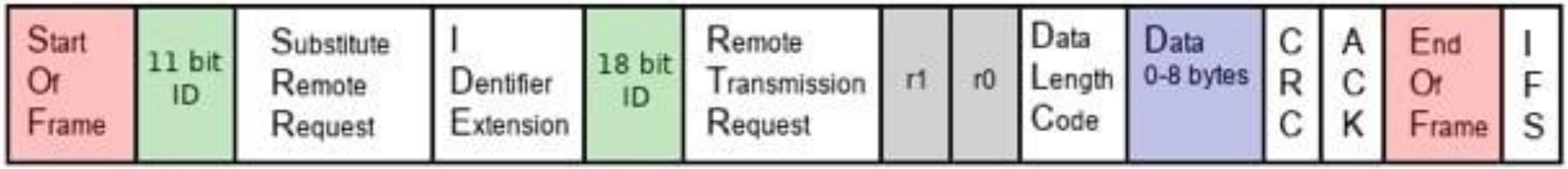
CRC Sequence – 15-bit cyclic redundancy check

ACK – Acknowledges the CRC status of receiving nodes

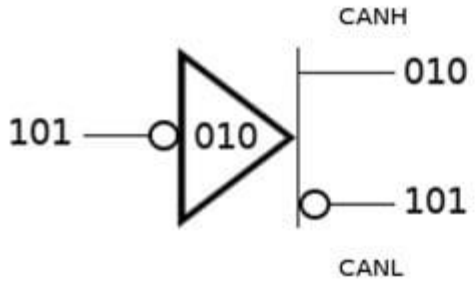
End of Frame – Marks the end of data and remote frames

Controller Area Network Protocol

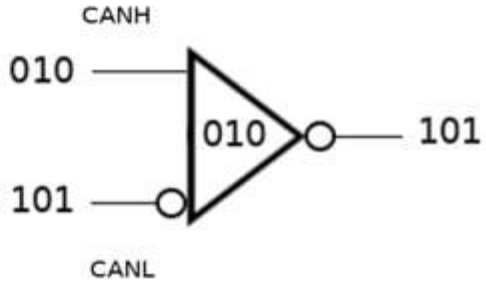




CAN Output Driver

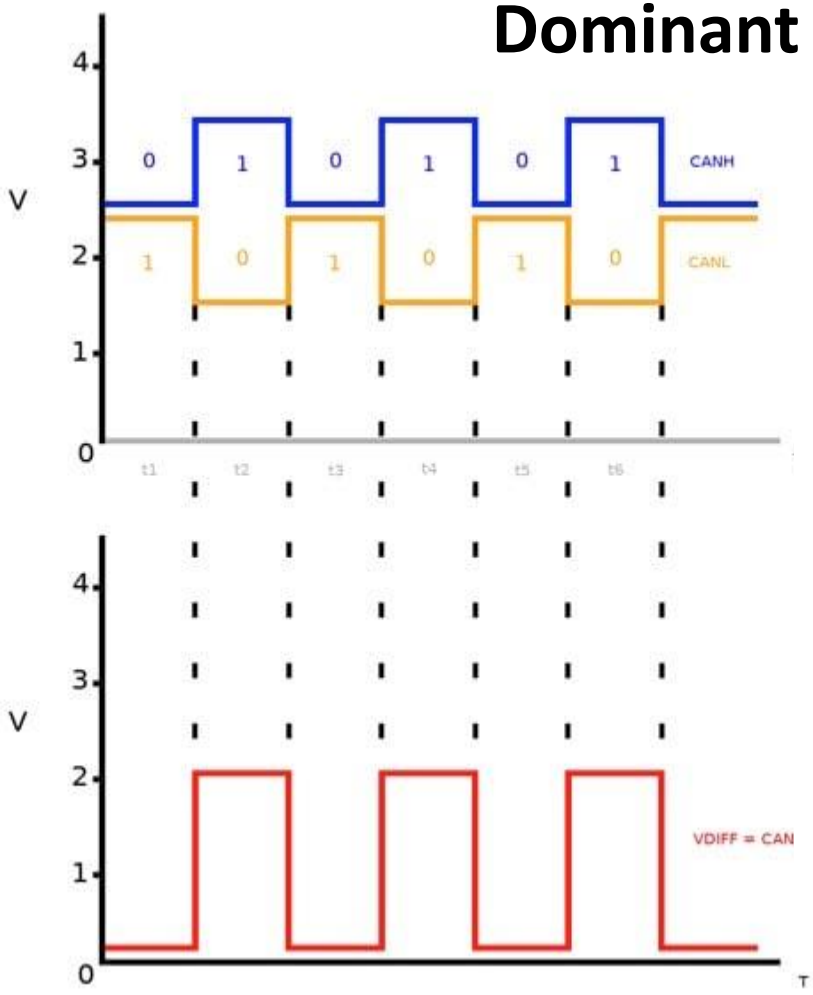


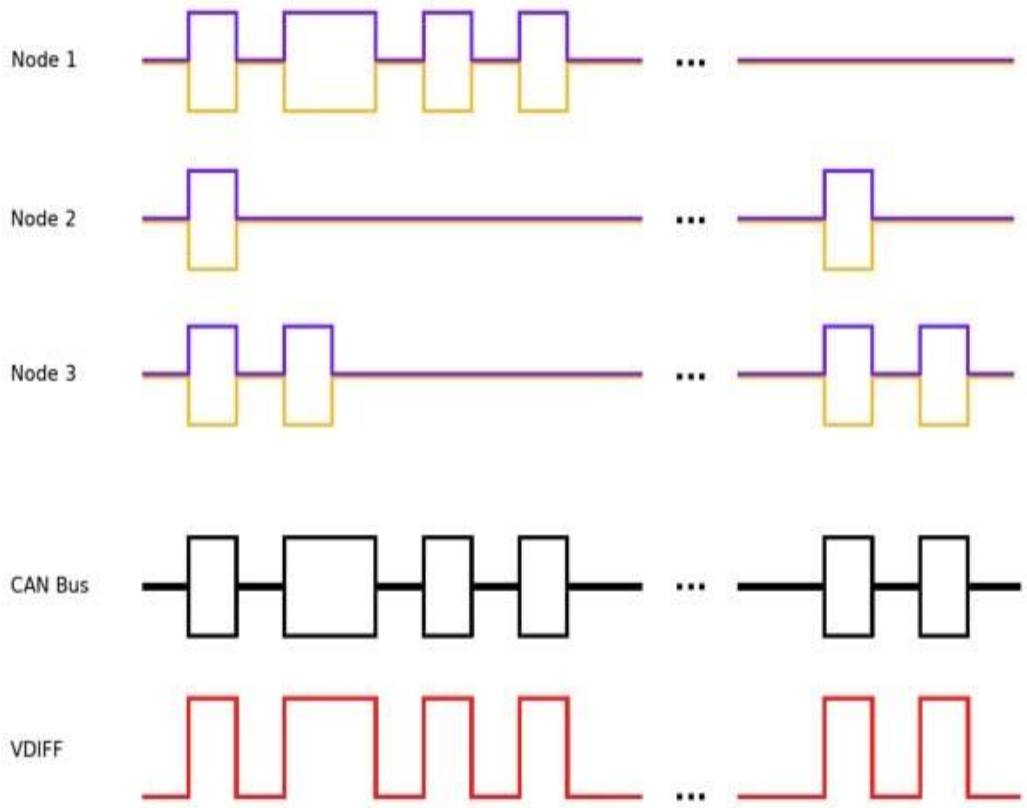
CAN Input Receiver



Controller Area Network Protocol

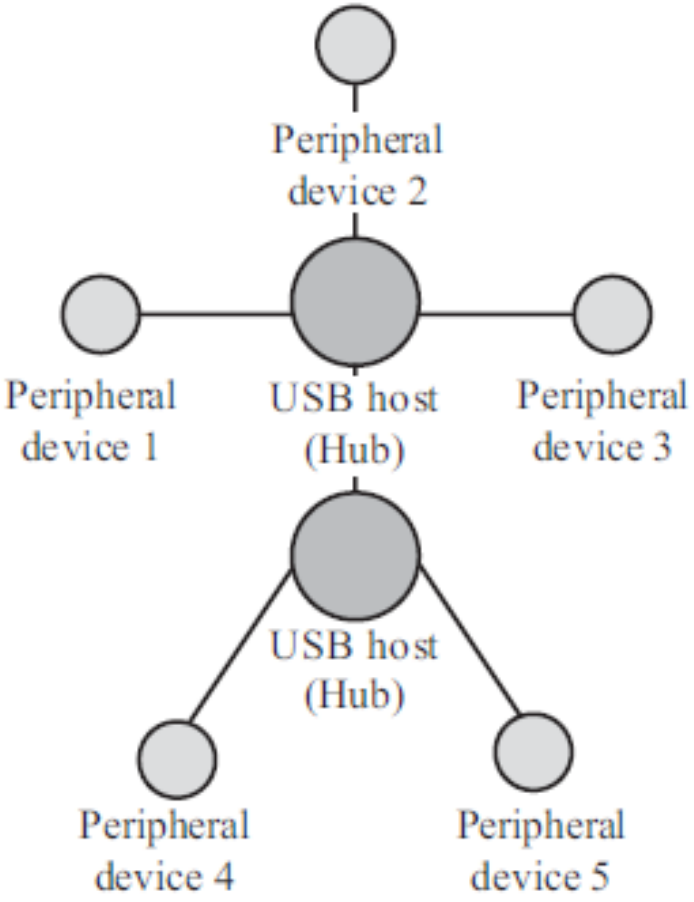
Dominant and Recessive states





USB

- USB2.0 can connect up to 127 devices
- Differential Signalling



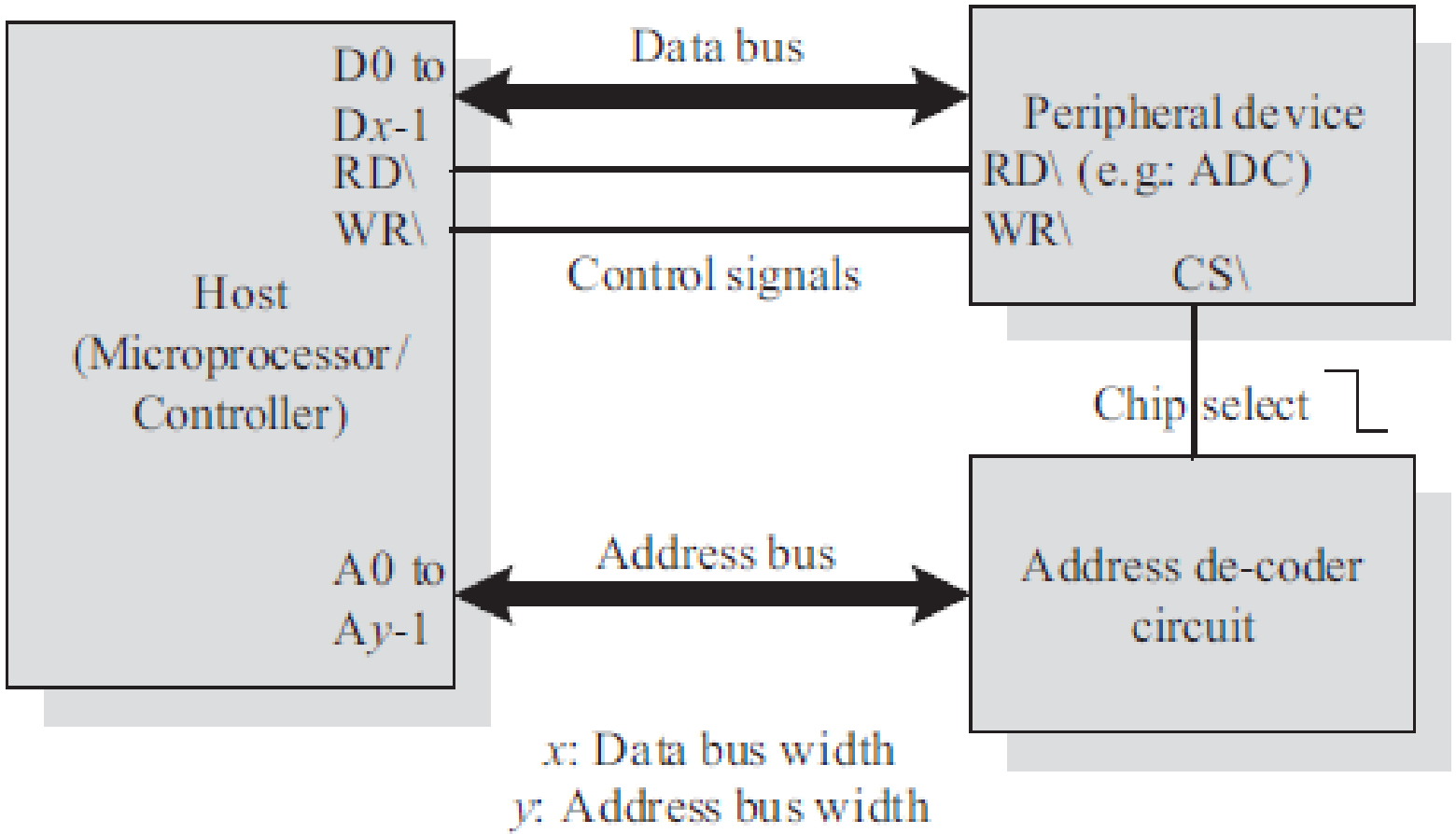
Pin no.	Pin name	Description
1	V_{BUS}	Carries power (5V)
2	D–	Differential data carrier line
3	D+	Differential data carrier line
4	GND	Ground signal line

USB

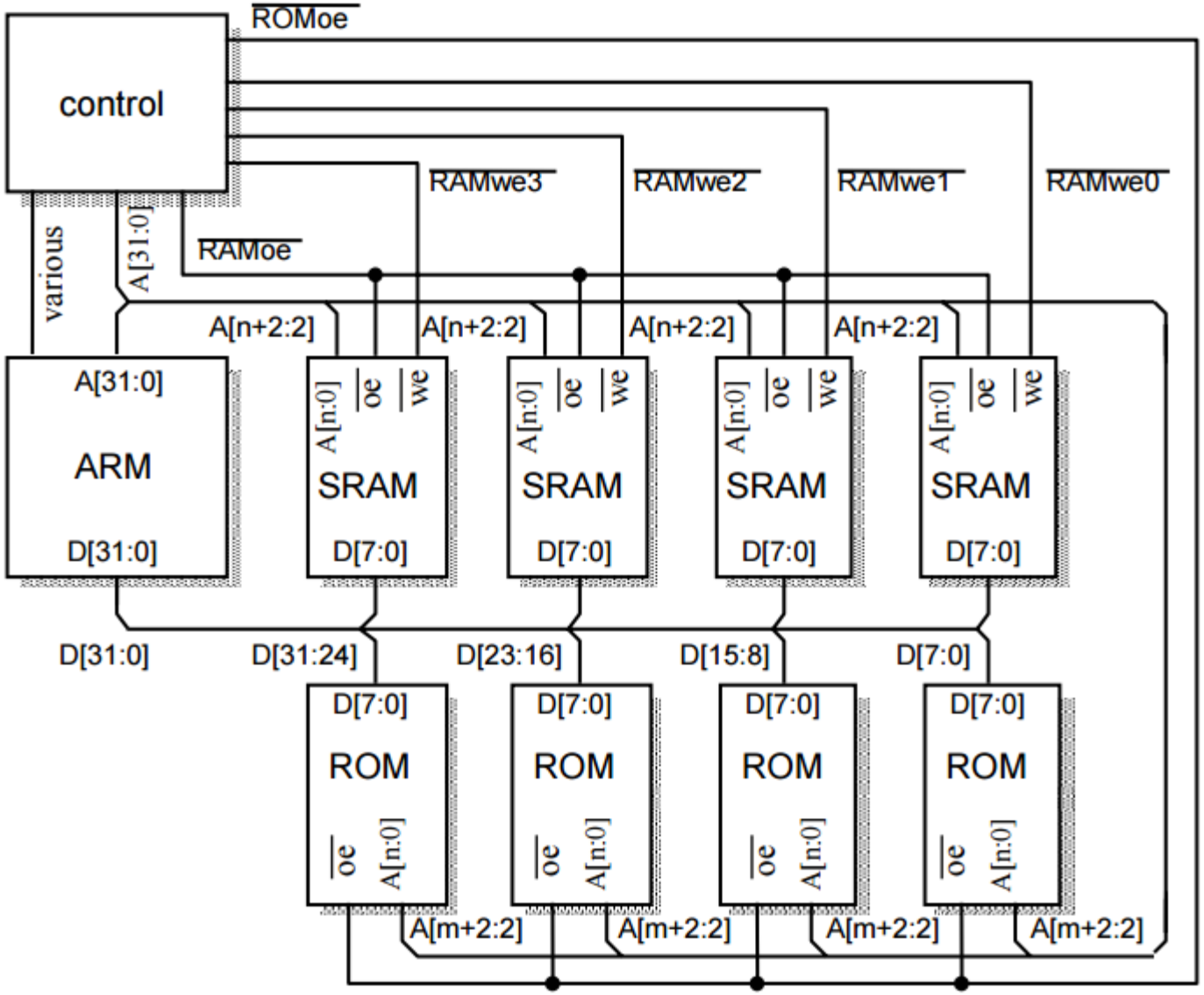
Types of USB data transfer

- Control: Query, configure, issue commands
- Bulk: Sending block of data,
- Isochronous: Real time data communication
- Interrupt: Small amount of data based on polling
- USB3.0 has a data transfer mode of super speed in which data can be send at a speed up to 4.8Gbps

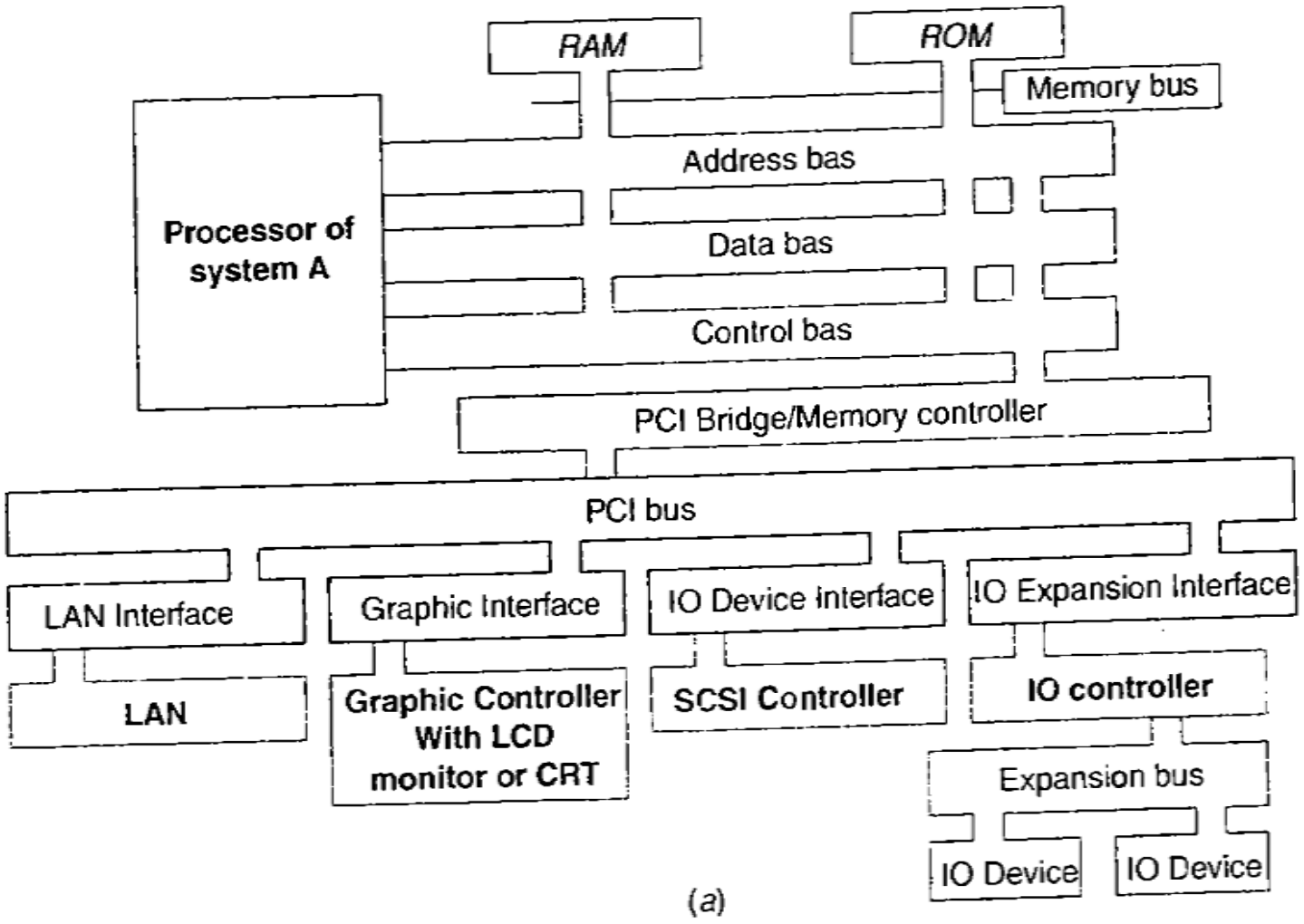
Parallel Interface



ARM Memory Interface

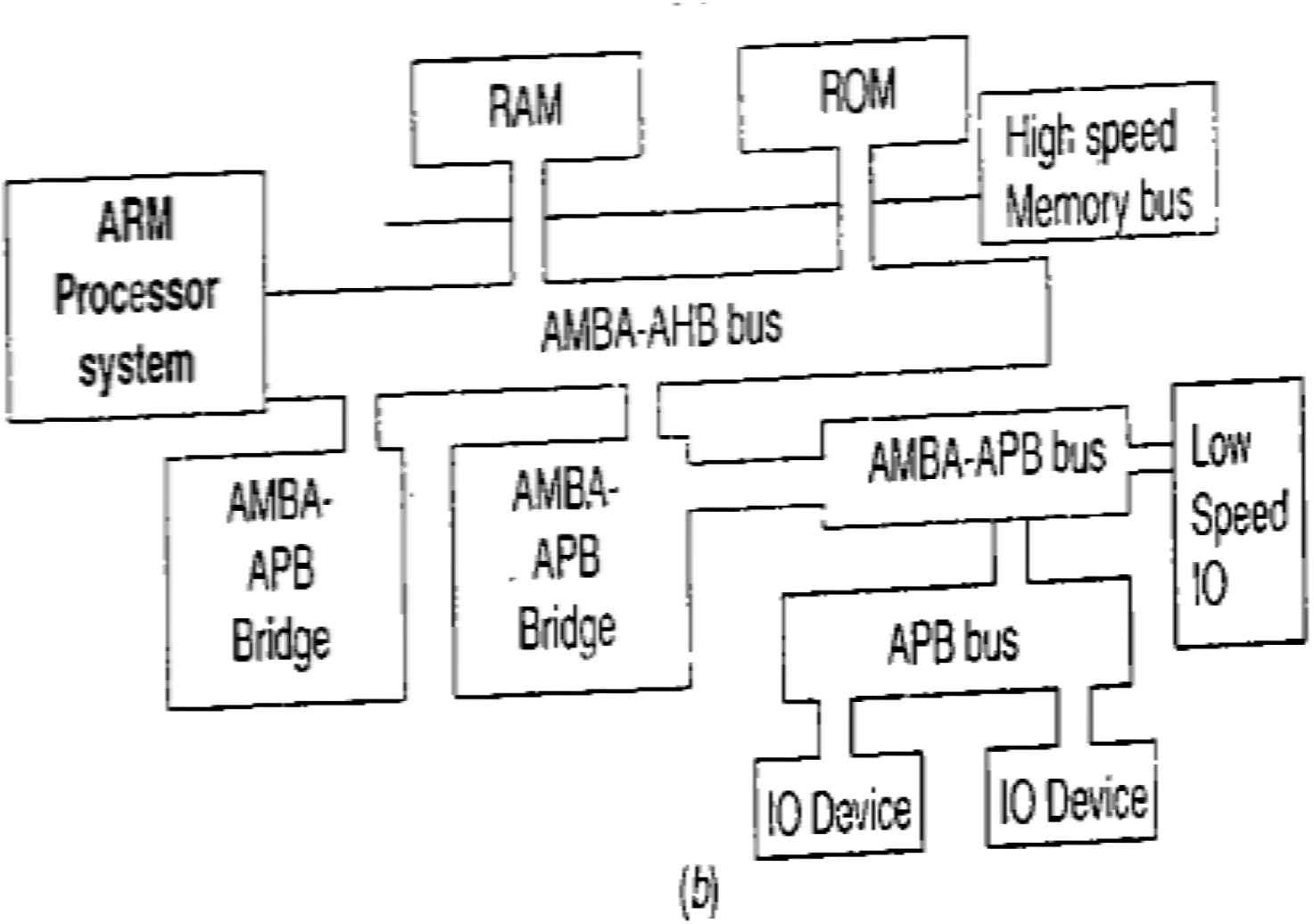


Parallel Interface-PCI Bus



(a)

Parallel Interface-AMBA Bus



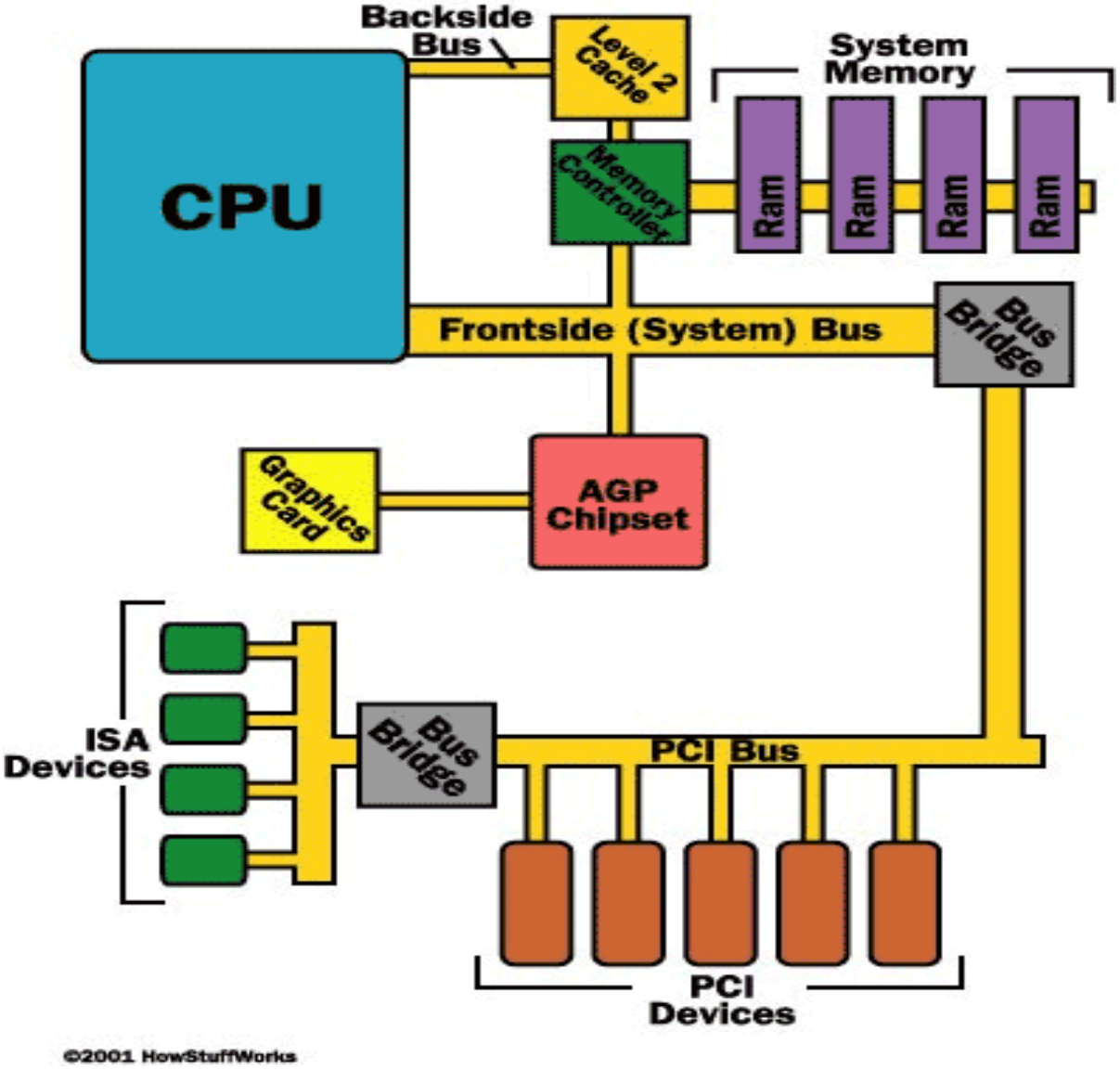
(b)

ISA

IBM **S**tandard **A**rchitecture/Industry Standard Architecture

- 8086, 80186, 80286 processors
- 16 bits at 8 MHz
- This bus design is capable of passing along data at a rate of up to 16 MBps (megabytes per second)
- ISA allows only 10bit I/O addressing using I/O mapped I/O
- Only 256 Interrupt vectors are available
- EISA is a 32bit address/data bus version of ISA
- EISA device driver first checks the EISA bus availability on Host

PCI/PCI-X


Backside Bus
Level 2 Cache
System Memory
CPU
Memory Controller
Ram
Ram
Ram
Ram
Frontside (System) Bus
Bus Bridge
Graphics Card
AGP Chipset
ISA Devices
Bus Bridge
PCI Bus
PCI Devices
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PCI/PCI-X

- Peripheral Component Interconnect
- PCI gives synchronous parallel interfaces at 32/33MHz, 64/66MHz
- PCI-X is an extension of PCI and handles 64/100MHz
- Throughput is 132/528 Mbytes/s
- Global number and device ID number are kept in PCI 16 bit registers to identify the PCI device and connects to it and assigns an address

PCI/PCI-X

- Each PCI device has 256 bytes address space allocation.
- Host identifies the address space of a device using 1. I/O port, 2. Memory locations and 3. Configuration registers
- Uniquely assigned interrupt type handles an interrupt.

Objective Type Questions

- What is the minimum number I/O line required to interface a 16-Key matrix keyboard?

  (a) 16 (b) 8 (c) 4 (d) 9

- Which is the optimal row-column configuration for a 24 key matrix keyboard?

  (a) 6 × 4 (b) 8 × 3 (c) 12 × 2 (d) 5 × 5

- What is the minimum number of interface lines required for implementing I2C interface?

  (a) 1 (b) 2 (c) 3 (d) 4

- What is the minimum number of interface lines required for implementing SPI interface?

  (a) 2 (b) 3 (c) 4 (d) 5

Objective Type Questions

- Which of the following are synchronous serial interface?

  (a) I2C (b) SPI (c) UART (d) All of these

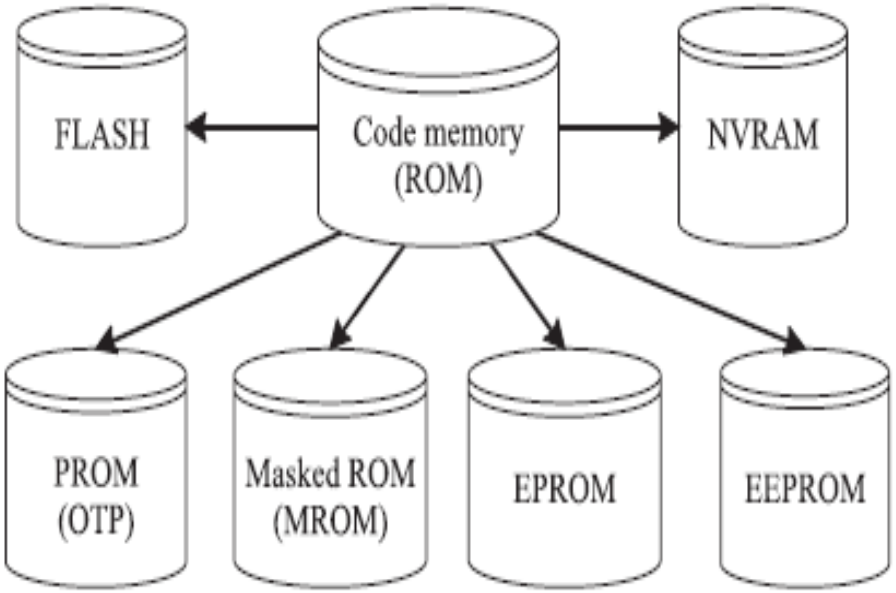
  (e) Only (a) and (b)
- RS-232 is a synchronous serial interface. State True or False

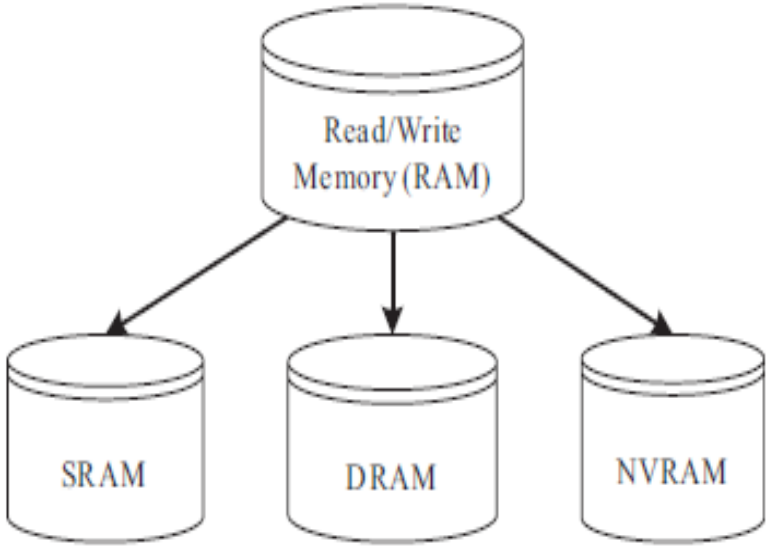
  (a) True (b) False
- What is the maximum number of USB devices that can be connected to a USB host?

  (a) Unlimited (b) 128 (c) 127 (d) None of these

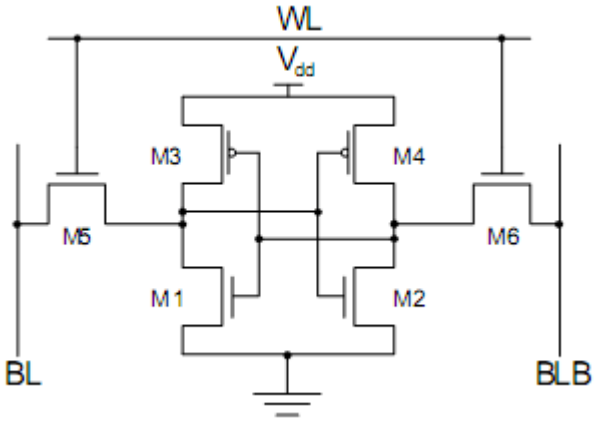
Memory

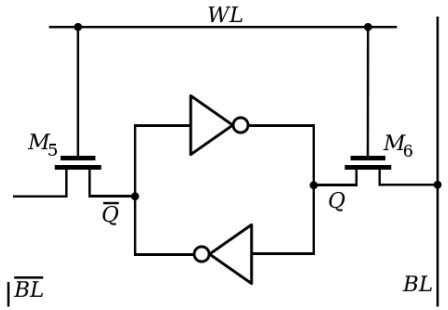
- **Program Memory**
- **Data Memory**

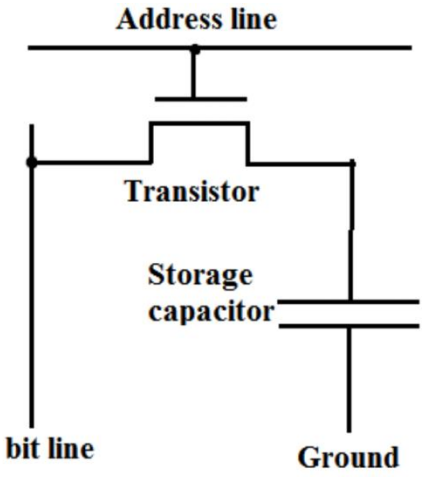




SRAM



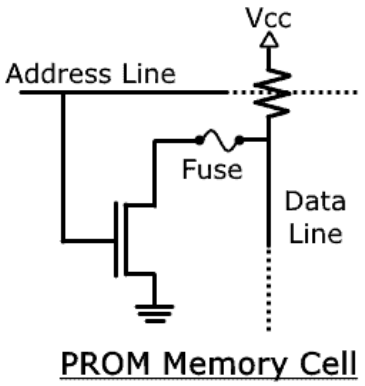




SRAM	DRAM
6 transistors cell	1 Transistor and 1 capacitor
Do not require refreshing	Require refreshing
Low capacity (less dense)	High capacity (highly dense)
More expensive	Less cost
Fast operation. Typical access time is 10ns	Slow in operation. Typical access time is 60ns.

ROM

- MROM: one time programmable in fab
- PROM: one time programmable in field
- EPROM: UV erasable and reprogrammable
- EEPROM: Electrically erasable
- FLASH: EEPROM in NAND/NOR style
- NVRAM: RAM with backup battery



PROM Memory Cell

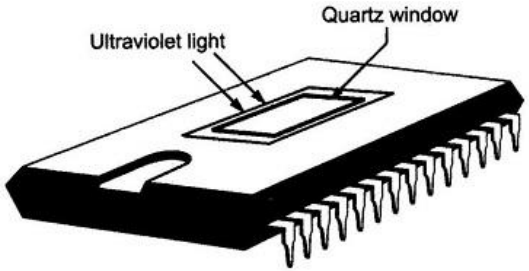
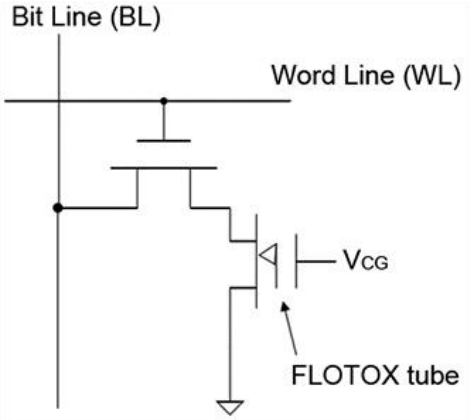
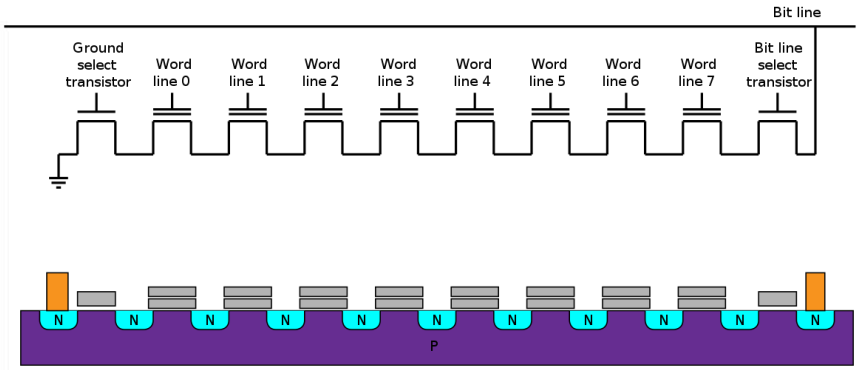


Fig. 3.72 EPROM

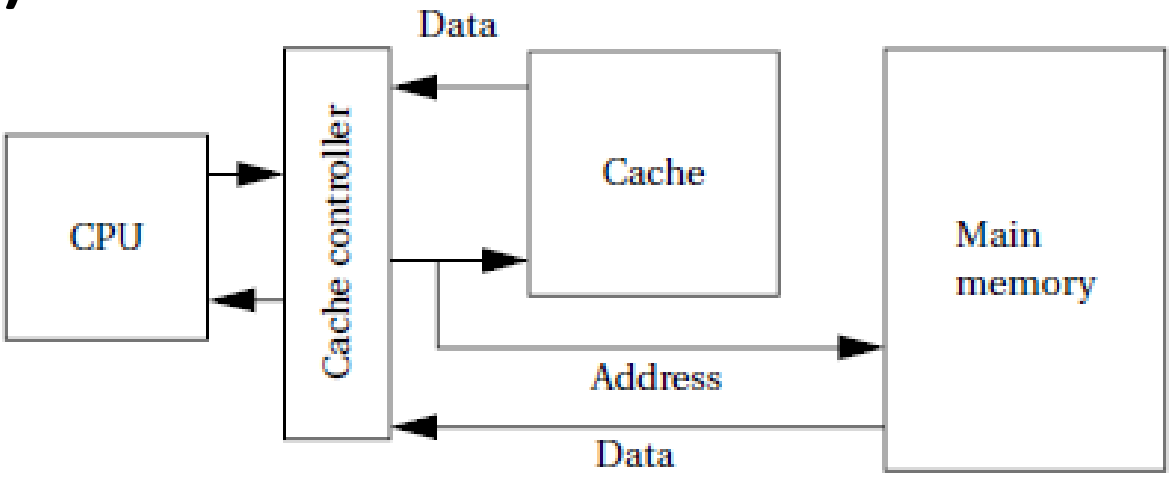


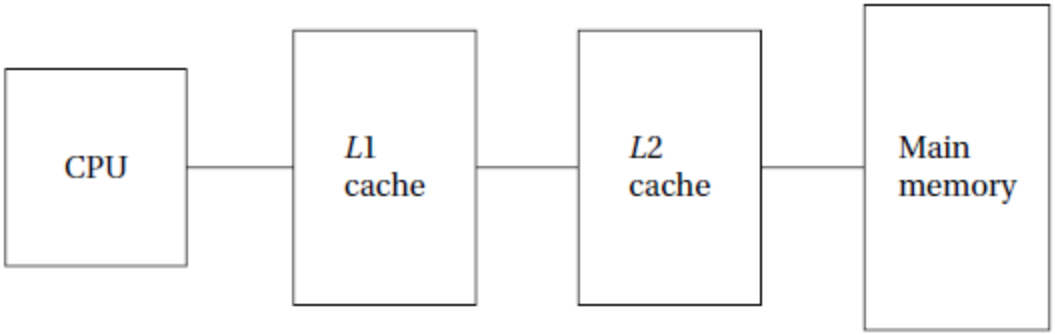


Cache Memory

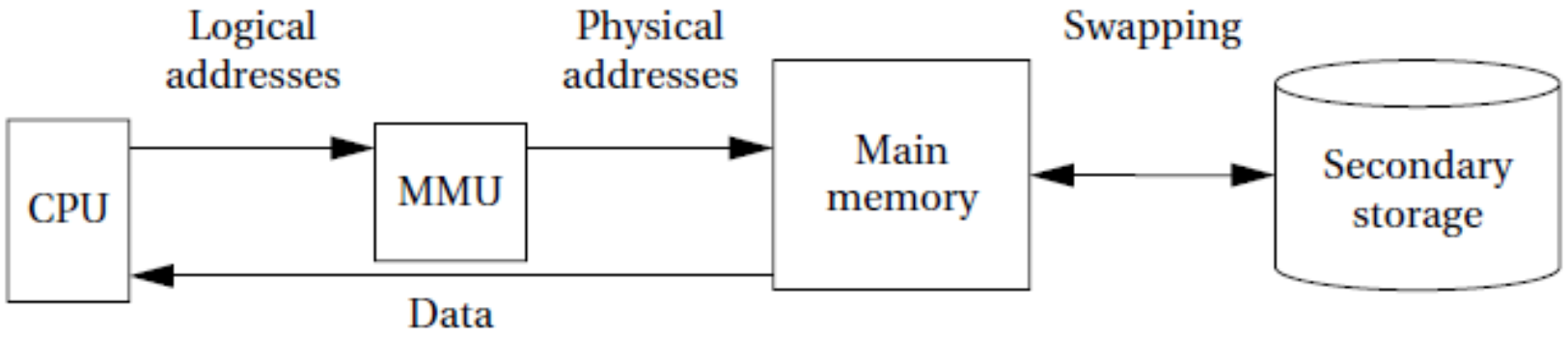
Cache memory-----HIT/MISS

Tave=h*tcah+(1-h)*tmem





Memory Management



- Logical addresses
- Physical addresses
- Virtual Memory
- Page fault
- Required memory has been read back into the main memory
- MMUs table has been updated to reflect the changes

Segmentation and Paging