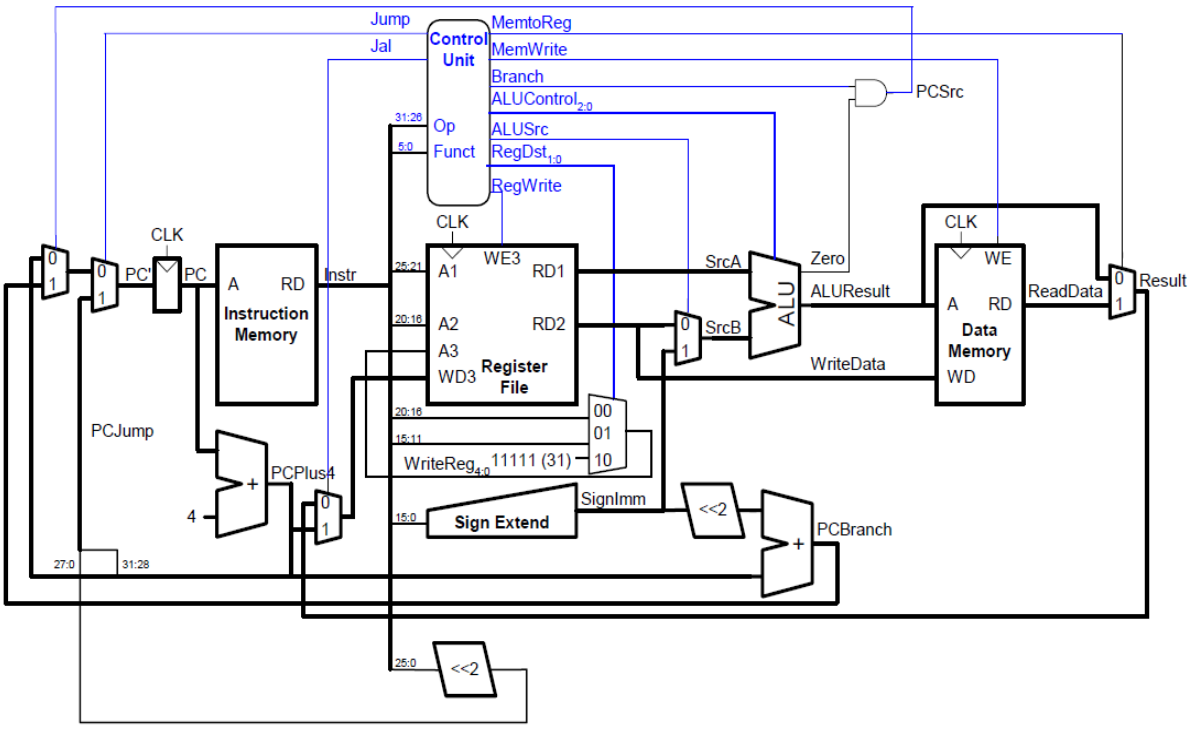
Lab 10: Implement a RISC single Cycle Processor (Logic-sim)

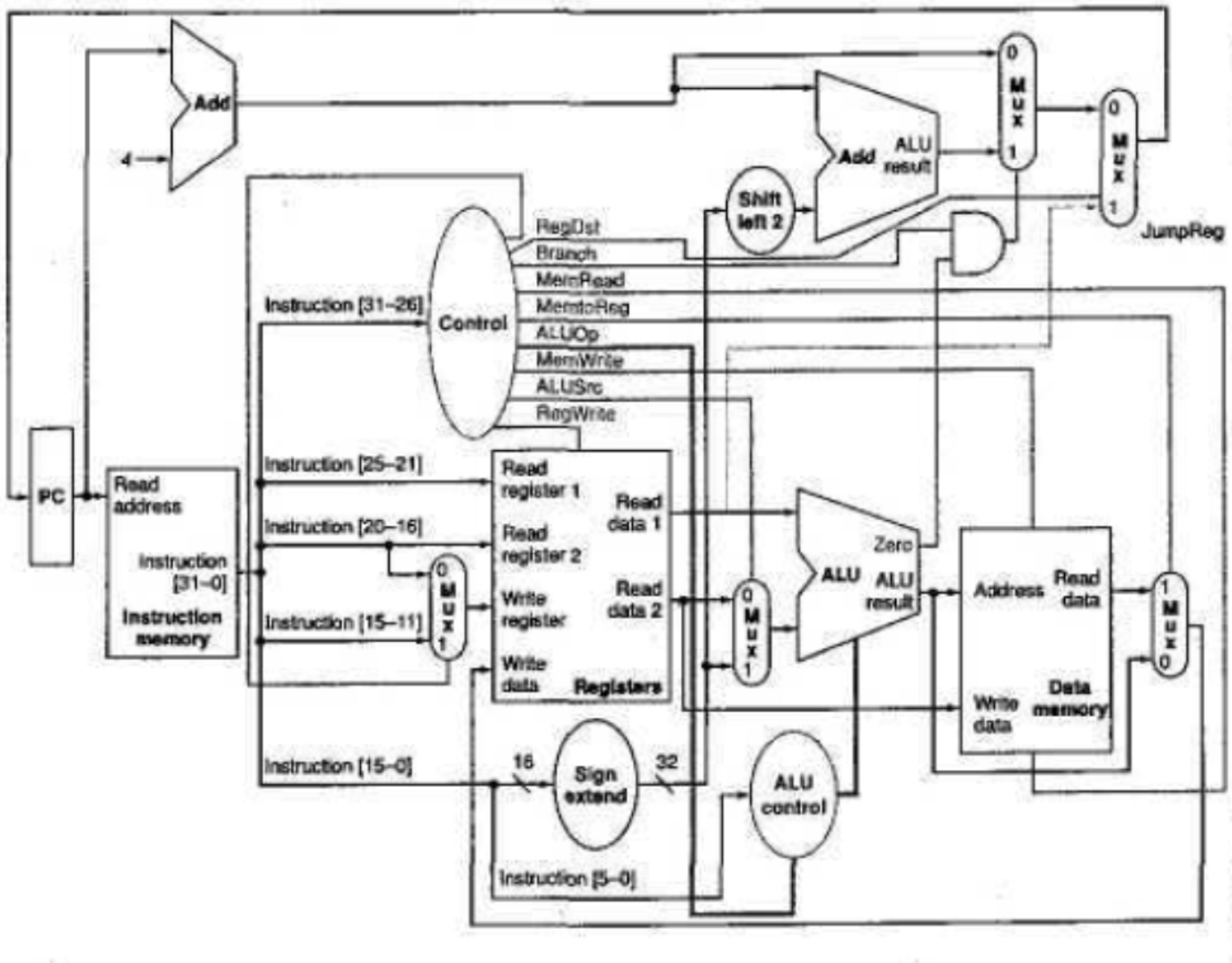
Task 1: Using blocks (lab 8/lab9) extend single cycle, implement single cycle processor RISC which could run jal and jr. Test these instructions in the sample code given.

Hints:

instruction	opcode	regwrite	regdst	alusrc	branch	memwrite	memtoreg	aluop	jump	jal
R-type	000000	1	01	0	0	0	0	10	0	0
lw	100011	1	00	1	0	0	1	00	0	0
sw	101011	0	XX	1	0	1	X	00	0	0
beq	000100	0	XX	0	1	0	X	01	0	0
addi	001000	1	00	1	0	0	0	00	0	0
j	000010	0	XX	X	X	0	X	XX	1	0
jal	000011	1	10	X	X	0	X	XX	1	1

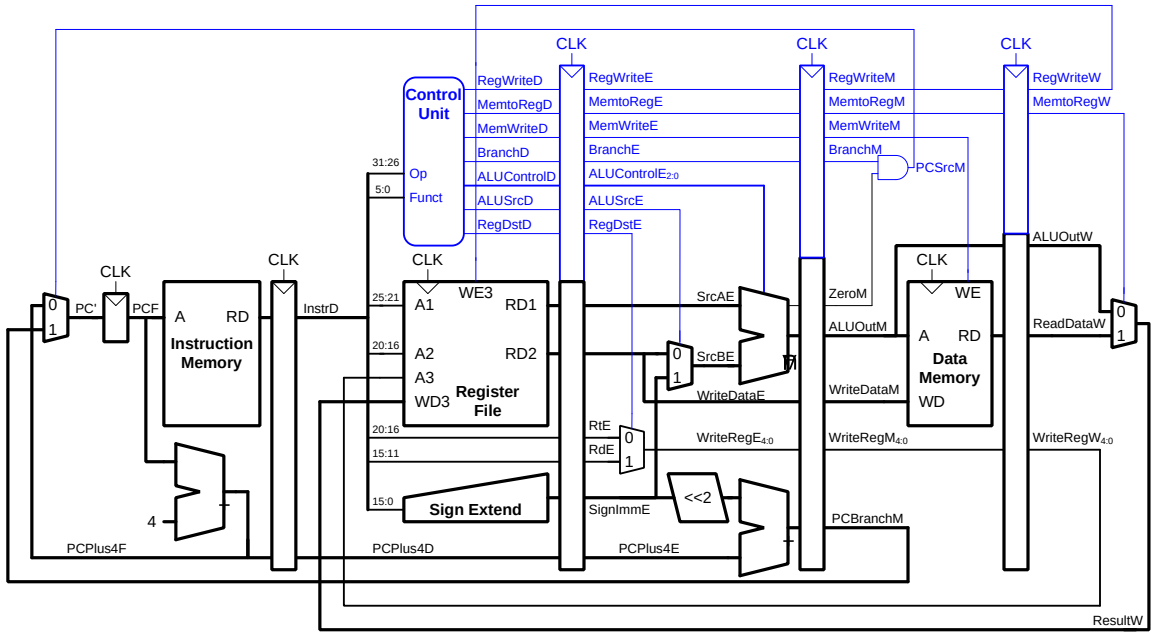


Jr (Jump register)


Add
4
Add
ALU result
Shift left 2
M u x
JumpReg
RegDst
Branch
MemRead
MemtoReg
ALUOp
MemWrite
ALUSrc
RegWrite
Control
Instruction [31–26]
PC
Read address
Instruction [31–0]
Instruction memory
Instruction [25–21]
Instruction [20–16]
Instruction [15–11]
Instruction [15–0]
Instruction [5–0]
Read register 1
Read register 2
Write register
Write data
Read data 1
Read data 2
Registers
16
Sign extend
32
ALU
Zero
ALU result
ALU control
Address
Read data
Write data
Data memory

Task 2:

Extend lab9 to a pipelined version



Submission :

Submit single doc/pdf file with above answers and *.circ files . Course work submission through cs322.iitp@gmail.com with subject: YourrollNo_Lab10. **Due on 26**th October 2018 , 5PM**.**