Roll no:

CS321: Quiz 4

Q1: Suppose we have two implementations of the same instruction set architecture (ISA). For some program, Machine A has a clock cycle time of 10 ns. and a CPI of 2.0 Machine B has a clock cycle time of 20 ns. and a CPI of 1.2. Which machine is faster for this program, and by how much? Assume that # of instructions in the program is 1,000,000,000.

Ans:
CPU TimeA= 109* 2.0 * 10 * 10-9 = 20 seconds
CPU TimeB= 109* 1.2 * 20 * 10-9= 24 seconds
Machine A is faster
24
20
= 1.2 times

Q2: (a) A hypothetical MIPS style processor instruction requires four stages to execute: stage 1 (instruction fetch) requires 30 ns, stage 2 (instruction decode) = 9 ns, stage 3 (instruction execute) =20 ns and stage 4 (store results) = 10 ns. An instruction must proceed through the stages in sequence. What is the minimum time for add instruction to complete?
(b) We want to set this up as a pipelined operation. How many stages should we have and at what rate should we clock the pipeline? What is the latency through the pipe.?

Ans:
30 + 9 + 20 + 10 = 69 ns.

Ans:
We have 4 natural stages given and no information on how we might be able to further subdivide them, so we use 4 stages in our pipeline. We have a choice of what clock rate to use. The simplest choice would be to use a clock cycle that accommodates the longest stage in our pipe – 30 ns. This would allow us to initiate a new instruction every 30 ns with a latency through the pipe of 30 ns x 4 stages = 120 ns.

(We could also pick a finer clock cycle that more closely matches the shortest stage (9 ns) but is integrally divisible into the other stages. A clock of 10 ns would be a good match and would require three clocks for the first stage, 1 clock for the second, 2 clocks for the third and 1 clock for the fourth. This would allow us to initiate a new instruction every 30 ns but provide a latency of 70 ns rather than 120. Either 30 ns or 10 ns is acceptable.)

Consider cache with the following properties:

- Data words are 32 bits each
- A cache block will contain 2048 bits of data
- The cache is direct mapped
- The address supplied from the CPU is 32 bits long
- There are 2048 blocks in the cache
- Addresses are to the word

Design a direct mapped cache structure and show general structure of the cache organization.

Number of bits in offset?
- There are still 6 bits in the offset; (word addressed)
Number of bits in index?

2**11 blocks ; 11 bits for index

Number of bits in tag?
- 32 – 11 – 6 = 15 bits.

(b) What is the total size of the cache?

2**11(15 (tag) +1 bit valid +2048 (data))= 0.5099MB

(c) Repeat problem for two and 4-way set associate cache (figure not required in this cases)

2-way set associative

Offset= 6 bits

Index= 10 bits
Tag= 16 bits

4-way set associative
Offset= 6 bits

Index=9 bits

Tag = 17

Q4: A computer system has a 36-bit virtual address space with a page size of 8K, and 4 bytes per page table entry. (10 points)

1. How many pages are in the virtual address space?
2. What is the page table size in Kbyte assuming 4 bytes per table entry.
3. What is the maximum size of addressable physical memory in this system?

Ans:

1. 2^{23} pages in the page table. (36-13= 23)
2. 2^{23} x4 = 32768 Kbyte
3. 4 bytes per page table entry = 2^{32}. 2^{13} = Maximum size of address addressable Physical Memor y = **2^{45} Bytes**