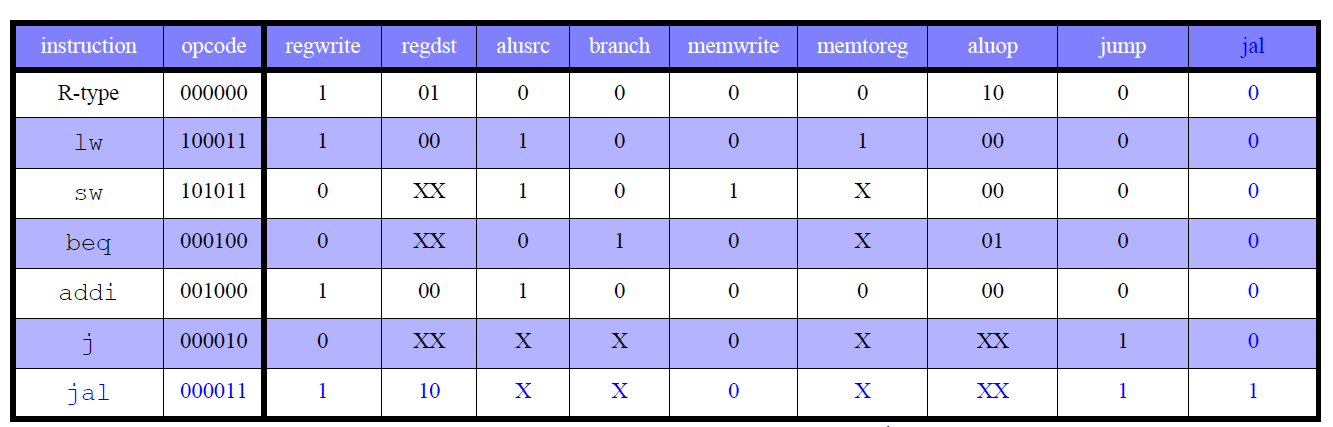
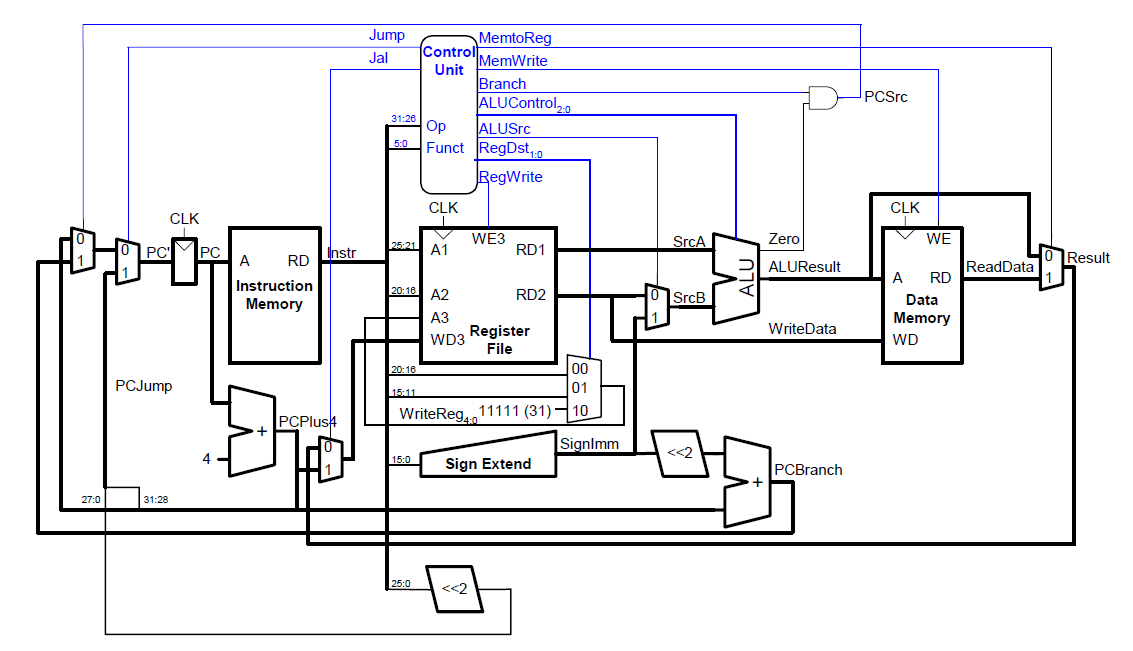
**Lab 10: Implement a RISC single Cycle Processor (Logic-sim)**

Task 1: Using blocks (lab 8/lab9) extend single cycle, implement single cycle processor RISC which could run jal and jr. Test these instructions in the sample code given.

Hints:





***Jr (Jump register)***

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***Task 2:***

Extend lab9 to a pipelined version



**Submission :**

Submit single doc/pdf file with above answers and \*.circ files . Course work submission through cs322.iitp@gmail.com with subject: YourrollNo\_Lab10. **Due on 26**th October 2018 , 5PM**.**