Assignment 2
Valid Invalid Protocol

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Task

In this task, extending the work from our previous implementation of Least Recently Used(LRU) cache for a single processor of 32 KB and 8 way set associative; we implement a shared memory architecture for multi-processor environment with each processor having a private L1 cache connected to a shared memory with a bus interface.

To maintain data coherency in above mentioned architecture we have used a Valid-Invalid protocol and assuming the cache is write through. Figure 1 shows the state transitions of the protocol.

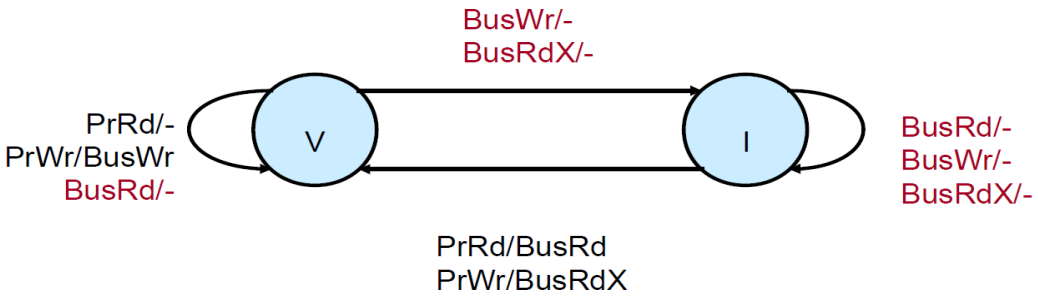

Fig. 1 State transitions of Valid-Invalid protocol

The simulator for the above mentioned protocol was implemented using SystemC. The simulator was used to test the protocol for different number of processors namely 1, 2, 4 and 8 processors. The following table gives a brief overview of the results obtained using the tracefiles provided for different number of processors in the architecture. The simulator also gives a waveform output of the simulator with important parameters.

The following are the results obtained with a single processor:

Tracefile Category : Debug

CPU	Reads	Read Hit	Read Miss	Writes	Write Hit	Write Miss	Hit Rate
0	40	19	21	60	26	34	45.000000

- Main memory access rates
  Bus had 21 reads and 60 writes : total of 81 accesses

- Average time for bus acquisition
  0 waits for the bus.
  Average waiting time per access: 0.000000 cycles.

Time of execution : 11726 ns

Tracefile Category : FFT 16 point

CPU	Reads	Read Hit	Read Miss	Writes	Write Hit	Write Miss	Hit Rate
0	86298	7652	78646	43195	10882	33313	14.312743

- Main memory access rates
  Bus had 78646 reads and 43195 writes : total of 121841 accesses

- Average time for bus acquisition
  0 waits for the bus.
  Average waiting time per access: 0.000000 cycles

Time of execution : 15685268 ns

Tracefile Category: Random

CPU	Reads	Read Hit	Read Miss	Writes	Write Hit	Write Miss	Hit Rate
0	33031	18659	14372	32505	18306	14199	56.404114

- Main memory access rates
  Bus had 14372 reads and 32505 writes : total of 46877 accesses

- Average time for bus acquisition
  0 waits for the bus.
  Average waiting time per access: 0.000000 cycles.

Time of execution : 6256978 ns

The following are the results obtained with two processors:

Tracefile Category: Debug

CPU	Reads	Read Hit	Read Miss	Writes	Write Hit	Write Miss	Hit Rate
0	30	0	30	25	1	24	1.818182
1	32	0	32	35	1	34	1.492537

- Main memory access rates
  Bus had 62 reads and 60 writes : total of 122 accesses

- Average time for bus acquisition
  There were 8730 waits for the bus.
  Average waiting time per access: 71.557377 cycles.

Time of execution : 14291 ns

Tracefile category: FFT with 16 points

CPU	Reads	Read Hit	Read Miss	Writes	Write Hit	Write Miss	Hit Rate
0	29312	3402	25910	15417	2013	13404	12.106240
1	29262	3151	26111	14801	1898	12903	11.458593

- Main memory access rates
  Bus had 52021 reads and 30218 writes : total of 82239 accesses

- Average time for bus acquisition
  There were 4143023 waits for the bus.
  Average waiting time per access: 50.377838 cycles.

Time of execution : 7628563 ns

Tracefile Category: Random

CPU	Reads	Read Hit	Read Miss	Writes	Write Hit	Write Miss	Hit Rate
0	16496	385	16111	16402	393	16009	2.364885
1	24556	865	23691	24804	877	23927	3.529173

- Main memory access rates
  Bus had 39802 reads and 41206 writes : total of 81008 accesses

- Average time for bus acquisition
  There were 5490498 waits for the bus.
  Average waiting time per access: 67.777232 cycles.

Time of execution : 10060998 ns

The following are the results obtained with four processors:

Tracefile Category: Debug

CPU	Reads	Read Hit	Read Miss	Writes	Write Hit	Write Miss	Hitrate
0	8	0	8	8	1	7	6.250000
1	27	0	27	32	0	32	0.000000
2	43	1	42	38	2	36	3.703704
3	45	0	45	42	0	42	0.000000

- Main memory access rates
  Bus had 122 reads and 120 writes : total of 242 accesses

- Average time for bus acquisition
  There were 44571 waits for the bus.
  Average waiting time per access: 184.177686 cycles.

Time of execution : 25895 ns

Tracefile Category: FFT 16 Point

CPU	Reads	Read Hit	Read Miss	Writes	Write Hit	Write Miss	Hitrate
0	11274	1743	9531	6552	936	5616	15.028610
1	9417	1461	7956	6083	760	5323	14.329032
2	9834	1526	8308	5523	613	4910	13.928502
3	9881	1498	8383	5972	706	5266	13.902731

- Main memory access rates
  Bus had 34178 reads and 24130 writes : total of 58308 accesses

- Average time for bus acquisition
  There were 10523057 waits for the bus.
  Average waiting time per access: 180.473640 cycles.

Time of execution : 5052367 ns

Tracefile Category : Random

CPU	Reads	Read Hit	Read Miss	Writes	Write Hit	Write Miss	Hitrate
0	8039	85	7954	8251	89	8162	1.068140
1	20450	0	20450	20221	0	20221	0.000000
2	26553	982	25571	26498	1056	25442	3.841586
3	29600	0	29600	29695	3	29692	0.005059

- Main memory access rates
  Bus had 83575 reads and 84665 writes : total of 168240 accesses

- Average time for bus acquisition
  There were 33544216 waits for the bus.
  Average waiting time per access: 199.383119 cycles.

Time of execution : 18434230 ns

The following are the results obtained with eight processors:

Tracefile category : Debug

CPU	Reads	Read Hit	Read Miss	Writes	Write Hit	Write Miss	Hitrate
0	6	0	6	4	0	4	0.000000
1	34	0	34	22	0	22	0.000000
2	35	0	35	43	0	43	0.000000
3	39	2	37	46	2	44	4.705882
4	36	0	36	55	0	55	0.000000
5	52	0	52	46	0	46	0.000000
6	48	3	45	51	2	49	5.050505
7	42	1	41	55	5	50	6.185567

- Main memory access rates
  Bus had 286 reads and 322 writes : total of 608 accesses

- Average time for bus acquisition
  There were 335554 waits for the bus.
  Average waiting time per access: 551.898026 cycles.

Time of execution : 64998 ns

Tracefile Category : FFT 16 Point

CPU	Reads	Read Hit	Read Miss	Writes	Write Hit	Write Miss	Hitrate
0	4956	1114	3842	3153	747	2406	22.949809
1	3983	819	3164	2890	542	2348	19.802124
2	3997	872	3125	2703	507	3196	20.582090
3	4043	867	3176	2695	497	2198	20.243396
4	4055	854	3201	2662	475	2187	19.785619
5	4055	852	3203	2733	512	2221	20.094284
6	4074	821	3253	2710	490	2220	19.324882
7	4124	833	3291	2705	471	2234	19.095036

- Main memory access rates
  Bus had 26255 reads and 22251 writes : total of 48506 accesses

- Average time for bus acquisition
  There were 24386388 waits for the bus.
  Average waiting time per access: 502.749928 cycles.

Time of execution : 4165313 ns

Tracefile category : Random

CPU	Reads	Read Hit	Read Miss	Writes	Write Hit	Write Miss	Hitrate
0	4113	22	4091	4030	35	3995	0.699988
1	18318	0	18318	18440	0	18440	0.000000
2	25834	21	25813	25470	30	25440	0.099407
3	29549	1275	28274	28801	1180	27621	4.207369
4	31366	2	31364	30548	1	30547	0.004845
5	32015	12	32003	31781	26	31755	0.059565
6	32327	1626	30701	32285	1653	30632	5.074909
7	32536	1687	30849	32584	1771	30813	5.310197

- Main memory access rates
  Bus had 201413 reads and 203939 writes : total of 405352 accesses

- Average time for bus acquisition
  There were 209784639 waits for the bus.
  Average waiting time per access: 517.536953 cycles.

Time of execution : 41207484 ns

Implementation and Observations :

- When we have a write hit or write miss followed by a read miss on the same address by different CPUs, it leads to data inconsistency, this situation is handled using a bus locking mechanism so that we ensure data coherency.

- When we disable snooping mechanism on the bus by the processors, data inconsistency is observed.