Fully Automated Traffic Light Controller system for a four-way intersection using Verilog

Pranaav Jothi M
Department of Electronics Engineering
Madras Institute of Technology
Anna University
Chennai, India
pranaavjothi@gmail.com

Srivatsan M
Department of Electronics Engineering
Madras Institute of Technology
Anna University
Chennai, India
srivatsanmohan2001@gmail.com

Krishna Kumar P
Department of Electronics Engineering
Madras Institute of Technology
Anna University
Chennai, India
thekrishnakumar01@gmail.com

Prakash P
Department of Electronics Engineering
Madras Institute of Technology
Anna University
Chennai, India
prakashp79@gmail.com

Kasthuri P
Department of Electronics Engineering
Madras Institute of Technology
Anna University
Chennai, India
kasthurip94@gmail.com

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***Abstract*—Traffic lights are placed in roads to control the flow of traffic and to prevent accidents. This paper proposes a Moore machine based fully automated and efficient traffic light controller system for four-way intersection. The system is designed on Xilinx Artix-7 xc7a100tcsg324-1 FPGA using Xilinx Vivado and Verilog Hardware Description Language. The designed system runs up to a maximum operating frequency of 10 MHz.**

Keywords— Field Programmable Gate Array, Finite State Machine, Hardware Description Language, Light Emitting Diode, Verilog.

I. INTRODUCTION

Traffic congestion is one of the predominant problems prevailing in cities and towns. In T-intersection and four-way intersection, the probabilities of accidents are slightly higher. So, to ensure smooth flow of traffic and to avoid road accidents, traffic light systems are used.

The proposed traffic light controller system is designed for four-way intersection roads. In this system, the waiting time of vehicles at the intersection is reduced by a great extent. Microcontroller and Microprocessor based traffic light systems are already present. But the disadvantage associated with these systems is that, they work on fixed time, and doesn't have flexibility. So, this paper concentrates on developing a reconfigurable traffic light controller system, which works on Field Programmable Gate Array (FPGA) as it doesn't have a fixed hardware structure and can be reprogrammed by using Hardware Description Language (HDL). Verilog is chosen for modelling the traffic light controller system, as usage of Verilog HDL allows to define the specifications of the parameters used in the design of the system. Also, Verilog HDL is one of the commonly used HDLs as it has simple syntax and it resembles software programming languages to some extent.

FPGA boards have many input switches and output Light Emitting Diodes (LEDs) in it, which make it suitable for the design of traffic light controller systems. FPGAs are used for designing prototypes for many electronic applications. Another advantage of FPGA is that, it makes the whole system more efficient. The FPGA chosen here is Artix-7, which is a product of Xilinx, a semiconductor manufacturing company. Artix-7 is preferred as it is cost efficient and for its high performance. It is used in systems so as to have optimum power consumption.

There are different types of traffic control systems which are put forth by researchers for different real time situations. A traffic light controller was designed using Verilog HDL considering two roads [1] and for a T-junction [2]. A system for four-way intersection was implemented using two signals, red and green [3]. Another system makes use of three signals, red, yellow and green to regulate the traffic [4]. But the drawback of these systems for four-way intersection was that they don't allow the maximum possible movement of vehicles across the intersection [3][4]. Vehicles from few roads are made to wait at the intersection unnecessarily as allowing them doesn't disturb the moving vehicles. The proposed system makes sure that this drawback is removed to allow the maximum transportation of vehicles across the intersection and to prevent the unnecessary waiting time of the motorists.

Moore model of Finite State Machine (FSM) is used to design the traffic light controller system as the output of the system (traffic light signals) depends only upon the current state of the system. This feature makes the system fully automated. The system considers the four roads to have equal traffic and makes use of the Binary encoding scheme. Compared to other works, the proposed system is more efficient by making use of minimal number of states which are necessary enough to allow the maximum transportation of vehicles across the intersection. The reduction in number of states also helps in achieving minimal power consumption. The traffic controller system also makes use of the maximum possible number of safe states. Before the stoppage of traffic across each direction, yellow signal is displayed in the corresponding displays which indicate that the flow of traffic will be stopped in few seconds. The states containing yellow signals act as safe states and prevent the possibility of accidents. A Simulation based system is designed and the same is done using Xilinx Vivado. Complete information of the system designed is obtained using various facilities present in this software like timing report, utilization report, power report, etc.

II. METHODOLOGY

The paper concentrates on developing a traffic light controller system for a four-way intersection. Each road has three light displays corresponding to the flow of traffic

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towards the other three roads. Hence there are twelve light displays in total at the intersection. By using a common control logic, the system is designed in such a way that, certain light displays operate in the same manner. This simplifies the design with ten light displays. Each of these light displays have the provision to show red, green and yellow signals. The red signal specifies to stop, the green signal allows the flow of traffic and the yellow signal specifies that the flow of traffic will be stopped in few seconds. The proposed system helps to prevent vehicle collisions at the intersection by use of 'safe' states. The red, yellow and green signals of each of the light displays are modeled as individual output LEDs. So a total of thirty output LEDs are used. A state diagram and a state table are constructed based upon the simplified logic to model a finite state machine for the proposed traffic light controller system.

III. IMPLEMENTATION OF TRAFFIC LIGHT CONTROLLER SYSTEM

A. Light Display assignment

The proposed traffic light controller system is designed to operate at a maximum frequency of 10.0 MHz. The time period (T) of the clock used in this system is given by the formula

$$T = \frac{1}{f} \qquad (1)$$

Where f is the maximum operating frequency of the system. The ten light displays are labelled as D0, D1, D2, D3, D4, D5, D6, D7, D8 and D9 respectively. Light displays are assigned according to the direction of traffic flow. Two directions are grouped together in D0 and D2 states instead of employing separate light displays representing the traffic flow along those directions. Table I represents the assignment of light displays according to the directions of flow of traffic.

TABLE I. LIGHT DISPLAYS AND THE CORRESPONDING DIRECTIONS

Direction name	Corresponding movement of vehicles at the intersection
D0	
D1	
D2	
D3	
D4	
D5	
D6	
D7	
D8	
D9	

B. State assignment

Based on the 10 light displays and according to the movement of the vehicles, 12 different states are used for traffic control. The assignment of states is given in Fig. 1.

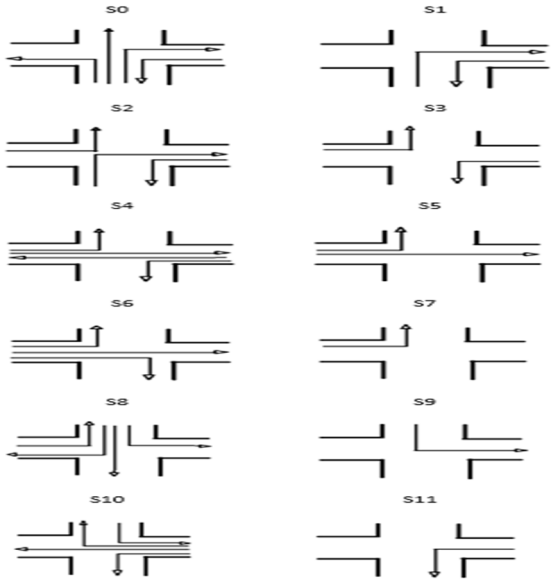

Fig. 1. Assignment of states

C. State Diagram

The vehicle movement during the even states such as S0, S2, S4, S6, S8 and S10 are comparatively higher than that during the odd states such as S1, S3, S5, S7, S9 and S11. So, the green signal timing for even states are set to be more than that of odd states. The signal timing for even states are set to 10 seconds and for odd states, the signal timing is set to 5 seconds. This implies that during the even states, the present state of the displays will continue for 10 seconds and when the time exceeds 10 seconds, the system goes into the succeeding odd state. Similarly, in odd states, the present status of the displays will continue for 5 seconds and when the time exceeds 5 seconds, it moves into the succeeding even state. After S11 state, the system again enters into S0 state and this cycle continues. The time taken for the system to complete one full cycle is 90 seconds. The system also makes use of Reset signal. Once the system detects the Reset signal, the system enters into the initial state S0. Fig. 2 illustrates the state diagram of the proposed system.

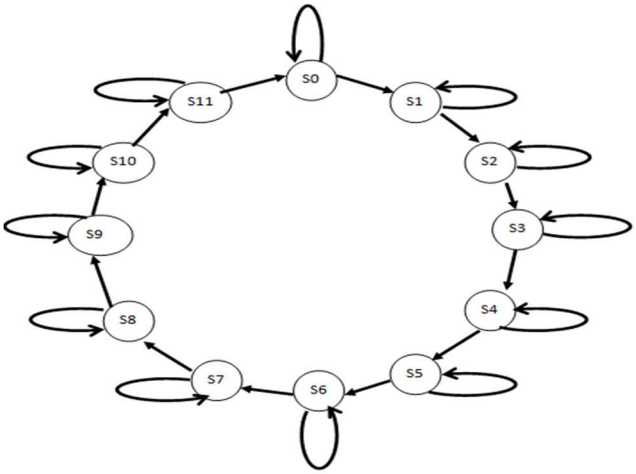

Fig. 2. State diagram of the proposed system

D. State Table

Having defined the state diagram, a state table is now formed. Initially, in state S0, vehicle movement is allowed only for directions corresponding to the light displays D0, D4 and D7. So, green signal is enabled only for these directions, and for the other directions, red signal is enabled on their corresponding light displays. Similarly, according to each state, red, yellow and green signals are enabled for each of the light displays. Binary encoding scheme is used in the proposed system. Table II illustrates the state table of the system.

TABLE II. STATE TABLE OF THE PROPOSED SYSTEM

State	Traffic signal status for each direction									
	D0	**D1**	**D2**	**D3**	**D4**	**D5**	**D6**	**D7**	**D8**	**D9**
S0	001	100	100	100	001	100	100	001	100	100
S1	010	100	100	100	001	100	100	001	100	100
S2	100	100	100	100	001	001	100	001	100	100
S3	100	100	100	100	010	001	100	001	100	100
S4	100	100	100	001	100	001	100	001	001	100
S5	100	100	100	010	100	001	100	010	001	100
S6	100	001	100	100	100	001	100	100	001	100
S7	100	010	100	100	100	001	100	100	010	100
S8	100	100	001	100	100	001	001	100	100	100
S9	100	100	010	100	100	010	001	100	100	100
S10	100	100	100	001	100	100	001	001	100	001
S11	100	100	100	010	100	100	010	001	100	010

In each of the states, if MSB is 1, it indicates that the light display is showing red signal, and so, the movement of vehicles in the direction corresponding to the light display is restricted. Similarly, if the middle bit is 1, it corresponds to yellow signal, and indicates that the traffic flow will stop soon. If LSB is 1, it corresponds to green signal and the flow of traffic in the corresponding direction is allowed. The odd states act as 'safe' states as few of the light displays show yellow signal indicating that the flow of traffic will be stopped soon, so that vehicles from those directions can stop, since crossing the intersection during the period of the yellow signal of the current state may lead to accidents due to the flow of traffic regulated during the succeeding even state.

IV. RESULTS

The proposed system is designed as a Moore FSM using Xilinx Vivado and Verilog HDL. Simulation, synthesis, implementation and generation of bit stream were done and no DRC violations were found.

A. Simulation

Fig. 3 displays the result of behavioral simulation showing the waveform of the Traffic light controller system for the test bench applied using Verilog HDL.

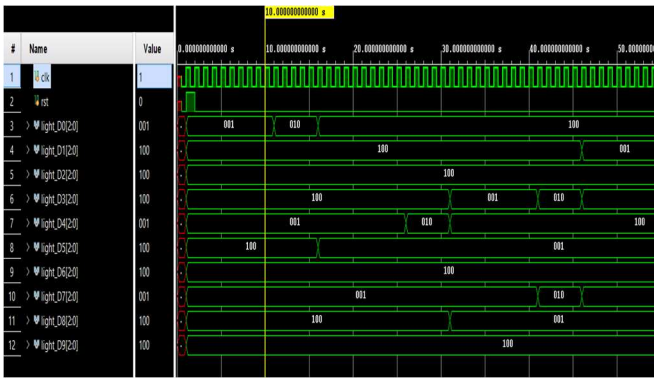

Fig. 3. Simulated waveform of the system

B. RTL Schematic

Fig. 4 shows the RTL schematic of the designed system.

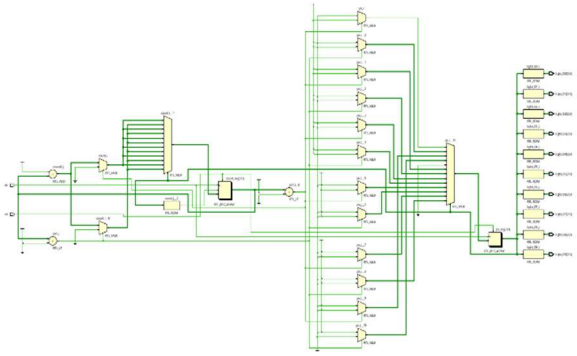

Fig. 4. RTL schematic of the system

C. Timing report

It was observed that the timing report generated during synthesis matched with the timing report generated during implementation. The obtained timing report is shown in Fig. 5.

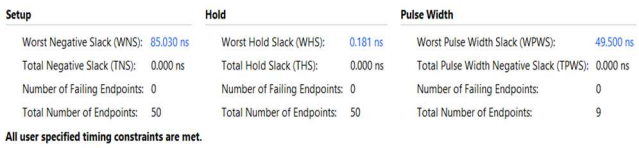

Fig. 5. Timing report of the system

D. Utilization report

It was observed that the utilization report generated during synthesis matched with the utilization report generated during implementation. The obtained utilization report is shown in Fig. 6.

Resource	Utilization	Available	Utilization %
LUT	21	63400	0.03
FF	8	126800	0.01
IO	32	210	15.24

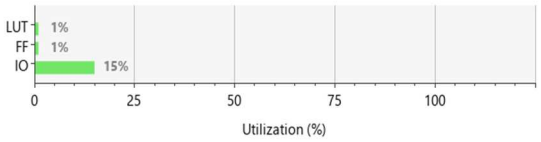

Fig. 6. Utilization report of the system

E. Power report

It was observed that the power report generated during synthesis matched with the power report generated during implementation. The obtained power report is shown in Fig. 7.

Total On-Chip Power:	**0.098 W**
Junction Temperature:	**25.4 °C**
Thermal Margin:	59.6 °C (12.9 W)
Effective ϑJA:	4.6 °C/W
Power supplied to off-chip devices:	0 W

Fig. 7. Power report of the system

F. Technology schematic

It was observed that the technology schematic generated during synthesis matched with the technology schematic generated during implementation. The obtained technology schematic is shown in Fig. 8.

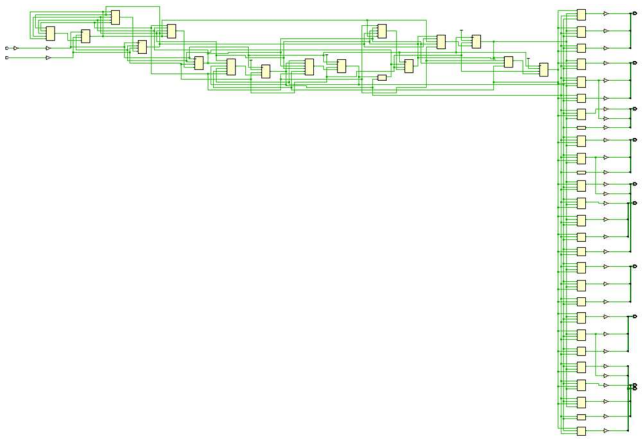

Fig. 8. Technology schematic of the system

G. Device layout after implementation

Fig. 9 shows the device layout obtained after implementation.

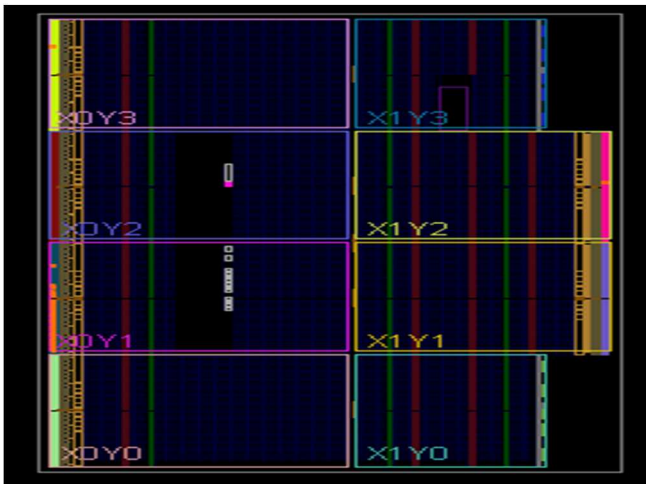

Fig. 9. Device layout of the system

V. CONCLUSION AND FUTURE WORK

The traffic light controller system designed is well suited to regulate traffic at four-way intersection. The system is designed in Artix-7 FPGA so as to utilize its advantage of efficient power consumption. Verilog HDL is used for programming purpose because if the user wishes to make any changes in the system, it is possible to apply the required changes easily through Verilog HDL code. One of the advantages of this system is its 'safe state' feature implemented in every odd state, which plays a major role in preventing vehicle collisions.

The simulated waveform matched the traffic light signals obtained from the state table. The implemented system had a minimal power utilisation of 0.098 W and had used only 0.01% of the flip flops and 15.24% of the total IO (Input Output) facilities present in the FPGA.

As a future scope, cameras and sensors can be integrated to the designed system so that when the traffic controller system sees an ambulance, it can automatically divert the traffic accordingly so as to ensure that there is no obstacle and the way for the ambulance is clear.

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