# Control signals flow

## Instruction Fetch:

1. PC is incremented and sent to PC register
2. Instruction is fetched from Memory
3. Branch Prediction Table (BPT) is used if possible

## Instruction Decode:

1. Creation of Signals:
   1. Control Signals for multiplexors in the other pipeline stages
   2. Sign Extended value of the Immediate data in the instruction if present
   3. The addition of the sign extended value and the current PC value (SE + PC)
   4. Control line for the mux which decides if PC+1 has to be sent or (SE+PC) value to the PC register (SE+PC) value is sent to PC when decoder encounters with JAL instruction
   5. Clear bit for when JAL instruction arrives to clear the pipeline register (IF-ID)
   6. Control Signal for SE which decides if to sign extend 6 bit or 9 bit immediate data
   7. LLI bit for SE which just packs the immediate data with zeros to make the data 16bit
   8. Address of the register file (AR1, AR2, AR3)
   9. The LM or SM data to be given to the LM\_SM block This contains the data of the registers whose data has to be either stored or loaded
   10. The ALU control bits which tells the ALU of its operations
   11. Flag control bits which enables or disables the flag registers
   12. The condition bits which indicates the presence of conditional arithmetic instruction
   13. Register write and Memory write signals
   14. Control Signal for the BPT telling it whether the instruction is BEQ type or not
   15. Branch Prediction Table produces the index of the instruction from the table and also information on whether the branch was taken or not

## Register Read:

1. Consumption of Signals:
   1. The LM or SM data is consumed by the LM\_SM block and also LM or SM bit which activates the LM\_SM block
   2. AR1 and the AR2 data for the register file
   3. The control signal for the mux which steers inputs between (SE+PC) and the left shifted value of the sign extended immediate data
   4. LM\_SM block creates the control signal for the mux before AR2 which steers the input between the original AR2 and the AR2 created by the LM\_SM block which sets data bits to zero
   5. LM\_SM block also creates the signal for the mux which decides the data to be sent in the DO1 register. The original DO1 value or the auto incremented value of DO1 by the LM\_SM block
   6. RR\_PC created by the hazard block in RR stage which controls the mux which decides the input to PC should be PC+1 or SE value (when R7 is AR3 in LLI) or left shifted SE (when R7 is AR3 in LHI) or DO1 (when the instruction is JLR)
2. Creation of Signals :
   1. DO1 and DO2 data created from the register file

## Execution:

1. Consumption of Signals:
   1. Two control signals for the forwarding mux created by the forwarding logic block
   2. The control signal for the mux which steers input between DO2 or the sign extended value DO2 is used for arithmetic operations whereas sign extended value is used for address calculation
   3. The control signal for the mux which is created by the LM\_SM block to select 1 such that the required address is always incremented by 1 during the LM or SM instruction
   4. The control signal for the hazard mux
   5. The control signal for the mux created by LM\_SM block to store the created address in the register file for storing data during LM from the memory
2. Creation of Signals:
   1. The flag register values after the ALU operation
   2. The ALU output data after ALU operation

## Data Memory Write/Read

1. Consumption of Signals:
   1. Memory write control for the data memory during instructions like SW or SM
   2. The control signal for the mux created by the LM\_SM block which steers inputs between the ALU output or the address calculated by the LM\_SM block
   3. The control signal for the hazard mux in the Memory Write stage
2. Creation of Signals:
   1. The data after reading from the data memory

## Write Back:

1. Consumption of Signals:
   1. Flag values to be written in the user flag registers
   2. The control signals for the mux which decides the data to be written in the register file according to the instruction (ALU output, left shifted sign extended value, (SE+PC), SE, PC+1, Memory out data)
   3. Flag control bits, Condition bits, Control Signals is sent to the hazard logic block in WB stage
   4. The control signal for the mux which decides the input to R7 in register file This created by the hazard block

The data after WB mux, AR3 and some of the control signals (valid, the control signals for WB mux) is sent to a temporary register This register holds data for the forwarding logic.