Design of Digital Systems with VHDL

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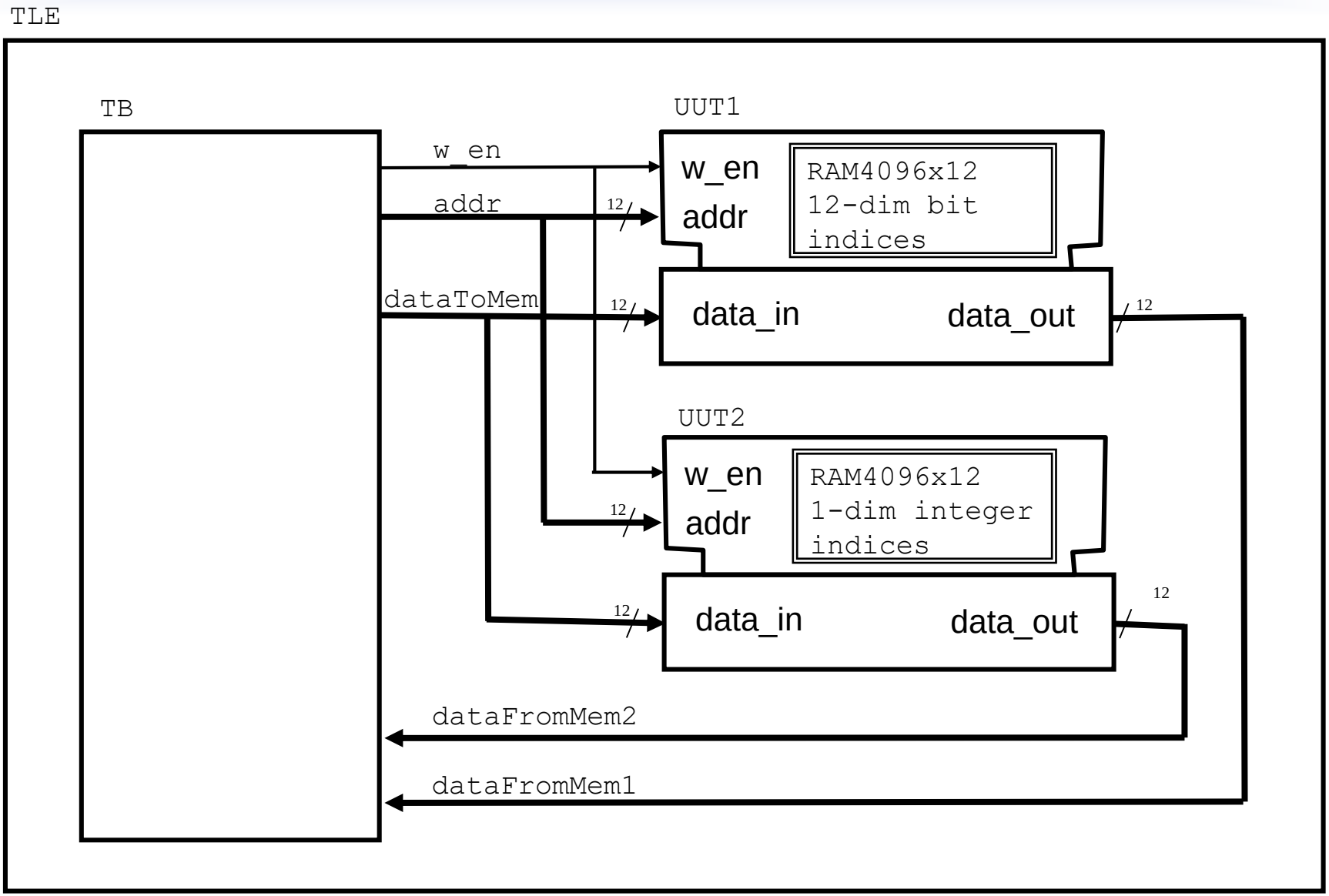
Memory Model LAB

- Block diagram
- Description
- Work-Split Option

Testbench with two Memories



Description of Work

- Two memory models have to be build
  - One with 12-dimensional bit indices
  - One with 1-dimensional integer index

  The blue-print for the models has been presented in the lecture
- One testbench model has to be build
  - The testbench takes care, that the value of the address of each memory cell is written to the cell. I.e. Cell with address 0 gets the value 0, Cell with address 1 gets the value 1, … The memories are written in parallel
  - The testbench then reads the content from each memory address – i.e. `dataFromMem1` and `dataFromMem2` - and makes sure, that the two memories return the same value.
    It is important to wait for some ns before the values from the memories stabilize in simulation and can be compared.
  - This testbench is a simplified version of the complete testbench from the lecture
- Top Level Entity Instantiating and Connecting the 3 Models from above

Options for Work-Split

- The work offers to be split in 4 tasks
  1. Memory Model with 12-dimensional Index
     1. Entity Declaration
     2. Architecture Body
  2. Memory Model with Integer Index
     1. Entity Declaration same as 1.a. – need not be re-modeled!
     2. Architecture Body (`IEEE.numeric_std.to_integer`) can be used
  3. Testbench
     1. Entity Declaration
     2. Architecture Body
  4. Top Level Entity Instantiating and Connecting the 3 Models from above
     1. Entity Declaration
     2. Architecture Body
     3. Configuration

- Each of the 4 models described above may be saved in one file!