No of Pages : 2 Course Code : 12XW25

Roll No:
(To be filled in by the candidate)

PSG COLLEGE OF TECHNOLOGY, COIMBATORE - 641 004

SEMESTER EXAMINATIONS, MAY - 2015

MSc – SOFTWARE SYSTEMS Semester : 2

12XW25 COMPUTER ORGANISATION

Time : 3 Hours **Maximum Marks : 100**

INSTRUCTIONS:

1. Answer **ALL** questions from GROUP – I.
2. Answer any **5** questions from GROUP – II.
3. Answer any **ONE** question from GROUP – III.
4. Ignore the box titled as **"Answers for Group III"** in the Main Answer Book.

GROUP - I **Marks : 10 x 3 = 30**

1. How does the CPU recognize the negative result in 2's complement subtraction? Justify your answer with an example.
2. Given the following micro operations for data register DR in a basic computer, design the associated control logic for the same.

   $D_0 T_4$: DR ← M[AR]

   $D_0 T_5$: AC ← AC + DR

   $D_1 T_5$: AC ← AC ^ DR

   $D_2 T_4$: DR ← M[AR]

   $D_2 T_5$: AC ← DR

   $D_6 T_5$: DR ← DR + 1
3. A digital computer has a common bus system for 16 registers of 32 bits each. The bus is constructed with multiplexers. Find the quantity and configuration of each multiplexer in terms of selection inputs and size.
4. Why does a DMA have a priority over the CPU when both request a memory transfer?
5. A Virtual memory has a Page Size of 1K words. There are eight Pages and four blocks. The associative memory page table contains the following entries.

Page	*Block*
6	0
1	1
4	2
0	3

   Give the list of virtual addresses in decimal that will cause a Page fault if used by CPU.
6. How many characters per second can be transmitted over a 1200 baud line in asynchronous serial transmission in following modes assuming the character code is of eight bits?

   (i) Synchronous Serial transfer

(ii) Asynchronous Serial Transfer with 2 stop bits (1 bit duration)

(iii) Asynchronous Serial Transfer with one stop bit. (1 bit duration)

7. Why is a page-table required in a virtual memory system? List the different ways of organizing a page table.
8. An output program resides in memory starting from 2300. It is executed after the computer recognizes an interrupt when FGO becomes a 1 (while IEN =1)
   - What address must be placed at Address 1?
   - What must be the last two instructions of the program?
9. Differentiate between loosely coupled and tightly coupled systems in the context of multiprocessor.
10. Enumerate the different multiprocessor architecture according to Flynn's taxonomy.

GROUP - II Marks : 5 x 10 = 50

11. a) Design the single stage of Arithmetic and logical unit and draw the functional table of the same. Design a hardware circuit to implement logical shift, arithmetic shift and circular shift operations and state your design specifications.

    b) Differentiate between Isolated and memory mapped method of IO interfacing.

12. a) Explain the organization of control memory and its operation with a block diagram.

    b) What is a micro program sequencer? Explain the working of micro program sequencer with block diagram.

13. Discuss different techniques used for interfacing I/O units with the processor. With a suitable block diagram, explain how asynchronous data transfer is carried out with an interface.
14. State two limitations of programmed I/O method of data transfer scheme. How are these limitations eliminated in DMA? Explain this method with the help of a basic diagram showing CPU, memory and DMA controller connectivity.
15. a) Describe with the help of a block diagram how multiple matched words can be read from an associative memory?

    b) A computer employs RAM chips of 256 x 8 and ROM chips of 1024 x 8. The computer system needs 2K bytes of RAM, 4K bytes of ROM. The two highest-order bits of the address bus are assigned 00 for RAM, 01 for ROM.

    Draw a memory-address map for the system and Give the address range in hexadecimal for RAM, ROM, and interface.

16. a) Justify how pipelining in the CPU design would improve the performance of CPU. What are the reasons of pipeline conflicts in pipelined processor and how are they resolved?

    b) Discuss some of the interconnection structures used in connecting the multiprocessors and the memory modules.

GROUP - III Marks : 1 x 20 = 20

17. Explain in detail the different methods of mapping used in Cache memory organisation with suitable examples. Show how the contents of the cache memory are initialised and how the main memory is updated.
18. Discuss on the process of interrupt initiated IO and its advantage over the programmed IO. How does a basic computer handle an interrupt? Explain the different ways by which priority interrupts are handled with suitable diagrams.

FD/RL /END/