No of Pages : 2 Course Code : 15XW25

Roll No:
(To be filled in by the candidate)

PSGCOLLEGE OF TECHNOLOGY, COIMBATORE - 641 004

SEMESTER EXAMINATIONS MAY 2017

MSc - SOFTWARE SYSTEMS Semester :2

15XW25 COMPUTER ORGANIZATION

Time : 3 Hours **Maximum Marks :100**

INSTRUCTIONS:

1. Answer **ALL**questions from GROUP – I.
2. Answer any **5** questions from GROUP – II.
3. Answer any **ONE**question from GROUP – III.
4. Ignore the box titled as **"Answers for Group III"** in the Main Answer Book.

GROUP - I **Marks : 10 x 3 = 30**

1. Express the following numbers in IEEE 754 single precision floating-point format:
   (i) $+5.4 * 10^{-15}$ (ii) -0.5
2. With an example, show the difference between 1's complement subtraction and 2's complement subtraction of binary numbers.
3. What do you understand by the term micro-operation? Show the hardware realization of decrement micro-operation.
   T1: X ← X −1
4. Given the following micro operations for data register DR in a basic computer, design the associated control logic for the same.
   $D_0 T_4$: DR ← M[AR]
   $D_0 T_5$: AC ← AC + DR
   $D_1 T_5$: AC ← AC ^ DR
   $D_2 T_4$: DR ← M[AR]
   $D_2 T_5$: AC ← DR
   $D_6 T_5$: DR ← DR + 1
5. A digital computer has a memory unit of 64 K x 16 and a cache memory of 1K words. The cache uses direct mapping with a block size of four words. How many bits are there in the tag, index, block and word fields of the address format? How many blocks can the cache accommodate?
6. Comment on the two methods of updating the cache memories in the context of word associative cache systems.
7. Why are the read and write control lines in a DMA controller bidirectional? What are conditions that make these control lines input and output?
8. What is the advantage of interrupt initiated data transfer over transfer under program control without an interrupt?
9. Formulate the logical and physical address formats for the following case: The logical address space in a computer system consists of 128 segments. Each segment can have

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upto 32 pages of 4K words in each. Physical memory consists of 4K blocks of 4K words in each.

10. Depict the three computer architectural classification schemes in parallel processing.

GROUP - II Marks : 5 x 10 = 50

11. a) Design a hardware circuit to implement logical shift, arithmetic shift and circular shift operations. State your design specifications. [6+4]
    b) Discuss the different characteristics of RISC and compare RISC with CISC.
12. a) Register R5 is used in a program to point to the top of the stack. Write a sequence of instructions using the Indexed addressing mode to POP the two top items off the stack, add them and PUSH the result onto the stack.
    b) Explain the functioning of a control unit with the help of a block diagram. Write a micro program for the fetch routine of the CPU
13. a) Consider a memory system having 16K of main memory with 12 K of RAM and 4 K of ROM. The RAM and ROM memory chips are available in 2K x 8 and 1K x 8 sizes respectively. Draw the memory map showing the addresses in Binary and in Hexadecimal. Draw the interface circuit connecting the CPU to memory.
    b) The access time of a cache memory is 100 ns and that of main memory is 1000 ns. It is estimated that 80 percent of the memory requests are for read and the remaining 20 percent are for write. The hit ratio of read access only is 0.9. A write through procedure is used. For the above scenario, calculate the following:
    (i) average access time of the system considering only the memory read cycle
    (Ii) average access time of the system for both read and write requests
    (iii) hit ratio taking into consideration the read cycles.
14. Discuss the methods of asynchronous data transfer in a system. Also draw the interface circuit meant for the asynchronous data transfer.
15. Explain the concept of virtual memory address mapping using a Page Table with suitable diagrams .
16. Differentiate between tightly coupled multiprocessors and loosely coupled multiprocessors from the viewpoint of hardware organisation. Discuss the different types of interconnection structures between the CPU, IOPs and Memory modules.

GROUP - III Marks : 1 x 20 = 20

17. Write short notes on CPU-IOP communication. With suitable diagram, discuss how the interrupts are recognized by the CPU. Explain the various ways in which the interrupts from multiple devices are handled.
18. Explain how pipelining in the CPU design would improve the performance of CPU.by illustrating with the following case study:
    In certain scientific computations it is necessary to perform the arithmetic operation with a stream of numbers. Specify a pipeline configuration to carry out this task $(A_i + B_i)$ $(C_i + D_i)$ listing the contents of all registers in the pipeline for i = 1 through 6.
    What are reasons of pipeline conflicts in pipelined processor and how are they resolved?

/END/

FD/JU