No of Pages : 2 **Course Code : 15XW25**

Roll No:
(To be filled in by the candidate)

PSG COLLEGE OF TECHNOLOGY, COIMBATORE - 641 004

SEMESTER EXAMINATIONS, MAY 2018

MSc - SOFTWARE SYSTEMS Semester : 2

15XW25 COMPUTER ORGANISATION

Time : 3 Hours **Maximum Marks : 100**

INSTRUCTIONS:

1. Answer **ALL** questions. Each question carries 20 Marks.
2. Subdivision (a) carries 3 marks each, subdivision (b) carries 7 marks each and subdivision (c) carries 10 marks each.
3. Course Outcome : Table

Qn.1	CO.1	Qn.2	CO.2	Qn.3	CO.3	Qn.4	CO4.	Qn.5	CO.5

1. a) How does the CPU recognize the negative result in 2's complement subtraction? Justify your answer with an example

   b) i) Design an arithmetic circuit with one selection variable S and two n-bit data inputs A and B. The circuit generates the following four arithmetic operations in conjunction with the input carry C_{in}. Draw the logic diagram for the first two stages

S	$C_{in} = 0$	$C_{in} = 1$
0	$D = A + B$ (add)	$D = A + 1$ (increment)
1	$D = A - 1$ (decrement)	$D = A + \overline{B} + 1$ (subtract)

   ii) The operations to be performed with flip flop F are specified by the following register transfer statements. Otherwise, the contents must not change. Draw the logic diagram showing the connections of the gates that form the control functions and the input of the flip flop F. Use a JK flip flop with minimum number of gates.

   xT3 : F← 1 Set F to 1
   yT1 : F← 0 Reset F to 0
   zT2 : F←F' Set F to F'
   wT4: F← G Transfer value of G to F

   c) Design the single stage of Arithmetic and logical unit and draw the functional table of the same. Include the shifter circuit for the same. Design a hardware circuit to implement logical shift, arithmetic shift and circular shift operations. State your design specifications.

2. a) Show how the addition is performed in a single bus organization, if the operands are available in two registers R1 and R2?

   b) i) What is a micro program sequencer? With a block diagram, explain the working of micro program sequencer .

   ii) Define the acronyms CISC and RISC and explain the fundamental differences between the two architectures.

   c) With the help of a flow chart, explain the fetch and execute cycle of the basic CPU.

No of Pages : 2 **Course Code : 15XW25**

3. a) What do you mean by locality of reference? State how different policies of writing into cache are implemented.

   b) Calculate the hit and miss using various replacement policies for the following sequences (Page frame 3) 4,7,3,0,1,7,3,8,5,4,5,3,4,7. State which one is better for the above example.

   c) (i) Explain the Virtual memory architecture with suitable diagrams. Show with an example, how the virtual address is converted into real address in a paged virtual memory system.

   (OR)

   (ii) A computer has 64MB byte addressable main memory. A proposal is made to design a 1 MB cache memory with a block size of 64 bytes.

   i) Show how the memory address bits would be allocated from a direct mapped cache organization.

   ii) Repeat (i) for a four way set associative cache organization.

   iii) Given the direct mapped organization and ignoring any extra bits, what would be the overall size of the memory used to implement the cache? (Tag bits, Index Bits etc.,)

   iv) Which lines of the direct mapped cache could main memory location $1E0027A_{16}$ map into? Give the memory address (in hexadecimal) of another location that could not reside in cache at the same time as this one, if such a location exists.

4. a) What are handshaking signals? Why does asynchronous data transfer require handshaking signals?

   b) State two limitations of programmed I/O method of data transfer scheme. How are these limitations eliminated in DMA? Explain this method with the help of basic diagram showing CPU, memory and DMA controller connectivity. The DMA block in the diagram is to be drawn with its essential components.

   c) How does a basic computer handle an interrupt? Discuss the process of interrupt initiated IO and its advantage over the programmed I/O. With suitable diagrams, explain the different ways by which priority interrupts are handled.

5. a) How are vectored and non vectored interrupts different? Show an example.

   b) What is Flynn's taxonomy of Multiprocessor organisation? Explain with suitable diagram

   c) (i) Explain about the interconnection structures used in multiprocessor systems.

   (OR)

   (ii) Discuss how pipelining improves the performance of a system. Derive the speed up ratio for a pipelined system.

/END/

FD/RL