No of Pages : 2 **Course Code : 12XW25**

Roll No:
(To be filled in by the candidate)

PSG COLLEGE OF TECHNOLOGY, COIMBATORE - 641 004

SEMESTER EXAMINATIONS, AUGUST / SEPTEMBER - 2015

MSc - SOFTWARE SYSTEMS Semester : 2

12XW25 COMPUTER ORGANIZATION

Time : 3 Hours **Maximum Marks : 100**

INSTRUCTIONS:

1. Answer **ALL** questions from GROUP – I.
2. Answer any **5** questions from GROUP – II.
3. Answer any **ONE** question from GROUP – III.
4. Ignore the box titled as **"Answers for Group III"** in the Main Answer Book.

GROUP - I **Marks : 10 x 3 = 30**

1. What is the difference between 1's complement subtraction and 2's complement subtraction of binary numbers? Show it by example.
2. The following register transfer statements specify a memory operation . What is the memory operation in each case.

   R2←M[AR]

   M[AR]←R3

   R5←M[R5]
3. What is the difference between a direct and an indirect address instruction? How many references to memory are needed for each type of instruction to bring an operand into a processor register?
4. What is meant by memory interleaving? Show the distribution of addresses for a memory system consisting of two banks of four 1K memory modules to form an 8K memory system. Give the main memory address format.
5. What are the basic differences between a branch instruction, a call subroutine instruction, and program interrupt?
6. Justify the need for a page replacement algorithm in memory management and list the two types.
7. Define the following: (a) microoperation; (b) microinstruction; (c) microprogram; (d) microcode.
8. What are the functions of an Communication Interface in IO communication?
9. In a memory system having a address space of 8K and a memory space of 4K words with a page and block sixe of 1K words each. If the following page references are made by the CPU , determine the four pages that may reside in the memory at the end, if FIFO policy is used

   4 2 0 1 2 6 1 4 0 1 0 2 3 5 7
10. Define Pipelining and determine the number of clock cycles that CPU takes to process 200 tasks in a six-segment pipeline.

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GROUP - II Marks : 5 x 10 = 50

11. a) What is the use of tristate buffer? Design a bus system for bus and memory transfer that would connect four registers of size 8 bits to the common bus. Explain how a memory transfer could take place. (8)

    b) Explain the micro operations related to the functions of the stack. (4)

12. a) With a suitable block diagram, explain the functioning of a control unit. (6)

    b) The content of the top of a memory stack is 5320. The content of the stack pointer SP is 3560. A two-word call subroutine instruction is located in memory at address 1120 followed by the address field of 6720 at location 1121. What are the content of PC, SP, and the top of the stack:

    i) Before the call instruction is fetched from memory?

    ii) After the call instruction is executed?

    iii) After the return from subroutine?

13. Justify the need for an Asynchronous Communication Interface in IO communication and describe the features of asynchronous communication interface.

14. Explain in detail the different methods of mapping used in Cache memory organisation, with suitable examples. Show how the contents of the cache memory are initialised and the main memory is updated.

15. Justify the need for DMA in interfacing an I/O device to a processor using DMA? Explain how DMA performs data transfer with the help of neat diagram.

16. Discuss on the process of interrupt initiated IO and its advantage over the programmed IO. How does a basic computer handle an interrupt and with suitable diagrams, explain the different ways by which priority interrupts are handled.

GROUP - III Marks : 1 x 20 = 20

17. What are reasons of pipeline conflicts in pipelined processor and how are they resolved? Justify how pipelining in the CPU design would improve the performance of CPU. Illustrate with the following case study.

    In certain scientific computations it is necessary to perform the arithmetic operation with a stream of numbers. Specify a pipeline configuration to carry out this task (Ai + Bi) (Ci + Di) listing the contents of all registers in the pipeline for i = 1 through 6.

18. Why page-table is required in a virtual memory system and List the different ways of organizing a page table and the memory mapping techniques. Discuss the segmented memory mapping techniques with suitable example.

/END/

FD/JU