**No of Pages : 2** **Course Code : 15XW25**

Roll No:
(To be filled in by the candidate)

**PSGCOLLEGE OF TECHNOLOGY, COIMBATORE - 641 004**

**SEMESTER EXAMINATIONS MAY - 2016**

**MSc - SOFTWARE SYSTEMS Semester : 2**

**15XW25 COMPUTER ORGANISATION**

**Time : 3 Hours** **Maximum Marks :100**

**INSTRUCTIONS:**

1. Answer **ALL** questions from GROUP – I.
2. Answer any **5** questions from GROUP – II.
3. Answer any **ONE** question from GROUP – III.
4. Ignore the box titled as **"Answers for Group III"** in the Main Answer Book.

**GROUP - I** **Marks : 10 x 3 = 30**

1. With suitable examples, show how an arithmetic overflow is detected by the hardware.
2. Show how the multiple devices connected to a common bus are allowed to communicate only one at a time.
3. The following register transfer statements specify a memory operation. What is the memory operation carried out in sequence?

   R2←M[AR];R3 ←M[AR+1] ; R2← R2+R3 ; M [AR] ←R3
4. What do you mean by content accessible memory and state its use?
5. What is the difference between the temporal and spatial locality of reference?
6. State the purpose of FGI and FGO flags in IO communication.
7. What are the differences between internal, software and external interrupts?
8. Strobe control mechanism for asynchronous data transfer does not ensure whether the data transmitted by source unit is accepted by the destination unit. Suggest possible enhancements to this mechanism to overcome this limitation.
9. What happens in a daisy chain priority interrupt when device 1 requests an interrupt after device 2 has sent an interrupt request to the CPU but before the CPU responds with the interrupt acknowledge?
10. What are the reasons for the pipeline conflict in a pipelined processor? Determine the number of clock cycles that it takes to process 200 tasks in a six-segment pipeline.

**GROUP - II** **Marks : 5 x 10 = 50**

11. a) Design an arithmetic circuit with one selection variable S and two n-bit data inputs A and B. The circuit generates the following four arithmetic operations in conjunction with the input carry $C_{in}$ Draw the logic diagram for the first two stages

| $S$ | $C_{in} = 0$ | $C_{in} = 1$ |
|---|---|---|
| 0 | $D = A + B$ (add) | $D = A + 1$ (increment) |
| 1 | $D = A - 1$ (decrement) | $D = A + \overline{B} + 1$ (subtract) |

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b) The operations to be performed with flip flop F are specified by the following register transfer statements. Otherwise, the contents must not change. Draw the logic diagram showing the connections of the gates that form the control functions and the input of the flip flop F. Use a JK flip flop with minimum number of gates.

$xT_3$ : F← 1 Set F to 1

$yT_1$ : F← 0 Reset F to 0

$zT_2$ : F←F' Set F to F'

$wT_5$: F← G Transfer value of G to F

12. a) With the help of a flow chart explain the fetch and execute cycle of the basic CPU with interrupts.

b) Explain why each of the following micro operations cannot be executed during a single clock pulse in the system. Specify a sequence of micro operations that will perform the following operations.

i) IR← M [PC]

ii) AC ← AC + TR

iii) DR←DR + AC

13. a) Why page-table is required in a virtual memory system? List the different ways of organizing a page table and the memory mapping techniques.

b) Justify the need for an interface in IO communication. With a diagram, explain the functions of asynchronous communication interface.

14. What are ways by which the main memory is updated while cache memory is accessed? Explain how the direct mapping is different from set associative mapping in cache memory.

15. What is the need for DMA in interfacing an I/O device to a processor using DMA? Explain how DMA performs data transfer with the help of neat diagram.

16. a) Write short notes on memory stacks and also explain how stacks are effectively used for evaluating arithmetic expressions with an example.

b) With suitable diagrams, explain the three computer architectural classification schemes in parallel processing.

## GROUP - III Marks : 1 x 20 = 20

17. What are reasons of pipeline conflicts in pipelined processor and how are they resolved?Explain how pipelining in the CPU design would improve the performance of CPU.by illustrating with the following case study:

In certain scientific computations it is necessary to perform the arithmetic operation with a stream of numbers. Specify a pipeline configuration to carry out this task (Ai + Bi) (Ci + Di) listing the contents of all registers in the pipeline for i = 1 through 6.

18. With suitable diagram, discuss how the interrupts are recognized by the CPU. Explain the various ways in which the interrupts from multiple devices are handled.

**/END/**

**FD/RL**