No of Pages : 3 Course Code : 15XW25

Roll No:

(To be filled in by the candidate)

PSG COLLEGE OF TECHNOLOGY, COIMBATORE - 641 004

SEMESTER EXAMINATIONS, SEPTEMBER / OCTOBER 2018

MSc - SOFTWARE SYSTEMS Semester : 2

15XW25 COMPUTER ORGANIZATION

Time : 3 Hours **Maximum Marks : 100**

INSTRUCTIONS:

1. Answer **ALL** questions. Each question carries 20 Marks.
2. Subdivision (a) carries 3 marks each, subdivision (b) carries 7 marks each and subdivision (c) carries 10 marks each.

1. a) The following register transfer statements specify a memory operation. What is the memory operation in each case?

   R2←M[AR]

   M[AR]←R3

   R5←M[R5]

   b) Explain how a set of registers are connected to a common bus. Discuss the two approaches with a suitable diagram, by taking 2 registers of 8 bits each.

   c) Design the single stage of a 4 bit Arithmetic and logical unit and draw the functional table of the same. Use appropriate selection variables. Show the logic diagram of one typical stage.

2. a) What is the difference between a direct and an indirect address instruction? How many references to memory are needed for each type of instruction to bring an operand into a processor register?

   b) Derive the control gates for the write input and read input of the memory in the basic computer. Make use of the table given below

   c) Draw the block diagram of the control unit and explain its function with reference to the basic architecture. Draw the interrupt cycle of the basic computer and explain how the system responds to an interrupt with an example. Also explain the IO operation with reference to the FGI and FGO flags.

Fetch	$R'T_0$:	$AR \leftarrow PC$
	$R'T_1$:	$IR \leftarrow M[AR]$, $PC \leftarrow PC + 1$
Decode	$R'T_2$:	$D_0, \ldots, D_7 \leftarrow$ Decode $IR(12\text{–}14)$,
		$AR \leftarrow IR(0\text{–}11)$, $I \leftarrow IR(15)$
Indirect	D_7IT_3:	$AR \leftarrow M[AR]$
Interrupt:		
$T_0'T_1'T_2'(IEN)(FGI + FGO)$:		$R \leftarrow 1$
	RT_0:	$AR \leftarrow 0$, $TR \leftarrow PC$
	RT_1:	$M[AR] \leftarrow TR$, $PC \leftarrow 0$
	RT_2:	$PC \leftarrow PC + 1$, $IEN \leftarrow 0$, $R \leftarrow 0$, $SC \leftarrow 0$
Memory-reference:		
AND	D_0T_4:	$DR \leftarrow M[AR]$
	D_0T_5:	$AC \leftarrow AC \wedge DR$, $SC \leftarrow 0$
ADD	D_1T_4:	$DR \leftarrow M[AR]$
	D_1T_5:	$AC \leftarrow AC + DR$, $E \leftarrow C_{out}$, $SC \leftarrow 0$
LDA	D_2T_4:	$DR \leftarrow M[AR]$
	D_2T_5:	$AC \leftarrow DR$, $SC \leftarrow 0$
STA	D_3T_4:	$M[AR] \leftarrow AC$, $SC \leftarrow 0$
BUN	D_4T_4:	$PC \leftarrow AR$, $SC \leftarrow 0$
BSA	D_5T_4:	$M[AR] \leftarrow PC$, $AR \leftarrow AR + 1$
	D_5T_5:	$PC \leftarrow AR$, $SC \leftarrow 0$
ISZ	D_6T_4:	$DR \leftarrow M[AR]$
	D_6T_5:	$DR \leftarrow DR + 1$
	D_6T_6:	$M[AR] \leftarrow DR$, if $(DR = 0)$ then $(PC \leftarrow PC + 1)$, $SC \leftarrow 0$

3. a) A computer uses a memory unit with 256K words of 32 bits each. A binary instruction code is stored in one word of memory. The instruction has four parts: an indirect bit, an operation code, a register code part to specify one of 64 registers, and an address part.

   i). How many bits are there in the operation code, the register code part, and address part?

   ii) Draw the instruction word format and indicate the number of bits in each part.

   iii) How many bits are there in the data and address inputs of the memory?

   b) Describe the various cache memory mapping techniques , with an example.

   c) i) Draw the hardware organization of associative memory and explain how it works in mapping the virtual address into physical memory address. Deduce the logic equation used to find the match in the associative memory.

   (OR)

   ii) What is virtual memory? Explain how the logical address is translated into physical address in the virtual memory system with a neat diagram. Explain the virtual memory address translation and TLB with necessary diagram.

4. a) What are the two ways of addressing the IO devices and mention the merits of each scheme.

b) i) Justify the need for an Asynchronous Communication Interface in IO communication and describe the features of asynchronous communication interface, with suitable diagram

ii) The content of the top of a memory stack is 5320. The content of the stack pointer SP is 3560. A two-word call subroutine instruction is located in memory at address 1120 followed by the address field of 6720 at location 1121. What are the content of PC, SP, and the top of the stack:

i. Before the call instruction is fetched from memory?

ii. After the call instruction is executed?

iii. After the return from subroutine?

c) State two limitations of programmed I/O method of data transfer scheme. How are these limitations eliminated in DMA? Explain this method with the help of basic diagram showing CPU, memory and DMA controller connectivity. The DMA block in the diagram is to be drawn with its essential components.

5. a) How does a basic computer handle an interrupt? Explain what happens during the interrupt with the help of an example.

b) Describe various interconnection structures used in a multiprocessor system for connecting the processor with the memory modules..

c) Explain in detail how the multiple priority interrupts are handled through hardware, by the CPU.

/END/

FD/RL