No of Pages : 3 **Course code: 18XW25**

Roll No:
(To be filled in by the candidate)

PSG COLLEGE OF TECHNOLOGY, COIMBATORE - 641 004

SEMESTER EXAMINATIONS, APRIL 2019

MSc - SOFTWARE SYSTEMS Semester : 2

18XW25 COMPUTER ORGANIZATION

Time : 3 Hours **Maximum Marks : 100**

INSTRUCTIONS:

1. Answer **ALL** questions. Each question carries 20 Marks.
2. Subdivision (a) carries 3 marks each, subdivision (b) carries 7 marks each and subdivision (c) carries 10 marks each.
3. Course Outcome : Table

Qn.1	CO.1	Qn.2	CO2	Qn.3	CO3	Qn.4	CO4	Qn.5	CO5

1. a) Why is biased exponent required in IEEE floating point representation? Suppose there was a large floating point representation which used 8 bits for the exponent. If the exponent was represented using a bias, what would you expect the bias to be?

   b) i) What value is represented by the given number in IEEE 754 single precision format? **0 1000 0000 110 0000 0000 0000 0000 0000.** Is the number normalized? If not, represent in normalized form.

   ii) Register B has initial value of **11011000**. Write sequence of arithmetic/ logical operations to

   - clear 3rd and 4th bits in register B without affecting other bits
   - swap the two nibbles of register B.

   c) Design hardware circuits to implement Arithmetic, logical and shift operations. Integrate them to build a 4 bit ALU and represent the ALU operations through a function table. State your design specifications

2. a) While designing the instruction format of a computer, what factors are to be considered in fixing the length of the instruction? Show with an example.

   b) i) Consider a hypothetical 32-bit microprocessor having 32-bit instructions composed of two fields. The first byte contains the opcode and the remainder the immediate operand or an operand address (3)

   - What is the maximum directly addressable memory capacity (in bytes)? Assume memory is byte addressable.
   - How many bits are needed for the PC, IR, MBR and MAR registers?
   - What is the maximum memory address space that the processor can access directly if it is connected to a 32-bit memory?

   ii) Suppose that the instruction set of a machine has three instructions: Inst-1,Inst-2, and Inst-3; A, B, C, D, E, F, G, and H are the control lines. The following table shows the control lines that should be activated for the three instructions at the three steps T0, T1, and T2. Write Boolean expressions for all the control lines A–G (4)

Step	Inst-1	Inst-2	Inst-3
T0	D, B, E	F, H, G	E, H
T1	C, A, H	G	D, A, C
T2	G, C	B, C	

c) Explain the functioning of a control unit with the help of a block diagram. Describe the interrupt routine of the CPU along with the flowchart.

3. a) How are the changes in the cache write operation reflected in the main memory? Highlight the difference between cache write IO policies with reference to the following:

- the relative frequency of memory access
- the ability of multiple CPU systems to keep cache coherency

b) i) Consider the following stream of page requests: 1,2,3,4,5,1,2,3,4,5,1,2,3,4,5.Assume that the main memory consists of FOUR page frames. Show a trace of the status of the page frames in the main memory module and estimate the hit ratio for LRU page replacement algorithms.

ii) Suppose physical addresses are 32 bits wide; Addresses are to the word; a cache block contains 2048 bits of data and there are 2048 blocks in the cache; Data words are 32 bits each: Referring to the above specifications, specify how the 32 bit address would be partitioned for each of the following cache configurations:

- Direct mapped
- 2-way set associative

c) i) Draw the hardware organization of associative memory and explain how it works in mapping the logical address into physical memory address. Deduce the logic equation used to find the match in the associative memory

(OR)

ii) Explain the concept of virtual memory and why is it needed in the computer? Discuss the ways in which the Virtual addresses are mapped to physical addresses using Page Table with suitable diagrams.

4. a) How are the IO devices addressed by the CPU? Mention the merits of each scheme.

b) i) What entities in a computer system does a device driver communicate with? What are the functions of a device driver? Describe the features of asynchronous communication interface (device driver) , with suitable diagram .

ii) Assume that a program wants to copy a 500 word of data from an I/O device to memory. Complete the following table for each I/O technique.

	Programmed I/O	Interrupt driven I/O	DMA data transfer
Total no of interrupts for a block transfer			
Total no of READ IO commands issued by the CPU to the IO module			

c) i) What is the need for DMA in interfacing an I/O device to a processor using DMA?. Explain how DMA performs data transfer with the help of a neat diagram

(OR)

ii) Consider a computer without priority interrupt hardware. Explain how priority can be established in the interrupt service program? Also explain various methods by which the simultaneous interrupts from multiple devices are handled using hardware .

5. a) What are the different computer architectural classification schemes in parallel processing?

b) Differentiate between tightly coupled multiprocessors and loosely coupled multiprocessors from the view point of hardware organization. Discuss the different types of interconnection structures the CPU, IOPs and Memory modules.

c) Explain how pipelining in the CPU design would improve the performance of CPU by illustrating with the following case study:

Consider a pipeline with 4 stages: FI (Fetch Instruction), DA (Decode instruction and Calculate Address), FO (Fetch Operands) and EX (Execute). Draw the Timing Diagram for Instruction Pipeline operation for a sequence of 7 instructions, in which the third instruction is a branch instruction and there are no data dependencies.

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