No of Pages :2 **Course Code : 12XW25**

Roll No:
(To be filled in by the candidate)

PSGCOLLEGE OF TECHNOLOGY, COIMBATORE - 641 004

SEMESTER EXAMINATIONS, FEBRUARY / MARCH - 2016

MSc - SOFTWARE SYSTEMS Semester :2

12XW25 COMPUTER ORGANIZATION

Time : 3 Hours **Maximum Marks :100**

INSTRUCTIONS:

1. Answer **ALL**questions from GROUP – I.
2. Answer any **5** questions from GROUP – II.
3. Answer any **ONE**question from GROUP – III.
4. Ignore the box titled as **"Answers for Group III"** in the Main Answer Book.

GROUP - I **Marks : 10 x 3 = 30**

1. How does the CPU recognize the negative result in 2's complement subtraction? Justify your answer with an example.
2. An 8 bit register contains the binary value **10011100.** What is the register value after arithmetic shift right? Starting from the initial number **10011100**, determine the register value after an arithmetic shift left, and state whether there is an overflow.
3. Show the hardware that implements the following statement. Include the logic gates for the control function and the block diagram for the binary counter with a count enable input.

   $xy\ T_0 + T_1 + y'T_2$: AR ← AR +1
4. How many 128 x 8 RAM chips are needed to provide a memory capacity of 2048 bytes? How many lines of the address bus must be used to access 2048 bytes of memory?
5. What is the difference between a direct and an indirect address instruction? How many references to memory are needed for each type of instruction to bring an operand into a processor register?
6. A digital computer has a memory unit of 64 K x 16 and a cache memory of 1K words. The cache uses direct mapping with a block size of four words. How many bits are there in the tag, index, block and word fields of the address format? How many blocks can the cache accommodate?
7. Differentiate between hardwired and micro programmed control unit.
8. What is the need for a page replacement algorithm in memory management and list the two types.
9. What do you understand by Hit Ratio in Cache memory?
10. Define SIMD processor with the outline sketch.

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GROUP - II Marks : 5 x 10 = 50

11. a) Explain the significance of different fields of an instruction with an example. (4+6)

    b) List and explain all the phases of an instruction cycle with interrupts using a flowchart.

12. a) Explain with neat diagram the all the registers of a CPU could be connected through a common bus system. What the use of a tristate buffer. (5+5)

    b) What is a micro program? Write a micro program for the fetch routine of an instruction cycle.

13. a) Why does a DMA have priority over the CPU when both request a memory transfer? Explain how DMA transfer is accomplished with a neat diagram. (6+4)

    b) Discuss some of the interconnection structures used in connecting the multiprocessors and the memory modules.

14. a) Explain the organization of control memory and its operation with a block diagram. (5+5)

    b) What is a micro program sequencer? With block diagram, explain the working of micro program sequencer.

15. Discuss the various mapping functions used for mapping main memory blocks into cache memory.

16. Write short notes on any TWO of the following. (5+5)

    (i) Handshaking method of data transfer

    (ii) Associative memory

    (iii) Interrupt handling

GROUP - III Marks : 1 x 20 = 20

17. Describe with the help of a block diagram and necessary circuits how multiple matched words can be read from an associative memory?

18. Justify how pipelining in the CPU design would improve the performance of CPU. What are reasons of pipeline conflicts in pipelined processor and how are they resolved?Discuss the different pipelining concepts with suitable examples.

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/END/

FD/JU