No of Pages : 2 Course code: 15XW25

Roll No:
(To be filled in by the candidate)

PSG COLLEGE OF TECHNOLOGY, COIMBATORE - 641 004

SEMESTER EXAMINATIONS, APRIL 2019 (PHASE I)

MSc - SOFTWARE SYSTEMS Semester : 2

15XW25 COMPUTER ORGANIZATION

Time : 3 Hours **Maximum Marks : 100**

INSTRUCTIONS:

1. Answer **ALL** questions. Each question carries 20 Marks.
2. Subdivision (a) carries 3 marks each, subdivision (b) carries 7 marks each and subdivision (c) carries 10 marks each.

1. a) What are the operations that lead to arithmetic overflow? With suitable examples, show how an arithmetic overflow is detected by the hardware.

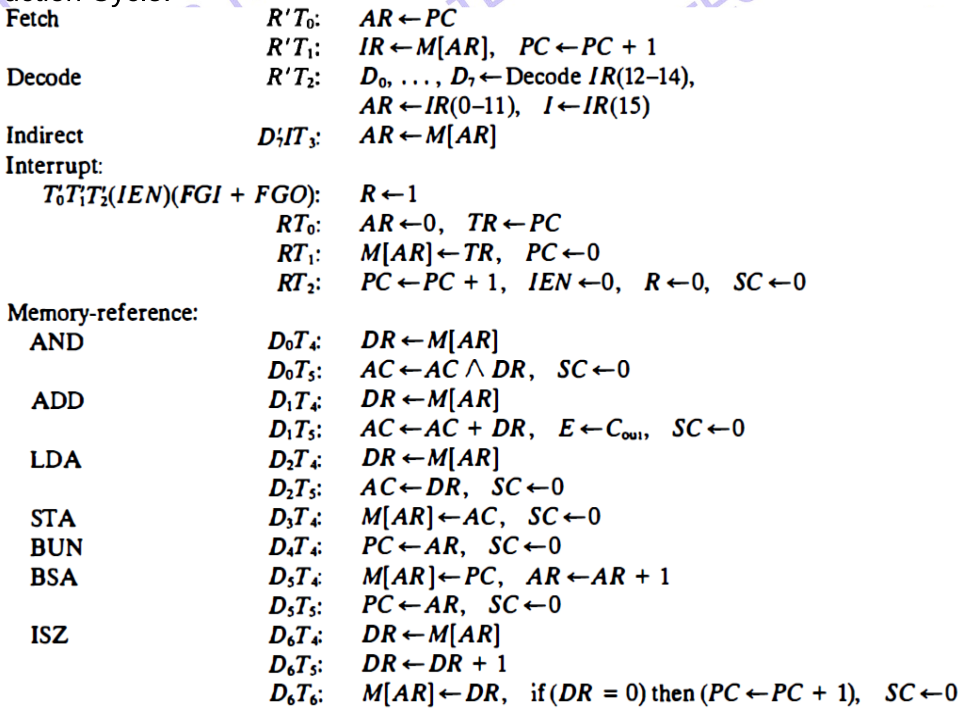
   b) Discuss the two approaches of connecting set of registers to a common bus with a suitable diagram, by taking 4 registers of 8 bits each.

   c) Design a hardware circuit to implement logical shift, arithmetic shift and circular shift operations. State your design specifications and function table.

2. a) What are the basic operations on a stack? Register R5 is used in a program to point to the top of the stack. Write a sequence of instruction to POP the two top items off the stack, add them and PUSH the result onto the stack

   b) Derive the control gates for the write input and read input of the memory in the basic computer. Make use of the table given below

   c) Explain the functioning of a control unit with the help of a block diagram. Write a micro program for the fetch routine of the CPU along with the flowchart for the Instruction Cycle.



Fetch	$R'T_0$:	$AR \leftarrow PC$
	$R'T_1$:	$IR \leftarrow M[AR], \quad PC \leftarrow PC + 1$
Decode	$R'T_2$:	$D_0, \ldots, D_7 \leftarrow \text{Decode } IR(12\text{–}14)$, $AR \leftarrow IR(0\text{–}11), \quad I \leftarrow IR(15)$
Indirect	$D_7'IT_3$:	$AR \leftarrow M[AR]$
Interrupt:		
$T_0'T_1'T_2'(IEN)(FGI + FGO)$:		$R \leftarrow 1$
	RT_0:	$AR \leftarrow 0, \quad TR \leftarrow PC$
	RT_1:	$M[AR] \leftarrow TR, \quad PC \leftarrow 0$
	RT_2:	$PC \leftarrow PC + 1, \quad IEN \leftarrow 0, \quad R \leftarrow 0, \quad SC \leftarrow 0$
Memory-reference:		
AND	D_0T_4:	$DR \leftarrow M[AR]$
	D_0T_5:	$AC \leftarrow AC \wedge DR, \quad SC \leftarrow 0$
ADD	D_1T_4:	$DR \leftarrow M[AR]$
	D_1T_5:	$AC \leftarrow AC + DR, \quad E \leftarrow C_{out}, \quad SC \leftarrow 0$
LDA	D_2T_4:	$DR \leftarrow M[AR]$
	D_2T_5:	$AC \leftarrow DR, \quad SC \leftarrow 0$
STA	D_3T_4:	$M[AR] \leftarrow AC, \quad SC \leftarrow 0$
BUN	D_4T_4:	$PC \leftarrow AR, \quad SC \leftarrow 0$
BSA	D_5T_4:	$M[AR] \leftarrow PC, \quad AR \leftarrow AR + 1$
	D_5T_5:	$PC \leftarrow AR, \quad SC \leftarrow 0$
ISZ	D_6T_4:	$DR \leftarrow M[AR]$
	D_6T_5:	$DR \leftarrow DR + 1$
	D_6T_6:	$M[AR] \leftarrow DR, \quad \text{if } (DR = 0) \text{ then } (PC \leftarrow PC + 1), \quad SC \leftarrow 0$

3. a) Comment on the use of the two methods of updating the cache memories in the context of cache systems.

   b) i) Consider a memory system having 16K of main memory with 12 K of RAM and 4 K of ROM. The RAM and ROM memory chips are available in 2K x 8 and 1K x 8 sizes respectively. Draw the memory map showing the addresses in Binary and in Hexadecimal. Draw the interface circuit connecting the CPU to memory. (4)

   ii) The access time of a cache memory is 100 ns and that of main memory is 1000 ns. It is estimated that 80 percent of the memory requests are for read and the remaining 20 percent are for write. The hit ratio of read access only is 0.9. A write through procedure is used. For the above scenario, calculate the following: (3)

   1) average access time of the system considering only the memory read cycle

   2) hit ratio taking into consideration, the read cycles.

   c) I) Explain the concept of virtual memory address mapping using a Page Table with suitable diagrams .

   (OR)

   II) Draw the hardware organization of associative memory and explain how it works in mapping the virtual address into physical memory address. Deduce the logic equation used to find the match in the associative memory

4. a) What are the two ways of addressing the IO devices and mention the merits of each scheme

   b) What is handshaking in asynchronous data transfer and state its purpose. Justify the need for an Asynchronous Communication Interface in IO communication and describe the features of asynchronous communication interface, with suitable diagram.

   c) What is the advantage of interrupt imitated data transfer over transfer under program control without an interrupt? With suitable diagram, discuss how the interrupts are recognized by the CPU. Explain the various ways in which the interrupts from multiple devices are handled.

5. a) What are the different computer architectural classification schemes in parallel processing?

   b) Differentiate between tightly coupled multiprocessors and loosely coupled multiprocessors from the viewpoint of hardware organization. Discuss the different types of interconnection structures the CPU, IOPs and Memory modules.

   c) Explain how pipelining in the CPU design would improve the performance of CPU by illustrating with the following case study:

   In certain scientific computations it is necessary to perform the arithmetic operation with a stream of numbers. Specify a pipeline configuration to carry out this task (A_i + Bi) (C_i + D_i) listing the contents of all registers in the pipeline for i = 1 through 6.

   What are reasons of pipeline conflicts in pipelined processor and how are they resolved

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