No of Pages : 2 Course Code : 12XW25

Roll No:
(To be filled in by the candidate)

PSG COLLEGE OF TECHNOLOGY, COIMBATORE - 641 004

SEMESTER EXAMINATIONS, MAY - 2013

MSc - SOFTWARE ENGINEERING Semester : 2

12XW25 COMPUTER ORGANIZATION

Time : 3 Hours **Maximum Marks : 100**

INSTRUCTIONS:

1. Group I, Group II and Group III questions should be answered in the Main Answer Book.
2. Ignore the box titled as **"Answers for Group III"** in the Main Answer Book.
3. Answer **ALL** questions from GROUP – I.
4. Answer any **FIVE** questions from GROUP – II.
5. Answer any **ONE** question from GROUP – III.

GROUP - I **Marks : 10 x 3 = 30**

1. Compute the arithmetic operations (+70) + (+80) and (-70) + (-80) with binary numbers in signed-2's complement representation. Use eight bits to accommodate number with its sign. Check whether there is an overflow.
2. Can the contents of two registers be exchanged during one common clock pulse? Justify your answer.
3. Differentiate arithmetic and logical shift right?
4. What is an instruction cycle? Write the sequence of steps to execute LDA instruction.
5. Write the machine (assembly) code for the following high level program.

```
if( a > b)
a=1;
else
b=1;
```

6. The control memory in micro programmed control unit has 1024 words of 32 bits each. The microinstruction has three fields namely select, address, and micro operation respectively. a) How many bits are there in the branch address field and the select field? b) If there are 16 status bits in the system, how many bits of the branch logic are used to select a status a status bit?
7. The content of the top of a memory stack is 5320. The content of the stack pointer SP is 3560. A two-word call sub routine instruction is located in memory at address 1120 followed by the address field of 6720 at location 1121. What are the content of PC, SP and top of the stack:

   i) Before the call instruction is fetched from memory?

   ii) After the call instruction is executed?

   iii) After the return from sub routine?

8. Why biasing is needed in floating point number representation? Justify with suitable example.
9. A two way set associative cache memory uses blocks of four words. The cache can accommodate a total of 2048 words from main memory. The main memory size is 128K x 32. Formulate all pertinent information required to construct the cache memory and what is the size of the cache memory?
10. How many switch points are there in a crossbar switch network that connects p processor to m memory modules?

GROUP - II Marks : 5 x 10 = 50

11. a) Explain the arithmetic and logic unit in detail.

    b) An instruction at address 021 in the basic computer has I =0, an operation code of AND instruction and an address part equal to 083. The memory word at address 083 contains the operand B8F2 and content of AC is A937. Go over the instruction cycle and find the contents of the following registers at the end of execute phase: PC, AR, DR, AC and IR.
12. Explain micro programmed control unit with suitable diagrams.
13. Explain the various CPU organizations in detail. Write a program to evaluate the arithmetic statement:

$$X = \quad X = \frac{A \quad B \quad C * (D \quad E * F)}{G \quad H * K}$$

    using general register with three addresses, two addresses, one address and zero address instructions.
14. Explain the Booth Multiplication algorithm. Assume 5-bit registers hold signed numbers, trace the multiplication (+15) x (-13) using Booth algorithm.
15. Explain cache memory and its different mapping procedures with necessary diagrams.
16. Discuss in detail various interconnection structures used in multiprocessor systems.

GROUP - III Marks : 1 x 20 = 20

17. a) Explain the memory hierarchy used in basic computer system. What is virtual memory? Explain how this memory enhances the main memory.

    b) A process contains eight pages on disk and is assigned a fixed allocation of four page frames in main memory. The following page trace occurs:

    1,0,2,2,1,7,6,7,0,1,2,0,3,0,4,5,1,5,2,4,5,6,7,6,7,2,4,2,7,3,3,2,3

    Show the successive pages residing in the four frames using LRU and FIFO replacement policy. Assume the frames are initially empty. Find the hit ratio and compare the two policies.
18. a) Explain the asynchronous data transfer in detail. What are the various modes of data transfer?

    b) Discuss in detail the DMA mode of data transfer. It is necessary to transfer 256 words from a magnetic disk to a memory section starting from address 1230. The transfer is by means of DMA. What are the initial values that the CPU must transfer to DMA controller and write step by step account of the actions taken during the input of first two words?

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