

# Lab notes

April 25, 2024

## 1 Lab-1

*How many clock cycles the tool estimates is the latency of the mmult hardware?*

Cycles: 366736 (3.66 ms)

*How many DSP blocks, BRAMs, FFs, and LUTs are used by the mmult hardware?*

DSP: 5

FF: 3651

LUT: 3816

BRAM: 16

*Q3*

1024

*Q4*

0x00 is AP\_START and AP\_STOP is present in the CTRL register.

*Q5*

2235 (22.3  $\mu$ s)

*Q6*

BRAM: 76

DSP: 160

FF: 20587

LUT: 28405

*Q7*

Interval: 1027 Loop1\_Loop2, Interval: 1191 Loop3\_Loop4

*Q8*

Cannot determine the interaction interval of the loops. The tool thinks that there is a data dependency between the loops.

Iteration Latency: - Loop1\_Loop2, Iteration Latency: - Loop3\_Loop4

## 2 Lab-2

- Q1* Slices LUTS: 11960
- Q2* Slice registers: 17289
- Q3* Block RAM tiles: 33.5
- Q4* DSPs: 160
- Q5* Worst negative slack: 0.317ns
- Q6* data path delay: 2.53 ns
- Q7* Logic delay: 0.124 ns (4.902%) and route: 2.406 ns (95.098%)
- Q8* LUTS in SLICEL: 4
- Q9* SLICEL registers: 8
- Q10* Inputs and outputs in LUT: 6 inputs and 2 outputs

### **3 Lab-3**

*Q1* The execution time was 124 us.

*Q2* 792 us