Battery Integrated Modular Multilevel Converters for Automotive Applications

Arvind Balachandran

LINKÖPING UNIVERSITY

Contributions

Design optimization Loss minimization, dc-link capacitor size vs switching frequency.
Experimental validation Harmonic allocations and loss distribution within a submodule.
Compaitirve analysis BI-MMC topologies with 2-level inverter.
DC charging Maximum DC charging power for BI-MMC topologies.

Topology overview

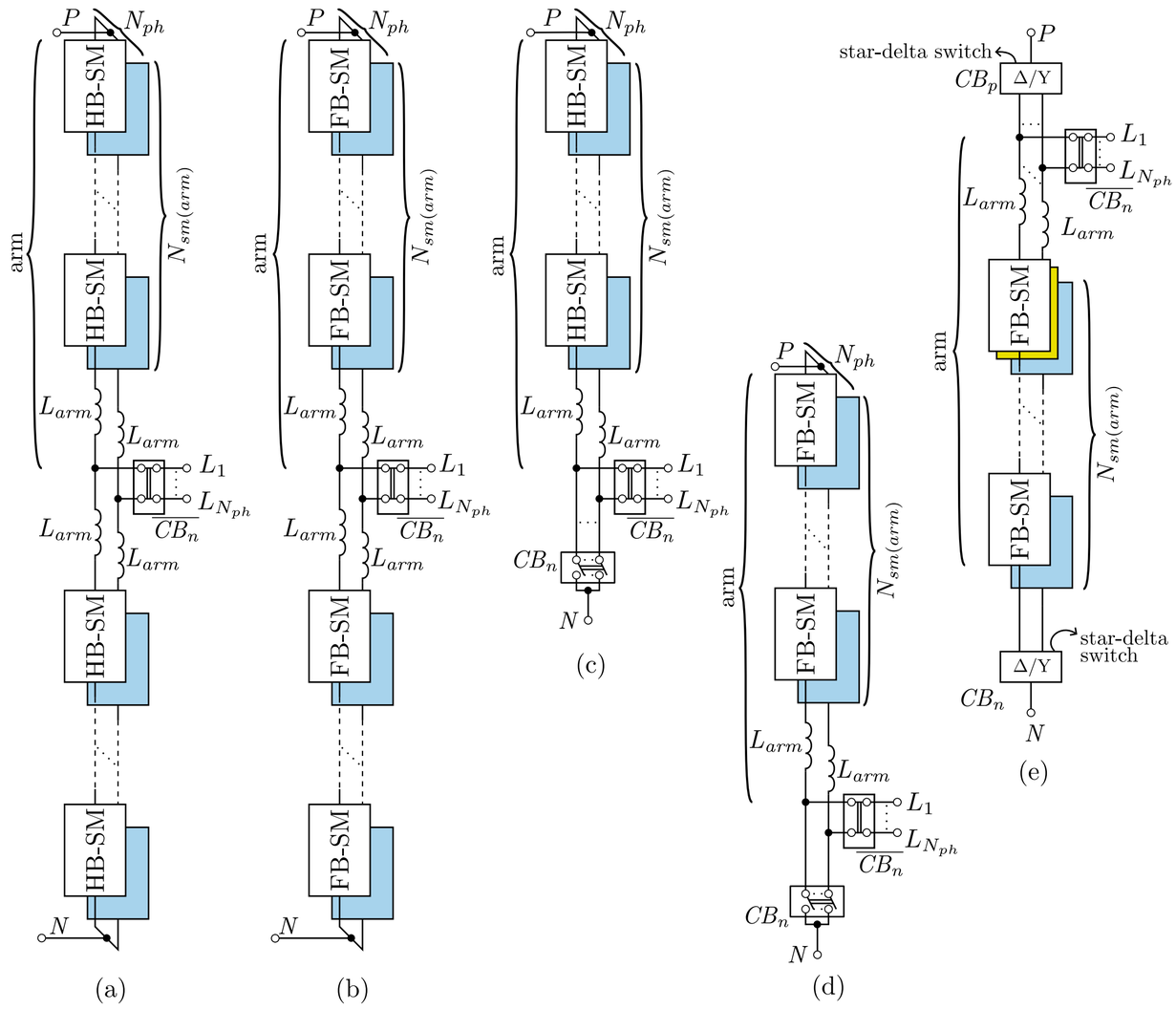
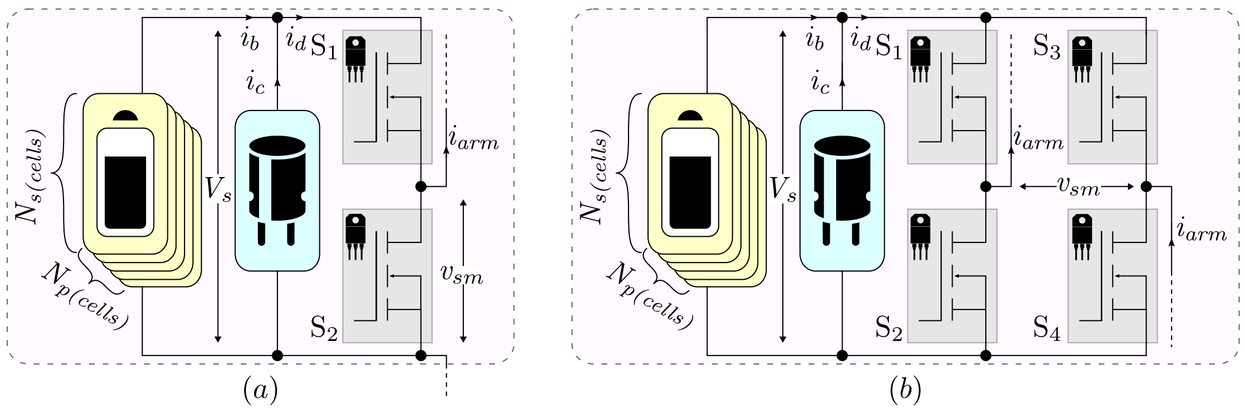


Figure: Double-star (DS), single-star (SS) with half-bridge (HB) and full-bridge (FB), and single-delta with FB.



(a) HB-SM $V_{sm(hb)} = M\dfrac{V_s}{2\sqrt{2}}$ (b) FB-SM $V_{sm(fb)} = M\dfrac{V_s}{\sqrt{2}}$

Submodule Loss distribution

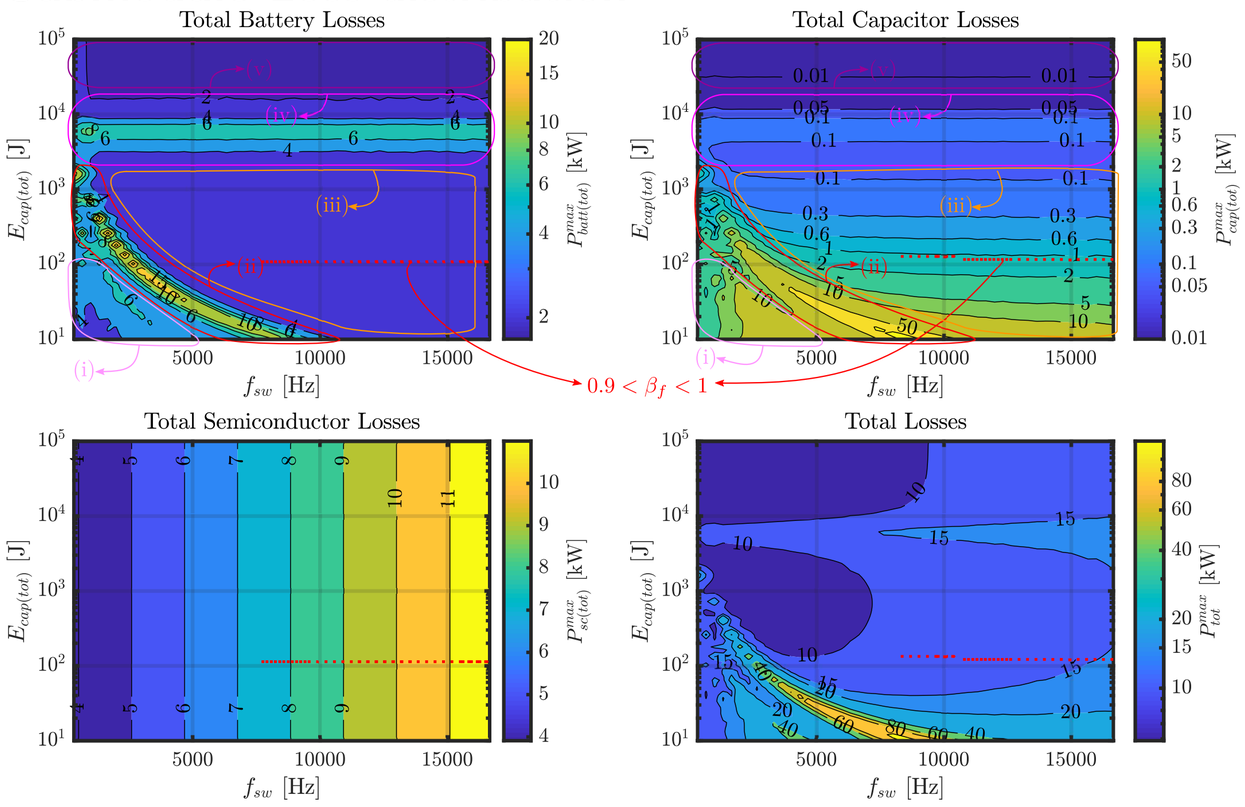


Figure: Losses for a 5-$N_{s(cells)}$, DSFB BI-MMC topology at a rated power of 400 kW.

region(i): $f_{sw} < f_{res}$ region(ii): $f_{sw} \approx f_{res}$ region(iii): $f_{sw} > f_{res}$ region(iv): $f_{sw} \approx 2\,f_1$ region(v): $f_{sw} > 2\,f_1$

$$f_{res} = \frac{1}{2\pi\sqrt{L_{\mathcal{B}} C_{cap}}} \qquad P^{\max}_{tot} = P^{\max}_{batt(tot)} + P^{\max}_{cap(tot)} + P^{\max}_{sc(tot)}$$

Battery and capacitor currents in a submodule

$I_{batt}(f_{sw}) < I_{cap}(f_{sw})$	$I_{batt}(f_{sw}) \approx I_{cap}(f_{sw})$	$I_{batt}(f_{sw}) > I_{cap}(f_{sw})$
$f_{sw} < f_{ref}$	$f_{sw} \approx f_{ref}$	$f_{sw} > f_{ref}$

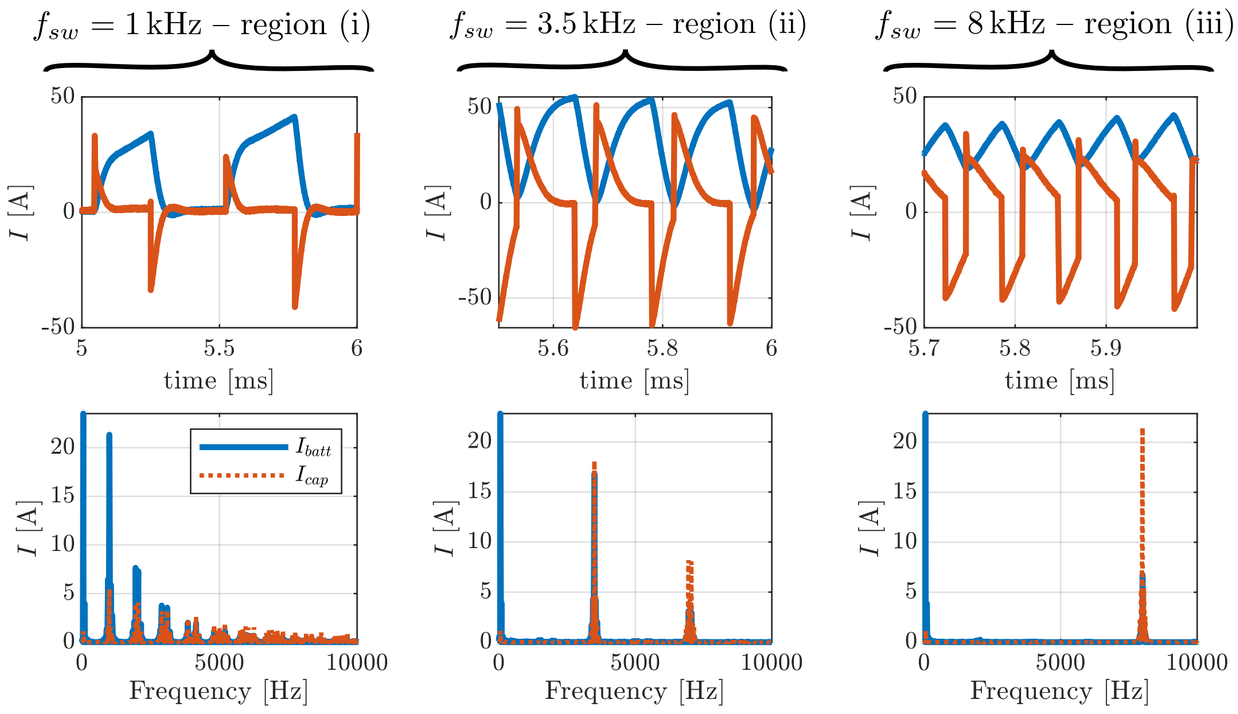
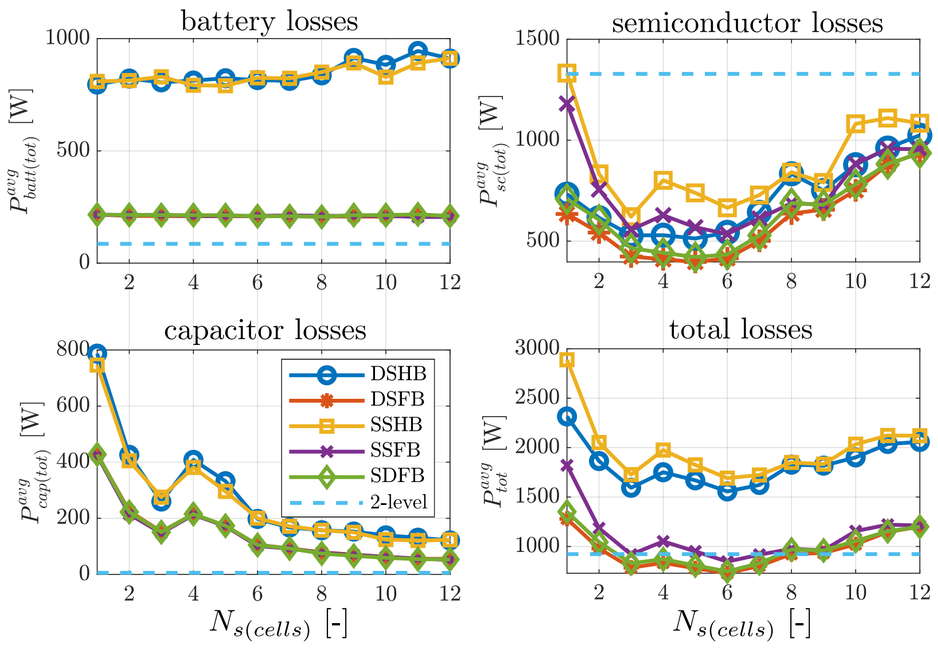


Figure: Current measurements on a 1-$N_{s(cells)}$, 15 V SSFB BI-MMC topology.

Power Losses

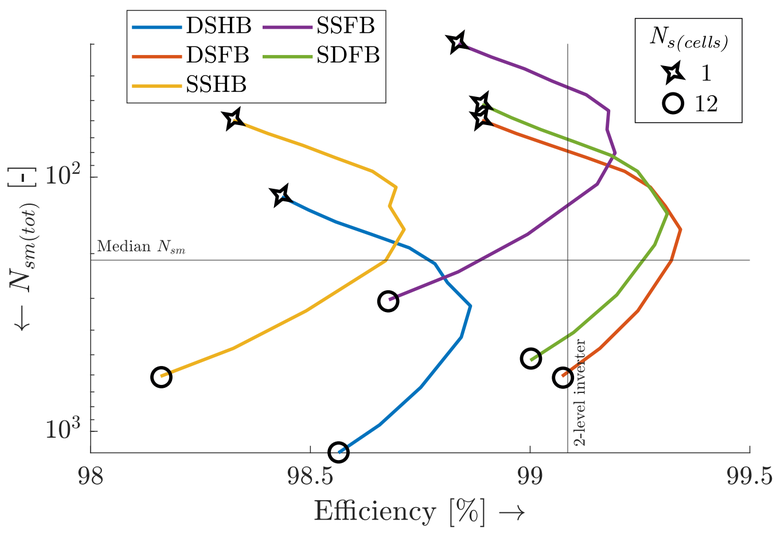


Total losses at 100 kW.

BI-MMC topologies have higher $P^{avg}_{batt(tot)}$ and $P^{avg}_{cap(tot)}$.

BI-MMC $P^{avg}_{sc(tot)}$ lower than 2-level inverter.

Performance Matrix (efficiency vs total submodules)



6 $N_{s(cells)}$ lowest losses, given topology.

FB topology lowest losses, given $N_{s(cells)}$.

Maximum DC charging power

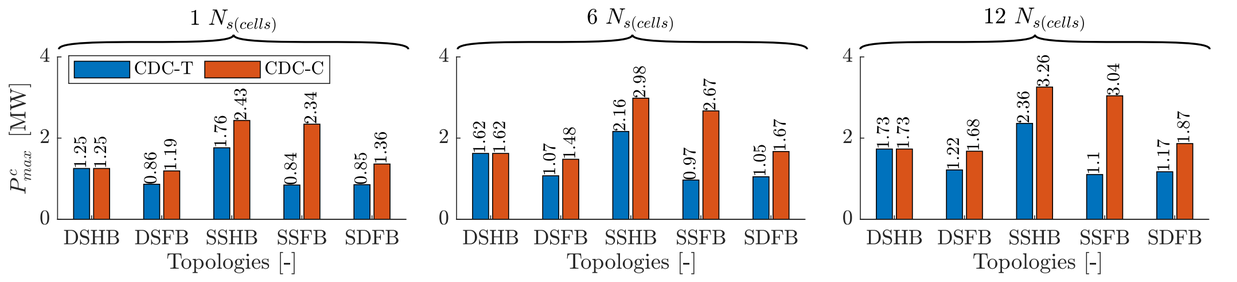


Figure: The losses during charging at P^c_{max} is equal to traction losses at 400 kW.

$N_{sm(tot)}$ based on traction voltage (CDC-T) and based on charger voltage (CDC-C).

Conclusions

Design optimization: DC-link capacitor and switching frequency choice such that $f_{sw} \neq f_{res}$.

Comparative analysis: BI-MMC topologies vs 2-level inverter:
Higher battery and capacitor losses, but Lower semiconductor losses.
Lower total losses for FB topologies with 5-6 $N_{s(cells)}$.

DC charging: maximum DC charging power for BI-MMCs is between 800 W to 3.26 MW with the same losses as traction.

arvind.balachandran@liu.se