
STM32
CubeMX

1. Description

1.1. Project

Project Name	UWB pcb
Board Name	custom
Generated with:	STM32CubeMX 6.1.1
Date	04/08/2021

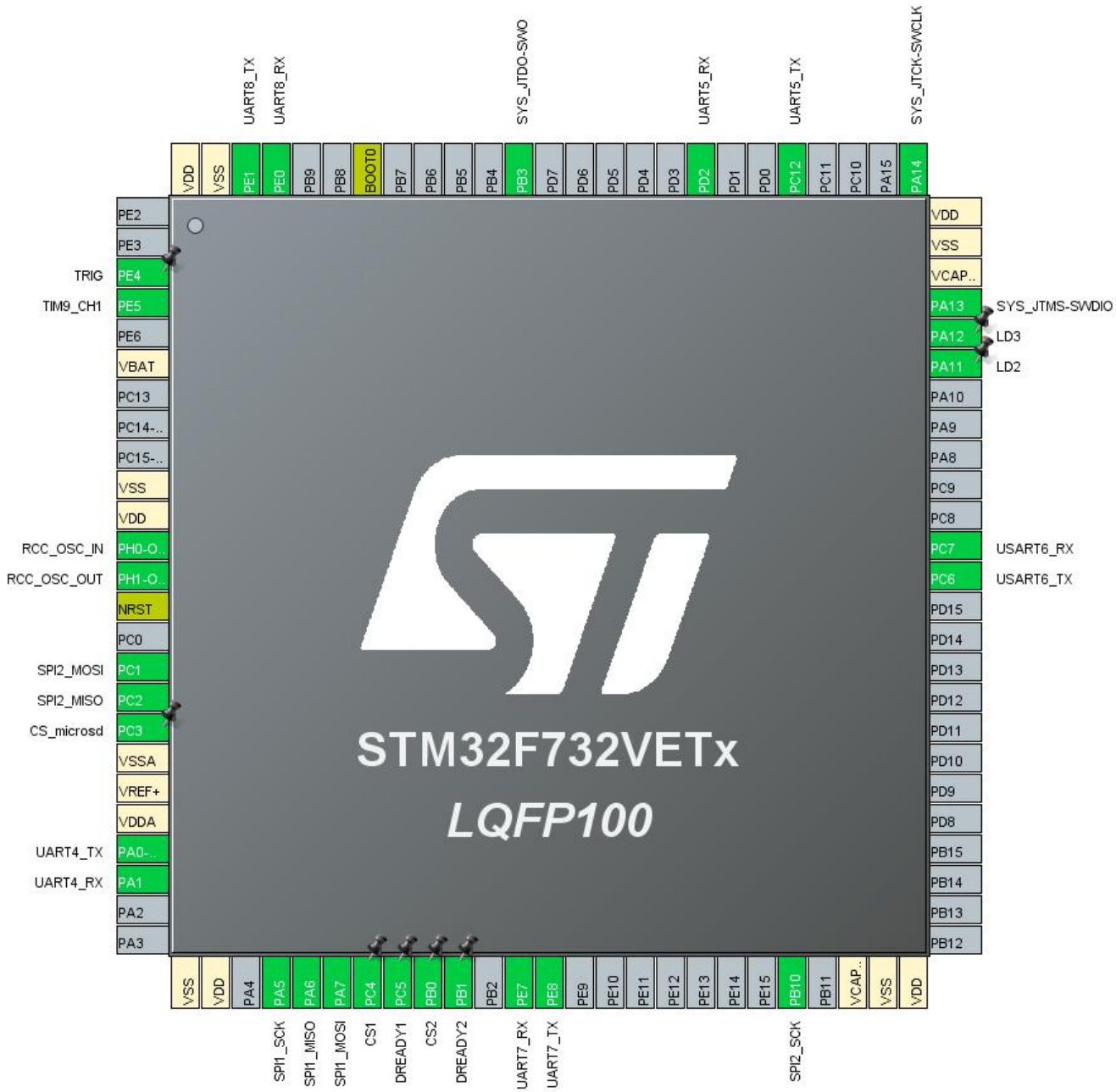
1.2. MCU

MCU Series	STM32F7
MCU Line	STM32F7x2
MCU name	STM32F732VETx
MCU Package	LQFP100
MCU Pin number	100

1.3. Core(s) information

Core(s)	Arm Cortex-M7

2. Pinout Configuration



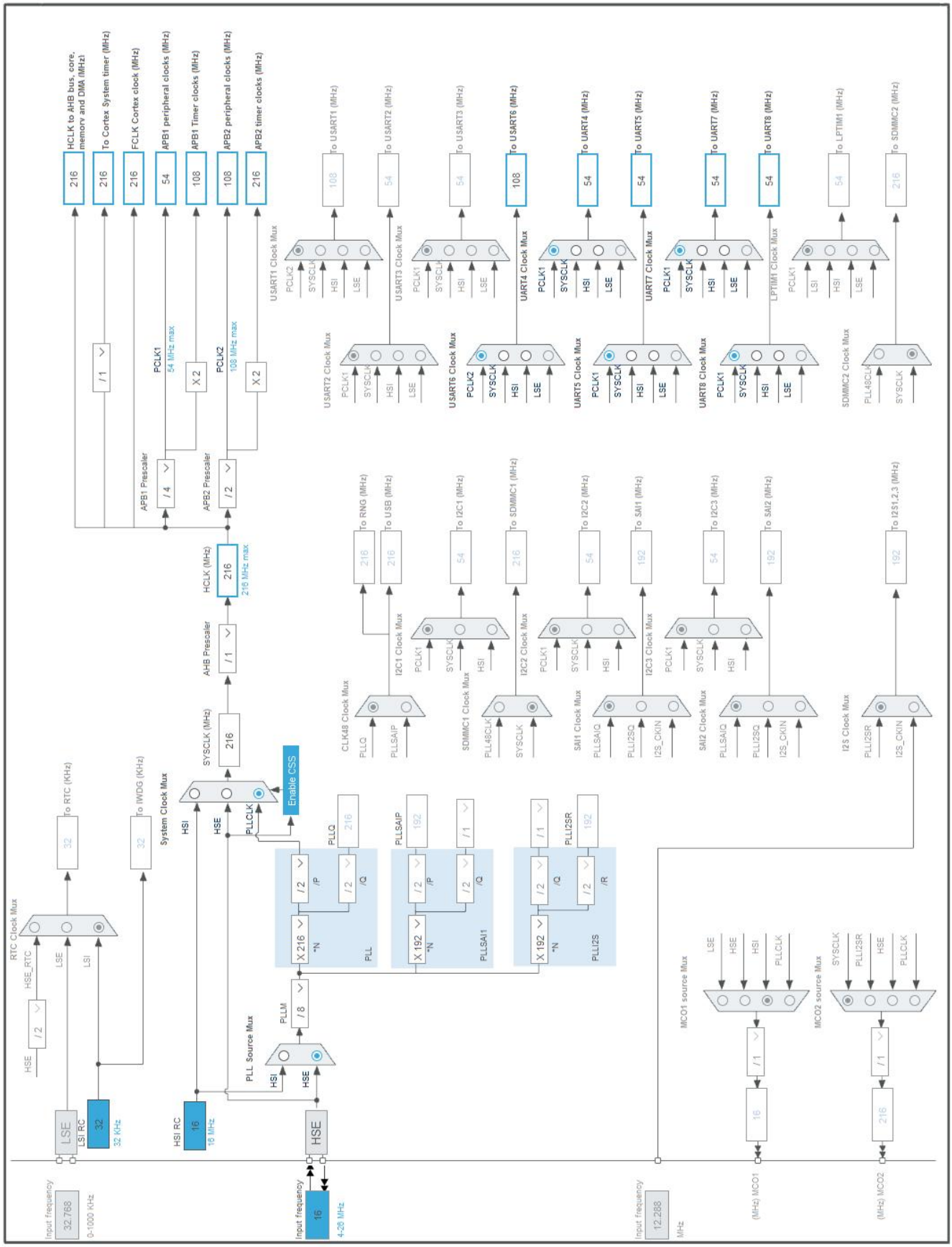
3. Pins Configuration

Pin Number LQFP100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
3	PE4 *	I/O	GPIO_Output	TRIG
4	PE5	I/O	TIM9_CH1	
6	VBAT	Power		
10	VSS	Power		
11	VDD	Power		
12	PH0-OSC_IN	I/O	RCC_OSC_IN	
13	PH1-OSC_OUT	I/O	RCC_OSC_OUT	
14	NRST	Reset		
16	PC1	I/O	SPI2_MOSI	
17	PC2	I/O	SPI2_MISO	
18	PC3 *	I/O	GPIO_Output	CS_microsd
19	VSSA	Power		
20	VREF+	Power		
21	VDDA	Power		
22	PA0-WKUP	I/O	UART4_TX	
23	PA1	I/O	UART4_RX	
26	VSS	Power		
27	VDD	Power		
29	PA5	I/O	SPI1_SCK	
30	PA6	I/O	SPI1_MISO	
31	PA7	I/O	SPI1_MOSI	
32	PC4 *	I/O	GPIO_Output	CS1
33	PC5 *	I/O	GPIO_Input	DREADY1
34	PB0 *	I/O	GPIO_Output	CS2
35	PB1 *	I/O	GPIO_Input	DREADY2
37	PE7	I/O	UART7_RX	
38	PE8	I/O	UART7_TX	
46	PB10	I/O	SPI2_SCK	
48	VCAP_1	Power		
49	VSS	Power		
50	VDD	Power		
63	PC6	I/O	USART6_TX	
64	PC7	I/O	USART6_RX	
70	PA11 *	I/O	GPIO_Output	LD2
71	PA12 *	I/O	GPIO_Output	LD3
72	PA13	I/O	SYS_JTMS-SWDIO	

Pin Number LQFP100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
73	VCAP_2	Power		
74	VSS	Power		
75	VDD	Power		
76	PA14	I/O	SYS_JTCK-SWCLK	
80	PC12	I/O	UART5_TX	
83	PD2	I/O	UART5_RX	
89	PB3	I/O	SYS_JTDO-SWO	
94	BOOT0	Boot		
97	PE0	I/O	UART8_RX	
98	PE1	I/O	UART8_TX	
99	VSS	Power		
100	VDD	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	UWB pcb
Project Folder	D:\KTUnas\Arvydo\Bakalauras\cube pcb\UWB pcb
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_F7 V1.16.1
Application Structure	Advanced
Generate Under Root	Yes
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	MX_GPIO_Init	GPIO
2	MX_DMA_Init	DMA
3	SystemClock_Config	RCC
4	MX_UART4_Init	UART4
5	MX_TIM3_Init	TIM3
6	MX_TIM4_Init	TIM4
7	MX_TIM5_Init	TIM5
8	MX_TIM8_Init	TIM8
9	MX_TIM9_Init	TIM9
10	MX_UART5_Init	UART5
11	MX_USART6_UART_Init	USART6

Rank	Function Name	Peripheral Instance Name
12	MX_SPI1_Init	SPI1
13	MX_SPI2_Init	SPI2
14	MX_UART7_Init	UART7
15	MX_UART8_Init	UART8

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32F7
Line	STM32F7x2
MCU	STM32F732VETx
Datasheet	DS11854_Rev3

6.2. Parameter Selection

Temperature	25
Vdd	3.3

6.3. Battery Selection

Battery	Alkaline(9V)
Capacity	625.0 mAh
Self Discharge	0.3 %/month
Nominal Voltage	9.0 V
Max Cont Current	200.0 mA
Max Pulse Current	0.0 mA
Cells in series	1
Cells in parallel	1

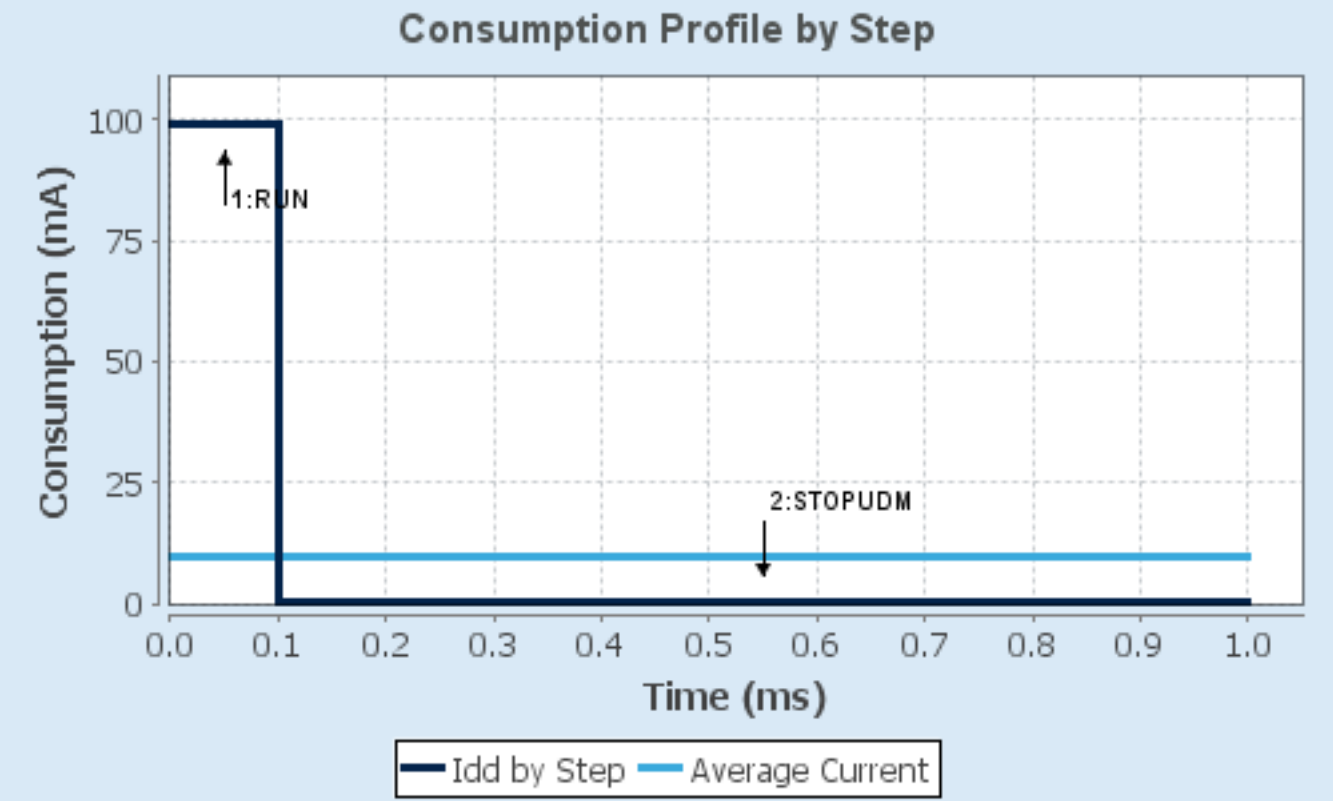
6.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP_UDM (Under Drive)
Vdd	3.3	3.3
Voltage Source	Battery	Battery
Range	Scale1-High	No Scale
Fetch Type	ITCM RAM REGON	n/a
CPU Frequency	216 MHz	0 Hz
Clock Configuration	HSE PLL	Regulator_LP Flash-PwrDwn
Clock Source Frequency	4 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	99 mA	100 µA
Duration	0.1 ms	0.9 ms
DMIPS	462.0	0.0
Ta Max	99.12	104.99
Category	In DS Table	In DS Table

6.5. Results

Sequence Time	1 ms	Average Current	9.99 mA
Battery Life	2 days, 14 hours	Average DMIPS	462.24005 DMIPS

6.6. Chart


Consumption Profile by Step
Consumption (mA)
100
75
50
25
0
1:RUN
2:STOPUDM
0.0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1.0
Time (ms)
Idd by Step
Average Current

7. Peripherals and Middlewares Configuration

7.1. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

7.1.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Flash Latency(WS)	7 WS (8 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
TIM Prescaler Selection	Disabled
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000

Power Parameters:

Power Over Drive	Enabled
Power Regulator Voltage Scale	Power Regulator Voltage Scale 1

7.2. SPI1

Mode: Full-Duplex Master

7.2.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	**8 Bits ***
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	**32 ***
Baud Rate	**3.375 MBits/s ***
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSSP Mode	Enabled
NSS Signal Type	Software

7.3. SPI2

Mode: Full-Duplex Master

7.3.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	**8 Bits ***
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	**16 ***
Baud Rate	**3.375 MBits/s ***
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSSP Mode	Enabled
NSS Signal Type	Software

7.4. SYS

Debug: Trace Asynchronous Sw

Timebase Source: SysTick

7.5. TIM3

Clock Source : Internal Clock

7.5.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**54000-1 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**1000-1 ***
Internal Clock Division (CKD)	**Division by 2 ***
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	**Update Event ***

7.6. TIM4

Clock Source : Internal Clock

7.6.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**54000-1 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**9-1 ***
Internal Clock Division (CKD)	**Division by 2 ***
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	**Update Event ***

7.7. TIM5

mode: Clock Source

7.7.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**54000-1 ***
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value)	**100-1 ***
Internal Clock Division (CKD)	**Division by 2 ***
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	**Update Event ***

7.8. TIM8

Clock Source : Internal Clock

7.8.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**216-1 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**0 ***
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 16 bits value)	0
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)
Trigger Event Selection TRGO2	Reset (UG bit from TIMx_EGR)

7.9. TIM9

Channel1: Input Capture direct mode

7.9.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**216-1 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**0xFFFF-1 ***
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Input Capture Channel 1:

Polarity Selection	**Both Edges ***
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter (4 bits value)	**4 ***

7.10. UART4

Mode: Asynchronous

7.10.1. Parameter Settings:

Basic Parameters:

Baud Rate	**9600 ***
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable

Advanced Features:

TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

7.11. UART5

Mode: Asynchronous

7.11.1. Parameter Settings:

Basic Parameters:

Baud Rate	**100000 ***
Word Length	**9 Bits (including Parity) ***
Parity	**Even ***
Stop Bits	**2 ***

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable

Advanced Features:

TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

7.12. UART7

Mode: Asynchronous

7.12.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable

Advanced Features:

TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

7.13. UART8

Mode: Asynchronous

7.13.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable

Advanced Features:

TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable

Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

7.14. USART6

Mode: Asynchronous

7.14.1. Parameter Settings:

Basic Parameters:

Baud Rate	**100000 ***
Word Length	**9 Bits (including Parity) ***
Parity	**Even ***
Stop Bits	**2 ***

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	**Enable ***
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

*** User modified value**

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
RCC	PH0-OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PH1-OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
SPI1	PA5	SPI1_SCK	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PA6	SPI1_MISO	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PA7	SPI1_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
SPI2	PC1	SPI2_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PC2	SPI2_MISO	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PB10	SPI2_SCK	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
SYS	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	
	PB3	SYS_JTDO-SWO	n/a	n/a	n/a	
TIM9	PE5	TIM9_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
UART4	PA0-WKUP	UART4_TX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PA1	UART4_RX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
UART5	PC12	UART5_TX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PD2	UART5_RX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
UART7	PE7	UART7_RX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PE8	UART7_TX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
UART8	PE0	UART8_RX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PE1	UART8_TX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
USART6	PC6	USART6_TX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PC7	USART6_RX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
GPIO	PE4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	TRIG
	PC3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**Medium ***	CS_microsd
	PC4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	CS1
	PC5	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	DREADY1
	PB0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	CS2
	PB1	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	DREADY2
	PA11	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LD2
	PA12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LD3

8.2. DMA configuration

DMA request	Stream	Direction	Priority
UART4_RX	DMA1_Stream2	Peripheral To Memory	Low
UART5_TX	DMA1_Stream7	Memory To Peripheral	**High ***
USART6_RX	DMA2_Stream1	Peripheral To Memory	**High ***

UART4_RX: DMA1_Stream2 DMA request Settings:

Mode:	**Circular ***
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

UART5_TX: DMA1_Stream7 DMA request Settings:

Mode:	**Circular ***
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

USART6_RX: DMA2_Stream1 DMA request Settings:

Mode:	Normal
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

8.3. NVIC configuration

8.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
DMA1 stream2 global interrupt	true	0	0
TIM1 break interrupt and TIM9 global interrupt	true	0	0
TIM3 global interrupt	true	0	0
TIM4 global interrupt	true	0	0
SPI1 global interrupt	true	0	0
DMA1 stream7 global interrupt	true	0	0
TIM5 global interrupt	true	0	0
UART5 global interrupt	true	0	0
DMA2 stream1 global interrupt	true	0	0
USART6 global interrupt	true	0	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
SPI2 global interrupt	unused		
TIM8 break interrupt and TIM12 global interrupt	unused		
TIM8 update interrupt and TIM13 global interrupt	unused		
TIM8 trigger and commutation interrupts and TIM14 global interrupt	unused		
TIM8 capture compare interrupt	unused		
UART4 global interrupt	unused		
FPU global interrupt	unused		
UART7 global interrupt	unused		
UART8 global interrupt	unused		

8.3.2. NVIC Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler

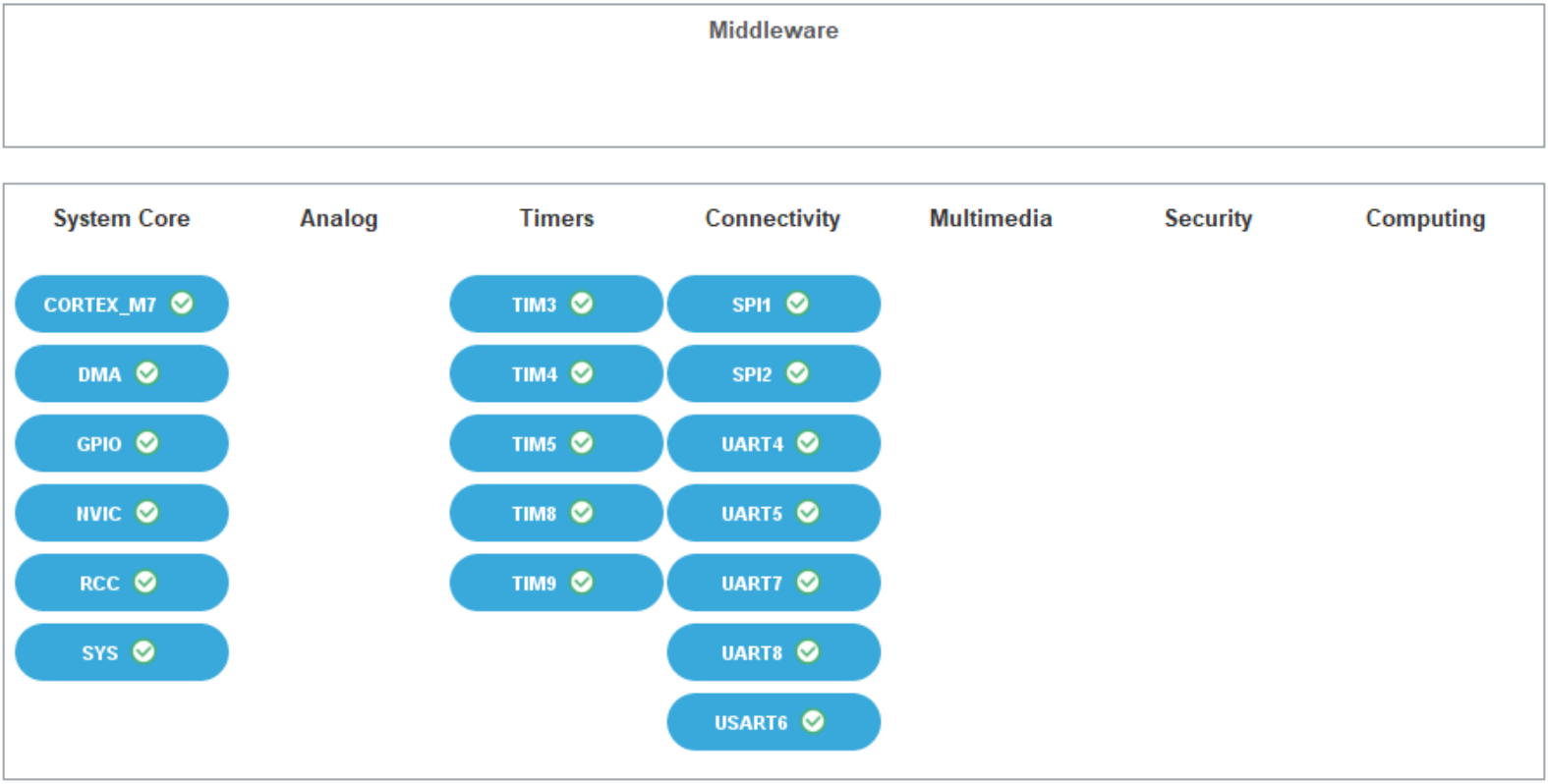
Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Pre-fetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	true	false
Debug monitor	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true
DMA1 stream2 global interrupt	false	true	true
TIM1 break interrupt and TIM9 global interrupt	false	true	true
TIM3 global interrupt	false	true	true
TIM4 global interrupt	false	true	true
SPI1 global interrupt	false	true	true
DMA1 stream7 global interrupt	false	true	true
TIM5 global interrupt	false	true	true
UART5 global interrupt	false	true	true
DMA2 stream1 global interrupt	false	true	true
USART6 global interrupt	false	true	true

*** User modified value**

9. System Views

9.1. Category view

9.1.1. Current



10. Docs & Resources

Type	Link
Datasheet	http://www.st.com/resource/en/datasheet/DM00330507.pdf
Reference manual	http://www.st.com/resource/en/reference_manual/DM00305990.pdf
Programming manual	http://www.st.com/resource/en/programming_manual/DM00237416.pdf
Errata sheet	http://www.st.com/resource/en/errata_sheet/DM00305994.pdf
Application note	http://www.st.com/resource/en/application_note/CD00167594.pdf
Application note	http://www.st.com/resource/en/application_note/CD00211314.pdf
Application note	http://www.st.com/resource/en/application_note/CD00259245.pdf
Application note	http://www.st.com/resource/en/application_note/CD00264321.pdf
Application note	http://www.st.com/resource/en/application_note/CD00264342.pdf
Application note	http://www.st.com/resource/en/application_note/CD00264379.pdf
Application note	http://www.st.com/resource/en/application_note/DM00042534.pdf
Application note	http://www.st.com/resource/en/application_note/DM00046011.pdf
Application note	http://www.st.com/resource/en/application_note/DM00072315.pdf
Application note	http://www.st.com/resource/en/application_note/DM00073742.pdf
Application note	http://www.st.com/resource/en/application_note/DM00073853.pdf
Application note	http://www.st.com/resource/en/application_note/DM00080497.pdf
Application note	http://www.st.com/resource/en/application_note/DM00081379.pdf
Application note	http://www.st.com/resource/en/application_note/DM00129215.pdf
Application note	http://www.st.com/resource/en/application_note/DM00160482.pdf
Application note	http://www.st.com/resource/en/application_note/DM00164538.pdf
Application note	http://www.st.com/resource/en/application_note/DM00164549.pdf
Application note	http://www.st.com/resource/en/application_note/DM00173083.pdf
Application note	http://www.st.com/resource/en/application_note/DM00210367.pdf
Application note	http://www.st.com/resource/en/application_note/DM00220769.pdf
Application note	http://www.st.com/resource/en/application_note/DM00227538.pdf

Application note	http://www.st.com/resource/en/application_note/DM00257177.pdf
Application note	http://www.st.com/resource/en/application_note/DM00272912.pdf
Application note	http://www.st.com/resource/en/application_note/DM00272913.pdf
Application note	http://www.st.com/resource/en/application_note/DM00226326.pdf
Application note	http://www.st.com/resource/en/application_note/DM00236305.pdf
Application note	http://www.st.com/resource/en/application_note/DM00281138.pdf
Application note	http://www.st.com/resource/en/application_note/DM00296349.pdf
Application note	http://www.st.com/resource/en/application_note/DM00327191.pdf
Application note	http://www.st.com/resource/en/application_note/DM00340311.pdf
Application note	http://www.st.com/resource/en/application_note/DM00337702.pdf
Application note	http://www.st.com/resource/en/application_note/DM00354244.pdf
Application note	http://www.st.com/resource/en/application_note/DM00315319.pdf
Application note	http://www.st.com/resource/en/application_note/DM00380469.pdf
Application note	http://www.st.com/resource/en/application_note/DM00395696.pdf
Application note	http://www.st.com/resource/en/application_note/DM00431633.pdf
Application note	http://www.st.com/resource/en/application_note/DM00493651.pdf
Application note	http://www.st.com/resource/en/application_note/DM00536349.pdf
Application note	http://www.st.com/resource/en/application_note/DM00600614.pdf
Application note	http://www.st.com/resource/en/application_note/DM00725181.pdf