
# Faculty of Engineering and Technology

# Department of Electrical and Computer Engineering

# DIGITAL INTEGRATED CIRCUITS- ENCS3330

## HW#4 : TOOL ASSIGNMENT EXPERIMENT-1

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Instructor
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Eng: Raha Ahmad

BIRZEIT
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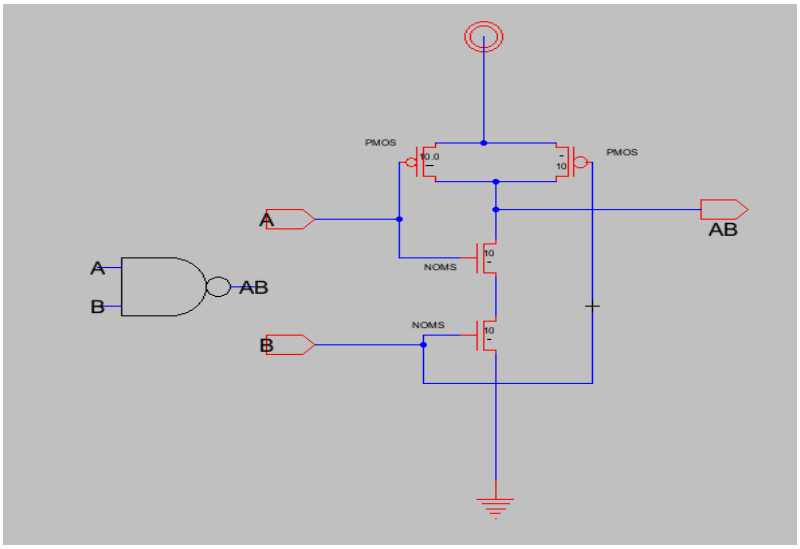
## Lab work:

1) Design, layout, and simulation of CMOS NAND gate:




```
vdd vdd 0 DC 5
va A 0 DC pwl 10n 0 20n 5 50n 5 60n 0 90n 0 100n 5 130n 5 140n 0 170n 0 180n 5
vb B 0 DC pwl 10n 0 20n 5 100n 5 110n 0
.measure tran tf trig v(AB) val=4.5 fall=1 td=4ns trag v(AB) val=0.5 fall=1
.measure tran tr trig v(AB) val=0.5 rais=1 td=4ns trag v(AB) val=4.5 rais=1
.tran 200n
.include C:\ICWORK\C5_models.txt
```

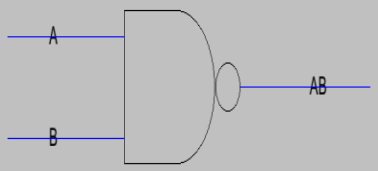



Figure 1.1: the schematic for NAND gate.

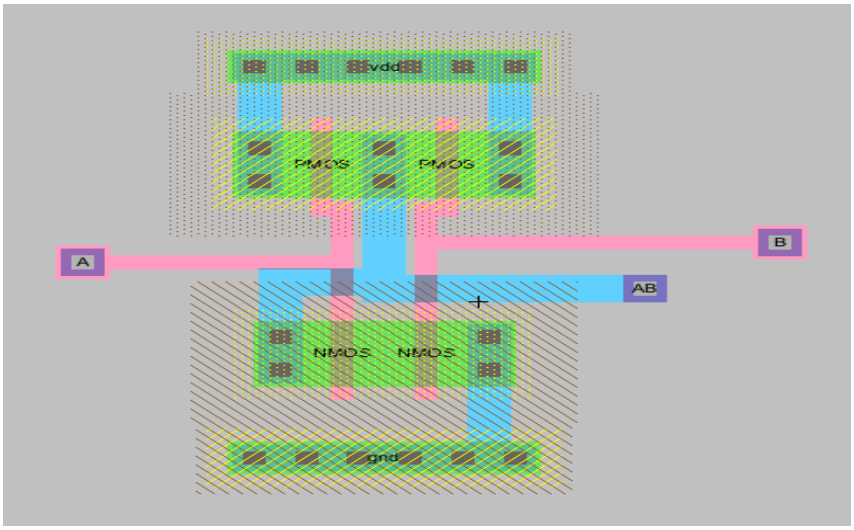



Figure 1.2: the layout for NAND gate.

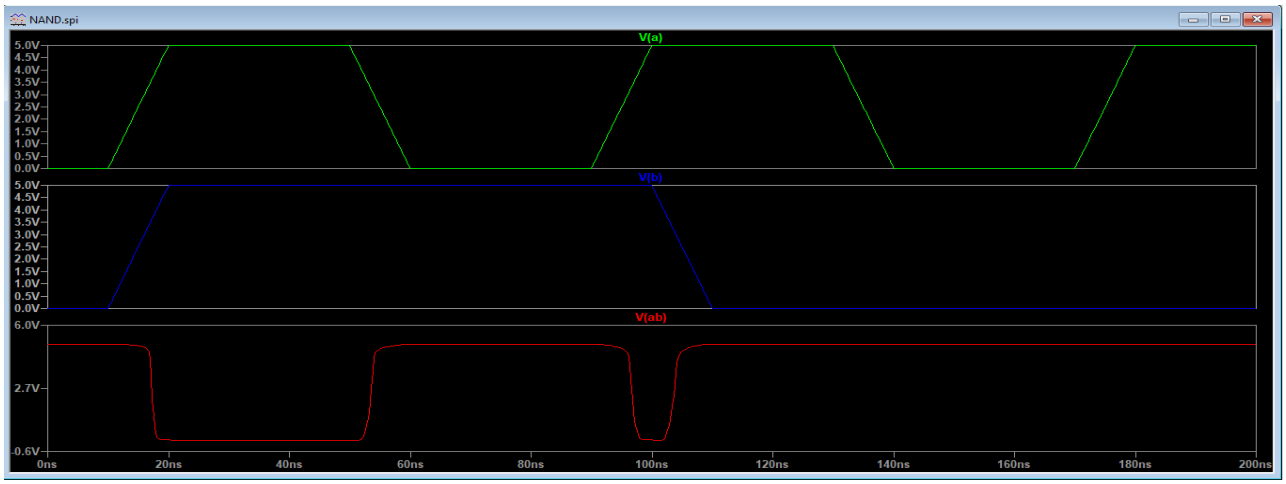
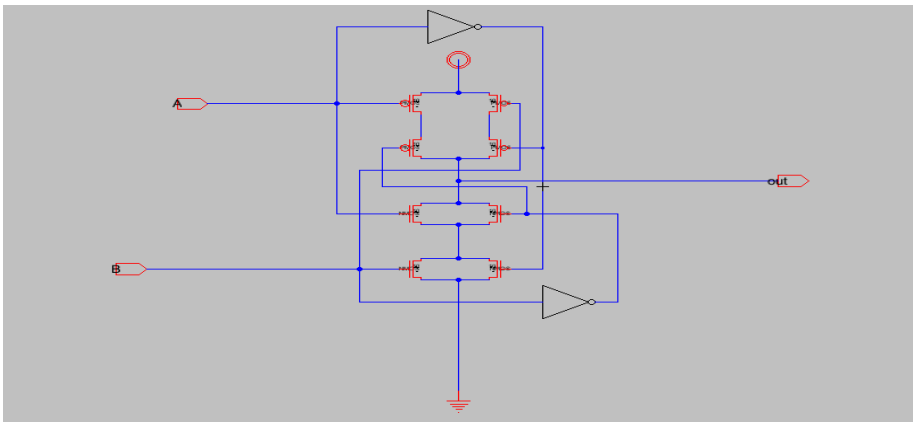



Figure 1.3: the symulation for NAND gate.

2) Design, layout, and simulation of CMOS XOR gate:



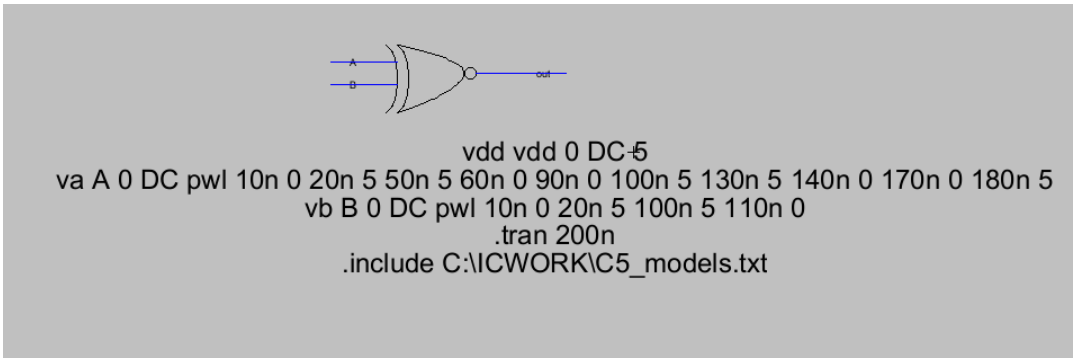




Figure2.1: the schematic for Xor gate.

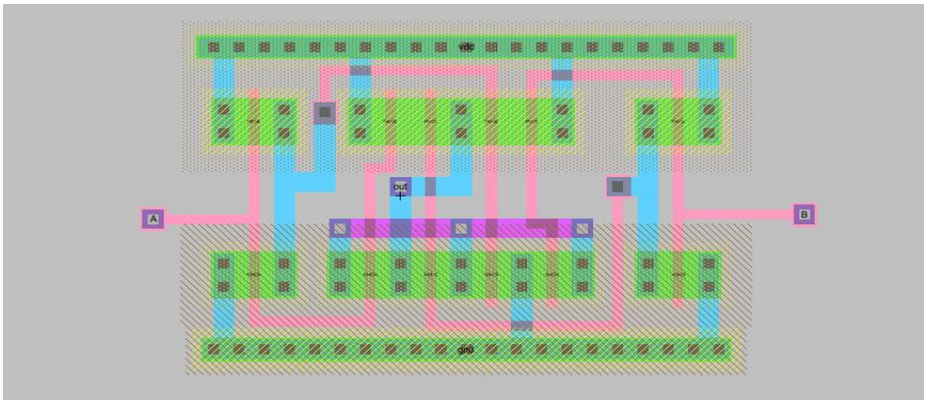



Figure 2.2: the layout for Xor gate.

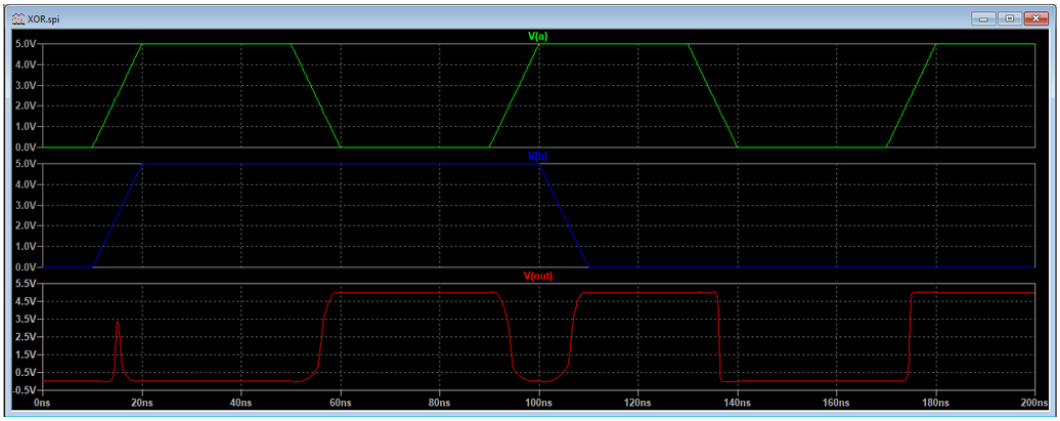



Figure 2.3: the symulation for Xor gate.

3) Design, layout, and simulation of CMOS Full adder gate using the previous components:

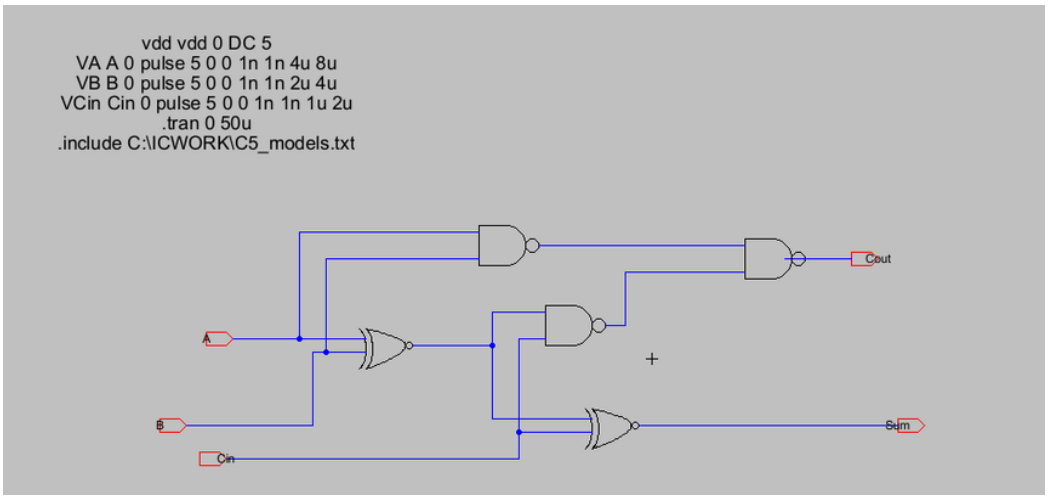



Figure 3.1: the schematic for Full adder.

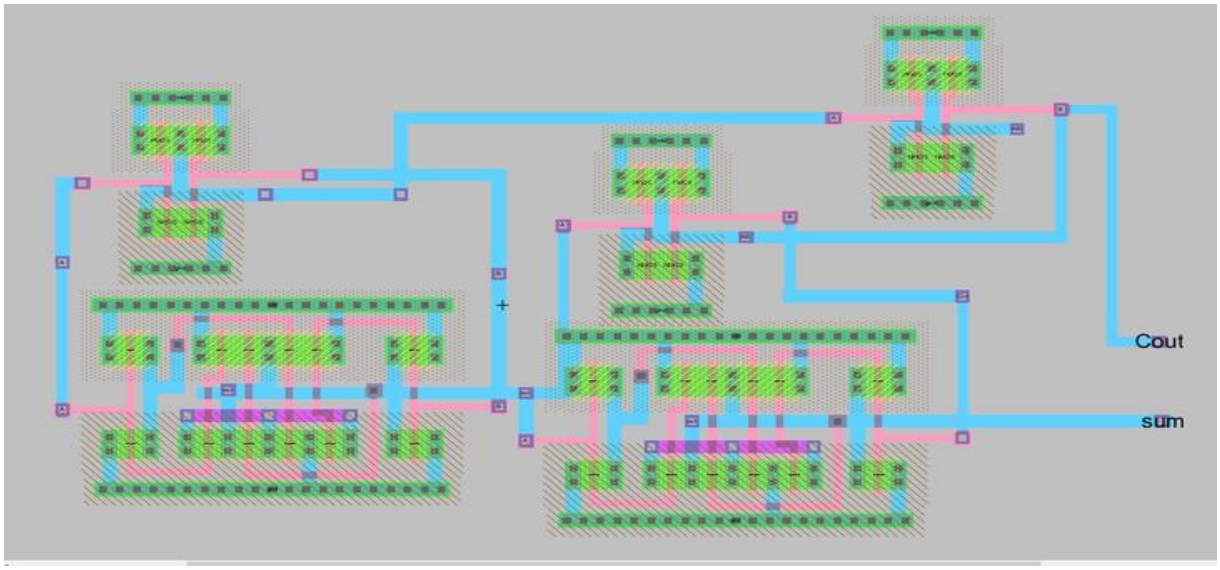



Figure 3.2: layout for Full adder.

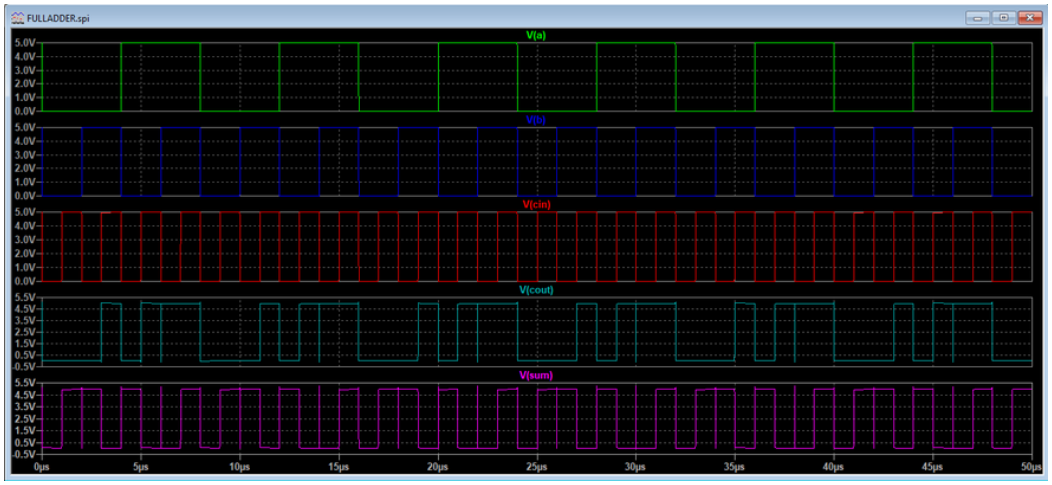



Figure 3.3: symulation for Full adder.