Ganxiang Yang

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github.com
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Education

Zhiyuan College, Shanghai Jiao Tong University Sep.2020 - Present
*Bachelor of Computer Science, member of **ACM Honor Class** (top 5% students in SJTU)* *Shanghai, China*

- Excellent Professional Courses Performance:
  Computer Architecture: 4.0/4.3 | Operating System: 4.3/4.3
- Excellent Math Courses Performance:
  Mathematical Analysis: 4.0/4.3 | Linear Algebra: 4.0/4.3
  Mathematical Logic: 4.0/4.3 | Probability: 4.0/4.3

Publications

PALANTÍR: Formally Verified Privileged Enclave as a Lightweight and Efficient Framework Extension
*Authors: **G. Yang**, C. Liu, Z. Huang, G. Chen, H. Fu, Y. Zhang, H. Zhu* [Code]

- Submitted to **Usenix Security 2024** (under review).
- We propose PALANTÍR, a novel Privileged Enclave (PE) framework for enclave platforms.
- We build TAP^2, an extended model of TEE platform for verifying PALANTÍR security properties.
- We implement PALANTÍR onto Penglai-TVM and conducted three various case studies to show flexibility.

Research Experience

Research Intern Feb.2023 – Present
Northwestern University, U.S.A. *Mentor: Xinyu Xing*

- Focusing on Web3 Security and bug exploitations.

Undergraduate Research Assistant Jul.2022 – Present
Network Security and Privacy Protection (NSEC) Lab, SJTU *Mentor: Guoxing Chen*

- Focusing on cross-platform Trusted Execution Environment (TEE) designs.
- Developing and extending on Penglai-TVM, a RISC-V trusted computing platform.
- Designing new primitives and make extension on TAP: a formal verified abstract model of TEE.

Honors & Awards

Freshmen Scholarship Shanghai Jiao Tong University
Awards to students with outstanding performance on admission *Sep.2020*

Zhiyuan Honorary Scholarship Shanghai Jiao Tong University
Top 2% in SJTU *2020, 2021, 2022*

Projects

Isaiah: A C-and-Java-like compiler [Github Link]

Compiler, Java

- Isaiah is a **compiler** written in Java for compiling a C-and-Java-like Language named Mx*.
- With **7k+ lines of codes** and performance **close to GCC-O1**.
- Use **ANTLR4** as frontend generator, LLVM-minor as IR, rv32im as assembly.
- Support **λ-function** and **more complex class grammar** than others.

YPU: An Speculative Executed CPU on FPGA [Github Link]

FPGA, CPU, Verilog

- YPU is a **rv32i CPU** written in Verilog HDL and working fine on FPGA at 100 MHz.
- With **3k+ lines of codes** and performance **much better than a 5-stage pipeline**.
- Supports fresh **Speculative Execution** based on **Tomasulo Algorithm**.
- Other features: precise interruption, BPU, icache, Load Buffer, prefetching.
- Well-designed modules and **much lower path delay** than others' design.

Specialized Skills

Programming Language: C, C++, Java, Python, Verilog, RISC-V Assembly, Bash, Boogie, Go
Frameworks & Tools: qemu, OpenSBI, Docker, Vivado
English : Fully professional. **TOEFL IBT** (Feb 2023): 107/120, speaking: 23/30
Mandarin : Native Speaker