



**Digit 360 ICS CMOS**

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A

B

C

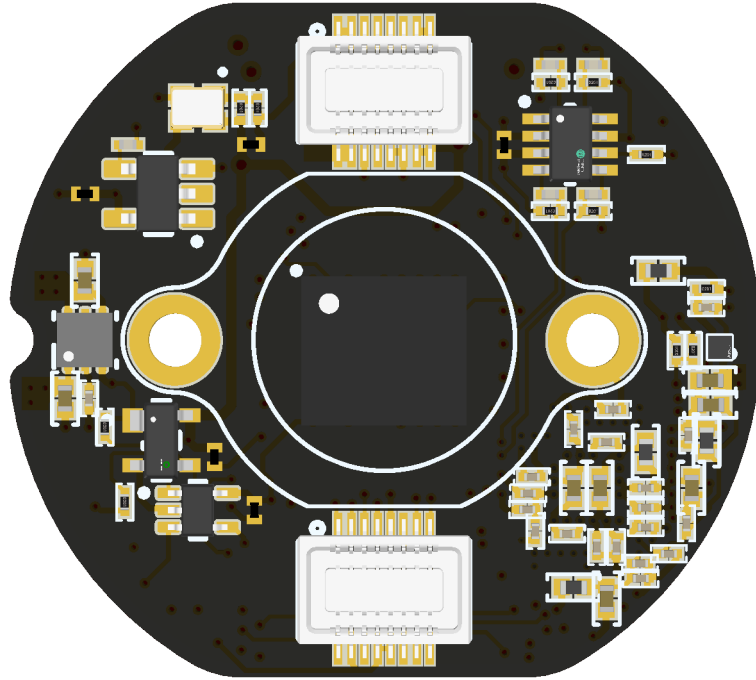
D

E

1

1

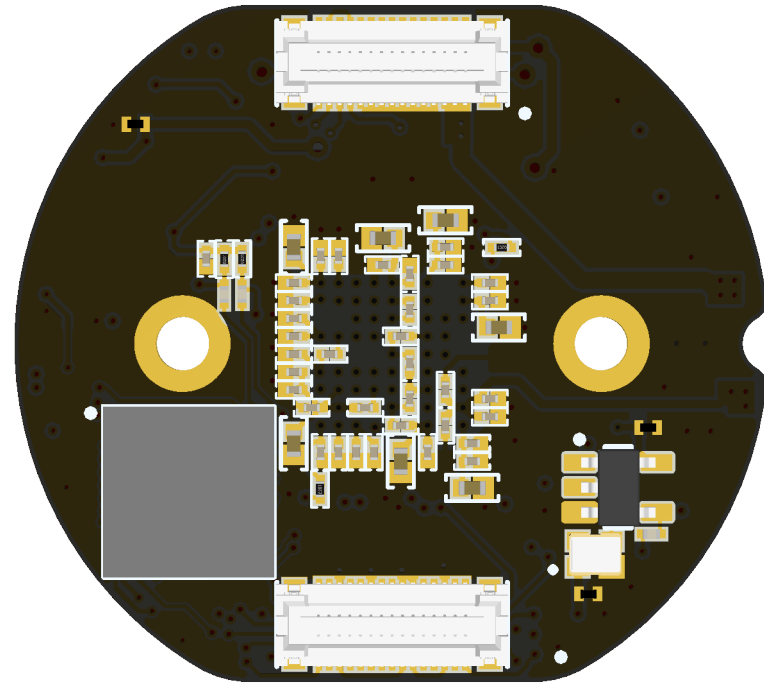
Realistic View



2

2

Realistic View



3

3

4

4

A

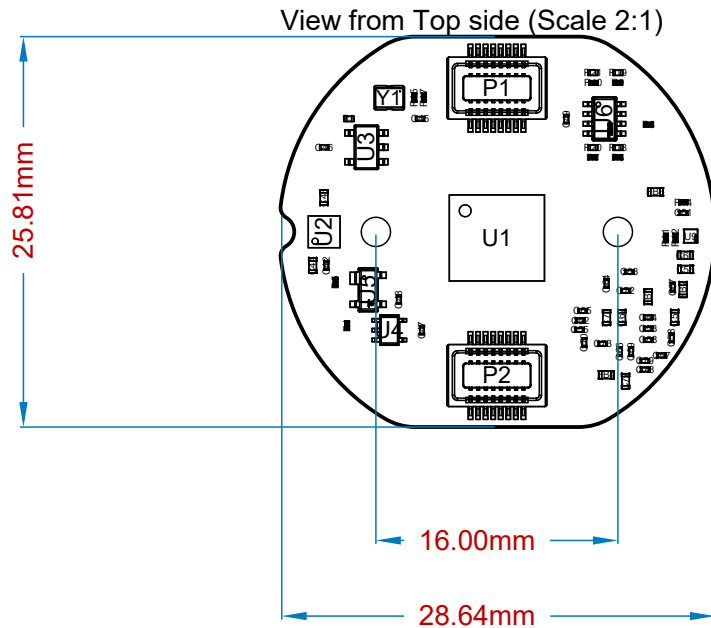
B

C

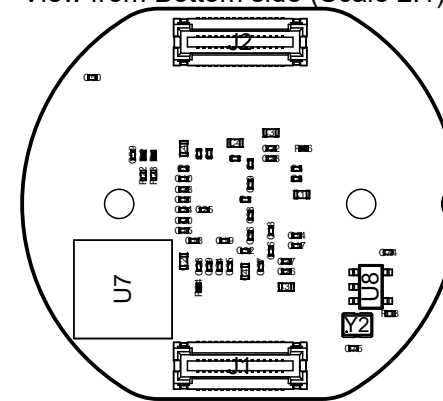
D

E

- NOTES: UNITS IN MILLIMETERS UNLESS OTHERWISE SPECIFIED
- 1. INTERPRET THIS DRAWING IN ACCORDANCE WITH IPC-D-325A
  - 2. BOARD FABRICATION AND QUALITY PER IPC-6012, CLASS 2, EXCEPT SPECIFIED HEREIN
  - 3. MUST COMPLY WITH EUROPEAN DIRECTIVE 2002/95/EC (RoHS)
  - 4. DIMENSIONAL LIMITS APPLY AFTER PLATING OR COATING
  - 5. BOW AND TWIST MAXIMUM IS 0.75%
  - 6. MATERIAL: LAMINATE AND PREPREG SHALL BE IN ACCORDANCE WITH IPC-4101/21. 170 DEGREES CELSIUS MINIMUM Tg, UL 94V-0
  - 7. STACKUP SUMMARY:
    - A. NUMBER OF COPPER LAYERS: 6
    - B. BOARD THICKNESS SHALL BE 62mil +/- 10%
    - C. COPPER: See Layer Stack
    - D. DEFAULT TRACE/SPACE: 4mil / 4mil
    - E. CONDUCTOR WIDTH TOLERANCE = +/- 0.01mm
  - 8. VIPPO (VIA IN PAD PLATED OVER) PER IPC-6012, CURRENT REVISION, CLASS 2, AS STATED IN NOTE 2.
    - a. FILL AND CAP All 0.2mm VIA HOLES WITH NON-CONDUCTIVE EPOXY
    - b. FILL AND CAP VIAS MUST BE PLANARIZED
  - 9. SURFACE FINISH/PLATING:
    - A. BOARD SHALL BE IMMERSION GOLD PLATED (ENIG) ACCORDING TO IPC-4552. THICKNESS SHALL BE A MINIMUM OF 0.05µm GOLD OVER 3-6µm NICKEL
  - 10. SOLDERMASK WITH LIQUID PHOTO IMAGEABLE (LPI) PER IPC-SM-840C, CLASS T. COLOR: MATTE BLACK
  - 11. SILKSCREEN PER SUPPLIED ARTWORK WITH ORGANIC, NON-CONDUCTIVE, EPOXY INK. SILKSCREEN MAY BE TRIMMED OFF ANY SOLDERABLE ENTITY. COLOR: WHITE
  - 12. 100% BARE BOARD ELECTRICAL TEST TO BE DONE WITH REFERENCE TO SUPPLIED NETLIST
  - 13. LOCATE MANUFACTURER'S IDENTIFICATION AND LOT CODE ON PRIMARY SIDE FREE FROM ALL METAL ENTITY RENDERED IN SILKSCREEN.
  - 14. DIFFERENTIAL CONTROLLED IMPEDANCE REQUIRED ON BOARD.  
SEE TABLE : DIFFERENTIAL CONTROLLED IMPEDANCE  
SEE TABLE : SINGLE ENDED CONTROLLED IMPEDANCE
  - 15. DETAILS NOT SPECIFIED ARE AT MANUFACTURER'S OPTION BUT FINAL APPROVAL MUST BE OBTAINED



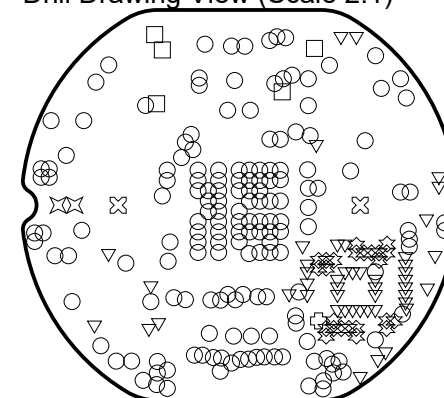
View from Bottom side (Scale 2:1)


















Drill Table

Symbol	Count	Hole Size	Plated	Hole Tolerance
⊕	1	0.10mm	Plated	
☆	24	0.15mm	Plated	
▽	47	0.18mm	Plated	
✕	2	0.20mm	Plated	
○	170	0.20mm	Plated	
□	5	0.41mm	Plated	
⊗	2	2.03mm	Plated	
251 Total				

Drill Drawing View (Scale 2:1)



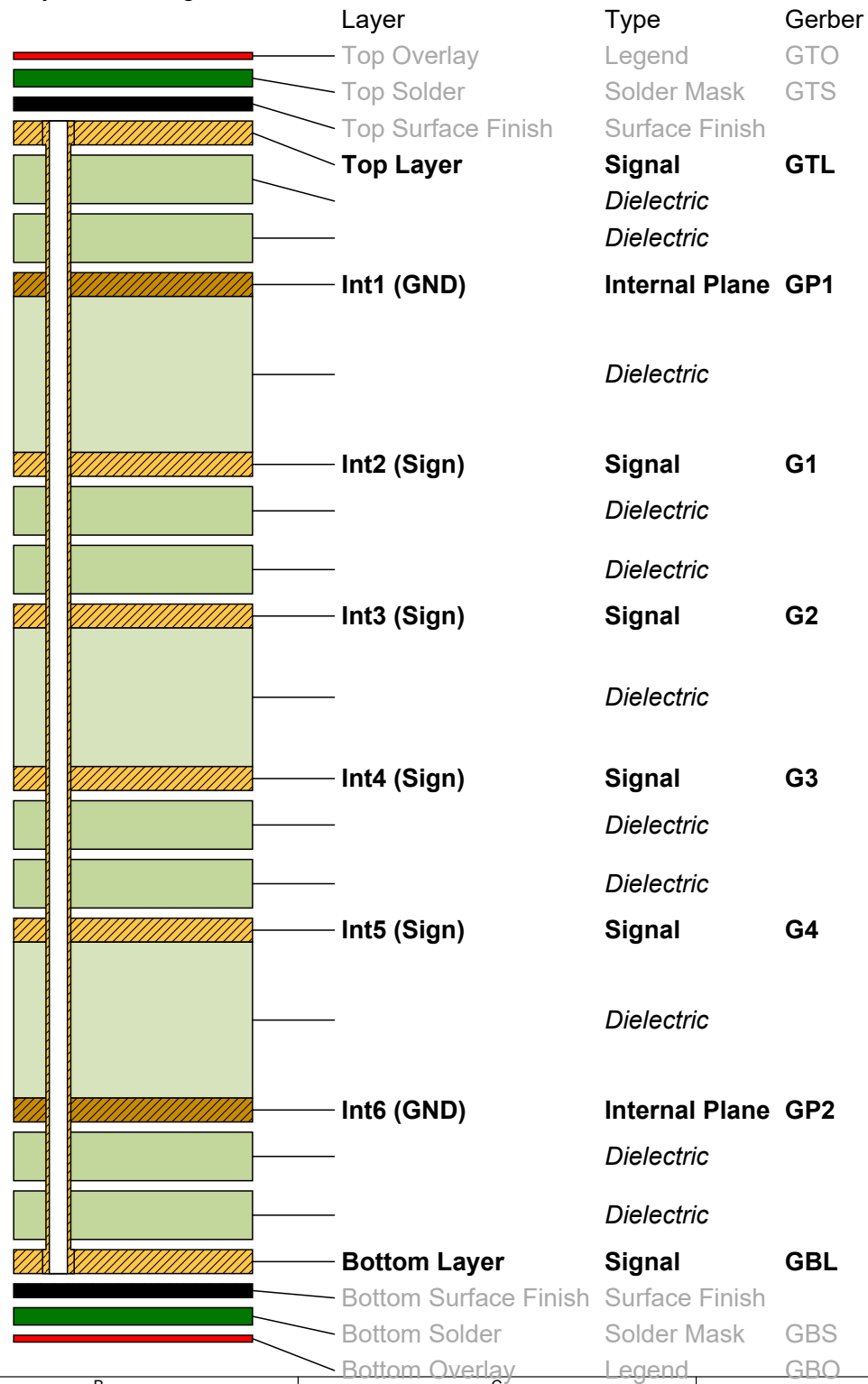
# Stack-Up (or similar)

Layer	Base CU / Plt	Thick	Type	Stackup	Subs	Imp	Material	Dk	Df
Silkscreen		0.00					Taiyo-SS - White		
Soldermask		0.60					Taiyo-SM - Green	2.70	0.033
Lyr1	0.5oz / Std	1.80	S						
Prepreg		7.64					370HR - 2x2113	3.99	0.022
Lyr2	1oz	1.20	P						
Core		14.00					370HR - 14.0mils	4.74	0.021
Lyr3	1oz	1.20	S						
Prepreg		9.08					370HR - 2x2113/1x1080	3.95	0.023
Lyr4	1oz	1.20	S						
Core		14.00					370HR - 14.0mils	4.74	0.021
Lyr5	1oz	1.20	P						
Prepreg		7.64					370HR - 2x2113	3.99	0.022
Lyr6	0.5oz / Std	1.80	S						
Soldermask		0.60					Taiyo-SM - Green	2.70	0.033
Silkscreen		0.00					Taiyo-SS - White		

## Required Thickness

Type	Req. Thick	Tol% +	Tol% -	Act. Thick	Measured
Overall	62.0	10.0	10.0	62.0	
Over lamination	58.4	10.0	10.0	58.4	
Over laminate	57.2	10.0	10.0	57.2	
Over metal	60.8	10.0	10.0	60.8	

### Layer Stack Legend



Transmission Line Structure Table

Target Impedance	Calculated Impedance	Trace layer	Wide Trace Width	Narrow Trace Width	Gap	Reference layers	Clearance	Target Tolerance
100	98.60	Top Layer	5.00mil	5.00mil	5.00mil	Int1 (GND)	5.00mil	10%
100	99.03	Int2 (Sign)	4.00mil	4.00mil	9.00mil	Int1 (GND),Int3 (Sign)	5.00mil	10%
100	99.03	Int5 (Sign)	4.00mil	4.00mil	9.00mil	Int4 (Sign),Int6 (GND)	5.00mil	10%
100	98.60	Bottom Layer	5.00mil	5.00mil	5.00mil	Int6 (GND)	5.00mil	10%