7447

37. In the circuit shown in Fig. 3.20, if $C = 0$, the expression for Y is
    a) $Y = A\overline{B} + \overline{A}B$
    b) $Y = A + B$
    c) $Y = \overline{A} + \overline{B}$
    d) $Y = AB$

(GATE EC 2014)

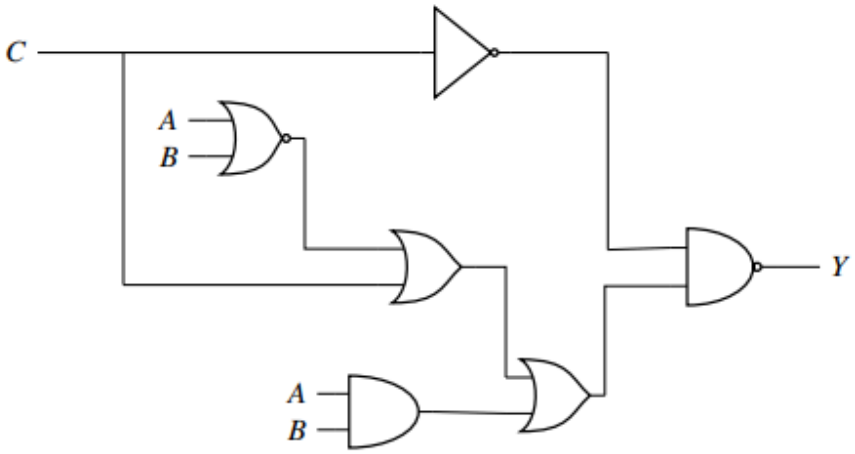

Fig. 3.20

44. In the circuit shown below in Fig. 3.26, X and Y are digital inputs, and Z is a digital output. The equivalent circuit is a (GATE EE 2019)
    a) NAND gate
    b) NOR gate
    c) XOR gate
    d) XNOR gate

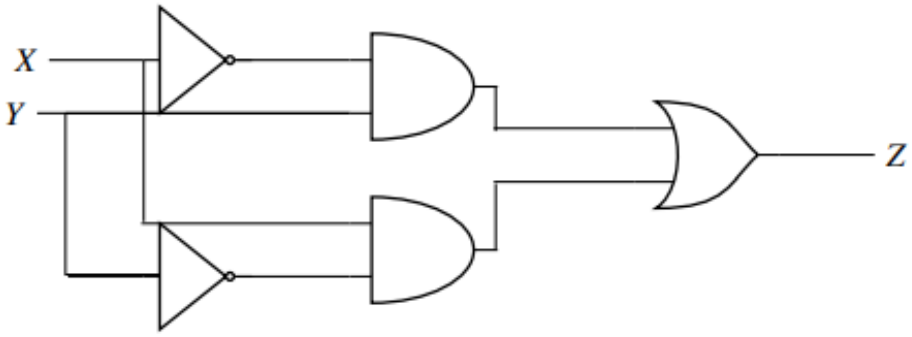

Fig. 3.26

K-Map

48. Find the Boolean logic realised by the following circuit in Fig. 4.23.
(GATE EC 2010)

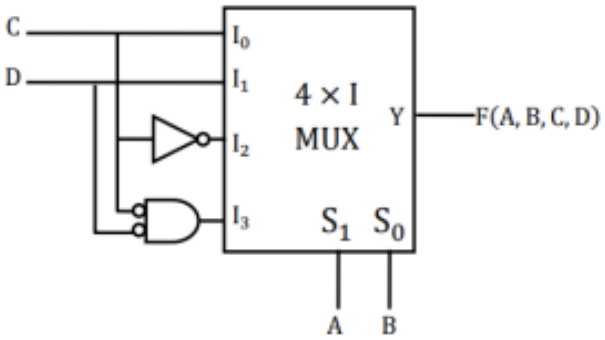

Fig. 4.23

51. Find the logic function implemented by the circuit given below in Fig. 4.26.
(GATE EC 2017)

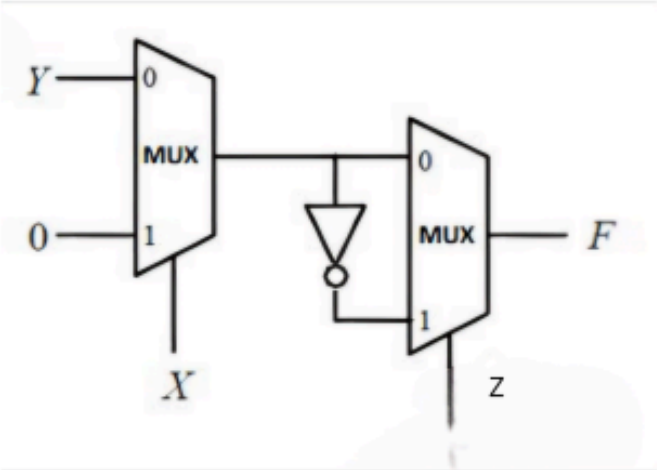

Fig. 4.26

7474

52

3. In the circuit in Fig. 5.3, the clock (Clk) frequency provided to the circuit is 500MHz. Starting from the initial value of the flip-flop outputs $Q2Q1Q0 = 111$ with $D2 = 1$, fine the time after which $Q2Q1Q0 = 100$. (GATE EC 2021)

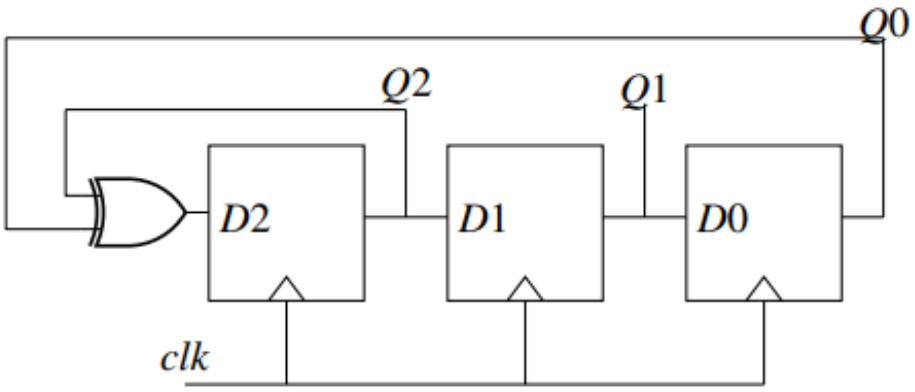

Fig. 5.3

9. Consider a sequential digital circuit consisting of T flip-flops and D flip-flops as shown in Fig. 5.9. CLKIN is is the clock input to the circuit. At the beginning,Q1,Q2 and Q3 have values 0,1 and 1, respectively. Which of the given values of (Q_1, Q_2, Q_3) can NEVER be obtained with this digital circuit? (GATE CS 2023)

a) $(0, 0, 1)$ b) $(1, 0, 0)$ c) $(1, 0, 1)$ d) $(1, 1, 1)$

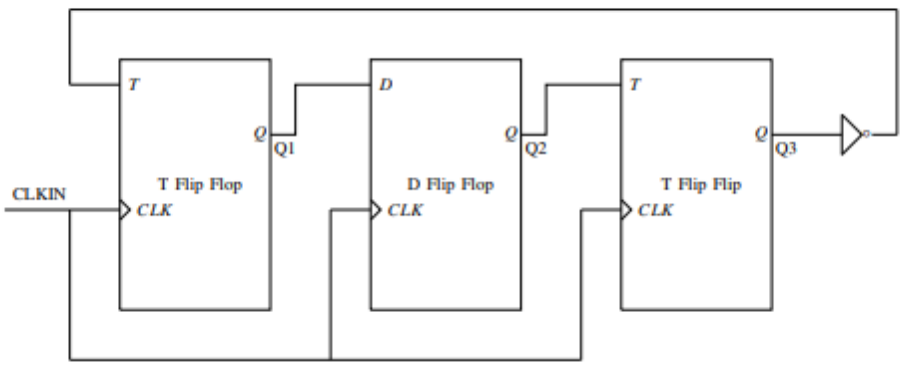

Fig. 5.9