CS 232 Lab 2 Q2

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22nd January 2022

NAND Gate(`nand_gate.vhd`)

I have designed the NAND Gate using Structural code. I have used AND Gate(`and_gate.vhd`) and NOT Gate(`not_gate.vhd`)

3×8 Decoder(`ThreebyEightDecode.vhd`)

I have designed the Decoder circuit using only NAND Gates directly.

The Encoder Logical Expression are as follows,

z(0) = en.($\overline{i(0)}.\overline{i(1)}.\overline{i(2)}$)
z(1) = en.($\overline{i(0)}.i(1).\overline{i(2)}$)
z(2) = en.($\overline{i(0)}.i(1).i(2)$)
z(3) = en.($i(0).\overline{i(1)}.\overline{i(2)}$)
z(4) = en.($\overline{i(0)}.\overline{i(1)}.i(2)$)
z(5) = en.($i(0).\overline{i(1)}.i(2)$)
z(6) = en.($\overline{i(0)}.i(1).i(2)$)
z(7) = en.($i(0).i(1).i(2)$)

To implement the NOT Gate used in the above logical Expression, I have used NAND Gate,

port map(a=>i(2),b=>i(2),c=>n0)

This gives n0 = $\overline{i(2)}$,
Similarly, n1 = $\overline{i(1)}$ and n2 = $\overline{i(0)}$.

To implement the AND Gate used in logical Expression, I have used NAND Gate 2 times,

AND = NAND + NOT(As done above).

port map(a=>n0,b=>n1,c=>s0);
s0 = $\overline{\overline{i(2)}.\overline{i(1)}}$

port map(a=>s0,b=>s0,c=>p0);
p0 = $\overline{i(2)}.\overline{i(1)}$

port map(a=>p0,b=>n2,c=>q0);
q0 = $\overline{\overline{i(2)}.\overline{i(1)}.\overline{i(0)}}$

port map(a=>q0,b=>q0,c=>r0);
r0 = $\overline{i(2)}.\overline{i(1)}.\overline{i(0)}$

port map(a=>r0,b=>en,c=>t0);
t0 = $en.\overline{i(2)}.\overline{i(1)}.\overline{i(0)}$

port map(a=>t0,b=>t0,c=>z(0));
z(0) = $en.\overline{i(2)}.\overline{i(1)}.\overline{i(0)}$

Therefore, when Enabler pin en=0 output is 00000000 else the signal will pass.

AND GATES = 2×8 + 4 (as i(2).i(1) is calculated only once but used two times) = 20
NOT GATES = 3
Thus total NAND Gates = 20×2 + 3×1 = 43