

CS 232 Lab 3 Q1

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1-bit half-adder(OnebitHalfAdd.vhd)

I have designed the 1-bit half-adder using the basic gates i.e. NOT Gate, AND Gate and OR Gate in a structural way.

The 1-bit half-adder Logical Expression is as follows,

$$\text{Sum} = A \text{ XOR } B = (A + B).(\overline{A} + \overline{B})$$
$$\text{Carry}(\text{cout}) = A.B$$

1-bit full-adder(OnebitFullAdd.vhd)

I have designed the 1-bit full-adder using only 1-bit half-adders and OR Gate.

The 1-bit full-adder Logical Expression are as follows,

$$\text{Sum} = (A \text{ XOR } B) \text{ XOR } \text{cin} = \text{Half-Adder-SUM}(\text{Half-Adder-SUM}(A,B), \text{cin})$$

$$\text{Cout} = A \text{ AND } B \text{ OR } \text{cin}(A \text{ XOR } B) = \text{Half-Adder-COUT}(A,B) + \text{Half-Adder-COUT}(\text{cin}, \text{Half-Adder-SUM}(A,B))$$

$$\begin{aligned} p &= \text{Half-Adder-SUM}(A,B), \\ q &= \text{Half-Adder-COUT}(A,B), \\ r &= \text{Half-Adder-COUT}(\text{cin}, p), \end{aligned}$$

$$\begin{aligned} \text{sum} &= \text{Half-Adder-SUM}(p, \text{cin}), \\ \text{cout} &= q + r \end{aligned}$$

Therefore using the above shown way I created the 1-bit half-adder where 'a' and 'b' are the two 1-bit numbers that are to be added. 'cin' is the input carry that should be added with 'a' and 'b'. 'sum' and 'cout' are the sum and carry outputs respectively.

$$\begin{aligned} \text{Half-Adders} &= 2 \\ \text{OR Gate} &= 1 \end{aligned}$$

Inside 1-bit Half Adder,
NOT Gate = 2
OR Gate = 2
AND Gate = 2