Experience

Computer Engineer III

Western Digital | 2021 – 2022

- Wrote machine learning software for identifying in-manufacturing hardware faults and anomalies
- Programmed low-level signal processing and testing tools in firmware
- Performed manual hardware failure analysis and staged large-scale data extraction

Graduate Researcher

UC Irvine | 2021 - 2022

- Wrote software and literature for modeling of multi-threaded / multi-core computers

Computer Engineer I

CiyaSoft | 2019 - 2021

- Developed low-level algorithms and testing tools for image processing and machine translation
- Wrote technical and analytical reports for legal team

Skills

Python	TypeScript	C & C++	Rust	General
SciKit	- D3.js	Boost	– Tauri	- SQL
NumPy	SvelteKit	SystemC	Rayon	Redis
Pandas	- WebGL 2			– DynamoDB
TensorFlow	- AWS SDK			- HTML & CSS

Projects

Website and blog

Python · SvelteKit · TypeScript · JavaScript

- Built with SvelteKit and Vite for easy server-side rendering and asset loading; deployed on Vercel
- Managing visitor analytics and auth with AWS DynamoDB, and API rate limiting with Upstash Redis

Signal classification and pattern matching

Western Digital | $C \cdot C + + \cdot Python$

- Built data extraction and transformation tools for factory testing data with Pandas
- Trained neural network to classify problematic data patterns in production with TensorFlow
- Wrote low-level DSP algorithms to extract statistical signal metrics for trainable pattern matching
- Designed and automated rich visualizations with Plotly to weigh manufacturing impact

Filmic, analog film emulation app

Rust · Svelte · WebGL · Python · TypeScript · JavaScript

- Developed photo editing app to mimic look of analog film stock
- Used Svelte for front-end logic and modularization, and D3.js for rich SVG UI manipulation
- Programmed GPU shaders for accelerated cubic interpolation and image processing in WebGL 2
- Implemented image processing features, e.g., tone curve, color response, granular noise, diffusion
- Developing cross-platform desktop version with Tauri for batch processing

Modeling of multi-core, checkerboard architecture

UC Irvine | $C++\cdot Python$

- Wrote software to model bespoke CPU architecture, with accompanying thesis and conf. paper

Education

M.S. Electrical and Computer Engineering

UC Irvine | 2022

B.S. Electrical Engineering, focus in DSP

CSU Long Beach | 2019