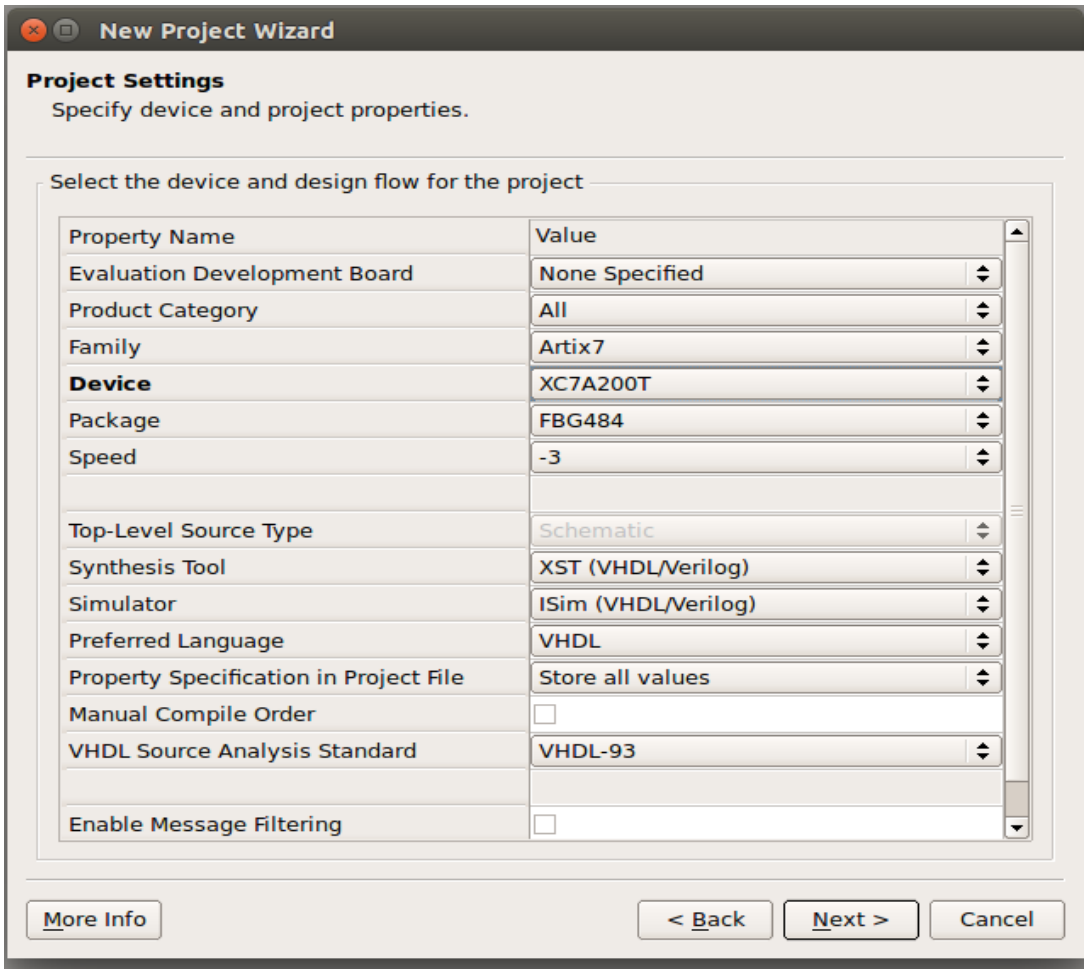
Tutorial – First project on Basys board using ISE and Vivado

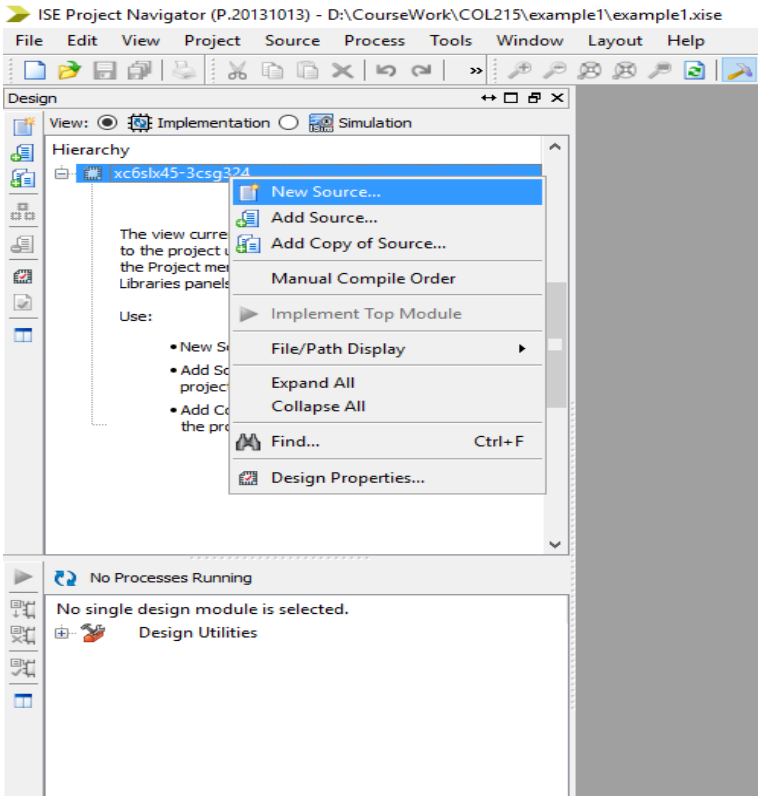
Using ISE

1. Open Xilinx ISE (type command ise in terminal).
2. File -> New Project -> Enter Name.

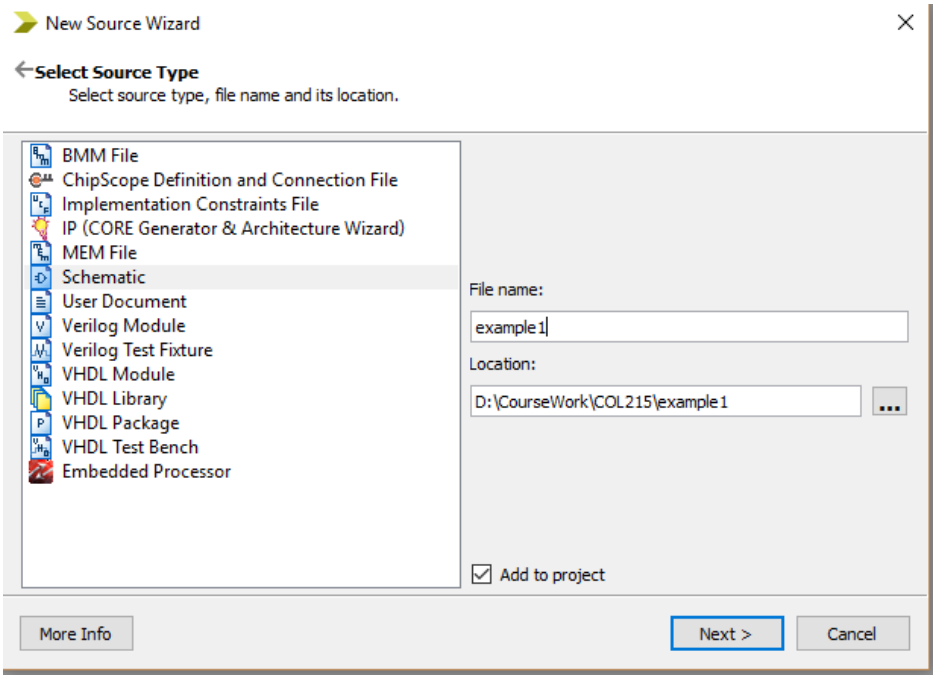


Use the settings indicated above and proceed.

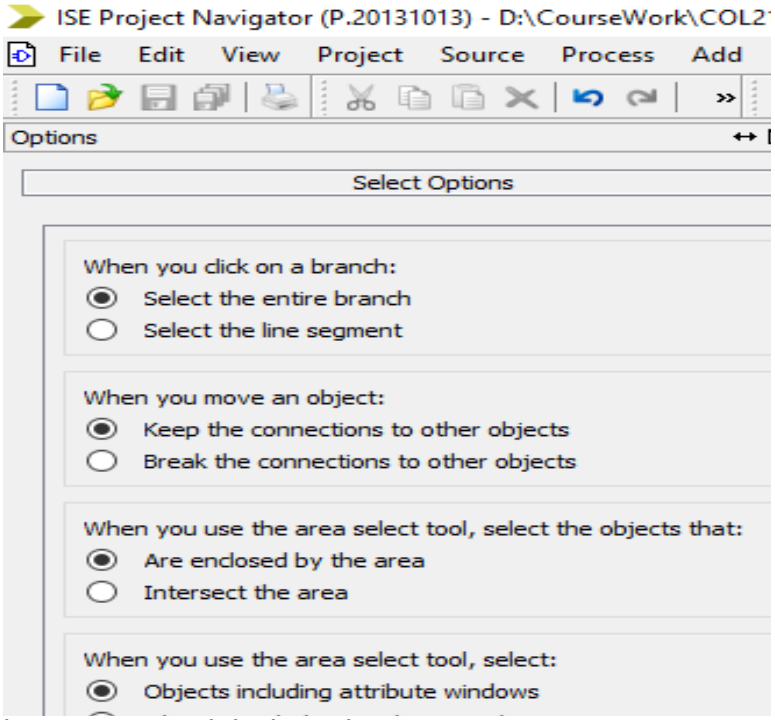
3. Click Finish.
4. Select New Source by right clicking on device name.



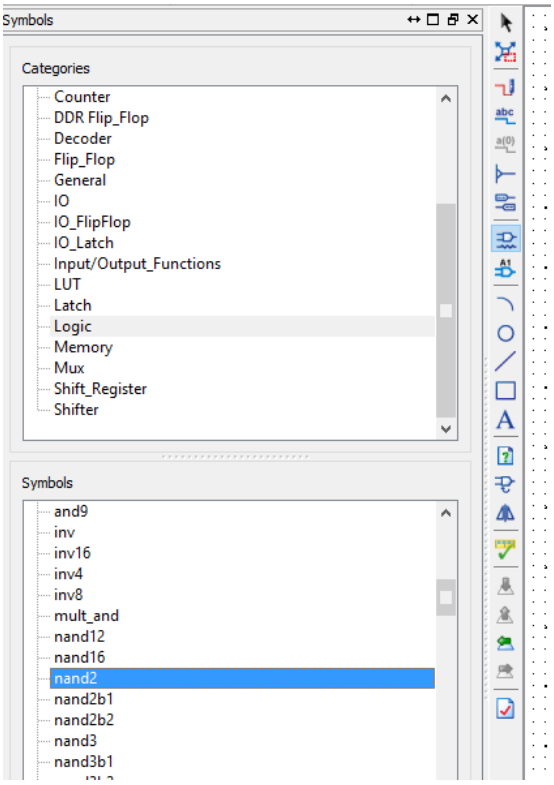
5. Select Source to be Schematic.



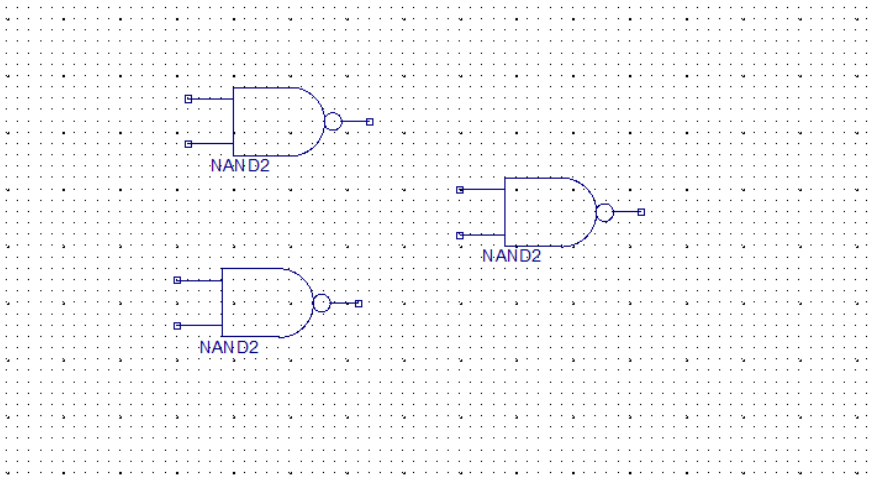
6. Next Finish. The schematic editor will open. Use zoom buttons on top to zoom in. (choose file name as specified in the problem statement).
7. Click on Add symbol button.



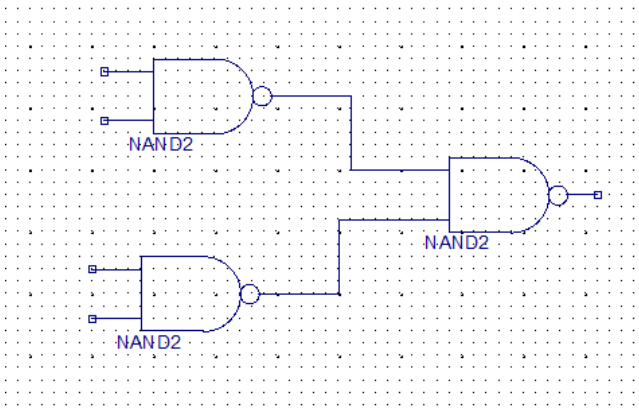
8. From the Logic Category, pick the relevant gates.



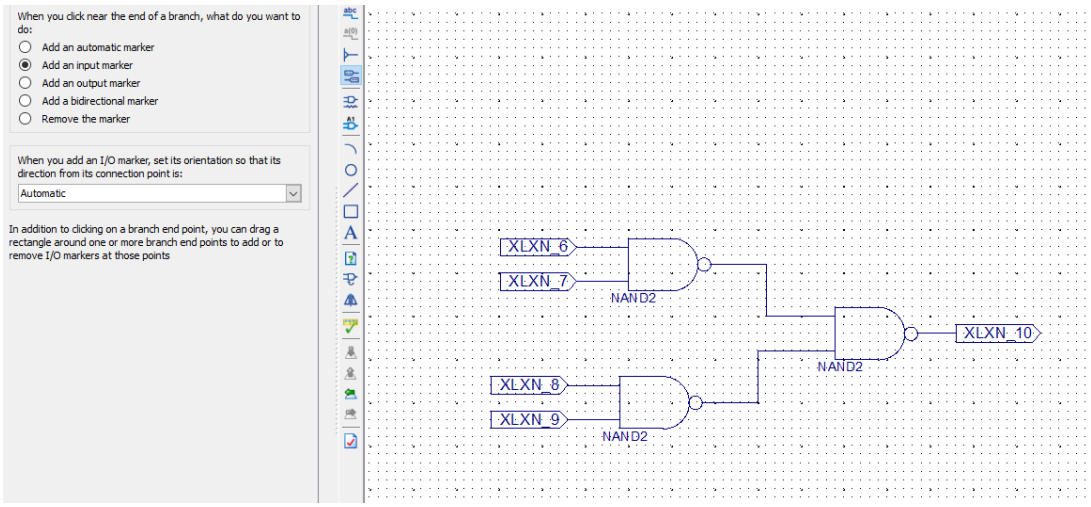
9. Make the circuit required.



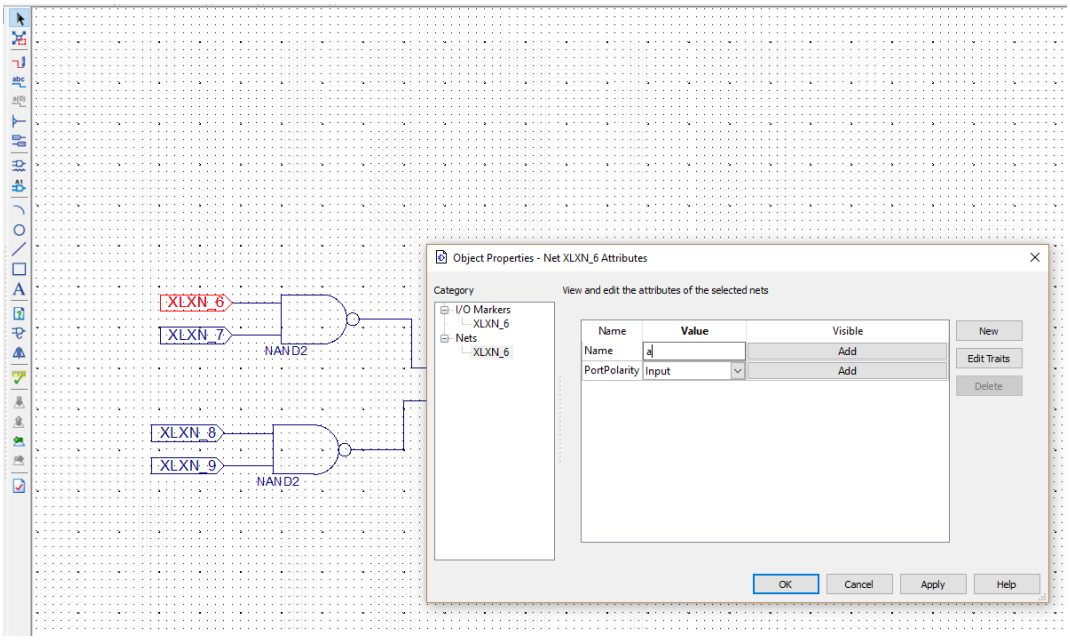
10. Use the wire button to connect these. (Tip: Click on the rectangles indicated to form the link).



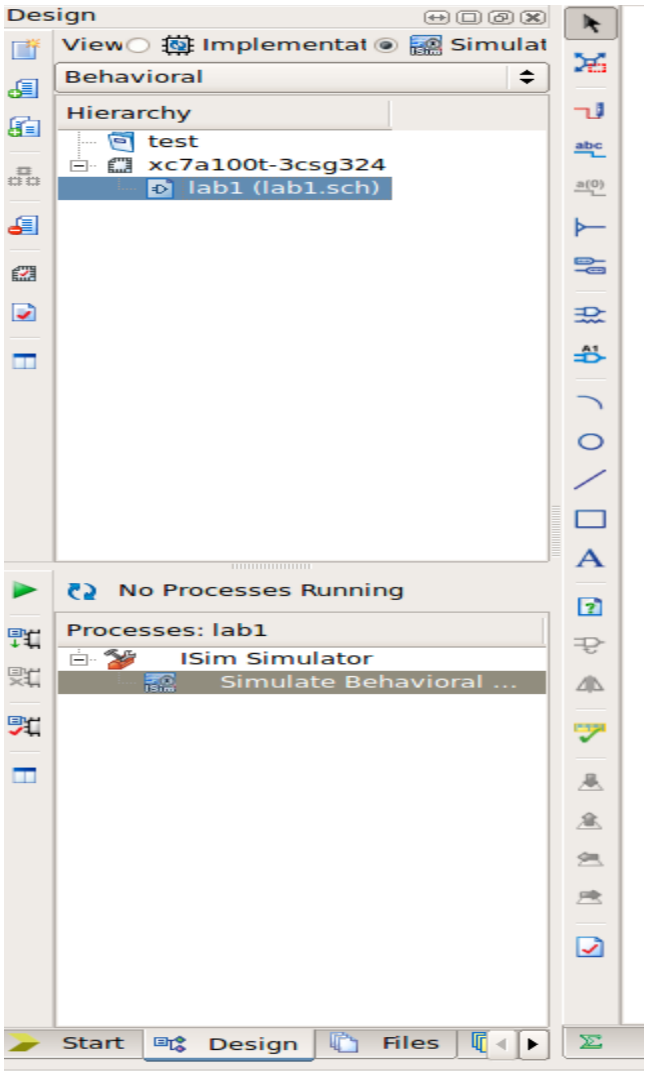
11. Add markers on input/output. (Choose I/O Marker tool -> select input marker/output marker from the menu on the left - click on the rectangles in order to form a connection.



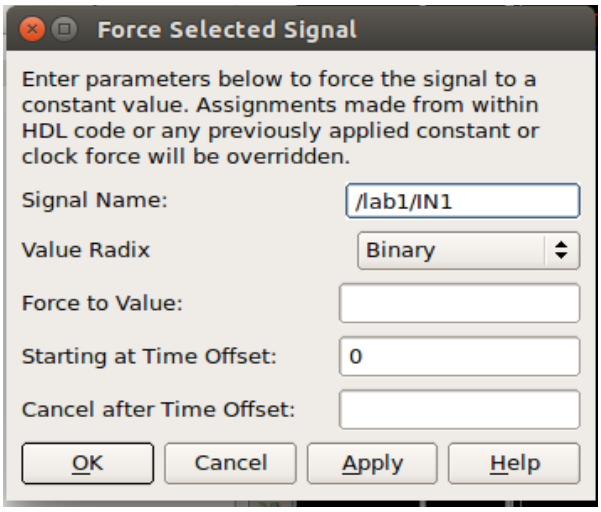
12. Using the select tool, double click on marker. Change the net name indicated in the window.



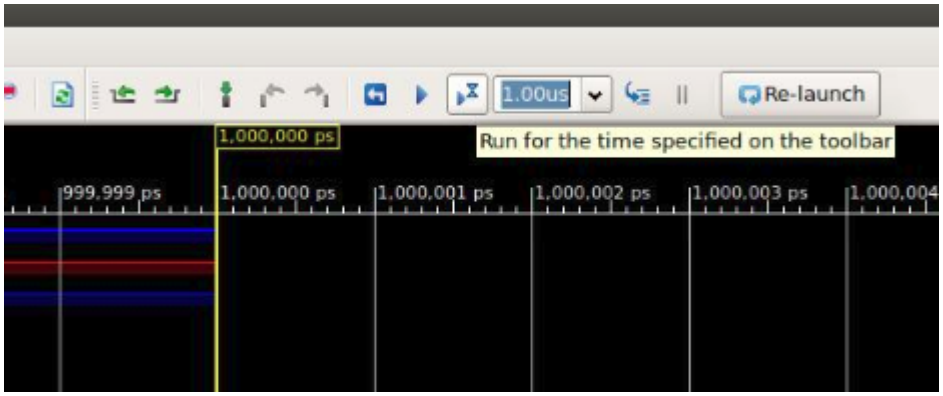
13. Similarly rename all markers in input/output. (use names as per the assignment document).
14. Click on Check schematic to check for any errors.
15. Click on the design tab in left bottom and then select simulation from the top. Expand Isim simulator and then click “simulate behavioral model”.



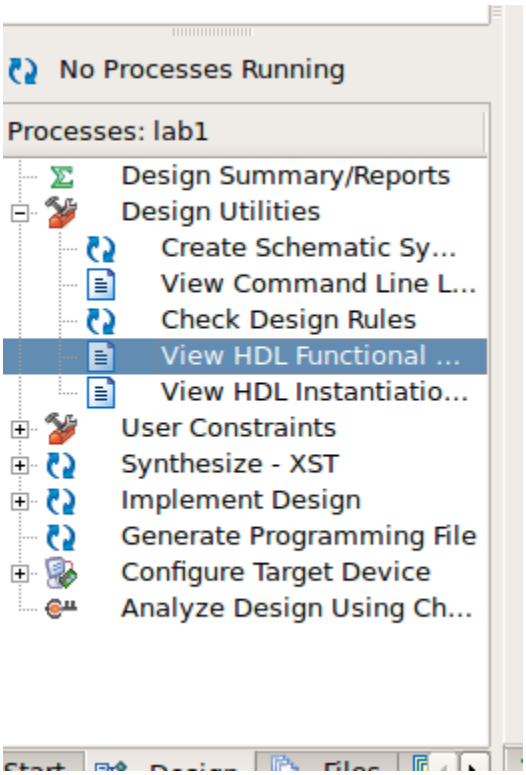
16. Once the new window opens, force different input signals and see the impact on output signals to ensure correctness of your design. To force a signal, right click on the signal and then select “Force constant”. (you can select force clock if you want a periodic toggle on the signal). In the window that pops up, write the value to be forced (0 or 1) in the “Force to value” box. Force either '0' or '1' on all the inputs.



17. Once required values are forced on all input ports, you can click on the button as highlighted in below image (run for time specified on the toolbar). It will run simulation for the duration specified in the time textbox. You can zoomin or zoomout to expand or compress the waveform view.

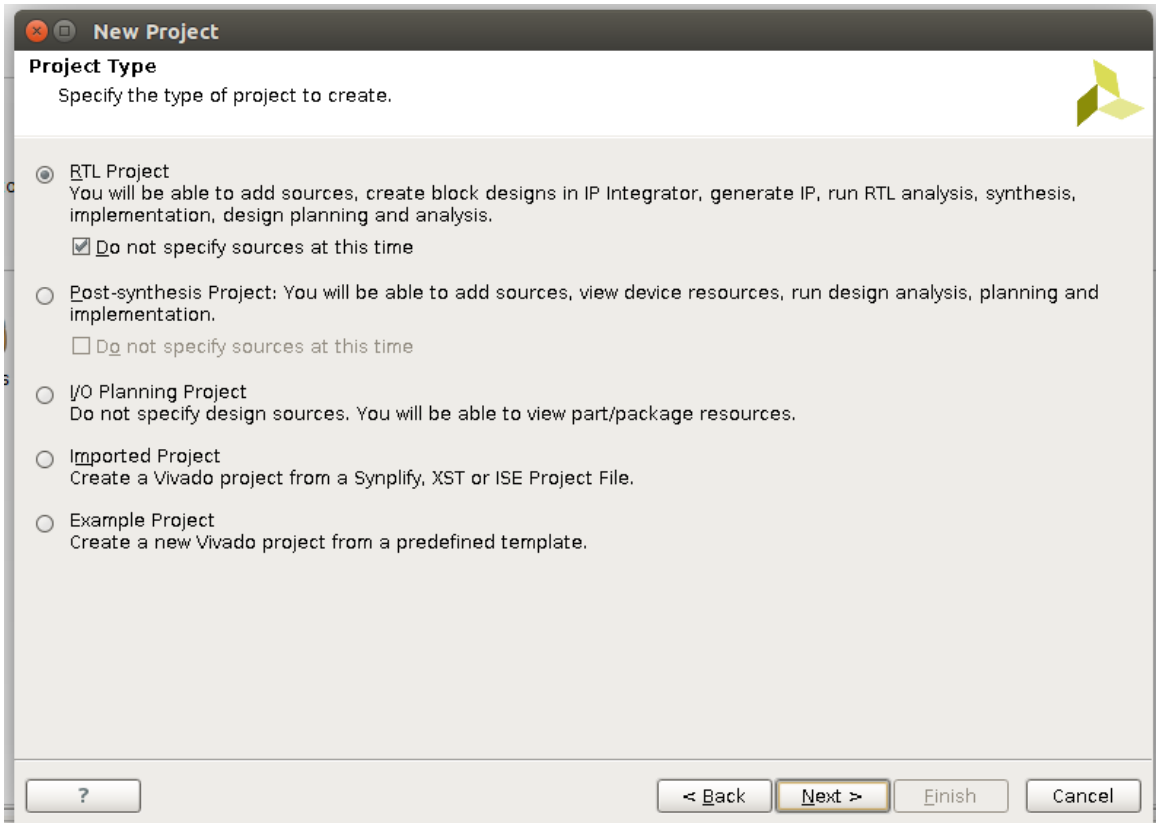


18. If you need to reset the simulation, you can click on re-launch as in the above window or close the window and re-invoke the same.
19. Verify different combinations of inputs to check for all possible scenarios. Once design is working correctly, now export the design as a vhdl design to be used in vivado. Click on the implementation in the left window and then expand design utilities tab. Click on “View HDL functional model”.
20. Copy the content of the file displayed into a new file named as per the requirement from the assignment document (e.g. in first lab it should be named as lab1_car_light.vhf). Save the file.

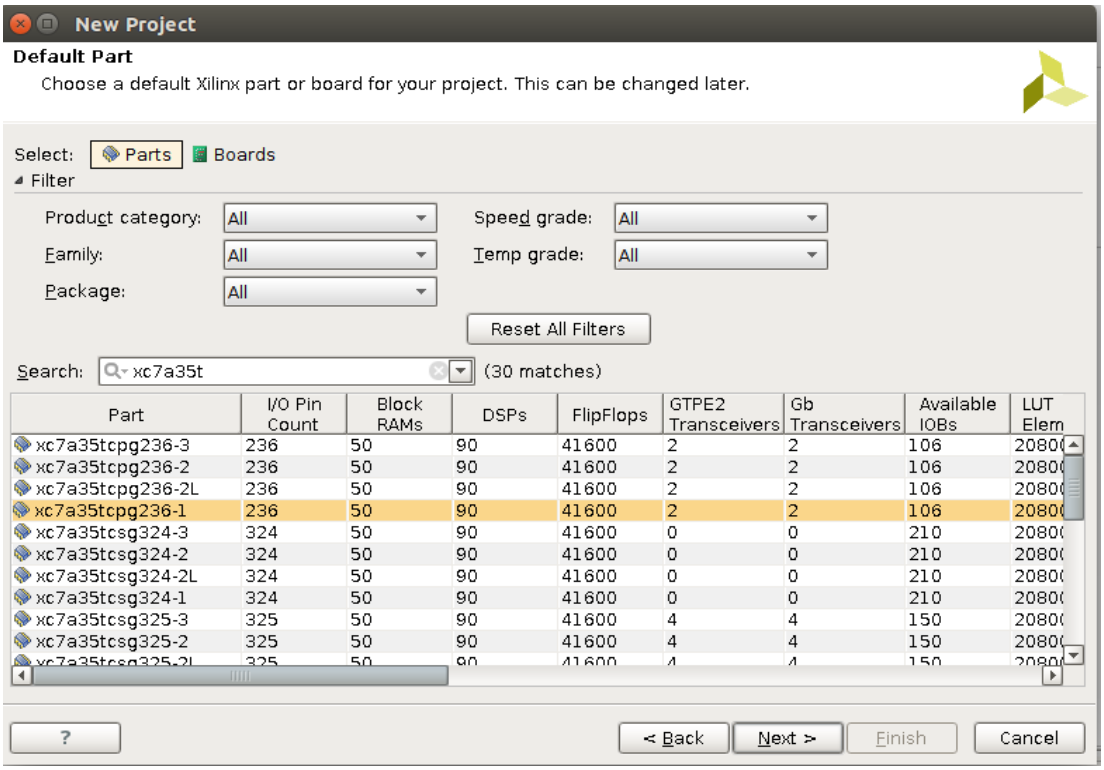

No Processes Running
Processes: lab1
Design Summary/Reports
Design Utilities
Create Schematic Sy...
View Command Line L...
Check Design Rules
View HDL Functional ...
View HDL Instantiatio...
User Constraints
Synthesize - XST
Implement Design
Generate Programming File
Configure Target Device
Analyze Design Using Ch...

Using Vivado

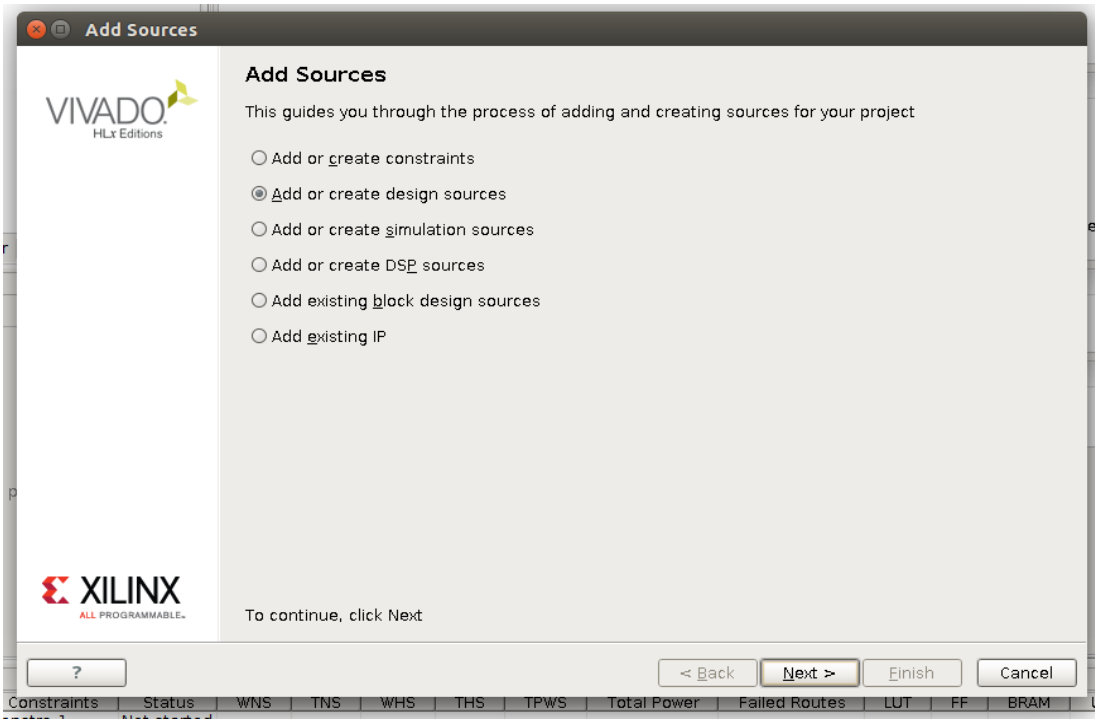
1. Open vivado (type command vivado in terminal).
2. Once the tool opens, click on Create New project.
3. Click Next.
4. Now select a directory for the project and a project name. (choose a relevant name, can be same as the ISE design name).
5. In the next screen, choose RTL project and enable the button “Do not specify sources at this time”.



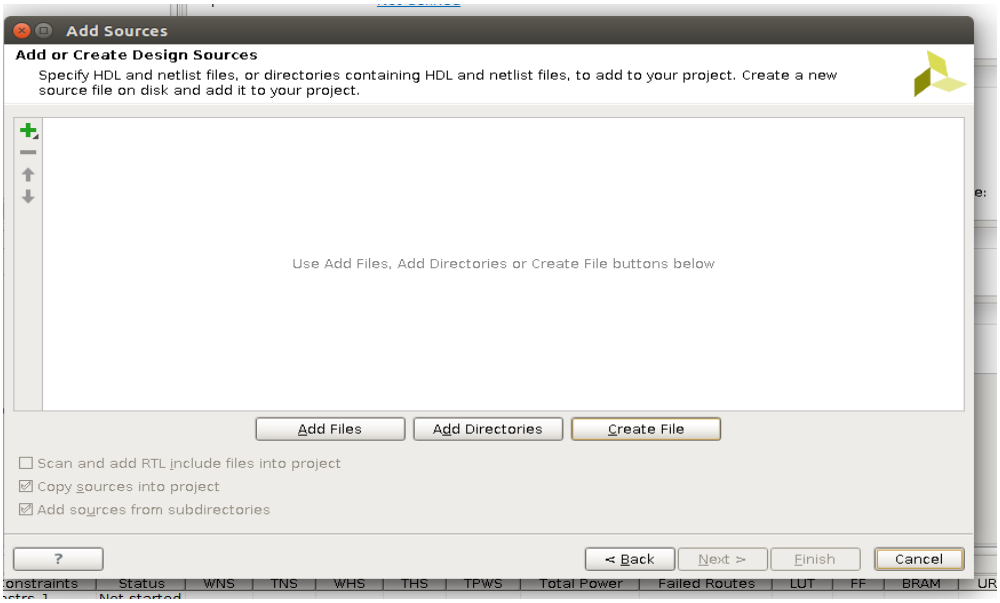
6. Click next and select the part number as xc7a35tcpg236-1 and click on next.



7. Click on Finish. The project is created.
8. Now we need to add sources. On the left pane, click on Add sources under project manager tab. Then click on “add or create design sources”

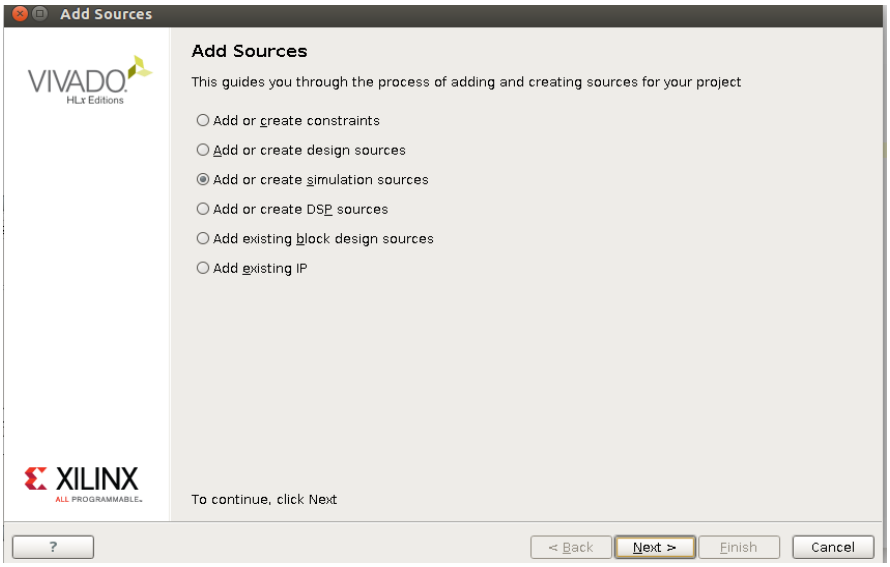


9. Click next and then on add files. Browse to add the vhdl file generated from ise schematic design. Enable the “copy sources into project” checkbox. Click on Finish.

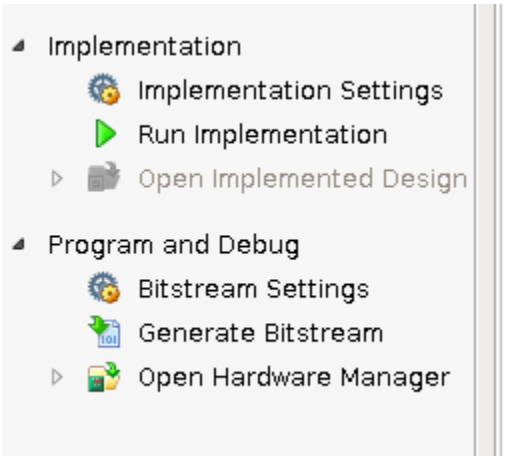


10. Similarly, add the constraints file (*.xdc file) that is provided to you by clicking on add design sources --> add or create constraints.

11. Also, add the testbench file (*test*.vhd file) that is provided to you by clicking on add design sources --> add or create simulation sources.



12. Click on Run simulation --> Run behavioral simulation and look at the tcl console window at the bottom. It shows your status of simulation and report any errors present. If you see errors, then please go back to schematic in ISE and fix it and repeat the process.
13. Click on generate bitstream in the left pane in the program and debug tab.



14. Once the process is complete, click on Open hardware manager → open target → Auto connect. Make sure that the basys board is ON.
15. Once this is over, you will see a link to program device. Click on it and check that the bit file path is correct. Click on program.
16. Now you can toggle switches on the board to ensure that your design works correctly on the board.