CA-memory QUIZ QUESTIONS

Q 1) .

	State of P0's cache	State of P1's cache	State of P2's cache	*State of P3's cache*
P0 reads a	*E*	*I*	*I*	*I*
P1 reads a	*S*	*S*	*I*	*I*
P2 reads a				
P3 writes a	*I*	*I*	*I*	*M*
P0 reads a	S	I	I	S

A four-processor shared-memory system implements the MESI protocol for the cache coherence.Each processors start out with the line containing a invalid in their cache. Tell the states of the columns which are not filled

A) S S I S
B) I S I S
C) S S S I
D) I I I S

Ans) c

Q 2)

```
int main()
{
    int sum =0;
    int array[16] = {0,1, 2,3,4 ,5,6, 7,8 ,9,10,11, 12,13 ,14,15


// loop 1
    for (int i = 0; i < 16; i++) {
    sum += array[i];
}

// loop2
for (int i = 0; i < 16; i += 4) {
    sum += array[i] + array[i+1] + array[i+2] + array[i+3];
}
}
```

Which of the following statements is true about the above code

A) The loop 2 reduces the number of iterations by a factor of 4 but requires more instructions per iteration.

B) The loop 2 will always execute faster than the first loop, regardless of the CPU architecture.

C) The loop 2 increases register pressure and might cause register spilling in some architectures, potentially degrading performance.

D) The loop 2 removes the loop overhead completely, leading to a significant performance improvement in all cases.

ans) c

Q 3)

```
int main()
{
    int x=0;
// Initially, x = 0  in main memory.

//  running on P1
P1: x = 1;

// running on P2(printing x)
P2: std::cout<<(x);
}
```

Consider the following pseudo-code running on two processors (P1 and P2) in a multi-core system with coherent caches. Which of the following statements is correct

A) In the MSI protocol, after P1 writes to x, the cache line will transition to the S (Shared) state in P1's cache.
B) In the MESI protocol, after P1 writes to x, the cache line in P1's cache will be in the E (Exclusive) state before it is modified.
C) In both MSI and MESI protocols, when P2 reads x after P1 writes to x, P2 will read the value 0 because the cache line is still dirty in P1's cache.

D) In the MESI protocol, after P2 reads x, the cache line in P1's cache will move to the M (Modified) state.
ans) B