Adder Chip Design

Need for Software

UET, Lahore Spring 2022

January 31, 2022

Contents

Addition of two 1-bit Numbers

A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Addition of two 1-bit Numbers

A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

The Equations for Sum and Carry can be found using a technique called *K-Maps*

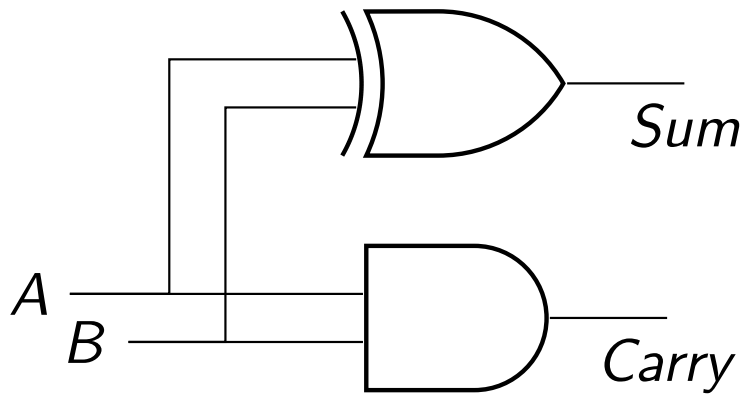
$$Sum = A \otimes B$$
$$Carry = A.B$$

Addition of two 1-bit Numbers

A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

The Equations for Sum and Carry can be found using a technique called *K-Maps*

$$Sum = A \otimes B$$
$$Carry = A.B$$



This is called a *Half Adder*.

Addition of three 1-bit Numbers

C	A	B	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Addition of three 1-bit Numbers

C	A	B	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

The Equations for Sum and Carry can be found using a technique called *K-Maps*

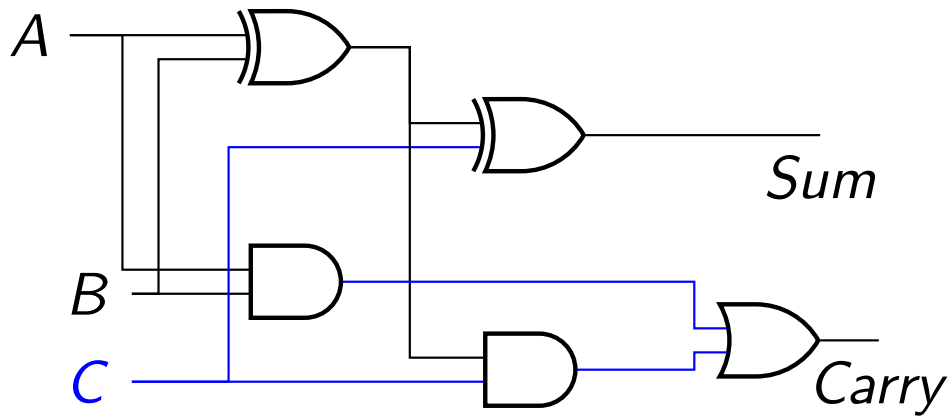
$$Sum = (A \otimes B) \otimes C$$
$$Carry = A.B + C(A \otimes B)$$

Addition of three 1-bit Numbers

C	A	B	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

The Equations for Sum and Carry can be found using a technique called *K-Maps*

$$Sum = (A \otimes B) \otimes C$$
$$Carry = A.B + C(A \otimes B)$$



This is called a *Full Adder*.

Addition of two 2-bit Numbers

For two bit numbers, bit wise addition is performed and the carry is carried to the next digit just like simple addition.

Addition of two 2-bit Numbers

For two bit numbers, bit wise addition is performed and the carry is carried to the next digit just like simple addition.

$$\begin{array}{cccc} & {\scriptstyle 1} & {\scriptstyle 1} & \\ & & 0 & 1 \\ + & & 1 & 1 \\ \hline & 1 & 0 & 0 \\ \hline \end{array}$$

Addition of two 2-bit Numbers

For two bit numbers, bit wise addition is performed and the carry is carried to the next digit just like simple addition.

$$\begin{array}{cccc} & {\scriptstyle 1} & {\scriptstyle 1} & \\ & & 0 & 1 \\ + & & 1 & 1 \\ \hline & 1 & 0 & 0 \\ \hline \end{array}$$

- Carry of first two bits becomes the third number for the second bits.

Addition of two 2-bit Numbers

For two bit numbers, bit wise addition is performed and the carry is carried to the next digit just like simple addition.

$$\begin{array}{cccc} & {\scriptstyle 1} & {\scriptstyle 1} & \\ & & 0 & 1 \\ + & & 1 & 1 \\ \hline & 1 & 0 & 0 \\ \hline \end{array}$$

- Carry of first two bits becomes the third number for the second bits.
- For addition of n-bits numbers, the C_{out} of previous bits will become the C_{in} for the next bits to be added. So a full adder will be required.

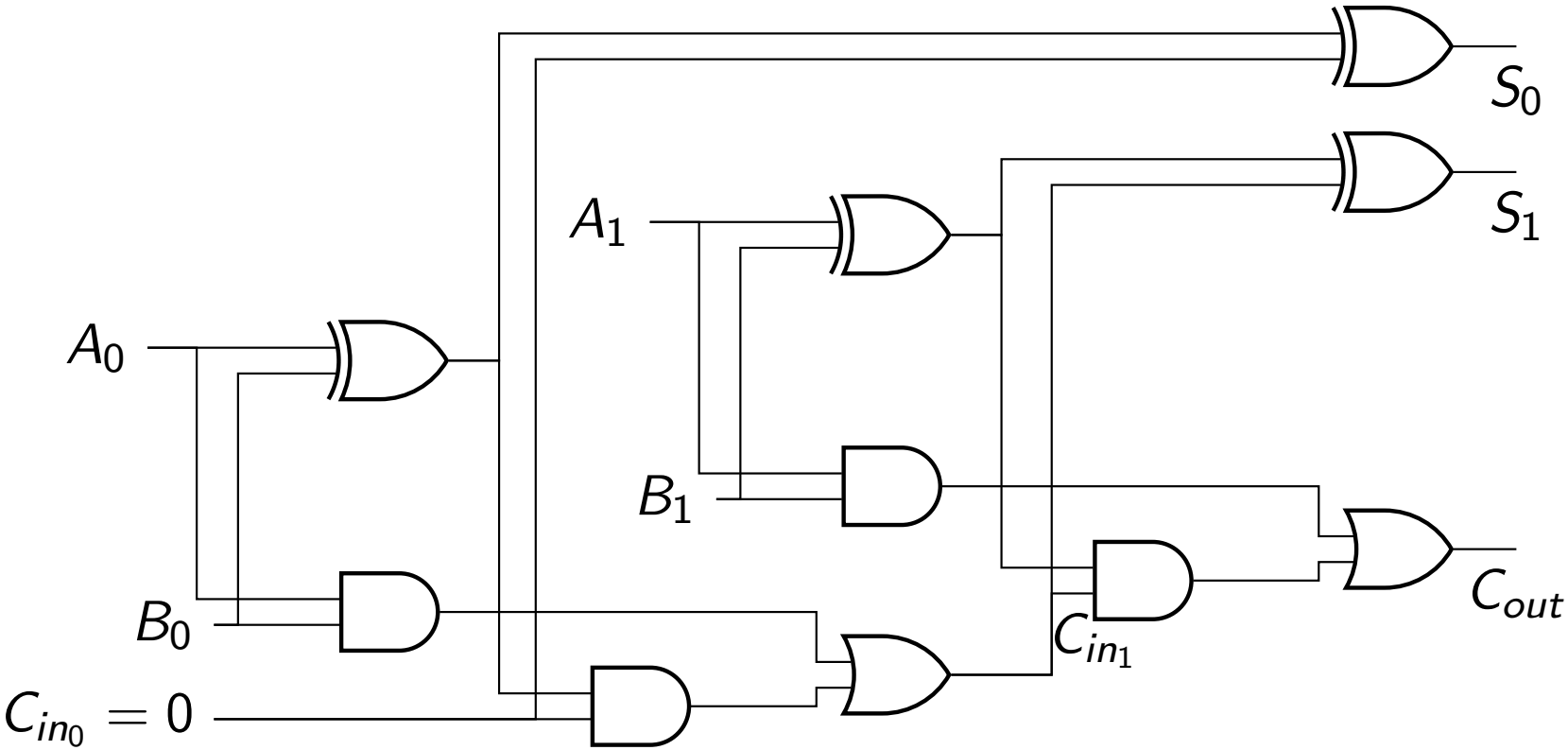
Addition of two 2-bit Numbers

For two bit numbers, bit wise addition is performed and the carry is carried to the next digit just like simple addition.

$$\begin{array}{cccc} & {\scriptstyle 1} & {\scriptstyle 1} & \\ & & 0 & 1 \\ + & & 1 & 1 \\ \hline & 1 & 0 & 0 \\ \hline \end{array}$$

- Carry of first two bits becomes the third number for the second bits.
- For addition of n-bits numbers, the C_{out} of previous bits will become the C_{in} for the next bits to be added. So a full adder will be required.
- For developing the gate level circuit, n-full adders will be implemented for adding n-bit numbers.

Gate Level Diagram for Addition of two 2-bit Numbers



Hardware Schematic and HDL

- The diagram which shows the connections of combinational gates is known as **Hardware Schematic**.
- It can be viewed in *Schematic* under RTL Analysis.
- The language which allows us to describe our code such that it gets translated to gate level is called **Hardware Descriptive Language**.
- Verilog is one of the hardware descriptive languages(HDL).

Synthesis and Implementation

- The software implements this design by alloting it the resouces it will require (limited by the total number of resources available in the FPGA) in **Synthesis**.
- Any code that is synthesizable is known as **RTL** (*Register Transfer Level*).
- Deciding which resource on the FPGA is actually used, is known as **Implementation**.
- Generating of 1's and 0's for this so that it can be understood by the FPGA is done by **Generating Bitstream**.