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Takafumi Kamimura, Yoshiaki Nakata, and Masataka Higashiwaki

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Takafumi Kamimura,[a] Yoshiaki Nakata, and Masataka Higashiwaki

AFFILIATIONS

National Institute of Information and Communications Technology, Koganei, Tokyo 184-8795, Japan

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[a]Author to whom correspondence should be addressed: kamimura@nict.go.jp

ABSTRACT

β-Ga_2O_3 metal-oxide-semiconductor field-effect transistors (MOSFETs) with gate lengths (L_g) of 50–1000 nm were fabricated, employing a thin channel layer formed by a shallow Si-ion implantation doping to maintain a high aspect ratio between an L_g and a gate-to-channel distance. The MOSFETs with $L_g = 200$ nm had a maximum drain current density of about 250 mA/mm and a peak extrinsic transconductance of 17 mS/mm. The short-channel effect was well suppressed for the devices with $L_g \geq 200$ nm, leading to excellent RF device characteristics represented by a record maximum oscillation frequency of 27 GHz at $L_g = 200$ nm. From simple delay-time analysis on the MOSFETs, the effective electron velocity passing through a region under the gate was estimated to be about 2×10^6 cm/s. Moreover, it was analyzed that the parasitic channel charging delay occupied a substantial proportion of the total delay due to a large sheet resistance of the Ga_2O_3 channel and thus limited their high-frequency device performance. These results suggest that both suppressing the short channel effect with a reduction in L_g to the sub-0.1-μm range and minimizing the access resistance are important to further improve RF device characteristics of Ga_2O_3 MOSFETs.

Beta-gallium oxide (β-Ga_2O_3) has been attracting a great deal of attention as an ultrawide-bandgap (UWBG) semiconductor with a bandgap energy of around 4.5 eV (Ref. 1) and a projected breakdown electric field of over 6 MV/cm.[2] β-Ga_2O_3 possesses some distinct features, surpassing other UWBG competitors in performance. For example, the electron density of β-Ga_2O_3 can be precisely controlled by intentional donor doping in a wide range, from low 10^{15} cm^{-3} to $>10^{20}$ cm^{-3}.[3–5] Bulk β-Ga_2O_3 single crystals with a low defect density can be synthesized applying atmospheric melt-growth techniques.[6–10] A variety of epitaxial growth techniques have also been used for Ga_2O_3.[11–16] These developments have reduced technological barriers to future practical applications and industrialization of Ga_2O_3 devices.

In terms of the high breakdown electric field and the predicted reasonable saturation electron velocity (v_{sat}),[17] Ga_2O_3 FETs can be expected to have an advantage in not only power switching but also RF applications over their competitors.[18–22] In fact, submicrometer-gate Ga_2O_3 FETs have exhibited good small-signal RF characteristics, such as a current-gain cutoff frequency (f_T) of 27 GHz (Ref. 21) and a maximum oscillation frequency (f_{max}) of 17 GHz.[19]

In addition, Ga_2O_3 metal-oxide-semiconductor field-effect transistors (MOSFETs) previously developed in our group have revealed superior operation stability at high temperature and/or under high-dose gamma-ray irradiation.[23,24] Considering the material properties of Ga_2O_3 that are strong against stresses caused by temperature and radiation and decent RF device performance of the Ga_2O_3 FETs reported so far,[18–22] high-frequency Ga_2O_3 FETs are promising for wireless communication applications in harsh environments where it is difficult to keep other semiconductor devices operational over an extended period of time.

In this study, we fabricated highly scaled Ga_2O_3 MOSFETs with gate lengths (L_g) of 50–1000 nm to systematically investigate the L_g dependences of their device characteristics. Typical MOSFETs with an L_g of 200 nm exhibited outstanding RF device characteristics, including a record f_{max} of 27 GHz. We also conducted simple delay-time analysis on the state-of-the-art MOSFETs to extract an effective electron velocity (v_e) and a proportion of each delay component to the total delay time (τ_{total}). Physical and technical knowledge on them is essential to develop further advanced high-frequency Ga_2O_3 FETs.

Figure 1 shows a schematic cross section of Ga_2O_3 MOSFET structures fabricated in this work. A 200-nm-thick unintentionally doped (UID) Ga_2O_3 layer was grown on an Fe-doped semi-insulating Ga_2O_3 (010) substrate by plasma-assisted molecular beam epitaxy.

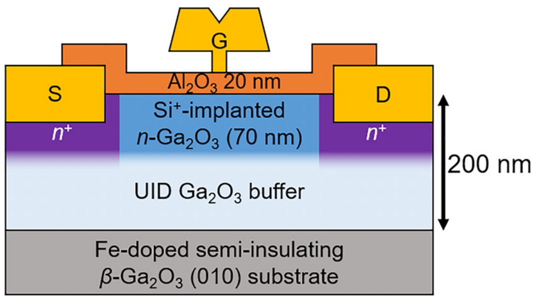

FIG. 1. Schematic cross section of T-gate Ga_2O_3 MOSFETs.

A standard effusion cell was used for Ga, and its beam flux was set at 1.9×10^{-7} Torr. Oxygen radicals were generated by decomposing high-purity O_2 gas with an RF-plasma cell. The O_2 flow rate was 2 sccm, and the plasma power was 250 W. The substrate temperature during the growth, monitored using an infrared pyrometer, was 630 °C. The growth rate of the UID Ga_2O_3 layer was 0.3 μm/h. The UID layer was nearly insulating with a high resistivity of 10^6–10^7 Ω·cm, which was obtained from two-terminal current–voltage characteristics for device isolation test structures fabricated on the same wafer.

Maintaining a high aspect ratio between an L_g and a gate-to-channel distance is well established as one of the most effective approaches to suppressing the short-channel effect. Based on this strategy, we designed the Ga_2O_3 MOSFETs incorporating a thin bulk channel with high-density donor doping to improve their RF performance by suppressing the short-channel effect while reducing L_g. For the device processing, selective-area Si-ion implantation doping at multiple energies and doses was first conducted to form a 70-nm-thick box profile with a plateau Si concentration of 4.8×10^{18} cm^{-3} in the MOSFET channel region.[25] Subsequently, Si ions were implanted to the source and drain Ohmic contact regions to form a 70-nm-thick box profile with Si $= 5 \times 10^{19}$ cm^{-3}. The implanted Si atoms in the channel and Ohmic contact regions were activated simultaneously by thermal annealing at 925 °C in N_2 for 30 min. After a 30-nm-deep recess was etched onto the Ohmic contact regions using BCl_3 reactive-ion etching (RIE) to ensure direct metal contact with the highly Si-doped region, a Ti(20 nm)/Au(230 nm) metal stack, for source and drain Ohmic electrodes, was deposited and then annealed at 470 °C. The contact resistance (R_c) of the source and drain electrodes was estimated to be 0.5 Ω·mm by the transmission-line method. A 20-nm-thick Al_2O_3 gate dielectric was formed by plasma atomic layer deposition at 250 °C using trimethylaluminum and O_2. T-shaped gate patterns with footprint lengths varying from 50 to 1000 nm were defined by a two-step 100-keV electron-beam lithography with a ZEP 520A/UV6 double-layer resist,[26] and a Ti(3 nm)/Pt(12 nm)/Au(350 nm) gate metal stack was deposited and lifted off. Finally, the Al_2O_3 placed atop the source and drain pad metals for probing was removed by BCl_3 RIE. We fabricated Ga_2O_3 MOSFETs with two-finger gates (50 μm × 2) and source-to-drain distances ($L_{s\text{–}d}$) of 2, 3, and 4 μm. The gate finger was placed at the center between the source and drain electrodes.

The room-temperature mobility, sheet carrier density, and sheet resistance (R_{sh}) of the Si-doped n-channel region were estimated to be 78 cm^2/V s, 1.0×10^{13} cm^{-2}, and 8 kΩ/□ by the Hall measurement, respectively.

Typical DC and pulsed drain current density–drain voltage (I_d–V_d) output characteristics and DC transfer characteristics are presented in Figs. 2(a) and 2(b), respectively, which were measured for the Ga_2O_3 MOSFETs with an L_g of 200 nm and an $L_{s\text{–}d}$ of 2 μm. The MOSFETs exhibited a maximum I_d of about 250 mA/mm at a V_d of 10 V and a gate voltage (V_g) of +4 V. Small current collapse was observed in the pulsed output characteristics compared with the DC ones, attributing to charge traps at the gate dielectric/Ga_2O_3 interface and/or in the Ga_2O_3 channel. The DC peak extrinsic transconductance (g_m) was 17 mS/mm at $V_d = 10$ V and $V_g = -18$ V. Additionally, a good pinch-off characteristic with a threshold V_g of −24 V was obtained. For the devices with $L_g = 300$ nm, the off-state breakdown voltages measured at $V_g = -30$ V were 73, 77, and 99 V for $L_{s\text{–}d} = 2$, 3, and 4 μm, respectively.

Small-signal RF performance of the Ga_2O_3 MOSFETs was characterized by on-wafer S-parameter measurements using an HP8510C vector network analyzer. S-parameters for open-pad structures fabricated on the same wafer were also measured to subtract the parasitic capacitance components related to the pad metals from the as-measured extrinsic parameters. It should be noted that no resistance and inductance components were subtracted from the extrinsic parameters. Current gain ($|H_{21}|^2$), maximum stable gain/maximum available gain (MSG/MAG), and unilateral gain (U_g) as a function of frequency of the MOSFETs with $L_g = 80$ and 200 nm are shown in Figs. 3(a) and 3(b), respectively. The f_T was determined by extrapolation of $|H_{21}|^2$ with a −20 dB/decade slope, and the f_{max} was defined at a frequency at which both MAG and U_g became 0 dB. The devices exhibited the state-of-the-art small-signal RF characteristics of an f_T of 10 GHz at $L_g = 80$ nm and an f_{max} of 27 GHz at $L_g = 200$ nm. Note that this f_{max} value is the highest ever reported for Ga_2O_3-based transistors.

Figures 4(a) and 4(b) present the L_g dependences of f_T and f_{max}, respectively. The f_T monotonically increased with decreasing L_g for $L_g > 200$ nm and remained at an almost constant value of 9–10 GHz

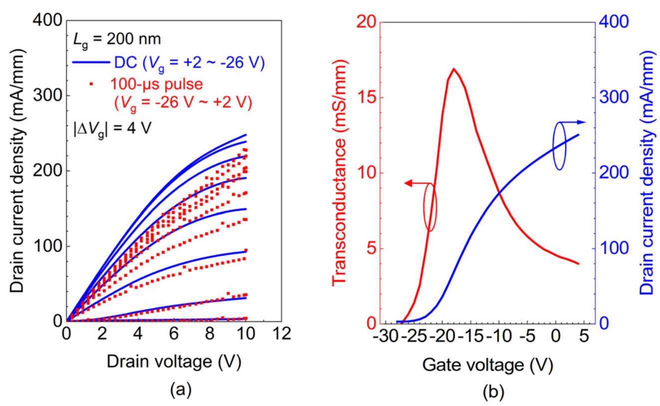

FIG. 2. (a) DC and pulsed I_d–V_d characteristics and (b) DC transfer characteristics at $V_d = 10$ V of Ga_2O_3 MOSFETs with $L_g = 200$ nm. In the pulse measurement, the off-state quiescent V_d and V_g were set at 10 V and −26 V, respectively. The pulse width and period were 100 μs and 100 ms, respectively.

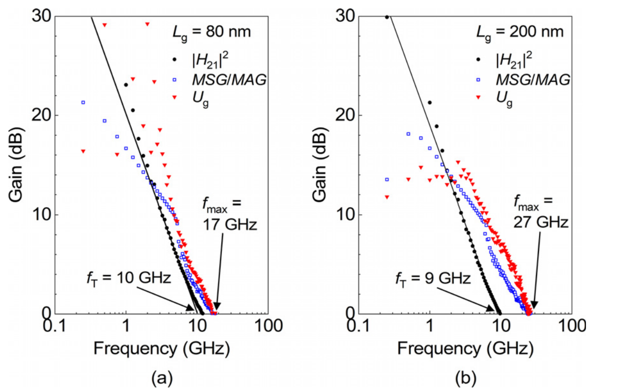

FIG. 3. RF small-signal characteristics of Ga_2O_3 MOSFETs with (a) $L_g = 80$ nm ($V_d = 10$ V, $V_g = -21$ V) and (b) $L_g = 200$ nm ($V_d = 10$ V, $V_g = -20$ V).

for $L_g < 200$ nm. However, the f_{max} increased inversely proportional to the L_g for $L_g > 200$ nm, which was similar to the f_T, peaked at $L_g = 200$ nm, and decreased sharply with decreasing L_g for $L_g < 200$ nm. It can be considered that the degradations of f_T and f_{max} at $L_g < 200$ nm were mainly due to insufficient suppression of the short-channel effect.

RF gate-to-source and gate-to-drain capacitances (C_{gs} and C_{gd}), and g_m and drain conductances (g_d) are plotted as a function of L_g in Figs. 4(c) and 4(d), respectively. Those were calculated using the S-parameters at 3 GHz. In the S-parameter measurements, the V_d was fixed at 10 V, and the V_g for each L_g was set at a value that the g_m peaked. Both the C_{gs} and C_{gd} gradually decreased with decreasing L_g over the entire range, indicating that the L_g were well controlled as designed. On the other hand, the g_m and g_d remained almost constant in the range of $L_g > 200$ nm, and decreased and increased with decreasing L_g for $L_g < 200$ nm, respectively. These behaviors were ones of the typical signatures of the short-channel effect.

In FET delay-time analysis, τ_{total} ($= 1/2\pi f_T$) consists of three components: an intrinsic transit delay (τ_{int}), a drain delay (τ_{drain}), and a channel charging delay (τ_{charge}), which are associated with carrier transport across a region under the gate, carrier transport across the depletion region extended from the gate edge toward the drain, and an RC time constant, respectively,[27] and is given by

$$\tau_{total} = \frac{C_{gs} + C_{gd}}{g_m} + (R_s + R_d) \times \left[C_{gd} + (C_{gs} + C_{gd}) \cdot \frac{g_d}{g_m} \right], \qquad (1)$$

where R_s and R_d are the source and drain parasitic access resistances, respectively.[28]

Figure 5(a) plots the τ_{total} of the MOSFETs with $L_{s\text{-}d} = 2\ \mu$m as a function of L_g. The τ_{total} linearly decreased with decreasing L_g in the range of $L_g > 200$ nm and deviated from the linear fitting line for $L_g < 200$ nm due to the short-channel effect. A v_e of 2.1×10^6 cm/s was extracted from the slope of the fitting line in Fig. 5(a). Similar extractions were also performed for the devices with $L_{s\text{-}d} = 3$ and 4 μm, yielding v_e values of 2.5×10^6 and 1.9×10^6 cm/s, respectively. The extracted v_e corresponded to the average velocities of electrons traveling in the whole region under the gate, and the analyses were carried out for the FETs with a relatively large L_g of over 200 nm. Therefore, it can be considered that the transit time at the v_{sat} in the high electric-field region around the drain-side gate edge occupied a

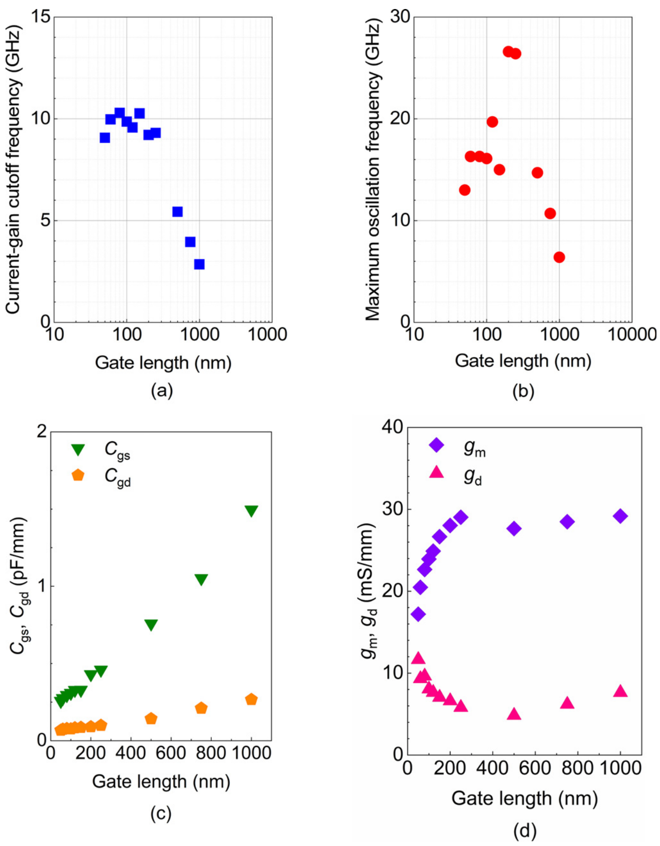

FIG. 4. L_g dependences of (a) f_T, (b) f_{max}, (c) C_{gs} and C_{gd}, and (d) g_m and g_d of Ga_2O_3 MOSFETs.

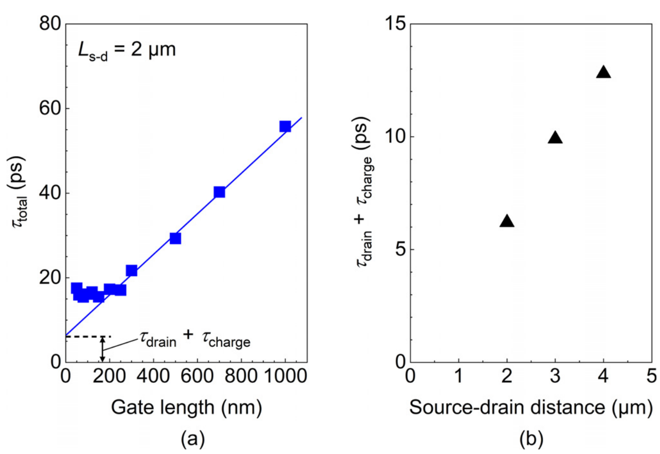

FIG. 5. (a) L_g dependences of τ_{total} for Ga_2O_3 MOSFETs with $L_{s\text{-}d} = 2\ \mu$m; (b) $\tau_{drain} + \tau_{charge}$ as a function of $L_{s\text{-}d}$.

small portion of the τ_{int}; therefore, the extracted v_e were rather reasonable values for the theoretical v_{sat} of 1.0–1.5 × 10^7 cm/s.[17]

We subsequently analyzed a ratio of the τ_{charge} in the τ_{total}. As presented in Fig. 5(a), the vertical-axis intercept of the fitting line in the τ_{total} vs L_g plot provides a sum of the τ_{drain} and τ_{charge} for the MOSFETs with $L_{s\text{–}d} = 2\,\mu$m. The same analyses were also conducted for the devices with $L_{s\text{–}d} = 3$ and $4\,\mu$m. The estimated $\tau_{drain} + \tau_{charge}$ values for $L_{s\text{–}d} = 2$, 3, and $4\,\mu$m are plotted in Fig. 5(b). The $\tau_{drain} + \tau_{charge}$ seems to increase roughly in proportion to $L_{s\text{–}d}$. It can be assumed in these analyses that the τ_{drain} is almost constant, irrespective of $L_{s\text{–}d}$, and that the τ_{charge} becomes a negligibly small value at $L_{s\text{–}d} = 0\,\mu$m, since the R_c occupies a very small portion of the R_s and R_d. Therefore, these results indicate that the τ_{charge} accounts for a considerable portion of the τ_{total}. In fact, for the FET with $L_g = 200$ nm and $L_{s\text{–}d} = 2\,\mu$m, the τ_{charge} was calculated to be ∼4 ps by substituting the experimental RF C_{gs}, C_{gd}, g_m, and g_d values plotted in Figs. 4(c) and 4(d), the R_s and R_d values of 85 Ω that were deduced from the channel R_{sh} (8 kΩ/□), and the source and drain R_c (0.5 Ω·mm) into the second term of Eq. (1). This value is one order of magnitude larger than those of high-frequency GaAs, InGaAs, and GaN FETs with the similarly dimensioned gates and structures.[27,29–32] From these analyses, the large τ_{charge} was attributed to the large R_s and R_d owing to the high R_{sh}. Significant reduction in the access resistance is considered to be indispensable in improving high-frequency performance of Ga_2O_3 MOSFETs, and self-aligned-gate FET structures would be one of the options.[33]

In conclusion, we fabricated highly scaled T-gate Ga_2O_3 MOSFETs using a Si-ion implantation doping process. The MOSFETs exhibited remarkable DC and small-signal RF device characteristics, represented by a maximum I_d of 250 mA/mm, an f_T of 10 GHz ($L_g = 80$ nm), and an f_{max} of 27 GHz ($L_g = 200$ nm). However, enhancements of the f_T and f_{max} by decreasing the L_g, respectively, saturated and peaked at $L_g \sim 200$ nm because the short-channel effect was not well suppressed for $L_g < 200$ nm. Simple delay-time analysis extracted a v_e of about 2×10^6 cm/s, which corresponds to L_g/τ_{int}. Furthermore, the analysis revealed that a large portion of the τ_{total} was occupied by the τ_{charge} due to a high R_{sh} of the channel. These results indicate that the optimization and modification of the device structure, both to suppress the short-channel effect and to minimize access resistance, will be required to further improve the RF device characteristics by decreasing the L_g to a sub-0.1-μm region.

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DATA AVAILABILITY

The data that support the findings of this study are available within the article.

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