Bias Dependence of the MODFET Intrinsic Model Elements Values at Microwave Frequencies

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Abstract—**S-parameters of MODFET's were measured versus bias instead of frequency with a special feature of the HP8510 Network Analyzer. Figure of merit plots, f_T and f_{max}, were quickly generated from the bias sweeps of S-parameters and optimum bias points were easily found. The intrinsic device elements of MODFET's were calculated after de-embedding the measurements from the device parasitics. The technique is demonstrated with a 0.15-μm pseudomorphic MODFET with an f_T of 150 GHz. The usefulness of the technique for understanding the operation of the MODFET's is discussed. With this technique a bias scan of an intrinsic element value can be measured and plotted in 13 s.**

I. Introduction

A TECHNIQUE for quickly measuring the strong bias dependence of MODFET microwave characteristics is important for understanding device physics and for improving device performance. The various delays in a MODFET can be analyzed by plotting $1/(2 \cdot \pi \cdot f_T)$ versus bias [1], [2]. Physical models that have recently been developed to predict the behavior and *Y*-parameters of MODFET's [3]–[5] need fast characterization techniques useful over a wide range of bias to provide the feedback necessary to increase our confidence in them so that they can be used for designing better MODFET's. Plots of f_T, f_{max}, etc. versus bias are important to circuit designers for finding the optimum bias point and knowing the sensitivity of performance to bias.

The usual method for determining the bias dependence of the small-signal model intrinsic device element values is to measure the *S*-parameters of the device versus frequency at several bias points, store the data, and then extract small-signal models at each point. This method is slow and laborious, often taking days to complete. This method is analogous to measuring device dc characteristics with voltmeters and ammeters. The microwave equivalent of a curve tracer (Tek 576) or dc parameter analyzer (HP4145) would greatly improve our understanding of device physics. The bias scan technique described in this paper brings us one step closer to this goal.

The bias scan technique described in this paper is virtually interactive. *S*-parameters are measured versus bias instead of frequency with the network analyzer. Algorithms were developed to de-embed the *S*-parameters from the device parasitics and then to calculate intrinsic element values from *S*-parameters at one frequency in real time. Element values at many bias points (>50) were quickly generated. This information is important for both understanding the physics of operation of MODFET's and optimization for their design for millimeter-wave circuit applications. Integration of output conductance (or transconductance) and capacitances with respect to bias voltages gives the microwave real current and charge functions necessary for large-signal models [6].

Extreme bias conditions, which are seldom explored with the usual method for extracting model element values because it is so laborious, are now easily measured. With the bias scan technique we routinely measured MODFET's in passive, pinched off, linear, and saturated conditions. The plots of intrinsic element values over wide ranges of bias were very useful for understanding the operation of MODFET's and determining parasitics. The bias scans revealed behavior not normally observed, such as bias regions where G_{ds} is negative. Frequency dispersion of g_m and G_{ds} (due to phenomena such as trapping by the DX center) are easily identified by comparing values of these elements measured with microwave bias scans and dc bias scans.

II. Bias Sweep Technique

The procedure is to first calibrate an HP8510 Automatic Network Analyzer (ANA) at a given center frequency (e.g., 25 GHz for a 0.15-μm gate-length MODFET) with a narrow span (e.g., 100 MHz). With such a narrow span, the frequency can be considered constant because devices have a low *Q*. The center frequency is chosen to be of interest for measuring gain versus bias or an optimal frequency for extracting the small-signal circuit elements. The second step is to calibrate the ANA by normal procedures.[1] Next put the HP8510 ANA in its "AUX VOLT" domain. In this mode (domain), the "START" and "STOP" stimulus keys control the sweep output of a 10-V bipolar supply at the rear of the instrument. This voltage is then used to control the device bias.

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[1] A calibration is not necessary if the HP8510 ANA has a synthesizer and there is a wide frequency calibration. The center frequency is set to one of the wide frequency sweep values. The calibration coefficients for that frequency are used for all the points for the bias sweep calibration. This procedure is implemented in software.

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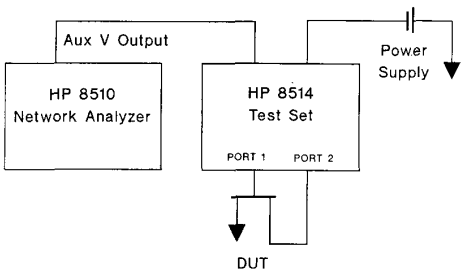

Fig. 1. Schematic drawing of setup for bias scan technique.

In this mode, the ANA measures and displays error-corrected S-parameters versus the many aux voltage bias points (e.g., 51 to 801) in a single sweep. The setup is shown schematically in Fig. 1. Small differences between the programmed and measured voltages are observed (e.g., 60 mV). It is usually not necessary to know the bias to this accuracy; however, when needed, the zero and ramp errors can be corrected with software or hardware.

The aux voltage can be used to control the gate voltage of a MODFET directly because it has a high dc input impedance. The aux voltage supply has a current limit of 10 mA. Higher current can be supplied by feeding the aux voltage to the remote programming voltage control available with many dc power supplies (e.g., HP6205C). A current source can be driven with the aux voltage for current sweeps. Software can be used to calculate the current at each point on the sweep.

III. Power Gain and Frequencies of Merit versus Bias

The S-parameters were acquired by an HP9836 computer with a HP85014 measurement program. Subroutines were added to this BASIC 5.1 program to calculate power gain (e.g., $G_{A\max}$, $G_{U\max}$, U, etc.) and frequencies of merit (f_T and $f_{\max}$) and then to plot or print the parameters versus bias.

The frequency of unity current gain f_T was estimated by calculating H_{21} at the measurement frequency f and assuming that $|H_{21}|^2$ decreased at -20 dB/decade.

$$f_T = |H_{21}| \cdot f. \tag{1}$$

This assumption is not always true [7], [30]. The slope of $|H_{21}|^2$ versus frequency can deviate from -20 dB/decade at high frequencies because of feedback inductances and capacitances and at low frequencies because of diode conductance in parallel with the input capacitance. If results are doubted at a particular bias range (e.g., forward-bias FET), normal frequency sweeps can be used to confirm the validity of the assumption. The frequency for bias sweeps is selected such that the assumption of calculating f_T or element values have the minimum errors.

The frequency of unity power gain $f_{\max}$ can be estimated from the maximum available gain $G_{A\max}$ at the bias sweep frequency if $G_{A\max}$ had a -20-dB/decade slope. To assume a -20-dB/decade slope, the stability factor K should be greater than about 2 at the measurement frequency. K was usually less than 1 at the measurement frequencies for the MODFET's that we were most interested in. Therefore, $f_{\max}$ could not be calculated from $G_{A\max}$. It had to be calculated from model element values. Approximate values for $f_{\max}$ were calculated with the following expressions:

$$f_{\max} = \frac{f_{Ti}}{\left[4 \cdot G_{ds} \cdot R_{\text{in}} \cdot (1 + F)\right]^{1/2}}. \tag{2}$$

F is a term containing the negative feedback terms

$$F = \frac{\omega_T \cdot L_s}{R_{in}} + \frac{2 \cdot \omega_T \cdot C_{gd}}{G_{ds}} \cdot \left[1 + \frac{R_g}{R_{in}} + \frac{\omega_T \cdot L_s}{2 \cdot R_{in}} + \frac{2 \cdot \pi \cdot \tau}{C_{gs} R_{in}}\right]. \tag{3}$$

f_{Ti} is calculated with (1) after de-embedding the H-parameters from the parasitics. In the saturated region, f_{Ti} can be approximated [31] with the common equation

$$f_{Ti} = \frac{g_m}{2 \cdot \pi \cdot (C_{gs} + C_{gd})} \tag{4}$$

$$R_{in} = R_g + R_s + R_{gs} \tag{5}$$

$$\omega_T = 2 \cdot \pi \cdot f_T. \tag{6}$$

The expression for $f_{\max}$ was obtained by combining the expressions given by Wolf [8] and Ohkawa *et al.* [9]. The elements have their usual meaning as shown in Fig. 2. An effective $f_{\max}$ was calculated using parasitic element values and the intrinsic element values calculated from the measured S-parameters after de-embedding them from the parasitics. The main utility of the calculated $f_{\max}$ plots was to indicate the approximate bias dependence of gain and the optimum bias point.

An example of the usefulness of the bias scanning technique in conjunction with Cascade Microtech microwave probes [10] is that f_T was quickly measured versus bias for each of the MODFET's on a wafer fabricated with a recently developed 0.1-μm gate-length process [11]. The MODFET's with the highest f_T (113 GHz) and their optimum bias points were easily found.

IV. Calculating Intrinsic Device Elements

The full model of the common source MODFET with parasitics is shown in Fig. 2. The parasitics are modeled as a shell of Y-parasitics (capacitances) and a shell of Z-parasitics (resistances and inductances). This simple model was sufficient for FET's with simple layouts (e.g., 2 fingers). More complex models of the parasitics are needed for multi-finger FET's. The measurements were de-embedded from the parasitics by essentially reversing the procedure that Wolf [8] used to derive the extrinsic Y-parameters of a FET. The method that we used [12] was similar to that described by Dambrine *et al.* [13]. The de-embedding procedure was as follows. The parasitic element values were input to the subprogram and the measured S-parameters were converted to Y-parameters. The Y-parasitics were subtracted. The stripped Y-parameters were converted to Z-parameters. The Z-parasitics were

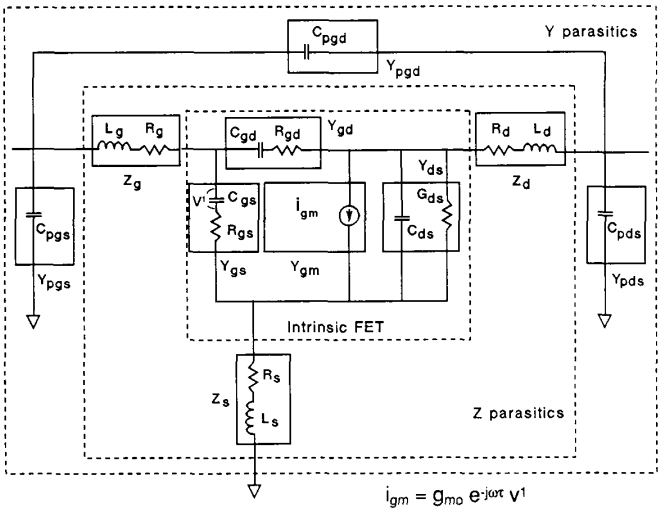

Fig. 2. MODFET circuit model.

subtracted. The stripped Z-parameters were converted to Y-parameters. The complex matrix math function available now made the conversions and stripping steps simple and fast. More Y- and Z-parasitic shells can be stripped if necessary.

The techniques for determining the bias-independent device parasitics are not discussed in detail here. The many alternative techniques for determining the parasitics should yield similar results. The parasitics can be found by fitting the measured S-parameters versus frequency at a single bias point [29]. The resistive elements can be determined from dc [14]–[16] or RF measurements [12], [13], [17] of the FET under extreme bias conditions. The layout inductances can also be determined from RF measurements under extreme bias conditions [12], [13], [17]. Other parasitics (e.g., pad capacitances) can be calculated or measured with special test patterns [12]. Precautions must be taken to understand the limits and errors associated with each technique if parasitics are to be determined accurately. An excellent fit of modeled to measured S-parameters is not sufficient evidence that the parasitics were correctly determined. Our criteria for parasitic determination requires that the device be modeled both over the measurement bandwidth and over a wide range of bias conditions (requiring only physically reasonable changes of intrinsic element values) [12]. The parasitics are verified by ensuring scaling of the intrinsic elements with width.

The small-signal model shown in Fig. 2 was found to accurately simulate the S-parameters of many short-gate-length MODFET's to 40 GHz [12]. Only the intrinsic circuit model elements were assumed to be bias dependent. The element values of the intrinsic model were calculated from the intrinsic Y-parameters with the following equations:

$$Y_{gs} = Y_{11} + Y_{12} \tag{7}$$

$$Y_{gd} = -Y_{12} \tag{8}$$

$$Y_{ds} = Y_{22} + Y_{12} \tag{9}$$

$$Y_{gm} = Y_{21} - Y_{12} \tag{10}$$

$$C_{gs} = \frac{-1}{\text{imag}\,(1/Y_{gs}) \cdot \omega} \tag{11}$$

$$R_{gs} = \text{real}\,(1/Y_{gs}) \tag{12}$$

$$C_{gd} = \frac{-1}{\text{imag}\,(1/Y_{gd}) \cdot \omega} \tag{13}$$

$$R_{gd} = \text{real}\,(1/Y_{gd}) \tag{14}$$

$$C_{ds} = \text{imag}\,(Y_{ds})/\omega \tag{15}$$

$$G_{ds} = \text{real}\,(Y_{ds}) \tag{16}$$

$$g_m = g_{mo} \cdot e^{-j \cdot \omega \cdot \tau} = Y_{gm} \cdot [1 + j \cdot \omega \cdot \tau_{gm}] \tag{17}$$

$$g_{mo} = \text{mag}\,[Y_{gm} \cdot [1 + j \cdot \omega \cdot \tau_{gm}]] \tag{18}$$

$$\tau = \text{phase}\,[Y_{gm} \cdot [1 + j \cdot \omega \cdot \tau_{gm}]] \cdot \frac{1}{\omega}. \tag{19}$$

The derivation of the intrinsic FET model was similar to the original analysis by Drangeid and Sommerhald [18] except the analysis was based on experimental data instead of theoretical data [12].

The intrinsic model has an $R_{gs}(R_i)$ element. FET's and MODFET's have been previously modeled with no R_{gs} because the optimizer of linear simulation programs cannot easily separate the elements of R_{in}: R_{gs}, R_s, and R_g. Here, the parasitics are assumed to be bias independent; R_{gs} is necessary to accommodate the bias dependence of R_{in}.

The magnitude of Y_{gm} is observed to decrease at high frequencies. The τ_{gm} in (17) models this roll off. Measured S-parameters have been accurately simulated [9], [24]–[27] with a model that assumes that the control voltage for g_m is across C_{gs}. This assumption is equivalent to

assuming τ_{gm} is the same as $C_{gs} \cdot R_{gs}$. While this assumption is not exactly correct [4], [18], it was adequate for the MODFET's investigated.

R_{gd} is not usually included in most FET models because it is not easily distinguished in series with the small C_{gd} of a normally operating FET, but it does appear in some FET models [4], [8], [26]. We found that our extraction gave values that were above the noise floor and independent of frequency; therefore, R_{gd} is a valid model element. Furthermore, the gate–source and gate–drain circuit topology of the intrinsic FET with zero drain voltage should be the same [6]. Consequently, R_{gd} is included in the model because the model is intended for all drain voltages.

It has been shown for many MODFET's that after the measured S-parameters are de-embedded from the parasitics and converted to Y-parameters, the intrinsic element values calculated from these intrinsic Y-parameters at each frequency are virtually independent of frequency over the measurement bandwidth [12] at a wide range of bias conditions. Consequently, the Y-parameters of the intrinsic FET at one frequency are sufficient to calculate the element values. The measurements at other frequencies are redundant. The four complex intrinsic Y-parameters can be used to calculate up to eight circuit element values (four resistive and four reactive) of the intrinsic FET, as shown in Fig. 2.

Before a bias scan, the usual procedure was to verify that the parasitics have been correctly removed by confirming that the intrinsic elements are independent of frequency at a typical operating point and under extreme bias conditions (e.g., pinched off and $V_{DS} = 0$). It is then assumed that intrinsic elements are frequency independent at all intermediate biases.

Some caution should be used in interpreting the element values at all bias points because the model is not always applicable. For example, under strongly forward bias conditions, the gate diode conductance in parallel with the gate capacitance becomes significant; the Y_{gs} element values are then not independent of frequency, and a meaningful gate capacitance and series resistance cannot be extracted with the algorithm. The adequacy of a model over a wide bias range is a good test of whether the model is physically correct and if the parasitics are correctly determined.

The intrinsic element values are calculated from the measured S-parameters in less time than it takes the computer to acquire the measured S-parameters. A measurement at 51 bias points and an intrinsic element value plot (or list) can be made in 13 s. Consequently, analysis of the device can be interactive with this technique.

V. Bias Scan Results

Example plots of intrinsic element values and extrinsic figures of merit (f_T and f_{max}) versus bias voltage (bias scans) for MODFET's are shown in this section. All element values are normalized for gate width. The bias scans were made at 25 GHz. The plots show 401 data points (e.g., <7.5 mV steps), not a line through the data points. The plots were usually smooth lines indicating little noise on these well averaged measurements. Some of the interesting features observed with the bias scans are discussed.

A. Gate Bias Scan

The figures of merit, f_T and f_{max}, for a 0.15-μm gate-length pseudomorphic MODFET [1] versus gate voltage V_{gs} are shown in Fig. 3. The drain voltage was 1 V, which is just beyond the knee of the dc FET curves. The Gaussian-shaped f_T behavior measured is typical of that for any MODFET structure at this low drain bias. This behavior relates directly to the physics of operation of MODFET's [3], [5] and these measurements confirm the modulation efficiency analysis [5], which explains the V_{gs} bias dependence of f_T and its relationship to epitaxial layer design. The gate bias dependence of f_T dominates the gate bias dependence of f_{max}.

The measured gate voltage dependence of f_T can be probed further by considering the C_{gs}/Z and g_m/Z variation with V_{gs}, which is shown in Fig. 4. For example, the decrease of f_T with increasing V_{gs} beyond its peak can be attributed to a rapid decrease in g_m/Z, which is consistent with the modulation efficiency analysis [5]. C_{gs}/Z did not increase significantly beyond the peak because this MODFET is atomic planar doped [19], not uniformly doped. This type of data is therefore very important for studying, understanding, and optimizing the epitaxial layer design to improve the high-frequency operation of MODFET's.

B. Drain Bias Scan

A plot of f_T and f_{max} versus drain bias is shown in Fig. 5 for the same 0.15-μm gate-length MODFET [1]. The gate bias was set for maximum f_T using the gate bias scan shown in Fig. 3. The f_T increased rapidly with increasing V_{DS} to 1.0 V; then f_T decreased slowly with increasing V_{DS}. The maximum f_T is just beyond the knee of the dc FET curves. f_{max} reaches a maximum value at V_{DS} higher than that for f_T. f_T and f_{max} are zero at 60-mV drain voltage instead of 0 mV because of the uncorrected supply voltage offset voltage.

The drain bias dependence of f_T can be analyzed by considering the variations of C_{gs}/Z, C_{gd}/Z, and g_m/Z with V_{DS}, as shown in Fig. 6. Below the knee voltage the g_m/Z is a rapidly increasing function reflecting the increase of electron velocity with increasing V_{DS} up to the saturation velocity. The total gate capacitance C_{gs}/Z plus C_{gd}/Z is approximately constant with V_{DS}. With increasing V_{DS} more of the gate capacitance is associated with C_{gs}/Z and less with C_{gd}/Z. Initially ($V_{DS} < 0.4$ V) the capacitances did not change much. This phenomena is associated with self-biasing due to the $R_s \cdot I_{DS}$ voltage. C_{gs}/Z and C_{gd}/Z are equal at zero drain voltage as one would expect after de-embedding from the parasitics.

The decrease of f_T with increasing V_{DS} beyond the knee voltage can be attributed to both the increase of C_{gs}/Z and a small decrease of g_m/Z. One might attribute the de-

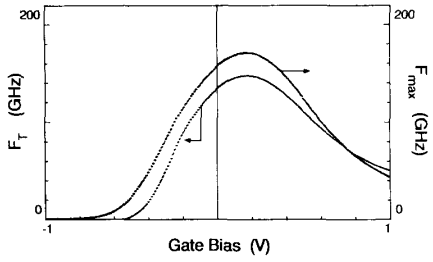

Fig. 3. Plot of f_T and f_{max} versus V_{gs} for a 0.15-μm pseudomorphic MODFET [1].

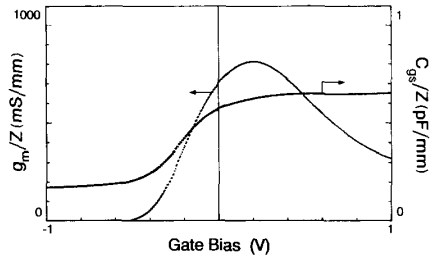

Fig. 4. Plot of g_m/Z, and C_{gs}/Z versus V_{gs} for a 0.15-μm pseudomorphic MODFET [1].

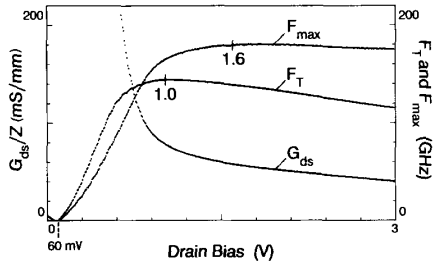

Fig. 5. Plot of f_T, f_{max}, and G_{ds}/Z versus V_{DS} for a 0.15-μm pseudomorphic MODFET [1].

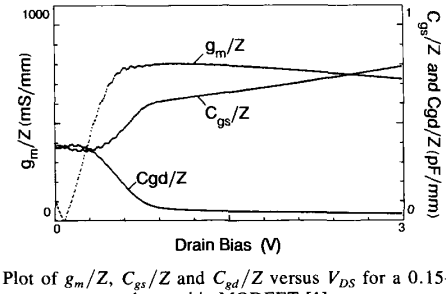

Fig. 6. Plot of g_m/Z, C_{gs}/Z and C_{gd}/Z versus V_{DS} for a 0.15-μm pseudomorphic MODFET [1].

crease of g_m/Z to self-heating causing a decrease of the saturation velocity of carriers. These FET's have a high current density of 240 mA/mm at peak g_m. The increase of C_{gs}/Z might be attributed to extension of the depletion region on the drain side of the gate. This would confirm recent analysis by Moll *et al.* [2] and Nguyen *et al.* [1] who analyzed the variation of f_T with V_{DS} in terms of the

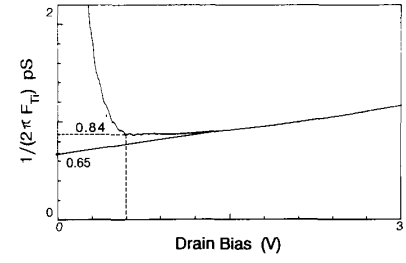

Fig. 7. Plot of intrinsic $1/(f_T \cdot 2 \cdot \pi)$ versus V_{DS} for a 0.15-μm pseudomorphic MODFET [1].

sum of three delays (intrinsic, channel charging (input), and drain delays). The measured bias scan data can be plotted in a delay time format, as shown in Fig. 7, and analyzed directly as discussed in [2]. In this plot the delay is calculated from f_T de-embedded from the parasitics, but the drain voltage is not corrected for the $I_{DS} \cdot (R_s + R_d)$ voltage. This type of bias scan data can be very useful for studying, understanding, and controlling this drain delay behavior.

The drain bias dependence of f_{max} can be understood by considering the variation of f_T and G_{ds}/Z with V_{DS} as shown in Fig. 5. G_{ds}/Z continues to decrease rapidly with increasing V_{DS} where f_T is a maximum. F_{max} thus approaches a maximum only when C_{ds}/Z decreases more slowly with increasing V_{DS}. This might be interpreted as evidence that more drain voltage is required to fully develop "region 2" [20] and bring G_{ds}/Z toward its lowest value than it takes for f_T to reach its maximum and to saturate the electron velocity. As a consequence, f_{max} reaches a maximum at a V_{DS} of 1.6 V. The decrease of f_{max} at higher V_{DS} then results from the decrease of f_T; hence, there is a need to understand and control this behavior.

There can be other interpretations of the data presented here than those suggested. The main point is that the bias scans are an interactive method for analyzing MODFET's, and the scans quickly provide the data necessary to verify models of MODFET's [3]–[5].

Small ripples can be seen on some of the plots versus V_{DS} at about 0.4 V. In this bias region C_{gs}/Z is changing rapidly. These ripples are attributed to source match error from an imperfect or drifted calibration. The ripples are an indication of a measurement accuracy of 1.5 fF.

In addition to the bias dependence of the main elements, C_{ds}/Z, $R_{gs} \cdot Z$, and the g_m delay τ can be plotted. C_{ds}/Z was found to be weakly dependent on bias when G_{ds}/Z was low, which confirms the common assumption that it is principally a parasitic. $R_{gs} \cdot Z$ increases rapidly as the MODFET is pinched off, as one might expect. R_{gd} and R_{ds} are plotted versus V_{DS} in Fig. 8. At zero V_{DS}, R_{gd} has a low value the same as $R_{gs}(R_i)$, as expected from symmetry. As V_{DS} is increased and the FET goes into saturation, R_{gd} increases rapidly and tends to saturate in a manner similar to R_{ds} $(1/G_{ds})$. R_{gd} is more difficult to extract than many of the other model elements in the sat-

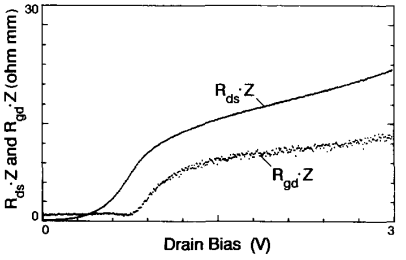

Fig. 8. Plot of R_{gd} and R_{ds} versus V_{DS} for a 0.15-μm pseudomorphic MODFET [1].

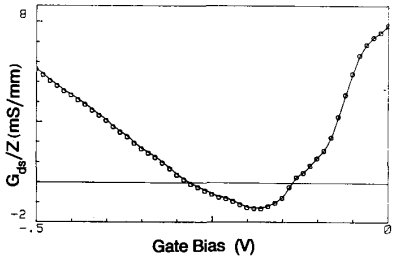

Fig. 9. Plot of G_{ds}/Z versus V_{gs} showing negative output resistance for a 0.25-μm double-doped AlGaAs/GaAs MODFET.

urated region because it is in series with the small capacitor C_{gd}. This difficulty is observed as noisier data.

C. Unusual Bias Regions

The bias sweep also allows one to quickly look at bias regions one might not normally model (e.g., pinched off FET). These sweeps can also reveal unusual behavior. The bias sweep of a double-doped quantum well AlGaAs MODFET at 5 GHz revealed a bias region where G_{ds}/Z was negative, as shown in Fig. 9. S-parameters measured versus frequency at this bias showed that S_{22} was outside the Smith chart at low frequencies. The negative resistance occurred with negligible gate current, and it could be interpreted as evidence of real space transfer from the 2DEG to the AlGaAs supply layer.

Bias scans of G_{ds}/Z versus V_{DS} revealed that the kinks in the dc FET characteristics of InAlAs/InGaAs/InAlAs heterojunction MESFET's were not present at 10 GHz [21]. The kinks were then associated with traps in the buffer layer that could only respond slowly to changes in V_{DS}.

The V_{gs} bias scan of a passive MODFET ($V_{DS} = 0$) also allows the determination of material parameters, and symmetry requirements prove this to be a stringent test of the parasitic model. The sum of C_{gs}/Z and C_{gd}/Z gives the total gate capacitance C_g. The V_{gs} dependence of C_g can be analyzed to give a carrier concentration profile versus depth [22]. The capacitance can be measured at more forward bias conditions than with a normal LCR meter because the measurement frequency is so much higher. The HP8510 ANA is an extremely accurate capacitance meter; therefore, C-V analysis can be applied to small FET's. In addition, since the values of G_{ds}/Z are measured simultaneously with C_g, the channel mobility or differential utility can easily be calculated [23]. This approach can be superior to previous techniques for extracting this information.

VI. Conclusions

The optimum bias point of a MODFET for maximum power and current gain is quickly found using our technique of measuring S-parameters versus bias. Intrinsic small-signal model element values were calculated in real time from the measured S-parameters at a fixed frequency after measurements were de-embedded from the device parasitics. The bias scan technique quickly provided the plots of intrinsic element values versus bias that are essential for understanding the operation of MODFET's, hence facilitating their optimization and design for higher frequency circuit applications.

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