# Theory of Ballistic Nanotransistors

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*Invited Paper*

***Abstract*—Numerical simulations are used to guide the development of a simple analytical theory for ballistic field-effect transistors. When two-dimensional (2-D) electrostatic effects are small (and when the insulator capacitance is much less than the semiconductor (quantum) capacitance), the model reduces to Natori's theory of the ballistic MOSFET. The model also treats 2-D electrostatics and the quantum capacitance limit where the semiconductor quantum capacitance is much less than the insulator capacitance. This new model provides insights into the performance of MOSFETs near the scaling limit and a unified framework for assessing and comparing a variety of novel transistors.**

***Index Terms*—Ballistic MOSFET, device simulation, double-gate MOSFETs, quantum effects, semiconductor device modeling, ultra-thin body.**

## I. Introduction

MOSFET channel lengths continue to shrink rapidly toward the sub-10 nm dimensions called for by the International Technology Roadmap for Semiconductors [1], [2]. Coupled with the use of high-mobility channel materials [3]–[9], nanoscale channel lengths open up the possibility of near-ballistic MOSFET operation. As MOSFET scaling continues, molecular transistors that could replace them are also being explored. Carbon nanotube transistors, for example, are especially interesting because their one-dimensional bandstructure suppresses backscattering and makes near-ballistic operation a possibility [10], [11]. Per unit width on-currents significantly higher than those of MOSFETs have already been reported [10 ], [12]. For these reasons, it is important to understand ballistic operation—both in conventional MOSFETs and in unconventional transistors. Our objectives in this paper are to present a simple analytical theory for ballistic transistors and to explore its application to MOSFETS and to unconventional field-effect transistors.

The operation of MOSFETs in the ballistic regime has recently been explored by simple, analytical models [13]–[16] as well as by detailed numerical simulations [17]–[22]. In Section II, we review our understanding of the device physics of ballistic MOSFETs as developed in previous publications [23]–[25]. In Section III, we present a simple, analytical model, and in Section IV, we show that it agrees with two-dimensional (2-D) numerical simulations of ballistic MOSFETs. In Section V, we apply the new model to ideal carbon nanotube FETs and discuss the interesting effects that occur in the quantum capacitance limit [26]. Finally, in Section VI, we discuss why the model developed here does not describe devices like Schottky barrier FETs before concluding in Section VII.

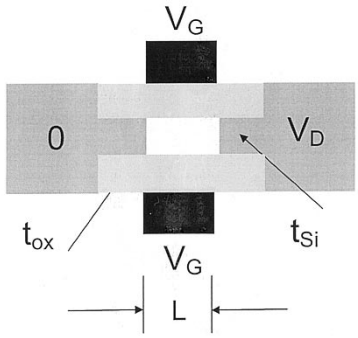


Fig. 1. Structure of the model device: a double-gate MOSFET. A body thickness of 1.5 nm and an oxide thickness of 1.5 nm were assumed. Both the source and drain regions were doped at $10^{20}/\text{cm}^3$. The gate workfunction was set to 4.25 eV, which produced an off-current of 1.6 nA/ $\mu$m.

## II. Device Physics of Ballistic MOSFETs

Numerical simulations provide detailed information on the operation of nanoscale devices. Two transport models have proven to be especially useful in our work. The first is a numerical solution of the ballistic Boltzmann equation [19], [25], and the second is the nonequilibrium Greens function (NEGF) formalism for quantum transport [27], [28]. Fig. 1 shows a model 10-nm MOSFET, and Fig. 2 shows the computed ballistic distribution function within the device under on-state conditions [25]. The results show that two distinct carrier populations exist: one due to source injection and another due to drain injection (scattering would mix these two populations). Deep within the channel, the drain-injected population retains a near-equilibrium shape, but the source-injected population is strongly distorted. Fig. 3 is an NEGF simulation of the energy-resolved electron density under on-state conditions. Although quantum interference effects are seen as well as tunneling of carriers beneath the source-channel barrier, NEGF simulations of the terminal $I$–$V$ characteristics of well-designed MOSFETs agree rather well with semi-classical

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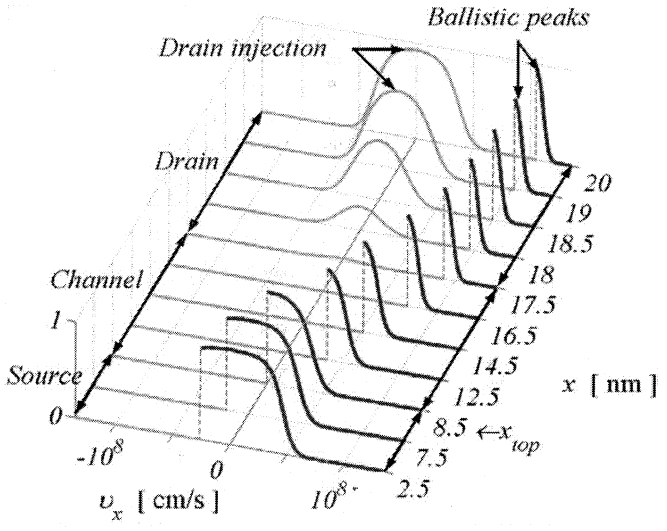
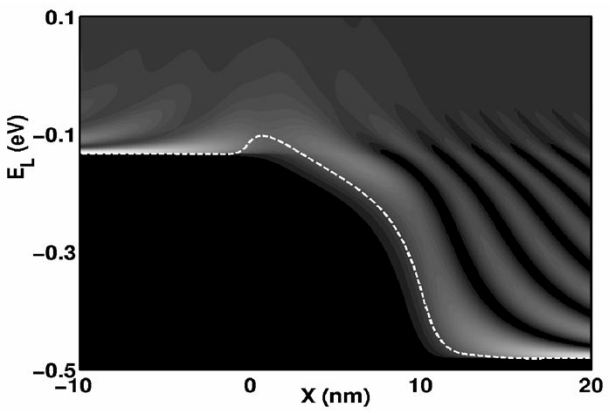
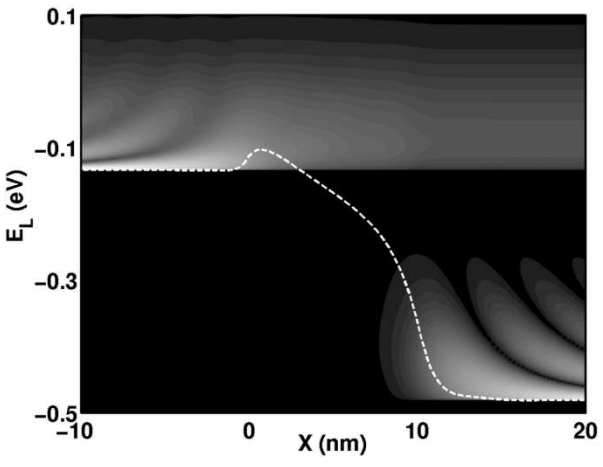



Fig. 2. Ballistic distribution function within the model device under on-state conditions as computed by solving the ballistic BTE. (From [25].)



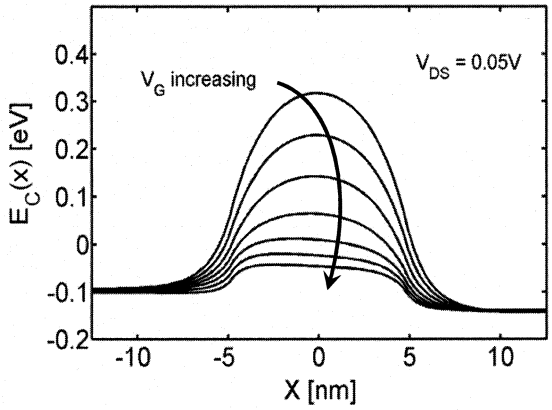

(a)



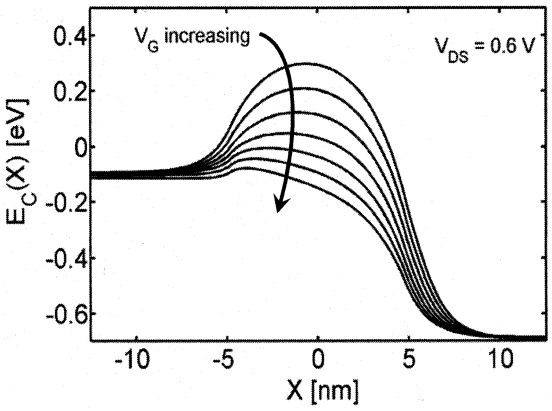

(b)

Fig. 3. Energy-resolved (a) density-of-states versus position and (b) electron density versus positions with the model device as computed using the ballistic NEGF formalism.

simulations—even at the 10-nm scale (when the strong effects of quantum confinement are included in both simulations) [18], [19]. Both the quantum and classical simulations show rich, complex phenomena within the device, but it turns out that a simple description of the current versus voltage characteristics is possible [24].




(a)

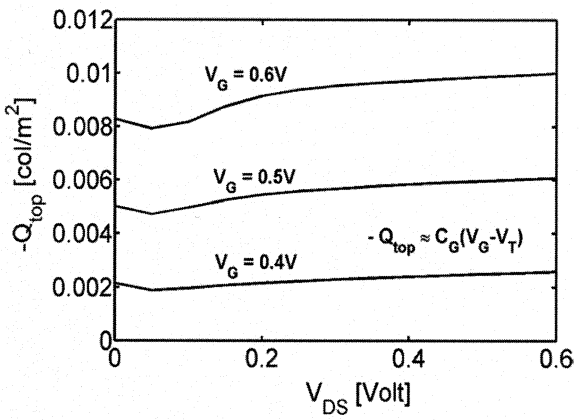



(b)

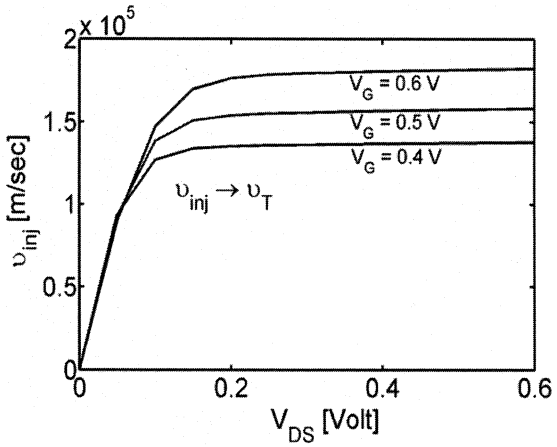
Fig. 4. Computed energy band diagrams under (a) low drain bias and (b) high drain bias. The parameter is the gate voltage.

Fig. 4 shows the computed self-consistent potentials within the model nanoscale MOSFET under low and high drain bias with gate voltage as a parameter. (What is plotted is actually the bottom of the first subband versus position.) At low gate voltages, the energy barrier between the source and drain is high, and the device is off. A high drain bias lowers the energy in the drain, and when a high gate voltage lowers the potential energy barrier, electrons flow from source to drain. This picture of the MOSFET is essentially that of the bipolar transistor [29]; transistor action occurs by modulating the height of an energy barrier. It is more common to think of MOSFETs in terms of the gate modulating the charge in the channel, but the charge in the channel is controlled by the height of the barrier. MOSFETs and bipolar transistors operate by similar principles (both below and above threshold); in the bipolar transistor, the height of the energy barrier is controlled directly by the base-emitter voltage, whereas in the MOSFET, it is controlled indirectly by the voltage on the gate [29]. As will be discussed in Section VI, not all transistors operate by this charge (or barrier height) modulation principle.

Current is the product of charge and velocity, which we plot separately in Fig. 5. In this figure, the gate voltage is high, and




(a)




(b)

Fig. 5. Computed behavior at the top of the source to channel barrier. (a) Electron charge $Q_n(0)$ at the top of the barrier versus $V_{DS}$. (b) Average electron velocity at the top of the barrier versus $V_{DS}$.

we plot the two quantities as a function of $V_{DS}$. Fig. 5(a) shows that the charge at the top of the barrier is nearly independent of $V_{DS}$ for a well-designed MOSFET, and for operation above threshold, it is given by MOS electrostatics as

$$Q_n(0) \approx C_{\rm ox}\,(V_{GS} - V_T)\,. \tag{1}$$

We will show in a later section that the initial dip in $Q_n(0)$ and the subsequent rise can also be explained. Fig. 5(b) shows that the average electron velocity at the top of the barrier increases with $V_{DS}$ and then saturates. The saturated velocity at the top of the barrier is simply the velocity of the thermal equilibrium hemi-Fermi–Dirac distribution shown in Fig. 2. (Note that above threshold, the electron gas is degenerate, and the magnitude of this injection velocity depends on the gate voltage [13], [15].) It is interesting to note that velocity saturation occurs in a ballistic MOSFET, but it occurs at the top of the barrier where the field is zero rather than at the drain end where the field is high [24]

Because the top of the barrier has special significance, it is the starting point for our analytical model. For a ballistic transistor, the states at the top of the barrier are filled from either the source or the drain. For a quantum transport model, the local density of states fillable by the source and drain can be evaluated directly from the spectral function [27], [28]. In a semiclassical model,

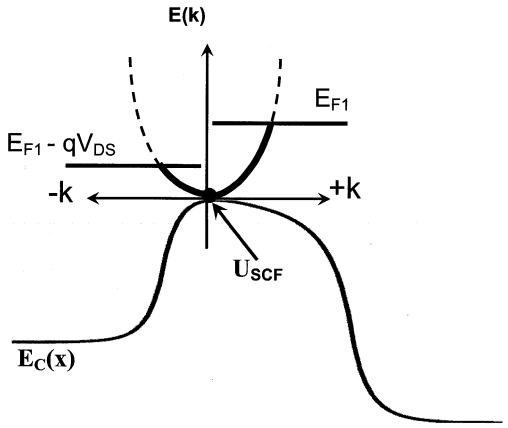



Fig. 6. Illustration of how the k-states at the top of the barrier are filled by the two Fermi levels.

the local density of states is determined by the $E(k)$ relation for the semiconductor shifted by the self-consistent potential at the top of the barrier. Fig. 6 shows how the states at the top of the barrier are filled for a simple bandstructure. The positive velocity states are populated according to the Fermi level of the source and the negative velocity states by the Fermi level of the drain. Our key task in developing an analytical model will be to devise a simple approach to determine the self-consistent potential at the top of the barrier.

Finally, we mention one subtle point. A careful examination of Fig. 4(b) indicates that the conduction band in the source region actually floats down by about 10 mV as the gate voltage increases. This unfamiliar behavior is a consequence of transport at the ballistic limit. The source Fermi level is fixed at 0 eV and represents the Fermi level of the equilibrium source reservoir/contact. Under low gate bias, most of the positive velocity electrons injected from the contact reflect from the energy barrier so that both positive and negative velocity states in the source extension are filled. When the gate voltage is high, however, the barrier decreases, and fewer of the injected electrons reflect from the barrier so that it is mainly positive-velocity states in the source that are occupied. To achieve space-charge neutrality in the highly doped source extension, the conduction band must float down so that more electrons are injected from the source contact. When strong scattering is present inside the source extension, electrons occupy both positive and negative velocity states, and this effect is absent. For a more complete discussion of boundary conditions for ballistic MOSFETs, see [30].

In the following section, we introduce a simple, analytical model, and in Section IV, we show that it accurately describes the physics of ballistic nanoscale MOSFETs.

## III. Model

A simple 2-D model for the ballistic MOSFET is shown in Fig. 7. It consists of three capacitors, which represent the effect of the three terminals on the potential at the top of the barrier. As also indicated by the shaded region in Fig. 7, mobile charge can be placed at the top of the barrier. The mobile charge is determined by the local density of states at the top of the barrier, the location of the source and drain Fermi levels $E_{F1}$ and $E_{F2}$, and by the self-consistent potential at the top of the barrier $U_{\rm scf}$.

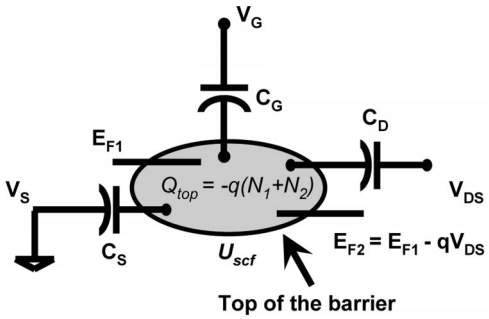



Fig. 7. Two-dimensional circuit model for ballistic transistors. The potential at the top of the barrier, $U_{\rm scf}$, is controlled by the gate, drain, and source potentials through the three capacitors shown. The mobile charge at the top of the barrier is determined by $U_{\rm scf}$ and by the location of the two Fermi levels. The nonlinear semiconductor (or quantum) capacitance is not shown explicitly but is implicit in the treatment of band filling.

Because there is a relation between the local potential and the charge, this effect can be described by a nonlinear quantum capacitance [26]. In equilibrium

$$C_Q \equiv \frac{d(qN)}{d(-U_{\rm scf}/q)} = q^2 \int_{-\infty}^{+\infty} D(E) \left(-\frac{\partial f(E-E_F)}{\partial E}\right) dE \qquad (2)$$

which, since $(-\partial f/\partial E)$ is sharply peaked about the Fermi energy, is $q^2$ times the density of states near the Fermi energy. Solomon *et al.* have pointed out [31] that Natoris analytical ballistic model [13] does not include this nongeometric, quantum (or degeneracy) capacitance. Neglecting the quantum capacitance is justified for thick gate insulators (i.e., when $C_G \ll C_Q$); however, it fails to describe gate electrostatics when the insulator capacitance is large compared with the quantum capacitance (i.e., when $(C_G \geq CQ)$, which occurs when the electrical thickness is small or when the quantum capacitance is small, as in a one-dimensional (1-D) conductor. Our model does not treat the quantum capacitance explicitly; however, it is included naturally through the treatment of self-consistent gate electrostatics.

When the terminal biases are zero, the equilibrium electron density at the top of the barrier is

$$N_0 = \int_{-\infty}^{+\infty} D(E) f(E-E_F)\, dE \qquad (3)$$

where $D(E)$ is the local density of states at the top of the barrier, and $f(E-E_F)$ is the equilibrium Fermi function. The function $D(E)$ is nonzero for positive values of its argument only, which represents the minimum of the density of states and is specified as $E=0$ in equilibrium. When a bias is applied to the gate and drain terminals (the source terminal is always grounded in this work), two things happen: i) The self-consistent potential at the top of the barrier becomes $U_{\rm scf}$, and ii) the states at the top of the barrier are now populated by two different Fermi levels. The positive velocity states are filled by the source, according to

$$N_1 = \tfrac{1}{2} \int_{-\infty}^{+\infty} D(E-U_{\rm scf}) f(E-E_{F1})\, dE \qquad (4a)$$

and the negative velocity states are filled by the drain according to

$$N_2 = \tfrac{1}{2} \int_{-\infty}^{+\infty} D(E-U_{\rm scf}) f(E-E_{F2})\, dE \qquad (4b)$$

where $E_{F1} = E_F$, and $E_{F2} = E_F - qV_{DS}$. A change of variables can be used to re-express these equations as

$$N_1 = \tfrac{1}{2} \int_{-\infty}^{+\infty} D(E) f_1(E)\, dE \qquad (5a)$$

$$N_2 = \tfrac{1}{2} \int_{-\infty}^{+\infty} D(E) f_2(E)\, dE \qquad (5b)$$

where

$$f_1(E) \equiv f(E+U_{\rm scf}-E_{F1}) \qquad (6a)$$

and

$$f_2(E) \equiv f(E+U_{\rm scf}-E_{F2}). \qquad (6b)$$

Given an arbitrary density of states $D(E)$ and the location of the source and drain Fermi levels, we can evaluate the electron density at the top of the barrier $N = N_1 + N_2$ *if* the self-consistent potential $U_{\rm scf}$ is known.

Finding the self-consistent potential involves solving the two-dimensional Poisson equation as represented by the three capacitors in Fig. 7 with the bias induced charge $\Delta N = (N_1+N_2) - N_0$ at their common terminal. We obtain the solution by superposition. First, ignoring the presence of the mobile charge in the channel, we calculate the Laplace potential at the top of the barrier due to terminal biases, which is

$$U_L = -q(\alpha_G V_G + \alpha_D V_D + \alpha_S V_S). \qquad (7a)$$

In this equation, the three $\alpha$s describe how the gate, drain, and source control the Laplace solution and are given by

$$\alpha_G = \frac{C_G}{C_\Sigma} \quad \alpha_D = \frac{C_D}{C_\Sigma} \quad \alpha_S = \frac{C_S}{C_\Sigma} \qquad (7b)$$

where $C_\Sigma$ is the parallel combination of the three capacitors in Fig. 7.

For a so-called, well-tempered MOSFET, the gate controls the potential, and $\alpha_G \approx 1$ and $\alpha_S$, $\alpha_D \approx 0$. The second part of the solution consists of grounding the three terminals and computing the potential due to the mobile charge, at the top of the barrier $\Delta N$, from

$$U_P = \frac{q^2}{C_\Sigma} \Delta N. \qquad (7c)$$

Physically, a positive bias applied to the drain and gate terminals pushes down the potential energy at the top of the barrier as described by $U_L$, but because of the charge, the potential floats up, as described by $U_P$. The complete solution is obtain by adding the two contributions to obtain

$$U_{\rm scf} = U_L + U_P = -q(\alpha_G V_G + \alpha_D V_D + \alpha_S V_S) + U_C \Delta N \qquad (8a)$$

where

$$U_C = \frac{q^2}{C_\Sigma} \qquad (8b)$$

is the charging energy.

Equations (5) and (8a) represent two, coupled nonlinear equations for the two unknowns $N$ and $U_{\rm scf}$. These equations can be solved iteratively to find the carrier density and self-consistent potential at the top of the barrier. Finally, the drain current is evaluated from

$$I_D = \int_{-\infty}^{+\infty} J(E)\,[f_1(E) - f_2(E)]\,dE \tag{9}$$

where $J(E)$ is the "current-density-of-states" defined in the Appendix.

In summary, the procedure for computing $I_D(V_G, V_{DS})$ consists of the following steps.

i) Specify the semiconductor carrier and current-densities-of-states $D(E)$ and $J(E)$ either analytically or by a numerical table.
ii) Specify $V_G$, $V_D$, $V_S$, and $E_F$.
iii) Iteratively solve (5) and (8a) for $U_{\rm scf}$ and $N$.
iv) Evaluate the current from (9) for the assumed $V_G$ and $V_{DS}$.

We have defined the model in terms of two densities-of-states—one for the carrier density $D(E)$ and one for the current density $J(E)$—which can be determined directly from the semiconductor bandstructure. In general, the integrals in (5) and (9) must be done numerically, but for simple bandstructures, they can be done analytically. In the Appendix, we evaluate these expression for 2-D carriers in a simple band and discuss how to use more general bandstructures.

## IV. Application to Ballistic MOSFETs

To illustrate the use of the model, we apply it to the double gate MOSFET presented in Fig. 1 and compare the results to 2-D numerical simulations with nanoMOS 2.0 [22]. Although the expressions for the $\alpha$s given in (7b) are exact, they are difficult to evaluate in practice because they depend on the 2-D structure of the device. We will, therefore, treat them as fitting parameters and present a step-by-step procedure for determining the three parameters $E_F$, $\alpha_G$, and $\alpha_D$. The results show that this simple, three-parameter model does a good job of fitting the simulated $I$–$V$ characteristics over the full range of operation.

### A. Parameters for the Analytical Model

The first step is to set the Fermi level $E_F = E_{F1}$ for the correct threshold voltage, which is equivalent to setting the correct gate work function. Alternatively, setting the Fermi level is equivalent to setting the correct equilibrium carrier density at the top of the barrier as given by (3). For a well-designed MOSFET at low gate and drain bias, $\alpha_D$, $U_L$, and $\Delta N$ are all small so $U_{\rm scf} \approx 0$, and (3) for $N_0$ depends on a single parameter $E_F$. In practice, we adjust the Fermi level in the analytical model so that the current matches that of the simulator for $V_G = 0$ and $V_{DS} = 50$ mV.

Next, after setting $E_{F1}$, we adjust the gate control parameter $\alpha_G$ until the analytical model gives the same low $V_{DS}$ subthreshold swing as does the simulation. We do this for $V_G \ll V_T$ and for $V_{DS} = 50$ mV. The induced charge at the top of the barrier $\Delta N$ is very small so that the gate controls the position of the top of the barrier $U_{\rm scf}$ through $U_L$. For complete gate control ($\alpha_G = 1$), the subthreshold swing is ideal, i.e., $S = 60$ mV/dec at room temperature. For our model device, we obtained $\alpha_G = 0.87$.

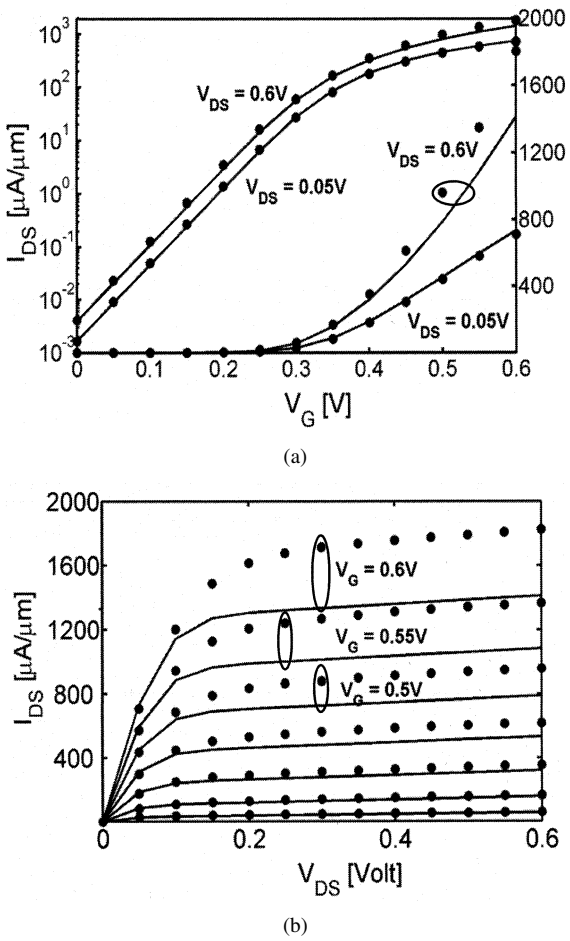



Fig. 8. Comparison of the analytical model to numerical simulations for the ballistic MOSFET of Fig. 1. (a) Transfer characteristics under both low and high drain bias. (b) Output characteristics. In both cases, the solid lines are from the analytical modes and the points are from nanoMOS simulations.

Finally, having specified $E_{F1}$ and $\alpha_G$, the drain control parameter $\alpha_D$ was obtained by horizontal shift of the $\log(I_D)$ versus $V_G$ characteristics in the subthreshold regime [i.e., by matching the drain-induced barrier lowering (DIBL) of the simple model to the detailed numerical model]. This parameter describes the additional change of the potential at the top of the barrier due to the drain bias. For our model device, we found $\alpha_D = 0.033$.

Fig. 8(a) and (b) compare the $I$–$V$ characteristics from the analytical to those obtained by numerical simulation. From the $\log(I_{DS})$ versus $V_G$ plot of Fig. 8(a), we see that the subthreshold characteristics match very well both for low and high $V_{DS}$. From the linear plot in the same figure, we also see that at low $V_{DS}$ and high $V_G$, the characteristics match very well. However, when both $V_{DS}$ and $V_G$ are high, the match is poor, and the analytical model underestimates $I_{DS}$. This mismatch is also clear in the output characteristics presented in Fig. 8(b), where we can see that for $V_G$ above threshold, the

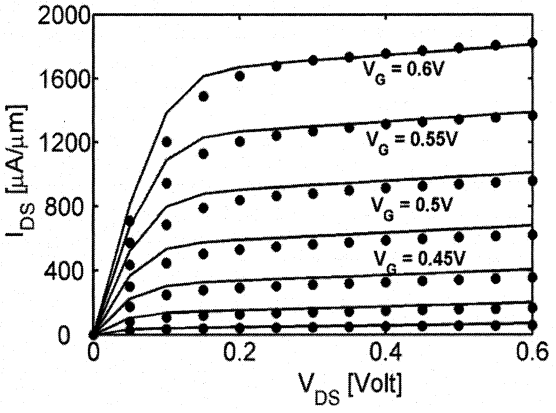



Fig. 9. Comparison of the analytical model to numerical simulations for the ballistic MOSFET of Fig. 1. In this case, the floating source potential was treated. In addition to good agreement at low gate and drain biases and as low gate and high drain biases, this plot shows that the agreement at high gate and drain biases is also good.

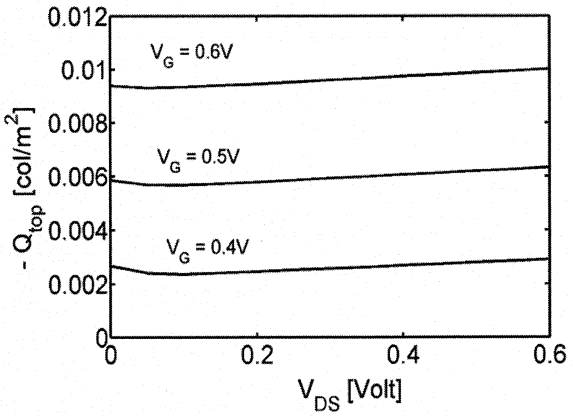
drain current from the analytical model saturates at a lower value than numerical simulation. The reason for this mismatch under high $V_G$ and $V_{DS}$ and a way to treat it are discussed next.

### *B. Treatment of the Floating Source Potential*

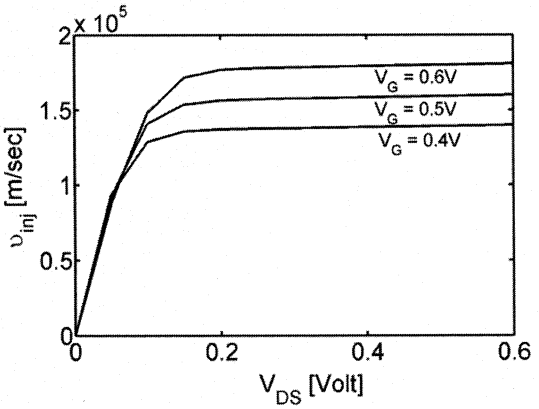
The discrepancy between the analytical and numerical models under high gate and drain biases is related to the floating source potential, which was discussed briefly in Section II. This phenomenon, which is important only in ballistic devices, is correctly implemented in the numerical simulator but has yet to be considered in our analytical model.

As discussed in Section II (and, at greater length, in [30]), for ballistic transport, a floating source potential is necessary to maintain charge neutrality in the highly doped source and the drain region under high bias conditions. As the gate voltage increases, fewer electrons are reflected from the barrier; the source potential must drop, so that enough additional electrons are injected to restore space-charge neutrality in the source. When the source potential decreases, so does $U_{\rm scf}$ at the top of the barrier. The result is that this floating source effect increases the carrier density at the top of the barrier, which explains the discrepancy observed in Fig. 8 under high gate and drain biases.

With regard to the simulation procedure, the floating source potential means that the source Fermi level $(E_{F1} - E_C)$ cannot be fixed at the beginning to produce a given $V_T$ since it is both gate and drain bias dependent. As discussed in the Appendix, one can readily extend the iterative procedure so that the Fermi level is iteratively adjusted to maintain space charge neutrality in the source under all bias conditions. Fig. 9 compares the $I_D$–$V_{DS}$ plots from the ballistic numerical simulation to the analytical model with the floating source treated, as discussed in the Appendix. Fig. 9 shows that when the floating source effect is included, the analytical model reproduces the full, numerical simulation quite well. The agreement is very good under high $V_G$ and $V_{DS}$ (where ignoring the floating source potential produced serious errors) but not quite as good under high $V_G$ and low $V_{DS}$, where the model without floating source correction worked better.




(a)




(b)

Fig. 10. Behavior at the top of the source to channel barrier as obtained from the analytical model. (a) Electron charge $Q_n(0)$ at the top of the barrier versus $V_{DS}$. (b) Average electron velocity at the top of the barrier versus $V_{DS}$

### *C. Charge and Velocity at the Top of the Barrier*

Finally, we examine the charge density

$$Q(0) = -q\ [N_1(V_G, V_{DS}) + N_2(V_G, V_{DS})] \tag{10a}$$

and the carrier velocity

$$\langle v(0)\rangle \equiv \frac{I_D(V_G, V_{DS})}{Q(V_G, V_{DS})} \tag{10b}$$

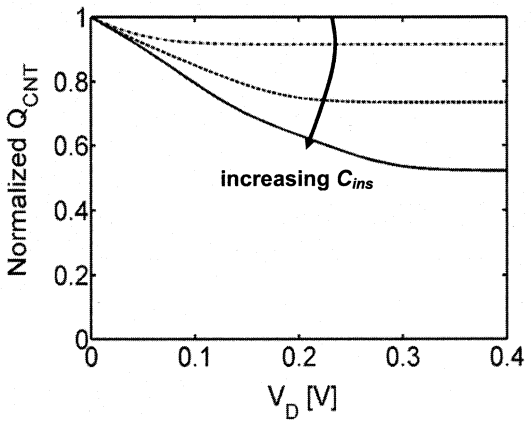
at the top of the barrier. Recall that the nanoMOS simulation of Fig. 5 shows that these quantities had a simple behavior at the top of the barrier. In Fig. 10(a) and (b), we plot these two quantities from the analytical model. Fig. 10(a) shows, in agreement with Fig. 5(a), that the charge at the top of the barrier is nearly independent of the drain bias. The initial dip and subsequent rise are also seen, although not as pronounced as in the full, numerical model. (The simpler model, which ignores the floating sources, actually does better in this regime.) The initial rise and subsequent saturation of the velocity at the top of the barrier is well-described by the simple model. These results show that Natoris assumption (and our own in subsequent publications), where $Q_n(0)$ is independent of drain bias, is a good one for typical MOSFETs. In Section V, however, we will discuss a case

for which the assumption of a constant charge at the top of the barrier is not valid.

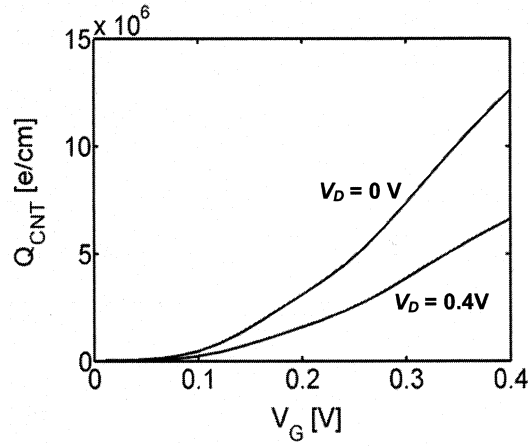
In practice, the model developed in this paper may be useful to compare the measured characteristics of nanoscale MOSFETs to their ballistic limits. From the measured electrical characteristic, the technique presented in this section can be used to extract the parameters needed for the model. Another use for the model might be to compare the upper limit performance of devices that use novel channel materials to that of the conventional silicon MOSFET. (The model has been formulated to allow the use of numerically tabulated bandstructures.) Finally, we note that the ballistic model is not entirely academic. Comparisons with experiments suggest that present-day MOSFETs operate at roughly 50% of the ballistic limit [16], [32], and much of the research on new channel materials is motivated by a desire to approach the ballistic limit.

## V. Molecular Transistors

The model presented in Section III was expressed in terms of a general density-of-states so that it could describe transistors made from different semiconducting materials, even single molecule transistors. Carbon nanotube field-effect transistors (CNTFETs) are a type of molecular transistor that has already demonstrated high on-currents [10]–[12]. Carbon nanotubes can be thought of as a sheet of graphene rolled up into a tube; depending on how the tube is rolled up, the nanotube may be either semiconducting or metallic. For semiconducting nanotubes, $E_G \approx 0.7$ eV/$d$, where $d$ is the diameter of the nanotube in nanometers [33]. For typical nanotube diameters (1–3 nm), the bandgaps are suitable for electronic devices, and the 1-D bandstructure allows ballistic transport over long distances [10]. CNTFET technology is at an early stage of development; it is still not clear how CNTFETs operate or even if they all operate in the same way. One possibility is that the gate modulates the conductance of the channel as in a MOSFET, which is supported by the observations that some long channel CNTFETs obey the MOSFET square law theory (with inferred mobilities of several thousand) and that ambipolar behavior is not observed in these devices [12]. Another possibility is that the gate modulates the transmission through a Schottky barrier between the source metal and the nanotube channel, which is supported by the observation of ambipolar operation of some CNTFETs and the transition from the p-type to the n-type operation after gas absorption [34]. Whether a CNTFET operates like a MOSFET or like a SBFET may depend on details of the processing and device structure that are still not fully understood at this time. The maximum performance of a ballistic carbon nanotube FET should, however, occur for MOSFET-like operation. Achieving MOSFET-like operation will require learning how to heavily dope nanotubes (both n- and p-type) or achieving small or even negative Schottky barriers [35], [36]. Such devices would behave much like ballistic MOSFETs with some differences due to the 1-D density of states. CNTFETs, however, also offer the possibility of operation at the quantum capacitance limit where some interesting effects that do not occur in MOSFETs arise.




(a)




(b)

Fig. 11. (a) Normalized electron density at the beginning of the channel versus the drain voltage at $V_G = 0.4$ V for three N-type, 3-nm-diameter CNTFETs with $C_{ins} = 0.4$ pF/cm (dash-dot line), 5 pF/cm (dashed line), and 90 pF/cm (solid line). (b) Charge versus the gate voltage curves for $C_{ins} = 90$ pF/cm. The power supply voltage specified by ITRS for the 2016 technology node [1] (0.4 V) is assumed in the subsequent calculations.

The quantum capacitance limit occurs when the gate insulator capacitance is much larger than the semiconductor (or quantum) capacitance. For MOSFETs, it is unlikely that operation in the quantum capacitance limit will be achieved, but for CNTFETs, the situation is different. Operation in an aqueous environment and the absence of dangling bonds, which facilitates the use of high-$\kappa$ gate dielectrics [12], provide the possibility to achieve large gate insulator capacitance, and the relatively low density of states in 1-D conductors reduces the quantum capacitance [recall (2)]. Consider, for example, an electrolytically gated CNTFET with the effective oxide thickness $t_{ins} \approx 1$ nm and dielectric constant $\kappa = 80$ [10]. The quantum capacitance of the nanotube can be estimated as 4 pF/cm, whereas that of the insulator is about 90 pF/cm; therefore, the total gate capacitance is approximately $C_Q$. Even for a recently reported 8-nm-thick $ZrO_2$-gated CNTFET [12], the insulator capacitance is about 5 pF/cm, which is larger than the quantum capacitance.

MOSFET-like CNTFETs can be treated with the analytical model described in Section III if the appropriate $E(k)$ is used [37]. Fig. 11(a) plots the charge density at the top of the barrier versus the drain voltage for three different gate capacitance

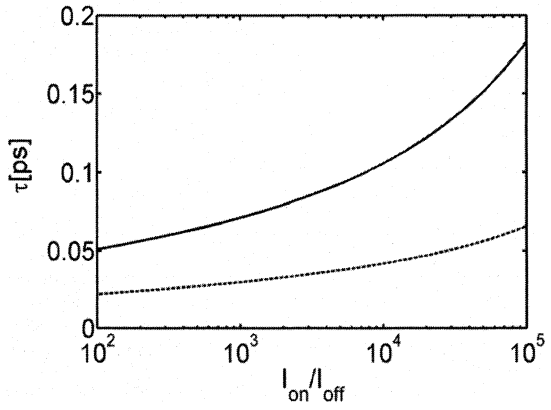



Fig. 12. Intrinsic device delay metric versus the on-off current ratio for a model ballistic MOSFET and for a MOSFET-like CNTFET. The solid line is for a double gate Si MOSFET with channel length $L_G = 10$ nm, gate oxide thickness $t_{ins} = 1$ nm, and dielectric constant $\kappa = 4$, and the dashed line is for a coaxially gated CNTFET with $L_G = 10$ nm, $t_{ins} = 2$ nm, and $\kappa = 25$. The power supply voltage $V_{DD} = 0.4$ V. By adjusting the gate work function, the $\tau$ versus $I_{\rm on}/I_{\rm off}$ characteristics was obtained.

values. When $C_{ins} \ll C_Q$, the charge at the beginning of the channel is nearly independent of the drain voltage, and the transistor operates at the charge control limit typical for MOSFETs. On the other hand, when $C_{ins} \gg C_Q$, the charge at the beginning of the channel decreases by a factor of two as $V_D$ increases. In the quantum capacitance limit, instead of holding the charge constant, the gate holds the nanotube potential constant at the gate potential. In this sense, the device operates more like a bipolar transistor [29]. Because the nanotube potential is pinned by the gate voltage, increasing the drain bias suppresses the $-$k by half of the distribution function and reduces the charge density by a factor of 2. At high $V_D$, therefore, the gate capacitance is only one half of its equilibrium value, as shown in Fig. 11(b). Operation in the quantum capacitance limit has some interesting implications: The on-off ratio increases, and the channel conductance and transconductance approach the same value [38].

To explore the possible role of CNTFETs in future electronic systems, it is important to compare the upper limit performance of a ballistic CNTFET to that of a ballistic silicon MOSFET. We consider MOSFET-like CNTFETs because they should have a higher performance limit that a Schottky barrier FET. Direct comparison of the on-current is clouded by the need to convert the CNTFET on-current to per unit width basis; it is preferable to compare quantities that are dimensionless or that have the same dimensions. A useful set of performance metrics, which are independent of the channel dimensions, are 1) the device delay metric $\tau = C_G V_{DD}/I_D$ (on) and 2) the on-off current ratio $I_{ON}/I_{OFF}$. For these comparisons, we consider two devices: 1) a 10-nm channel length ballistic, double-gate MOSFET with $t_{ins} = 1$ nm and $\kappa = 4$; and 2) a 10-nm channel length, ballistic coaxial-gate CNTFET with $t_{ins} = 2$ nm and $\kappa = 25$. A high-$\kappa$ dielectric is used for the CNTFETs because it has already been achieved [12].

Fig. 12 compares the on-off current ratio and the delay metric of MOS and CNT technologies. The power supply voltage was fixed at 0.4 V, the workfunction was varied, and the resulting $\tau$ and $I_{\rm ON}/I_{\rm OFF}$ plotted. The delay metric was evaluated using the simple, analytical model with $C_D = 0$ and a constant gate capacitance $C_G$, which was extracted from the charge versus the gate voltage relation above the threshold. On the $\tau$ versus $I_{\rm ON}/I_{\rm OFF}$ plane, operation in the lower right hand corner is preferred, and the CNTFET shows a clear advantage. For a device delay of 0.05 ps, the CNTFET has an on-off ratio that is more than 100 times that of the MOSFET. For an on-off ratio of 1000, the CNTFET operates at twice the speed of the MOSFET. The advantage arises from three factors. First, the nanotube bandstructure delivers higher carrier velocities, which translates directly to lower switching delays. Second, the use of high-$\kappa$ gate dielectrics leads to higher induced charge in the channel, which increases the carrier velocity by pushing the Fermi level high into the band where it is steep. Finally, the low quantum capacitance coupled with the use of high-$\kappa$ gate dielectrics facilitates the direct modulation of the barrier height by the gate voltage, without volt drops across the gate insulator. Although these are upper limit estimates for each device, they show a considerable performance promise for the CNTFET—one that merits serious study.

## VI. Discussion

The simple model we have developed does a rather good but not perfect job of reproducing more detailed numerical simulations. The discrepancy under high gate and drain bias was resolved by forcing the potential at the top of the barrier $U_{\rm scf}$ to follow the floating source potential, but the high-gate, low-drain bias region is better described when $U_{\rm scf}$ is not allowed to follow the floating source potential. The reason for this behavior can be understood from Fig. 4. Under high gate and drain bias, the potential energy maximum is pushed up against the source; therefore, it seems reasonable that $U_{\rm scf}$ follows the floating potential in the source. Under low drain bias, it is not pushed as close to the source, and therefore, $U_{\rm scf}$ is not as tightly coupled to the source potential. Whether this physics can be captured in an analytically simple way is still under investigation.

The model that we have developed describes MOSFET-like transistors in which the gate modulates the channel conductance and the contacts are nearly ideal. Other types of transistors are, however, possible. One possibility is that the source-drain current is limited by a metal/semiconductor junction at the source end of the channel whose tunneling resistance is modulated by the gate. The Schottky barrier MOSFET (SBFET), which replaces the heavily doped silicon source drain with a silicide, is one such example [39], [40]. The question of whether our model applies to SBFET-like transistors is the subject of this section.

Ballistic SBFETs can be simulated by NEGF techniques similar to those used for MOSFETS [35]. We simulate a 10-nm channel length, double-gate, ultra-thin body SBFET with a similar device geometry to the MOSFET shown in Fig. 1. Fig. 13 shows the $I_D$ versus $V_D$ characteristic compared with the result of the simple, analytical model described in Section III. Its clear that the simple model overestimates the on-current of this device. Fig. 14, which plots the first conduction subband minimum versus position at different gate voltages, explains why the simple model fails for the SBFET. At low gate bias, a large barrier limits the drain current. Gate modulation is achieved by reducing the barrier height, which is a mechanism similar to that

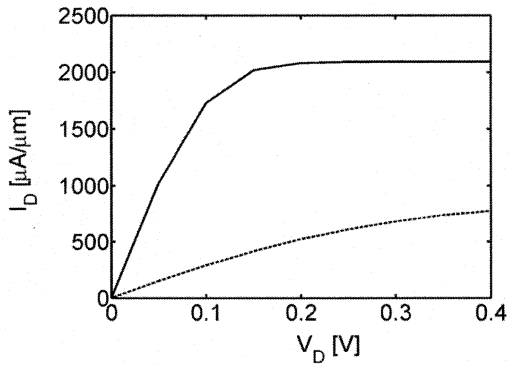



Fig. 13. $I_D$ versus $V_D$ characteristics of a ballistic SBFET as simulated by the NEFG approach (dashed line) and the corresponding ballistic MOSFET characteristics as obtained by the analytical model (the solid line). The double-gate SBFET has a gate and channel length $L_G = L_{CH} = 10$ nm, silicon body thickness of $t_{\rm si} = 1.5$ nm, gate oxide thickness of $t_{\rm ox} = 1$ nm with $\kappa = 4$, and an effective Schottky barrier height of $\phi_{eff} = 0.2$ eV. The off current was $I_{off} = 1$ $\mu$A/$\mu$m in both cases.

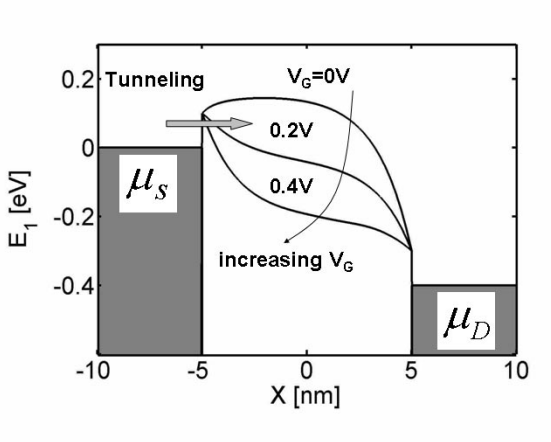



Fig. 14. First conduction subband energy versus position for the SBFET from the off-state ($V_G = 0$ and $V_D = 0.4$ V) to the on-state ($V_G = V_D = 0.4$ V). The shaded region is the silicide source (drain) with the Fermi level $E_{F1}$, $E_{F2}$.

of the MOSFETs, but at high gate voltages, a conduction band spike, which appears near the source end of the channel, limits the current. The gate modulates the current by squeezing the barrier width, which increases quantum mechanical tunneling through the barrier. Because device operation is not governed by thermionic emission, we cannot identify a beginning-of-the-channel, where the charge density is nearly independent of the drain voltage, and the average carrier injection velocity can be computed by simple semiclassical carrier statistics. The analytical model of Section III, as well as the semiclassical Boltzmann transport equation, do not apply to this device. In the conventional MOSFET, transistor action occurs by modulating the charge in the channel; in the SBFET, transistor action occurs by modulating the transmission coefficient of the device. To simulate typical SBFETs with a positive M/S barrier height, an approach that treats the gate-modulated tunneling at the source contact is needed.

## VII. Conclusions

In this paper, we have developed a simple analytical model for ballistic nanotransistors that operate by modulating the charge in the device (as opposed to modulating the current at the contact). For conditions typical of silicon MOSFETs and when 2-D effects are small, this surface potential model reduces to Natoris theory of the ballistic MOSFET. When the insulator capacitance exceeds the quantum capacitance, however, some interesting new effects arise. This analytical model captures the essential physics of MOSFET-like ballistic nanotransistors and provides a convenient way to assess and compare transistors at the ballistic limit.

## Appendix

Fig. 6 shows how the states at the top of the barrier are occupied for a simple $E$–$k$ relationship. As mentioned in Section III, the energy reference is the top of the barrier at zero terminal bias. We express the source Fermi level $E_{F1}$, drain Fermi level $E_{F2}$, and potential at the top of the barrier for first subband $U_{\rm scf}$ with respect to this reference. The positive $k$-states are then occupied according to the Fermi level of the source to find

$$\begin{aligned} N_1 &= \frac{1}{A}\sum_{k_x>0,\,k_y} f\left(E-E_{F1}\right) \\ &= \iint\limits_{k_x>0,\,k_y} 2\frac{d^2k}{(2\pi)^2} f\left(E-E_{F1}\right) \\ &= \int_{-\infty}^{\infty} dE f\left(E-E_{F1}\right)\frac{1}{2}\int_{S(E)}\frac{dS}{2\pi^2}\frac{1}{|\nabla E(k)|} \end{aligned}$$

where $S(E)$ is a constant energy surface in $k$-space, $dS$ is an elemental area on this surface, and $dE/|\nabla E(k)|$ is the distance between the surfaces $S(E+dE)$ and $S(E)$ [41]. Defining the density-of-states as

$$D(E-U_{\rm scf}) = \int_{S(E-U_{\rm scf})}\frac{dS}{2\pi^2}\frac{1}{|\nabla E(k)|}$$

we finally have

$$N_1 = \tfrac{1}{2}\int_{-\infty}^{+\infty} D(E-U_{\rm scf}) f\left(E-E_{F1}\right)\,dE. \tag{A1}$$

The last expression is valid for general bandstructure in 1-D, 2-D, or 3-D. The density-of-states function is either analytically expressed or is numerically tabulated. For a 2-D electron gas with isotropic and parabolic $E$–$k$ relationship, we have

$$D(E-U_{\rm scf}) = g_{2D}\theta(E-U_{\rm scf})$$

where $g_{2D} = 2m^*/\pi\hbar^2$ is the 2-D density-of-states, when spin degeneracy and a valley degeneracy of two for the unprimed subband in silicon are considered. In this case, the integral for $N_1$ can be analytically evaluated as

$$\begin{aligned} N_1 &= \frac{N_{2D}}{2}\log\left(1+e^{(E_{F1}-U_{\rm scf})/k_BT}\right) \\ &= \frac{N_{2D}}{2}\Im_0(\eta_{F1}) \end{aligned} \tag{A2}$$

where $N_{2D} = k_BTg_{2D}$ is the effective 2-D density-of-states, $\Im_0$ is the Fermi Dirac integral of order 0, and $\eta_{F1} = (E_{F1}-U_{\rm scf})/k_BT$. A similar expression exists for $N_2$ with $\eta_{F1}$ replaced by $\eta_{F2} = \eta_{F1} - qV_{DS}/k_BT$.

In addition to the carrier density, we can also evaluate current for the positive $k$ population from

$$\begin{aligned} I_1 &= \frac{q}{A}\sum_{k_x>0,\,k_y} v_x f\left(E-E_{F1}\right) \\ &= \iint_{k_x>0,\,k_y} \frac{d^2k}{2\pi^2}\, q v_x f\left(E-E_{F1}\right) \\ &= \int_{-\infty}^{\infty} dE f\left(E-E_{F1}\right)\frac{q}{2}\int_{S(E)}\frac{dS}{2\pi^2}\left|v_x\right|\frac{1}{|\nabla E(k)|} \\ &= \int_{-\infty}^{\infty} dE f\left(E-E_{F1}\right)\frac{q}{2}\overline{v_x}(E-U_{\rm scf})D(E-U_{\rm scf}) \end{aligned} \tag{A3}$$

where $\overline{v_x}(E)$ is the average value of $|v_x|$ over the constant energy surface $S(E)$, which is expressed as

$$\overline{v_x}(E-U_{\rm scf}) = \frac{\int_{S(E-U_{\rm scf})}\frac{dS}{2\pi^2}\left|v_x\right|\frac{1}{|\nabla E(k)|}}{\int_{S(E-U_{\rm scf})}\frac{dS}{2\pi^2}\frac{1}{|\nabla E(k)|}}.$$

Now, defining the current-density-of-states as

$$J(E-U_{\rm scf}) = \frac{q}{2}\overline{v_x}(E-U_{\rm scf})D(E-U_{\rm scf}) \tag{A4}$$

we have

$$I_1 = \int_{-\infty}^{+\infty} J(E-U_{\rm scf}) f\left(E-E_{F1}\right)\, dE. \tag{A5}$$

In general, this expression can be evaluated for either numerically tabulated or analytically calculated bandstructures. For the 2-D electron density considered here, we can analytically evaluate $\overline{v_x}(E)$ to obtain

$$J(E-U_{\rm scf}) = \frac{1}{2}\,q\left(\frac{2}{\pi}\sqrt{\frac{2(E-U_{\rm scf})}{m^*}}\right)D(E-U_{\rm scf}) \tag{A6}$$

where the factor $2/\pi$ appears because of averaging $v_x$ over all possible $k_y$ values at energy $E-U_{\rm scf}$. With this expression for $J(E-U_{\rm scf})$, we can analytically integrate (A5) to find

$$I_1 = \frac{1}{2}\,qN_{2D}\sqrt{\frac{2kT}{\pi m^*}}\Im_{1/2}\left(\eta_{F1}\right). \tag{A7}$$

Similar expression can be obtained for negative going carriers, with $\eta_{F1}$ replaced by $\eta_{F2}$.

When the drain bias $V_{DS}$ is large, only the $+k_x$ states are occupied, and we can evaluate the maximum velocity at the top of the barrier as

$$\langle v(0)\rangle_{\max} = v_{inj} \equiv \frac{I_1}{qN_1} = \sqrt{\frac{2kT}{\pi m^*}}\,\frac{\Im_{1/2}\left(\eta_{F1}\right)}{\Im_0\left(\eta_{F1}\right)}. \tag{A8}$$

The presence of the Fermi–Dirac integrals in this expression explains why the saturation injection velocities in Figs. 5(b) and 10(b) are gate bias dependent. Below threshold voltage, the ratio of the Fermi–Dirac integrals is one, and the injection velocity becomes constant. The injection velocity at the highest gate bias determines the maximum on-current that a transistor can deliver.

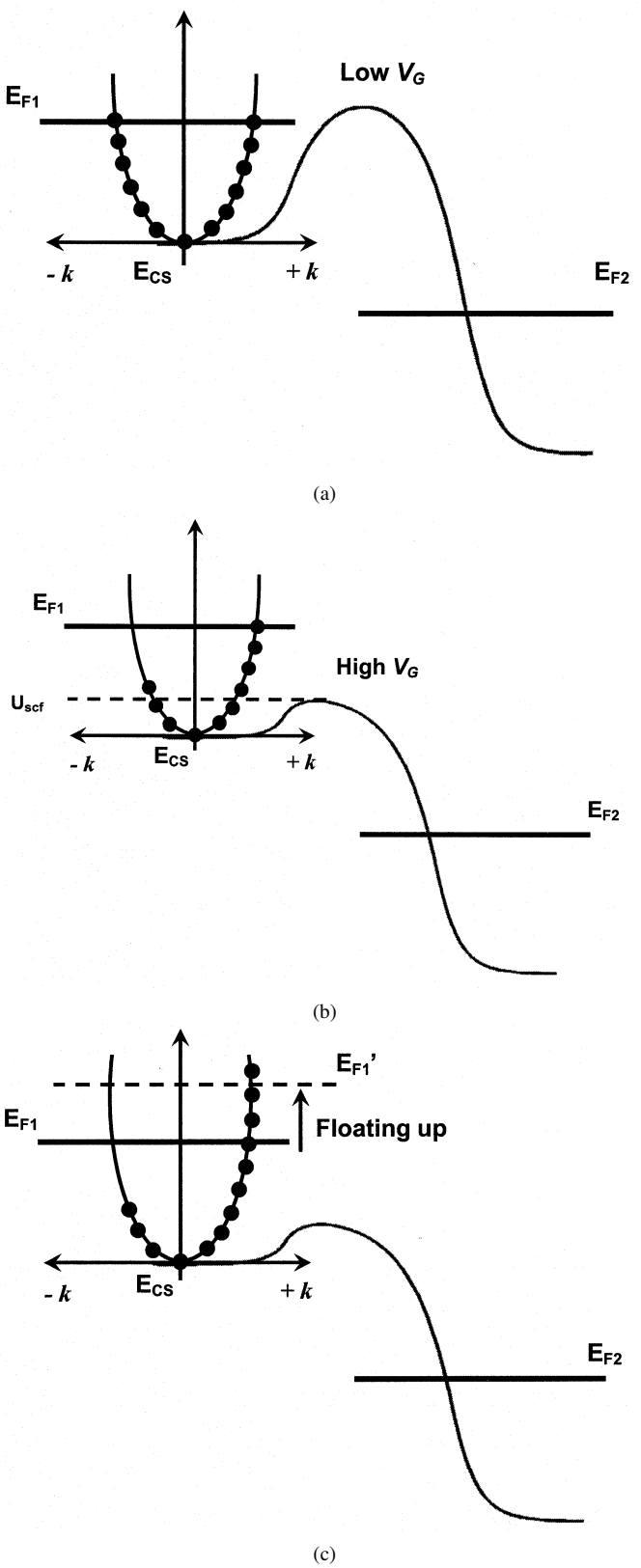



Fig. 15. Treating floating boundary condition. (a) Under low $V_G$, charge neutrality in source extension is maintained by only $E_{F1}$. (b) When $V_G$ is increased, barrier lowers and charge neutrality is not maintainted. (c) Raising $E_{F1}$ to $E'_{F1}$ restores charge neutrality in source entension.

Finally, we will discuss the treatment of the floating boundary condition in the analytical model. In Fig. 15(a), we see that at low gate and high drain bias the barrier height is large, i.e., $U_{\rm scf} \gg E_{CS}$, and inside the source, both positive and negative going states are at equilibrium with the source Fermi level. The charge neutrality condition demands

$$N_{SD} = \int_{-\infty}^{+\infty} D(E - E_{CS}) f\,(E - E_{F1})\; dE. \qquad \text{(A9)}$$

where $N_{SD}$ is the doping density in the source extension.

When high gate bias is applied, we can see in Fig. 15(b) that the barrier height becomes small, and there are three distinct groups of carriers: i) carriers with energy lower than the barrier height and are reflected by the barrier, ii) carriers with energy higher than the barrier and having positive velocity, and iii) carriers having energy above barrier and going in the negative direction. Population groups i) and ii) are at equilibrium with $E_{F1}$, and group iii) is in equilibrium with $E_{F2}$. Because the sum of the three populations in Fig. 15(b) is smaller than equilibrium carrier density in source, to maintain charge neutrality, we have to increase $(E_{F1} - E_{CS})$. Physically, $E_{F1}$ is fixed, and $E_{CS}$ floats down. Equivalently, as shown in Fig. 15(c), we can keep $E_{CS}$ fixed and float $E_{F1}$ up. In our analytical model, we have treated the floating boundary condition by fixing $E_{CS}$ and floating up $E_{F1}$ to $E'_{F1}$. Therefore, the charge neutrality condition in the source is

$$\begin{aligned} N_{SD} = &\int_{-\infty}^{U_{\rm scf}} D(E - E_{CS}) f\,(E - E'_{F1})\;\; dE \\ &+ \frac{1}{2}\int_{U_{\rm scf}}^{\infty} D(E - E_{CS}) \\ &\cdot \{f\,(E - E'_{F1}) + f\,(E - E'_{F1} + qV_{DS})\}\;\; dE. \end{aligned} \qquad \text{(A10)}$$

Equation (A10) is solved self consistently with (3)–(8), i.e., for each $E'_{F1}$, barrier height is computed to distinguish three carrier populations, and charge neutrality in the source is ensured.

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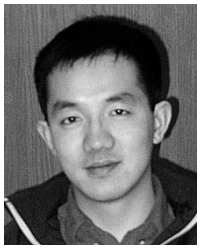

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