Transistor Delay Analysis and Effective Channel Velocity Extraction in AlGaN/GaN HFETs

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Abstract

We have performed a thorough transistor delay analysis on 0.2 μm AlGaN/GaN HFETs implemented on sapphire substrates to identify the various contributions to the total transistor delay $1/2\pi f_T = \tau_T$ as a function of gate-drain separation L_{GD}. We found that the main delay component depends linearly upon the total access resistance of the source and drain regions determined from 'COLDFET' *S*-parameter measurements, indicating the contribution of extrinsic regions to the transistor delay cannot be neglected for AlGaN/GaN HFETs. Stripping the masking effects of the R_S and R_D series resistances reveals an effective channel velocity of $\sim 3.3 \times 10^7$ cm/s which is much higher than the values of $1.2\text{-}1.3 \times 10^7$ cm/s generally inferred from f_T data, but in excellent agreement with predictions from Monte Carlo transport simulations. We also show that process-specific details for devices fabricated on the same epitaxial layers affect the $f_T(L_{GD})$ dependence.

Introduction

Because of their high-breakdown voltages and predicted high electron drift velocities in high electric fields, AlGaN/GaN heterostructure field-effect transistors (HFETs) have received much attention over the last decade. Steady progress in material preparation and device processing have enabled improvements in cutoff frequencies and power handling capability. Despite some marked progress, it can be argued that AlGaN/GaN HFETs have not yet fully lived up to expectations in terms of their ultimate frequency performance. Whereas electrons in AlGaN/GaN two-dimensional electron gases are expected to display peak velocities of $\sim 3.2 \times 10^7$ cm/s according to Monte Carlo simulations [1], significantly lower effective channel velocities of $1.2\text{-}1.3 \times 10^7$ cm/s are typically inferred from measurements of cutoff frequency for a given gate length [2, 3]. The causes of such low apparent electron velocities in the channel of AlGaN/GaN HFETs have so far remained mysterious. It has been suggested that scattering due to interface roughness at the AlGaN/GaN interface and/or scattering from charged threading dislocation lines might be responsible for the disappointing effective channel velocities. Alternative explanations could also involve carrier deconfinement leading to electron injection into the AlGaN barriers where they experience a lower drift velocity, and/or injection deep into the buffer layers resulting in a longer effective electronic path between the gate and drain regions.

Interface roughness and dislocation scattering can indeed reduce the low-field mobility of the AlGaN/GaN two-dimensional electron gas, leading to a reduction of the peak velocity at high electric fields. However, we note that interface roughness scattering is most effective when the characteristic roughness length matches the electronic wavelength, and we would therefore not anticipate strong roughness scattering of highly energetic electrons. Furthermore, Yu and Brennan [1] have shown that representative low-field mobilities of 1200-1500 cm^2/Vs are consistent with 300 K peak velocities of $\sim 3.2 \times 10^7$ cm/s in AlGaN/GaN channels, and even lower mobilities in bulk GaN should allow peak velocities of $\sim 2.5 \times 10^7$ cm/s [4]. Secondly, with threading dislocation densities of 10^9 to 10^{10} $/cm^2$ (corresponding to a linear dislocation spacing of 0.3 to 0.1 μm), many electrons likely transit across a 0.2 μm channel without encountering a single dislocation: this simple observation suggests another cause is responsible for the lower than expected apparent electron velocities generally extracted from AlGaN/GaN HFET $f_T \times L_G$ products. Finally, real space transfer to the AlGaN barrier, and injection into the buffer should happen in the high-field region near the drain edge of gate, and both mechanisms will thus mostly affect the drain delay component as opposed to the intrinsic channel velocity. For our work we have selected the delay analysis method of Moll *et al.* [5] because it allows the identification of the various transistor delay contributions such as the drain delay τ_D, the *RC* channel charging delay τ_{RC}, and the channel transit time delay τ_{TR}.

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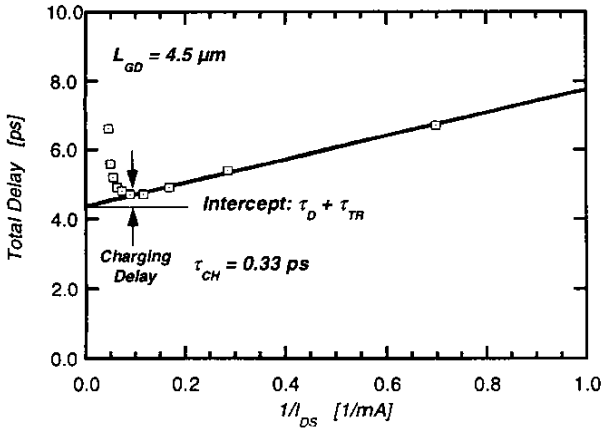

Fig. 1: Extraction of the minimum charging delay in a 0.2 μm gate AlGaN/GaN HFET with a 4.5 μm gate-to-drain separation.

The present work seeks to clarify the reasons behind the discrepancy between the apparent channel velocities in AlGaN/GaN HFET channels and their theoretically expected values. We have performed a thorough HFET transistor delay analysis following the technique of Moll *et al.* [5] to determine how the total transistor delay $1/2\pi f_T = \tau_T = \tau_{RC} + \tau_D + \tau_{TR}$ is partitioned between the channel *RC* charging delay τ_{RC}, the drain delay τ_D due to the extension of the gate depletion toward the drain electrode, and the transistor transit time τ_{TR} for devices fabricated with different values of gate-drain separation L_{GD} and with a gate length of $L_G = 0.2 \pm 0.01$ μm. Some published works indicate that AlGaN/GaN HFETs can show a dramatic decrease of f_T with increasing L_{GD} [6], suggesting a study of the impact of L_{GD} could reveal key information pertaining to the causes of low apparent electron velocities in AlGaN/GaN HFET channels. We found that τ_{TR} depends linearly upon the total access resistance of the source and drain regions, and that these contributions cannot be neglected due to relatively high values of sheet and contact resistances in AlGaN/GaN HFETs when compared to traditional III-V HFETs. One of the key findings of our study is that the effective intrinsic channel velocity extracted in this manner indeed matches theoretical predictions from Monte Carlo computations [1] when the masking effects of R_S and R_D are stripped.

Device Structure and Fabrication

Our HFETs were fabricated on commercially available piezoelectric doped $Al_{0.36}Ga_{0.64}N$/GaN HFET layers grown by MOCVD on a sapphire substrate with a 200 Å top barrier. The as-grown layers were characterized by a 300 K sheet electron density of 1.7×10^{13} cm^{-2} and $\mu = 1{,}070$ cm^2/Vs, corresponding to an original sheet resistance of ~340 Ω/□. Our devices were fabricated using a low-damage ultraviolet photo-assisted wet mesa isolation etching technique, and typically featured $f_T = 50$ GHz and $f_{MAX} = 100$ GHz for $L_{GD} = 2.5$ μm. In the present case device processing consists of first forming isolation mesas by UV photo-assisted etching using a $K_2S_2O_8$+KOH solution and an electron beam deposited platinum mask layer that is subsequently removed by etching in 100°C H_2O:HCl:HNO_3. Ohmic contacts were formed by rapid thermal annealing of Ti/Al/Ti/Au for 60 seconds at 850°C, and T-gates were defined in a tri-layer PMMA/co-PMMA stack by electron beam lithography and liftoff of a Ni/Au film. The above device fabrication process affects the 2DEG sheet resistance as seen by the post-process TLM sheet resistance of 550 Ω/□. The Ohmic contact resistance measured by the TLM method was $r_C \sim 1$ Ω·mm. In addition, transistors were also fabricated on a neighboring piece from the same epitaxial layers as above but with a process relying on ion implantation for device isolation in order to determine whether device processing has an impact on the $f_T(L_{GD})$ dependence. None of our devices were passivated.

Transistor Delay Extraction

The method described by Moll *et al.* [5] makes use of a series of judicious bias sweeps and extrapolations of the measured transistor delay in order to resolve how the delay is partitioned between its components. The method was therefore applied to transistors fabricated with the UV photo-assisted wet mesa etch process described above in order to characterize the effect of the gate-to-drain separation L_{GD} on otherwise nominally identical T-gate HFETs with $(0.20 \pm 0.01) \times 50$ μm^2 gate and a gate-to-source spacing $L_{GS} = 1.0 \pm 0.1$ μm for $0.5 \le L_{GD} \le 4.5$ μm. These tight dimensional tolerances were chosen so as to minimize any potential impact of L_{GS} and L_G critical dimension variations on device performance.

Following [5], we extract the channel charging delay τ_{CH} by plotting the minimum total delay $1/2\pi f_T = \tau_T$ as a function of $1/I_{DS}$: τ_{CH} is then the difference between τ_{Tmin1} (the minimum delay in the plot) and the delay extrapolated back to $1/I_{DS} = 0$, as shown in Fig. 1. The drain delay τ_D contribution is extracted by plotting the minimum delay achieved in a drain bias sweep against the reduced drain voltage $V_D' = V_D - I_D(R_S + R_D)$, where R_S and R_D are the HFET parasitic access resistances extracted from 'COLDFET' *S*-parameter measurements (measured with a forward biased gate diode and grounded source and drain). The drain delay is then extracted as the difference between the minimum measured delay in this plot τ_{Tmin2} and delay the value extrapolated to zero reduced drain voltage $\tau_T(V_D' = 0)$, that is, $\tau_D = \tau_{Tmin2} - \tau_T(V_D' = 0)$. The remaining transistor delay τ_{TR} is the

difference between the minimum transistor delay and the sum of τ_D and τ_{CH}: $\tau_{TR} = \tau_T - (\tau_D + \tau_{CH})$. In their original work, Moll *et al.* referred to τ_{TR} as the "intrinsic" transistor delay [5], a denomination that is quite suitable for conventional GaAs and InP based HEMTs with low access series resistances.

The original method of [5] suffers two drawbacks. Firstly, the method requires that rather large quantities of data be collected and processed for each point in a plot such as in Fig. 1. This drawback is offset by the rich amount of information the technique provides about the device under consideration. The second limitation is that the method does not account for the contribution of access resistances R_S and R_D to the total transistor delay as do equivalent circuit approaches such as those described by Tasker and Hughes [7] or Roblin and Rohdin [8]. This is generally not a serious drawback for HEMT technologies featuring low series resistances, but the impact of access resistances is potentially more important in AlGaN/GaN HFETs which tend to feature higher contact resistances and potentially bias dependent channel sheet resistances (due to the effect of surface state related channel depletion). When series resistance effects become non-negligible, the delay model of Moll *et al.* [5] must be augmented so that

$$\tau_{TR} = \tau_i + \tau_{RSD}(L_{GS}, L_{GD}, r_C) \qquad (1)$$

where τ_{RSD} is the series resistance contribution and τ_i is the transit time across the intrinsic channel under the gate. The intrinsic delay is then related to the gate length L_G and the effective electron velocity in the channel by $v_F = L_G/\tau_i$.

Fig. 2 shows the delay contributions for several devices with a $L_G = (0.20 \pm 0.01)\,\mu m$ gate length and a gate-source spacing $L_{GS} = 1.0 \pm 0.1$ μm for several values of gate-drain separation L_{GD} with the results plotted versus the total drain and source resistance $R_S + R_D$ determined from 'COLDFET' S-parameter data. The drain and channel charging delays τ_D and τ_{CH} are independent of L_{GD}. The independence of τ_D from L_{GD} indicates that the gate depletion does not extend all the way to the drain contact for the devices under consideration —this is the result to be expected for a high-density two-dimensional electron gas channel. On the other hand, τ_{TR} shows a clear dependence on $R_S + R_D$ (or equivalently L_{GD} plus a fixed L_{GS}) due to the τ_{RSD} contribution. Extrapolation of τ_{TR} to $(R_S + R_D) = 0$ yields the intrinsic transit delay $\tau_i = 0.61$ (± 0.18 ps), indicating an effective channel velocity of $\sim 3.3 \times 10^7$ cm/s based on a best fit to the data of Fig. 2. Even the worse case estimate of velocity from Fig. 2 is significantly higher than values inferred from f_T data.

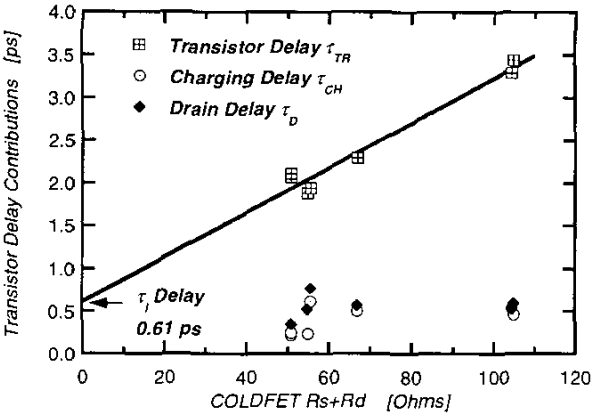

Fig. 2: Delay components as a function of total 'COLDFET' series resistance. A least square fit to the τ_{TR} data leads to an intrinsic delay $\tau_i = 0.61$ ps (correlation coefficient $R^2 = 0.958$, Σ(squared errors) = 0.107 ps^2, intercept error range ± 0.18 ps). The fit yields an effective channel velocity equal to $v_F = L_G/\tau_i = 3.3 \times 10^7$ cm/s. The data indicate that neither τ_D nor τ_{CH} depend on L_{GD}.

Fig. 2 shows that τ_{CH} and τ_D feature no dependence on the gate-to-drain spacing. The independence of drain delay upon L_{GD} indicates that the gate depletion layer does not extend all the way to the drain contact in the present devices.

Analysis and Discussion

Because of the low output conductance of our devices, τ_{RSD} is to first order $\tau_{RSD} \sim (R_S + R_D)C_{GD}$ [7, 8]. However, the slope of the $\tau_{TR}(R_S + R_D)$ fit in Fig. 2 is equal to 26 fF, and is significantly higher than expected for C_{GD}. Indeed, direct extraction of an equivalent circuit model from measured S-parameters indeed yields $C_{GD} = 5$ fF with $C_{GS} = 35$ fF, $G_M = 190$ mS/mm, and $G_{DS} = 0.2$ mS/mm. This indicates that the *effective* parasitic series resistances *under operational bias* (say, $V_{DS} = 15$ V) are roughly 5× higher than those indicated by 'COLDFET' and TLM measurements (the latter two being consistent with each other). Let us now consider the implications of this modulation of the series resistance by assuming a uniform 5× reduction in channel carrier density across the transistor extrinsic regions. Scaling $(R_S + R_D)$ in Fig. 2 does not change the intrinsic delay. Similarly, we have verified that such an increase in resistance does not significantly affect the extracted minimum drain delay τ_D: our conclusions about the effective channel velocity thus remain unaffected by the resistance modulation at high biases.

We now check for consistency between our conclusions and measured transistor parameters. The anticipated open-channel current based on low-bias quantities for the post-process wafer is $I_{DSS} = qv_F N_S' = 5.3$ A/mm: a 5× reduction in N_S' brings the current in-line with experimental results (0.8-1 A/mm). Next, a channel velocity of $v_F = 3.3 \times 10^7$ cm/s leads to an intrinsic transconductance value $G_{Mo} = C_{GS}v_F = 1.15$ S/mm: this results in a calculated intrinsic HFET delay $\tau_i' = (C_{GS} + C_{GD})/G_{Mo} = 0.69$ ps which is in reasonable agreement with the result of Fig. 2. Degenerating G_{Mo} by a 'COLDFET' $R_S = 30\ \Omega$ for $L_{GS} = 1$ µm gate-source spacing yields $G_M = 420$ mS/mm which is too high, but allowing a 5× increase of the channel sheet resistance at high biases results in a calculated $G_M = 207$ mS/mm which is in good agreement with the measured value of 190 mS/mm. Our assumptions, our delay extractions, and our measured data are thus self-consistent.

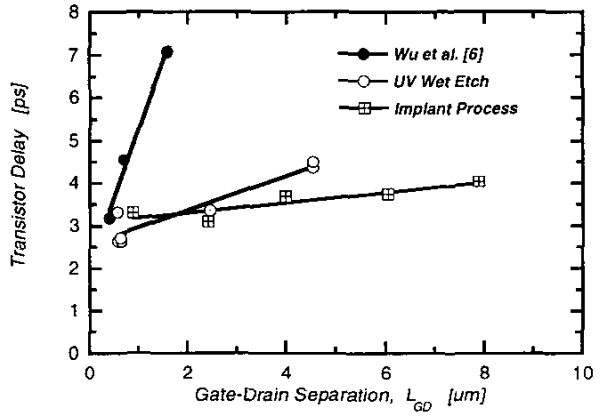

Fig. 3: Transistor delay dependence on gate-to-drain separation for implant isolated and wet etched mesa transistors fabricated on the same epitaxial layers. The gate-drain space contributes a delay of 0.12 ps/µm for the implanted process, 0.39 ps/µm for the UV wet etched mesa process, and ~3.1 ps/µm for the RIE process of [6].

The physical mechanism behind the 5× increase in resistance between low and high bias regimes remains unclear at the time of writing: surface state effects and/or heating effects cannot be ruled out. We have recently raised the possibility that the $f_T(L_{GD})$ dependence may provide a quantitative way to measure of the impact of surface states for various process architectures [9]. To test this idea, we show in Fig. 3 the measured $\tau_T(L_{GD})$ dependencies for both the wet etch isolation process and for ion implantation isolated HFETs fabricated from a nearby location on the same epitaxial layers. Clearly, the choice of process is seen to strongly affect the $f_T(L_{GD})$ behavior for devices made on the same layers, and the very weak impact of L_{GD} on the overall transistor delay (0.12 ps/µm) for the implant process allows what we believe is an unprecedented 40 GHz cutoff frequency for an 8 µm gate-drain spacing. By comparison, our wet etch process leads to $\tau_T(L_{GD})$ variation of 0.39 ps/µm based on the data from Fig. 2, and the RIE process of Wu *et al.* features a ~3.1 ps/µm dependence [6]. It is noteworthy that while our devices do not display noticeable current slump effects, the implanted samples show weaker evidence of trapping effects as judged from the degree of hysteresis in the *I-V* characteristics in comparison to the wet etched mesa devices. This observation lends further credibility to the idea that surface states play a role in the $f_T(L_{GD})$ dependence for a given process.

Acknowledgments

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