Delay Time Analysis for 0.4- to 5-μm-Gate InAlAs–InGaAs HEMT's

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Abstract—**InAlAs–InGaAs HEMT's with 0.4- to 5-μm gate lengths have been fabricated and a maximum f_T of 84 GHz has been obtained by a 0.4-μm-gate-length device. Simple analysis of their delay times is carried out. The gradual channel approximation with the field-dependent mobility model with E_c of 5 kV/cm holds for long-channel devices ($L_g > 2$ μm). The saturated velocity model with the saturated velocity of 2.7×10^7 cm/s holds for short-channel devices ($L_g < 1$ μm).**

I. Introduction

InP-based InAlAs–InGaAs HEMT's have demonstrated excellent high-frequency and low-noise performance. Mishra *et al.* reported a 250-GHz cutoff frequency using 0.12-μm-gate HEMT's [1]. Thus, this material system is promising for high-frequency and low-noise devices.

These high performances are generally explained by the high sheet carrier density and superior electron transport properties. In this report, we decompose the total delay times into transit times and charging times for fabricated InAlAs–InGaAs HEMT's with 0.4- to 5-μm gates for the first time, and discuss electron transports for long-channel and short-channel devices.

II. Device Structure and Performance

The $In_{0.52}Al_{0.48}As$–$In_{0.53}Ga_{0.47}As$ modulation-doped heterostructure utilized in this study is shown in Fig. 1. The structure was grown by molecular beam epitaxy on Fe-doped semi-insulating (100) InP substrates at a temperature of 540°C. The doping density for n^+-InAlAs was 4×10^{18} cm^{-3}. The undoped InAlAs layer between two highly doped InAlAs layers is to enhance the Schottky barrier of the gate metal. The upper n^+-InAlAs layer is designed to reduce the source and drain series resistance. The sheet resistance is 145 Ω/sq, and the carrier density and mobility of the two-dimensional electron gas under the gate metal were 3.0×10^{12} cm^{-2} and 9800 $cm^2 \cdot V^{-1} \cdot s^{-1}$ at 300 K, respectively.

The 0.4- to 5-μm-gate-length devices with 150-μm gate width were fabricated by conventional optical lithography. AuGe/Ni was used for source and drain ohmic contacts with a contact resistance of 0.14 $\Omega \cdot$ mm. The gate region was recessed to a desired drain current by wet etching and metallized with Ti/Au.

The source series resistance was estimated to be 0.30 $\Omega \cdot$ mm from the results of TLM measurements. The extrinsic transconductance and drain conductance were 620 and 560 mS/mm, respectively. The estimated intrinsic transconductance is 760 mS/mm. Devices were characterized in the frequency region from 0.5 to 25.5 GHz on a Cascade RF probe station. The current gains h_{21} were extracted from the S parameters and the unity-current-gain cutoff frequency f_T was calculated by extrapolating at 6 dB/octave. Fig. 2 shows the gate-length dependence of f_T. A maximum f_T of 83.5 GHz was obtained by the 0.4-μm-gate device. The f_T for the 0.5-μm gate device was 68 GHz. These values are comparable to the best values reported for a half-micrometer-gate-length device.

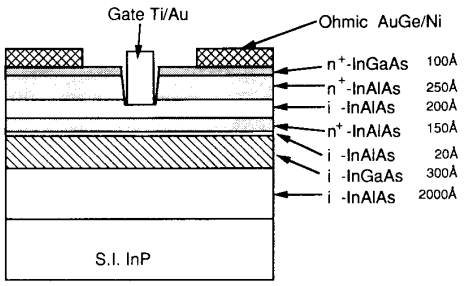

Fig. 1. $In_{0.52}Al_{0.48}As$–$In_{0.53}Ga_{0.47}As$ modulation-doped structure utilized in this study. The doping density of n^+-InAlAs was 4×10^{18} cm^{-3}. The Schottky contact was formed in the undoped InAlAs layer between two highly doped InAlAs layers.

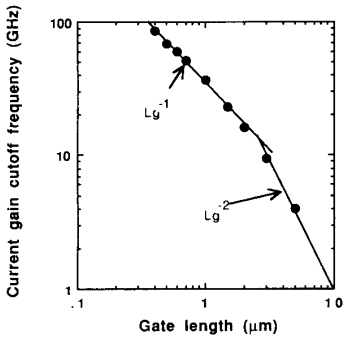

Fig. 2. Gate-length dependence of the current-gain cutoff frequency f_T. A maximum f_T of 83.5 GHz was obtained by the device with a gate length of 0.4 μm and a gate width of 150 μm.

III. Discussion

In order to discuss the intrinsic characteristics of devices, it is necessary to subtract the effect of parasitic elements, such as source and drain series resistances. According to the representation of f_T for an equivalent circuit model [2], we

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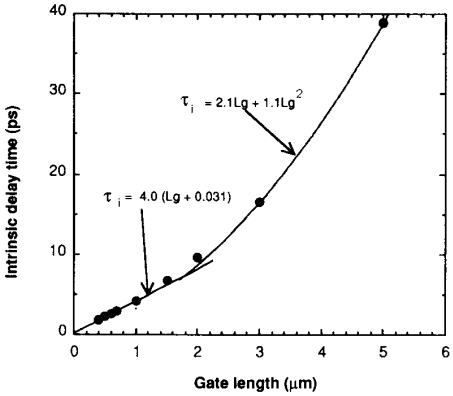

Fig. 3. Gate-length dependence of the intrinsic delay time (τ_i) which was obtained by subtracting parasitic charging time ($\tau_{s,d}$) from total delay time.

can derive the total delay time as

$$\tau_{\text{total}} = \frac{1}{2\pi f_T} = \frac{C_{gs} + C_{gd}}{g_m}\left(1 + \frac{R_s + R_d}{R_{ds}}\right) + C_{gd}(R_s + R_d) \quad (1)$$

where g_m is the intrinsic transconductance, C_{gs} is the capacitance between the gate and the source, C_{gd} is the capacitance between the gate and the drain, and R_{ds} is the channel resistance. The first term of this equation represents the intrinsic delay time. The second term of (1) can be considered the parasitic charging time ($\tau_{s,d}$) for C_{gd} through R_s and R_d. The $R_s + R_d$ and C_{gd} can be derived from the TLM measurement and the imaginary part of the Y_{12} parameter, respectively. This delay time was about 0.13 ps at the biases where f_T was maximum. Thus, the intrinsic delay time was estimated by subtracting $\tau_{s,d}$ from the total delay time. Fig. 3 shows the gate-length dependence of the τ_i.

The τ_{transit} for the long-channel devices can be represented as

$$\tau_{\text{transit}} = \frac{L_g}{\mu E_c} + \frac{2L_g^2}{3\mu V_c} \quad (2)$$

employing the gradual channel approximation with the field-dependent mobility model [3] where

$$v(E) = \frac{\mu E}{1 + \frac{E}{E_c}} \quad (3)$$

and V_c is the channel potential drop, μ is the low-field electron mobility, and E_c is the critical field. As shown in Fig. 3, it is apparent that the gradual channel approximation with the field-dependent mobility model holds for devices with gate lengths exceeding 2 μm. The E_c of 4.9 kV/cm is obtained by fitting the delay times for the >2-μm-gate-length devices using (2) and the measured low-field mobility of 9800 $\text{cm}^2 \cdot \text{V}^{-1} \cdot \text{s}^{-1}$. In the region of electric field strength below 5 kV/cm, the v–E curve represented as (3) agrees well with results obtained by the time-of-flight (TOF) method [4].

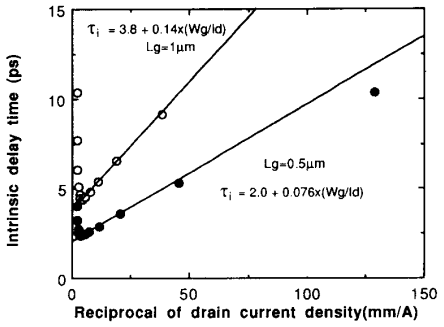

Fig. 4. Relationship between the intrinsic delay time and the reciprocal of the drain current density for 0.5- and 1-μm-gate-length devices. V_{ds} was fixed at 1.25 V. The τ_{transit}'s are 2.0 and 3.8 ps for 0.50- and 1.0-μm-gate devices.

On the other hand, the saturated velocity model holds for devices with gate lengths below 1 μm. The τ_i must be decomposed into the transit time of electrons (τ_{transit}) and the channel charging time (τ_{cc}), i.e., $\tau_i = \tau_{\text{transit}} + \tau_{cc}$. These delay times can be divided by the drain-current dependence of the τ_i as reported by Moll *et al.* [5]. Fig. 4 shows the relationship between the τ_i and the reciprocal of the drain current density for 1- and 0.5-μm-gate-length devices. The τ_{transit} is the linearly extrapolated delay time at $W_g/I_d = 0$ and the τ_{cc} was the difference between the τ_i and the τ_{transit}. The minimum τ_{cc}'s are 0.34 and 0.62 ps for 0.5- and 1-μm-gate-length devices, respectively. The τ_{transit}'s are 2.0 and 3.8 ps for 0.5- and 1-μm-gate devices.

The relationship between τ_{transit} and electron transport for the short-channel device can be represented as

$$\tau_{\text{transit}} = \frac{L_g + \Delta L}{v_s} \quad (4)$$

in terms of the saturated velocity model where v_s is the saturated velocity of electrons and ΔL is considered the spread of the depletion layer at the source and drain end of the gate. A ΔL of 0.031 μm and a v_s of 2.7×107 cm/s are obtained by fitting these delay times using (4). This value of 2.7×10^7 cm/s is higher by a factor of 1.5 than the steady-state electron velocity under the electric field strength of 12 kV/cm in InGaAs measured by TOF [4].

IV. Conclusions

InP-based InAlAs–InGaAs HEMT's with 0.4- to 5-μm gate lengths have been fabricated. Simple analysis of their delay times has been carried out. For devices with gate lengths exceeding 2 μm, the gradual channel approximation utilizing the simple field-dependent mobility model holds and the critical field is estimated to be 4.9 kV/cm. For devices with gate lengths less than 1 μm, the saturated velocity model holds and the saturated velocity is estimated to be 2.7×10^7 cm/s. This value is higher by a factor of 1.5 than the steady-state electron velocity under the high-field strength.

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