Importance of Source and Drain Resistance to the Maximum f_T of Millimeter-Wave MODFET's

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***Abstract*—The usual approximate expression for measured $f_T = [g_m/2\pi(C_{gs} + C_{gd})]$ is inadequate. At low drain voltages just beyond the knee of the DC *I–V* curves, where intrinsic f_T is a maximum for millimeter-wave MODFET's, the high values of C_{gd} and G_{ds} combine with the high g_m to make terms involving the source and drain resistance significant. It is shown that these resistances can degrade the measured f_T of a 0.30-μm GaAs/AlGaAs MODFET from an intrinsic maximum f_T value of 73 GHz to a measured maximum value of 59 GHz. The correct extraction of maximum f_T is essential for determining electron velocity and optimizing low-noise performance.**

SOURCE and drain parasitic resistances (R_s and R_d) are not usually expected to affect measured f_T. This assumption is not true at low drain voltages just beyond the knee of the dc *I–V* curves where intrinsic f_T is a maximum. A typical example is shown in Fig. 1, where the measured *extrinsic* f_T and the de-embedded *intrinsic* f_T are plotted versus drain voltage for a 0.3 × 120-μm double-doped quantum-well AlGaAs/GaAs MODFET, similar to that reported by Hueschen *et al.* [1]. The MODFET f_T data were extracted from *S*-parameters measured on-wafer at 5 GHz using a calibrated (Cascade Microtech Impedance Standard Substrate (ISS)) HP8510 network analyzer with Cascade Microtech microwave probes [2]. The measured *S*-parameters were corrected for the 6-fF pad capacitance and then the extrinsic f_T was extrapolated assuming a −20-dB/decade roll-off for the short-circuit current gain $|h_{21}|^2$[2]. The intrinsic f_T was extrapolated in a similar manner after first de-embedding the effect of the parasitic resistors from the measured *S*-parameters [3]–[5]. A maximum measured f_T of 59 GHz is observed at a drain voltage of 1.1 V. After de-embedding the parasitics the maximum intrinsic f_T is higher: 73 GHz. This value occurred at the lower drain voltage of 0.7 V where the extrinsic value was only 51 GHz.

The usual approximate expression for measured f_T is generally assumed to be the intrinsic expression:

$$f_T = \frac{g_m}{2 \cdot \pi \cdot [C_{gs} + C_{gd}]} \tag{1}$$

which does not include R_s and R_d terms [6], [7], since at first inspection, impedances in series with the input and output ports only affect voltage, not current. Even though R_s makes the extrinsic g_m smaller than the intrinsic g_m by a factor of

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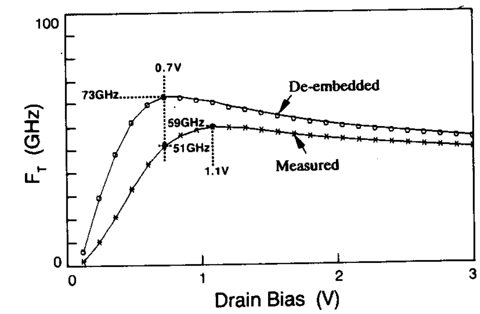

Fig. 1. Measured and de-embedded f_T versus drain voltage for a 0.3-μm double-doped AlGaAs/GaAs MODFET. The gate was biased for f_T maximum (−0.15 V).

$1/(1 + g_m \cdot R_s)$, it also decreases C_{gs} by the same factor and so should not affect f_T.

A more rigorous derivation for the short-circuit current gain of a FET [8] gave a better approximate expression for the extrinsic f_T:

$$f_T = \frac{g_m/(2 \cdot \pi)}{[C_{gs} + C_{gd}] \cdot [1 + (R_s + R_d)/R_{ds}] + C_{gd} \cdot g_m \cdot (R_s + R_d)}. \tag{2}$$

The additional terms in (2) can be explained as follows. Although the drain is effectively shorted to the source when calculating h_{21}, in the presence of R_s and R_d, all of the current from g_m does not pass through this current path; some flows through R_{ds}. The resulting resistive divider effect reduces the measured current gain by the factor $(1 + (R_s + R_d)/R_{ds})$. Also, the voltage drop across C_{gd} is now larger than that across C_{gs} because of the IR voltage developed across R_s and R_d. The resulting Miller effect increases the effective C_{gd} by a factor of $(1 + g_m \cdot R)$ where $R = (R_s + R_d)/(1 + (R_s + R_d)/R_{ds})$. These effects are shown schematically in Fig. 2.

Because g_m, C_{gs}, C_{gd}, and R_{ds} are strong functions of bias (see Fig. 3 and 4), the discrepancies between the f_T's predicted by (1) and (2) vary with drain bias as demonstrated in Fig. 1. As the drain voltage increases, C_{gd} decreases and C_{gs} increases while the total gate capacitance $(C_{gs} + C_{gd})$ is approximately constant (see Fig. 3). The intrinsic f_T, therefore, follows the behavior of g_m, which increases rapidly with increasing drain voltage reaching a maximum at approximately the knee voltage of the dc *I–V* curves (0.7 V; see Figs. 1 and 4). This value of V_{DS} further decreases to 0.5 V after the dc correction for $I_{DS} \cdot (R_s + R_d)$, the maximum intrinsic g_m and f_T occurring just when the drain voltage is sufficient to saturate the electron velocity.

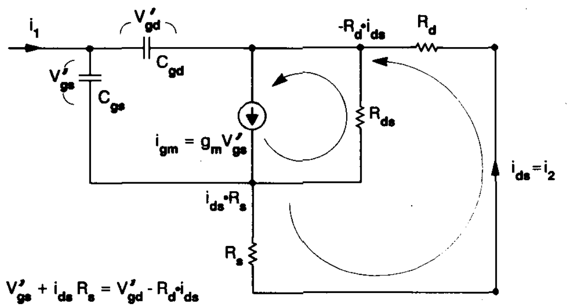

Fig. 2. Simple small-signal model of an FET indicating important terms for calculating f_T.

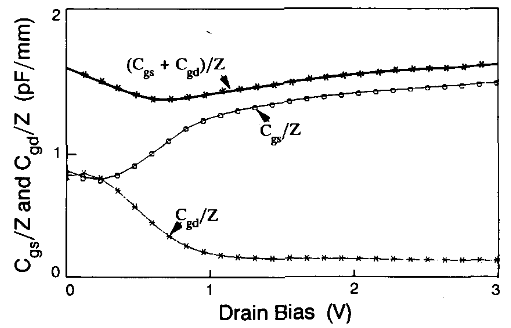

Fig. 3. C_{gs}/Z and C_{gd}/Z versus drain voltage for a 0.3-μm double-doped AlGaAs/GaAs MODFET.

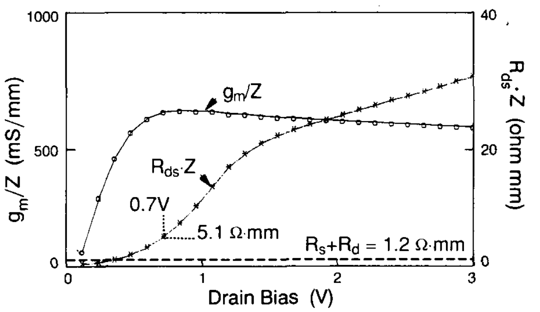

Fig. 4. g_m/Z and $R_{ds} \cdot Z$ versus drain voltage for a 0.3-μm double-doped AlGaAs/GaAs MODFET.

Since the intrinsic g_m and f_T reach their maximum value before C_{gd} and $G_{ds}(1/R_{ds})$ reach their low saturated values, the effect of R_s and R_d on extrinsic f_T dominates at this bias condition. For example, in this MODFET, when biased at maximum intrinsic f_T, $R_{ds} \cdot Z$ is only 5.1 $\Omega \cdot$mm compared to 1.2 $\Omega \cdot$mm for $R_s + R_d$; therefore the resistor divider effect reduces the extrinsic f_T by 18 percent. At the same bias C_{gd} is 23 percent of the total gate capacitance; therefore the Miller effect also reduced the extrinsic f_T by 15 percent. The measured f_T of 53 GHz is thus 30 percent lower than the intrinic f_T value of 73 GHz at V_{DS} of 0.7 V. The correct interpretation of MODFET performance at maximum f_T is required for correctly extracting electron velocity and optimizing low-noise performance. Note that it is easy to overestimate R_s and R_d during extraction which can lead to an overestimation of the intrinsic f_T.

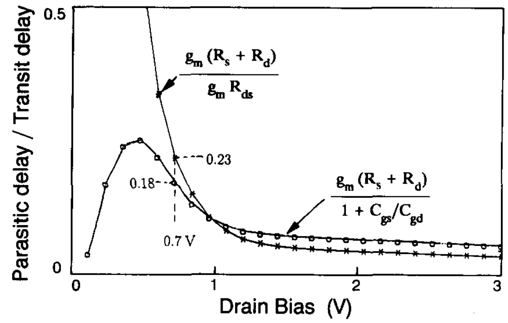

Fig. 5. Ratio of parasitic delay to transit delay versus drain voltage for a 0.3-μm double-doped AlGaAs/GaAs MODFET. * is R_{ds} delay ratio and ○ is C_{gd} Miller delay ratio.

The maximum measured extrinsic f_T is at a drain voltage of 1.1 V, where although the intrinsic f_T is lower, the parasitic effects are less dominant because G_{ds} and C_{gd} are lower. At high drain bias voltages (> 1.5 V) $R_{ds} \cdot Z$ is much larger (e.g., 33 $\Omega \cdot$mm for V_{ds} = 3 V) so the current flow through R_{ds} decreases (hence its effect on extrinsic f_T diminishes), down to 4 percent in this case. Also, at larger drain voltage, C_{gd} is a much smaller fraction of the total gate capacitance (e.g., 8 percent for V_{ds} = 3 V) so the Miller effect only degrades extrinsic f_T by 6 percent. Consequently, when this MODFET was biased with 3 V on the drain, the extrinsic f_T was 50 GHz, reduced from an intrinsic value of 55 GHz, which is only a 9 percent change. At large drain bias voltages the expression (1) is adequate for measured f_T, however, (2) is necessary near the knee where maximum f_T is obtained.

Another approach to understanding the role of R_s and R_d is via delays. $1/2\pi f_T$ is the total current delay through the device and, as for example in bipolar transistors, it is usually expressed in terms of transit and charging delays. Inverting (2) and rearranging gives the FET delays in terms of an intrinsic or transit delay [6] and two other parasitic delays:

$$\frac{1}{2 \cdot \pi \cdot f_T} = \frac{[C_{gs} + C_{gd}]}{g_m} + \frac{[C_{gs} + C_{gd}] \cdot (R_s + R_d)}{g_m \cdot R_{ds}} + C_{gd} \cdot (R_s + R_d). \quad (3)$$

The ratio of the parasitic delays to the transit delay is

$$\frac{\tau_p}{\tau_t} = g_m (R_s + R_d) \left[\frac{G_{ds}}{g_m} + \frac{1}{[1 + C_{gs}/C_{gd}]} \right]. \quad (4)$$

The resistor divider and Miller capacitance terms in (4) are plotted in Fig. 5. At maximum intrinsic f_T these terms are 0.23 and 0.18, respectively. Charging delays of GaAs MESFET's biased in the saturated region are not significant and have traditionally been ignored. However, charging delays in short gate length MODFET's biased for maximum f_T cannot be ignored until the parasitics are reduced in proportion to the reduction in intrinsic transit times. This point was recently made by Nguyen *et al.* [9] who attributed some of the high f_T of 150 GHz for a 0.15-μm 25-percent indium pseudomorphic MODFET to reduced parasitic resistances.

At the low drain bias required for maximum intrinsic f_T, the ratios g_m/G_{ds} and C_{gs}/C_{gd} are both approximately 3 for this

MODFET. Since similar ratios have been measured on other MODFET's and are expected to hold for most FET structures, the parasitic delays can only be reduced at low drain voltages by reducing the $g_m \cdot (R_s + R_d)$ term. For the parasitic delay to be less than 20 percent of the total delay the $g_m \cdot (R_s + R_d)$ product, F, has to be less than 0.4. This term is relatively large (0.8) for this and many other short gate length FET's compared to the more familiar longer gate length MESFET's because g_m is higher. A higher g_m is necessary for high f_T because C_{gs}/Z has to be approximately 1 pF/mm for fringing capacitance and aspect ratio considerations. To maintain a low $g_m \cdot (R_s + R_d)$ factor $R_s + R_d$ has to be reduced in proportion to the g_m increase. A rule of thumb can be made for scaling $R_s + R_d$ by assuming the saturated velocity FET model:

$$(R_s+R_d)Z = \frac{F}{g_m/Z} \approx \frac{F}{2\pi f_T C_{gs}/Z} \approx \frac{F L_g}{v_s C_{gs}/Z} = R_p L_g(\mu\text{m})\ \Omega\cdot\text{mm} \quad (5)$$

$$F = g_m(R_s+R_d) \quad (6)$$

where L_g is the gate length and v_s is the saturation velocity. For example, assume F is 0.4, C_{gs}/Z is 1 pF/mm, and v_s is 2×10^7 cm/s; then R_p is $2\Omega\cdot$mm. This suggests that $(R_s + R_d)\cdot Z$ should be 2 $\Omega\cdot$mm for a 1-μm gate length FET, and 0.66 $\Omega\cdot$mm for a 0.3-μm FET instead of the 1.2 $\Omega\cdot$mm reported here. In the MODFET reported here parasitic delay is 29 percent of the total delay.

Conclusion

De-embedding the microwave measurements from R_s and R_d was shown to both increase the maximum value of f_T and decrease the drain voltage at the maximum. The usual approximate expression for f_T is inadequate at low drain voltages just beyond the knee of the dc I–V curves where intrinsic f_T is a maximum. R_s and R_d have a significant effect on extrinsic f_T at this bias condition because R_{ds} is only a few times greater than $R_s + R_d$ and $C_{gd} \cdot g_m \cdot (R_s + R_d)$ is a substantial fraction of total gate capacitance. When MODFET's are made with short gate lengths and improved material systems [9]–[11], the parasitic resistances should be decreased in proportion to the increase of g_m to see all the increase in the intrinsic f_T.

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References

[1] M. R. Hueschen, N. Moll, and A. Fischer-Colbrie, "High-current GaAs/AlGaAs MODFET's with f_T over 80 GHz," in *IEDM Tech. Dig.* (Washington, D.C.), Dec. 1987, pp. 596–599.

[2] P. J. Tasker and B. Hughes, "Bias dependence of the MODFET intrinsic model element values at microwave frequencies," submitted to *IEEE Trans. Electron Devices,* 1989.

[3] P. J. Tasker and B. Hughes, in preparation.

[4] R. Vogel, "Determination of the MESFET resistive parameters using RF-wafer probing," in *Proc. 17th European Microwave Conf.* (Rome), 1987, pp. 616–621.

[5] G. Dambrine, A. Cappy, F. Heliodore, and E. Playez, "A new method of determining the FET small-signal equivalent circuit," *IEEE Trans. Electron Devices,* vol. 35, pp. 1151–1159, July 1988.

[6] K. E. Drangied and R. Sommerhalder, "Dynamic performance of Schottky-barrier field-effect transistors," *IBM J. Res. Develop,* vol. 14, no. 2, pp. 82–94, Mar. 1970.

[7] M. B. Das, "A high aspect ratio design approach to millimeter wave HEMT structures," *IEEE Trans. Electron Devices,* vol. ED-32, pp. 11–17, Jan. 1985.

[8] P. J. Tasker and L. F. Eastman, "Determination of intrinsic f_T of FET devices from measured microwave data," presented at WOCSEMMAD, Hilton Head Island, SC, Mar. 1987.

[9] L. Nguyen, P. Tasker, D. Radulescu, and L. Eastman, "Design, fabrication and characterization of ultra high speed 0.15 μm mushroom gate $Al_{0.30}Ga_{0.70}As/In_{0.25}Ga_{0.75}As$ MODFET's," in *IEDM Tech. Dig.* (San Francisco, CA), Dec. 1988, pp. 176–179.

[10] N. Moll, M. R. Hueschen, and A. Fischer-Colbrie, "Pulsed-doped AlGaAs/InGaAs pseudomorphic MODFET's," *IEEE Trans. Electron Devices,* vol. 35, pp. 878–886, July 1988.

[11] U. K. Mishra, A. S. Brown, and S. E. Rosenbaun, "DC and RF performance of 0.1 μm gate length $Al_{0.48}In_{0.52}As$-$Ga_{0.38}In_{0.62}As$ pseudomorphic HEMT's," in *IEDM Tech. Dig.* (San Franciso, CA), Dec. 1988, pp. 180–183.