```
1   ----------------------------------------------------------------------------------
2   -- Company:
3   -- Engineer:
4   --
5   -- Create Date: 11/30/2017 07:17:01 PM
6   -- Design Name:
7   -- Module Name: top - Behavioral
8   -- Project Name:
9   -- Target Devices:
10  -- Tool Versions:
11  -- Description:
12  --
13  -- Dependencies:
14  --
15  -- Revision:
16  -- Revision 0.01 - File Created
17  -- Additional Comments:
18  --
19  ----------------------------------------------------------------------------------
20
21
22  library IEEE;
23  use IEEE.STD_LOGIC_1164.ALL;
24
25  -- Uncomment the following library declaration if using
26  -- arithmetic functions with Signed or Unsigned values
27  --use IEEE.NUMERIC_STD.ALL;
28
29  -- Uncomment the following library declaration if instantiating
30  -- any Xilinx leaf cells in this code.
31  --library UNISIM;
32  --use UNISIM.VComponents.all;
33
34  entity top is
35    Port (
36      sw   : in std_logic_vector(7 downto 0);
37      btnR : in std_logic;
38      btnL : in std_logic;
39      clk  : in std_logic;
40
41      led  : out std_logic_vector(15 downto 0)
42    );
43  end top;
44
45  architecture Behavioral of top is
46      component debounce is
47          Port (
48                 CLK_100M : in std_logic;
49                 SW       : in std_logic;
50                 sglPulse : out std_logic;
51                 Sig      : out std_logic
52          );
53      end component;
54      signal reset, test : std_logic := '0';
55
56      signal value : std_logic_vector(7 downto 0);
57
58  begin
59
60      DEBL: debounce port map (
61          CLK_100M => clk,
62          SW => btnL,
63          sglPulse => open,
64          Sig => test
65      );
66
```

```
67          DEBR: debounce port map (
68              CLK_100M => clk,
69              SW => btnR,
70              sglPulse => open,
71              Sig => reset
72          );
73
74      --    test <= btnL;
75      --    reset <= btnR;
76
77          --led(15) <= '0';
78          led(14) <= '0';
79          led(13) <= '0';
80          led(12) <= '0';
81          led(11) <= '0';
82          led(10) <= '0';
83          led(9) <= '0';
84          led(8) <= '0';
85          led(7) <= sw(7);
86          led(6) <= sw(6);
87          led(5) <= sw(5);
88          led(4) <= sw(4);
89          led(3) <= sw(3);
90          led(2) <= sw(2);
91          led(1) <= sw(1);
92          led(0) <= sw(0);
93
94          GUESS: process (test)
95              variable led_15 : std_logic := '0';
96          begin
97              if (reset = '1') then
98                  value <= sw;
99                  led_15 := '0';
100             end if;
101
102             if (test = '1') then
103                 if (value = sw) then
104                     led_15 := '1';
105                 else
106                     led_15 := '0';
107                 end if;
108
109                 value <= value;
110             end if;
111
112             led(15) <= led_15;
113         end process GUESS;
114
115     end Behavioral;
116
```