Assignment 1:

The first part of the assignment went well, the assignment required us to implement an and gate of 2 inputs. The code simply was



The test bench was a bit harder, from reading the PowerPoint on canvas, I was able to deduce that the code must look something like this



However, this lead to very weird results, the a, b and y signals were off by one from the counter. For example, when the counter was 10, a and b were 0 and 1 respectably. I then looked at how the first (extra credit) VHDL assignment did its test bench and saw that I should have written my code like this



This test bench gave the correct results.

The second part of the assignment was very similar, Using what I learned in the first part of the assignment, I simply replicated the steps and came up with the code



And for the test bench



Assignment 2

This assignment was confusing at first, reading the assignment made me worry that we have to create the logic (using ‘and’ and ‘or’ gates) to transform the 4 bits to the 7 bits needed for the digits, however when reading the prewritten code, I realized that this could be done with a simple switch statement.



However, Vivado kept giving me a syntax error, after much googling, I realized that there must be process block surrounding the case statement like this



However, I still got an error that stated that I needed a when other statement, this was an easy fix, when we got a number other than the above 16, we would output nothing



This statement was placed after the all the when statements and before the end case statement. The test bench was very similar to part 1 of the assignments



The tb2 arbitrary and can be replaced with any name we want, as long as the both ends of the process has the same name.