INDIAN INSTITUTE OF TECHNOLOGY DELHI

ELL834

ASSIGNMENT

Assignment 2

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2021EE10137

Contents

Chapter 1

Cross Coupled Oscillator Design

1.1 Requirements

Frequency	2.4 GHz
Phase Noise @ 1 MHz	< -100 dBc/Hz
Tuning Range	Greater than 2.3 GHz to 2.5 GHz
Technology Node	Any
Inductor Q	10

Table 1.1: Requirements for the Cross Coupled Oscillator

1.2 Design

1.2.1 Preliminaries

Suppose we assume a Power Budget, $P = 3$ mW and rail voltage $V_{DD} = 1.2$ V. Then $P = V_{DD}I_{SS}$, so

$$\boxed{I_{ss} = \frac{P}{V_{DD}}}$$

For M1 to be in saturation throughout-

$$\begin{aligned} V_G - V_{th} &\leq V_D \\ V_G - V_D &\leq V_{th} \\ V_Y - V_X &\leq V_{th} \\ 2v_{y,pk} = v_{y,pk-pk} &\leq V_{th} \end{aligned}$$

$$\therefore v_{x,pk-pk} = v_{y,pk-pk} \leq V_{th}$$

Now,

$$\frac{4}{\pi} I_{ss} \frac{R_p}{2} = v_{x,pk-pk} = V_{th} \text{ for maximum swing}$$

$$\boxed{R_p = 2 * \frac{\pi V_{th}}{4 I_{SS}}}$$

Further,

$$Q = \frac{R_p}{L\omega_0}$$

$$\boxed{L = \frac{R_p}{2\pi f_0 Q}}$$

Also,

$$2\pi f_0 = \frac{1}{\sqrt{2LC}} \implies C = \frac{1}{2L(2\pi f_0)^2}$$

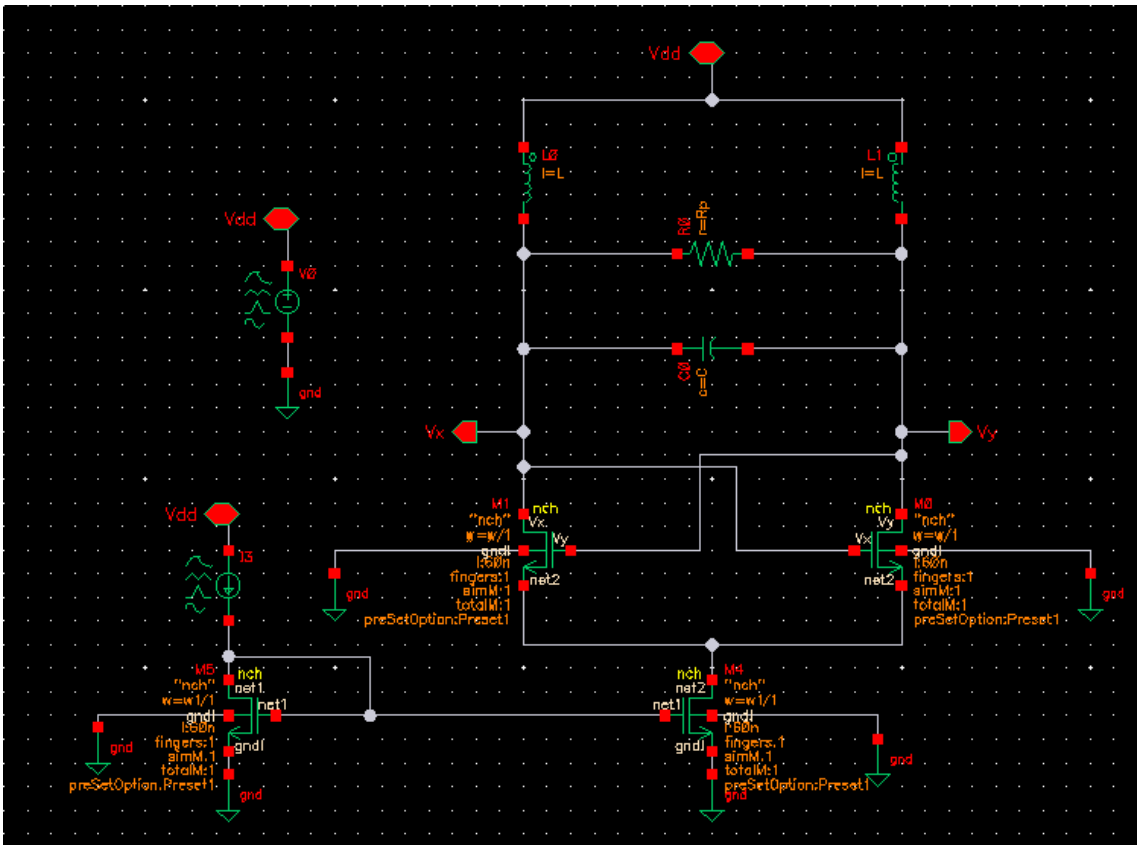

Figure 1.1: Schematic (w: width of differential NMOS, w1: width of current mirror NMOS)

$\frac{W}{L}$ is decided such that I_D swings between 0 and tail current value.

1.2.2 Oscillator at 2.5 GHz

We design the oscillator for 2.5 GHz initially so that on increasing the capacitance using the Cap. bank and varactor leads to increase in capacitance and therefore decrease in frequency. After some simulations, we use the following values-

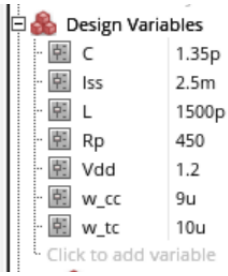

Figure 1.2: Design Variables

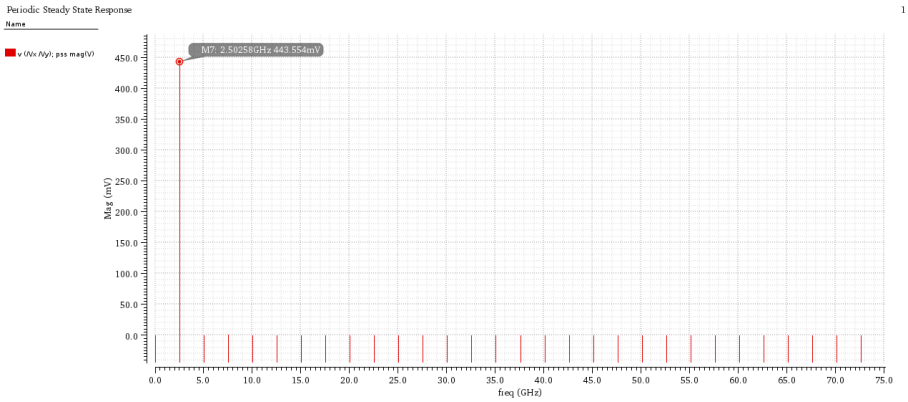

Figure 1.3: Differential Output Frequency Spectrum, peak at 2.5 GHz

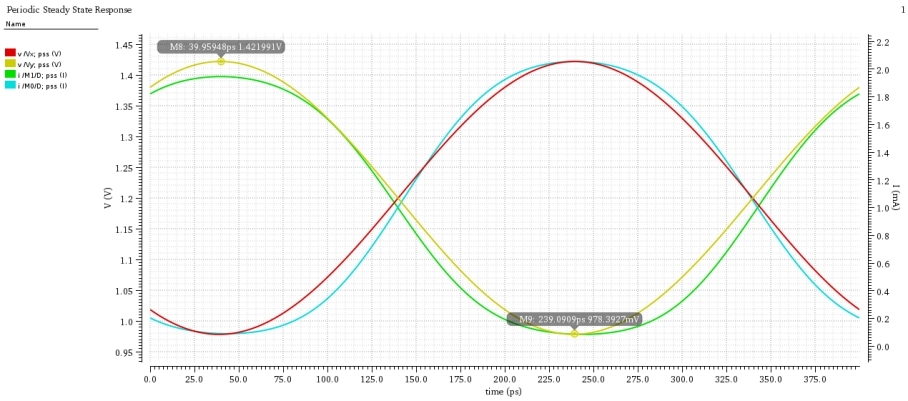

Figure 1.4: Transient Outputs

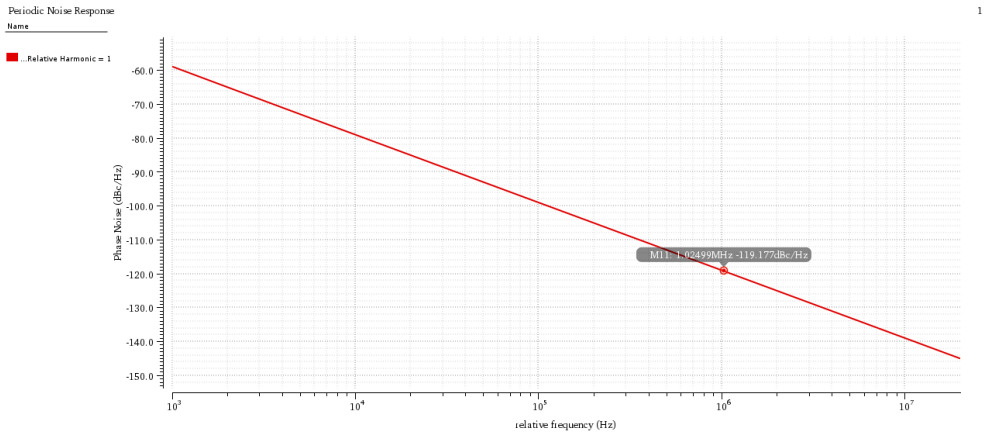

Figure 1.5: Phase Noise

1.2.3 Frequency Tuning

For $f_0 = 2.5$ GHz and $L = 1500$ pH

$$2\pi f_0 = \frac{1}{\sqrt{2LC}} \implies C = \frac{1}{2L(2\pi f_0)^2} \implies C_{min} = 1.35 \text{ pF}$$

For $f_0 = 2.3$ GHz and $L = 1000$ pH

$$2\pi f_0 = \frac{1}{\sqrt{2LC}} \implies C = \frac{1}{2L(2\pi f_0)^2} \implies C_{max} = 1.60 \text{ pF}$$

This range of capacitance is achieved using capacitor banks (discrete tuning) and varactors (continuous tuning).

$$\Delta C = 0.25 \text{ pF} = 250 \text{ fF}$$

Suppose we use an n-bit Cap-bank with capacitance range $0 \rightarrow (2^n - 1)C_{lsb}$
and Varactor with capacitance range $C_{min} \rightarrow C_{min} + \Delta C_{var}$
Then we have,

$$C_{max} - C_{min} = \Delta C_{var} + (2^n - 1)C_{lsb}$$

For continuous frequency range- $\Delta C_{var} \geq C_{lsb}$
Therefore,

$$\Delta C_{var} = C_{lsb} = \frac{\Delta C}{2^n}$$

Varactor Design

For n = 5 bits, $C_{lsb} = 7.8$ fF. For w = 60u, $\Delta C_{var} = 8.4$ fF.

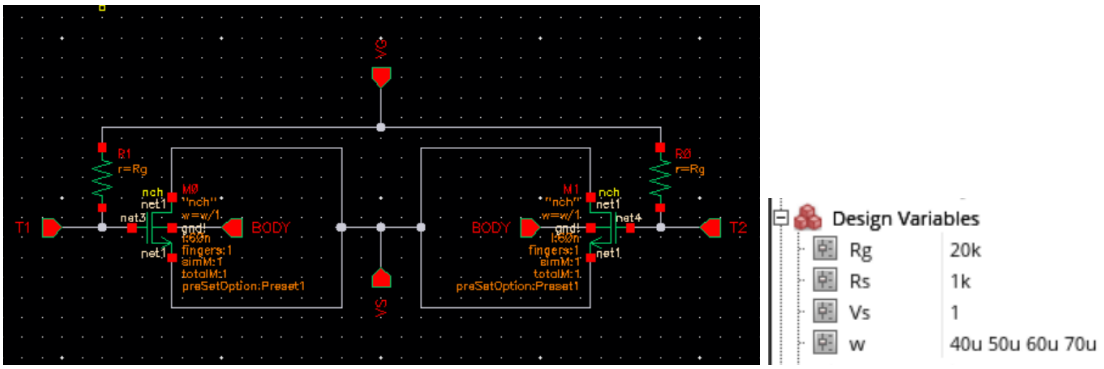

Figure 1.6: Varactor Block

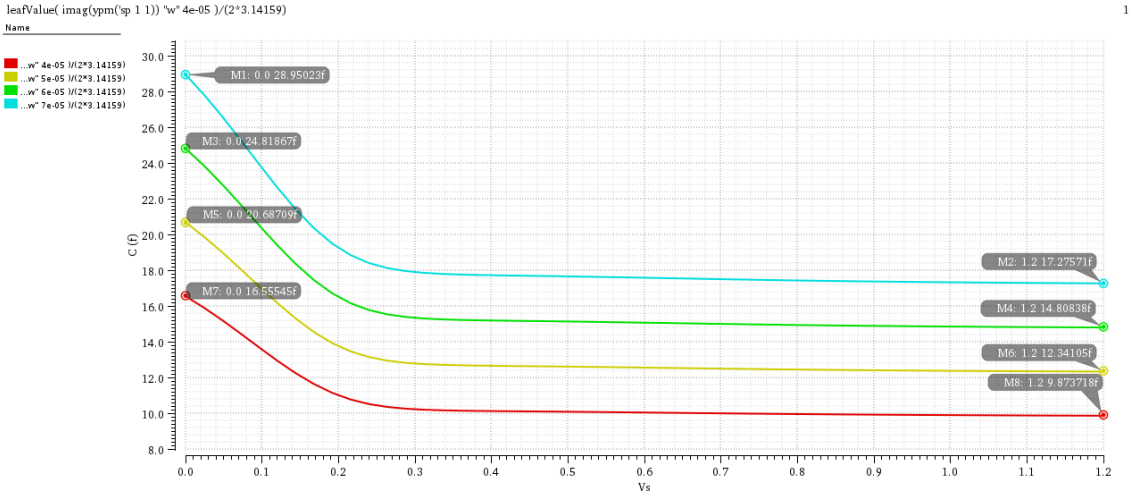

Figure 1.7: Varactor Capacitance vs V_{ctrl} using sp analysis for width 40u to 70u

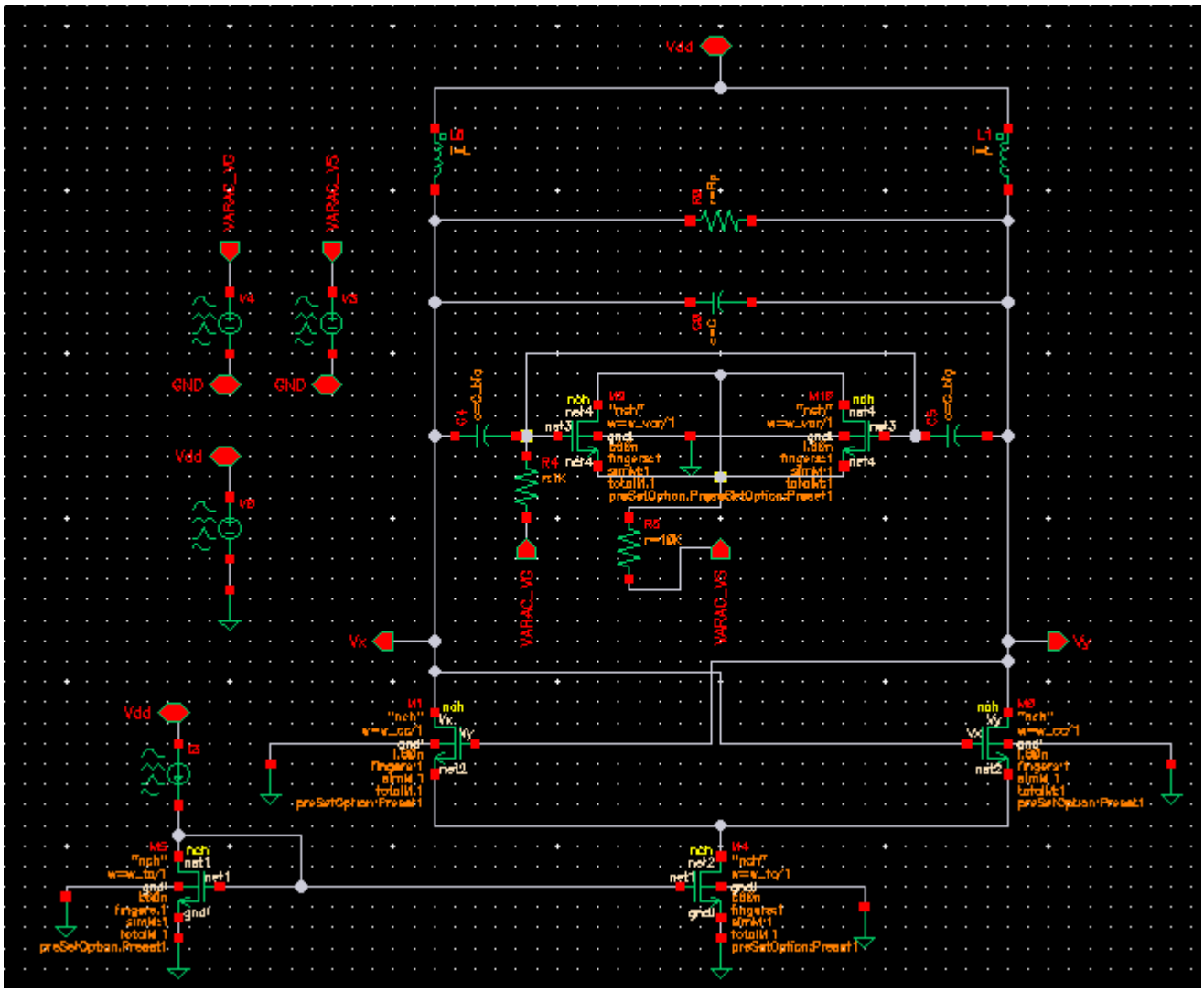

Figure 1.8: Circuit with Varactor

1.3 Performance

Specification	Value
Technology	60 nm
DC Power	3 mW
Frequency Range	
FTR	
PN@1MHz	-119.177 dBc/Hz
FoM@1MHz	182.01
FoMT@1MHz	

Table 1.2: Performance Table

Where[1],

$$\text{FoM} = |\text{PN}| + 20\log\left(\frac{f_0}{\Delta f}\right) - 10\log_{10}\left(\frac{\text{Pdc (mW)}}{1\text{mW}}\right)$$

$$\text{FoMT} = |\text{PN}| + 20\log\left(\frac{f_0}{\Delta f}\right) - 10\log_{10}\left(\frac{\text{Pdc (mW)}}{1\text{mW}}\right) + 20\log\left(\frac{\text{FTR}}{10}\right)$$

$$\text{FTR} = \left[\frac{(f_{\max} - f_{\min})}{f_c}\right] \times 100\%; \quad f_c = \frac{(f_{\max} + f_{\min})}{2}$$

[1] Cap. bank could not be designed, so blanks could not be filled

Chapter 2

Ring Oscillator Design

2.1 Requirements

Frequency	2.4 GHz
Phase Noise @ 1 MHz	< -80 dBc/Hz
Tuning Range	Greater than 2.3 GHz to 2.5 GHz
Technology Node	Any

Table 2.1: Requirements for Ring Oscillator

2.2 Design

2.2.1 Oscillator at 2.4 GHz

Initially we use L = 129 nm.

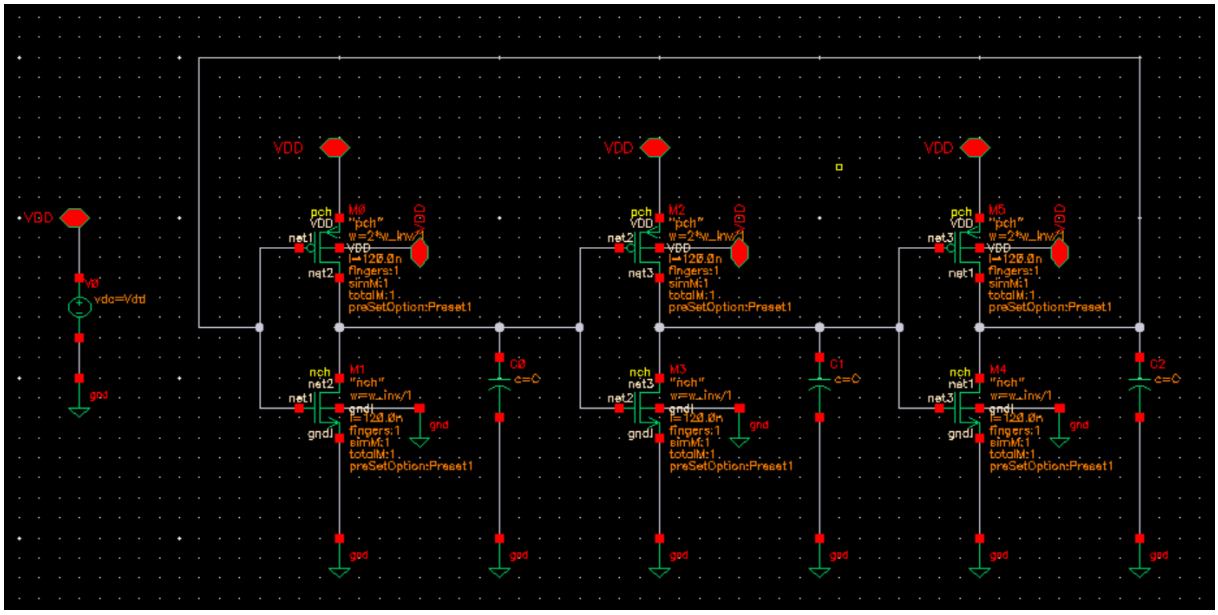

Figure 2.1: Schematic

$$T_{delay} = CV_{DD}/I_{DD}$$
$$f_0 \propto 1/C$$

However, the PN requirement is not fulfilled.
Increase L to 150nm.

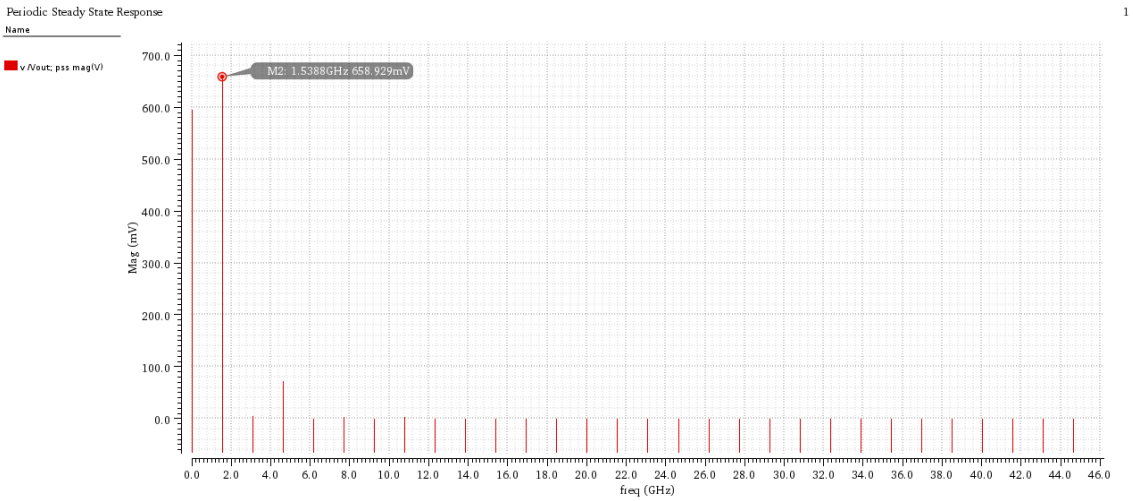

Figure 2.2: For C = 8 fF, therefore need to reduce C

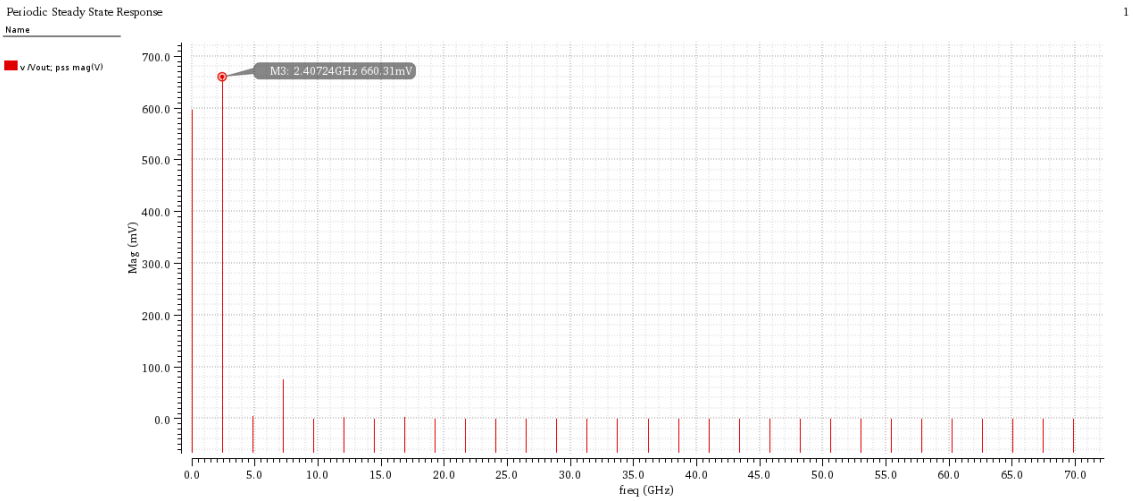

Figure 2.3: Oscillator at 2.4 GHz (C=4.5 fF)

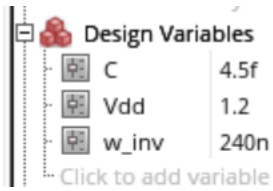

Figure 2.4: Design Parameters for 2.4 GHz

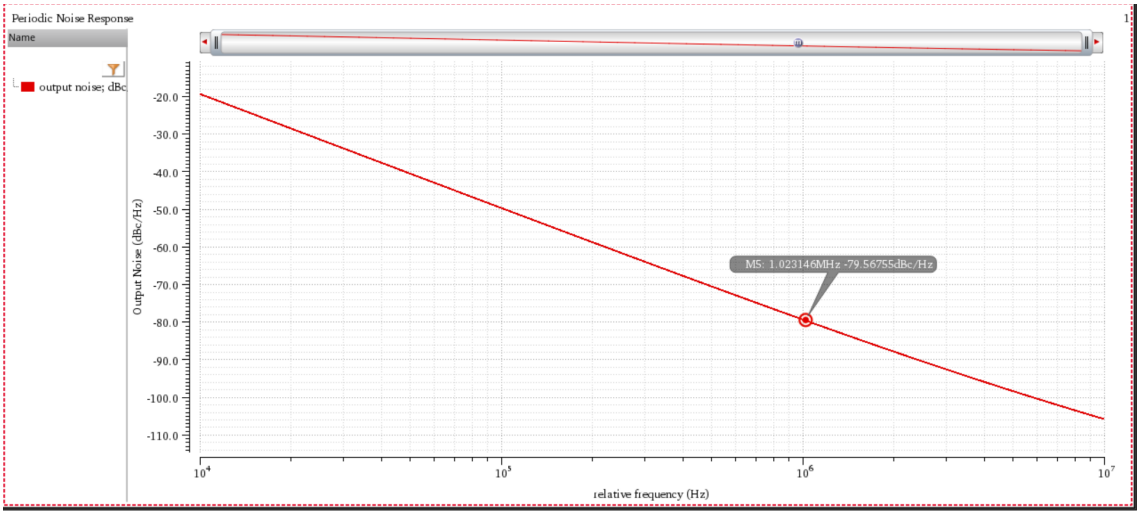

Figure 2.5: Phase Noise is more than -80 dBc/Hz (C=4.5 fF)

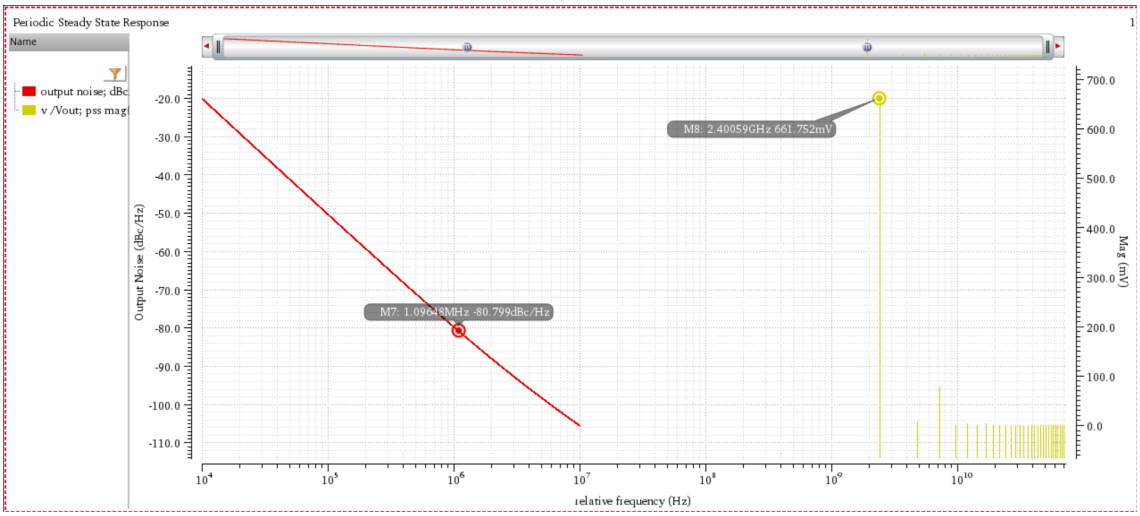

Figure 2.6: PN and PSS spectrum for L = 150 nm and C = 3.4 fF

2.3 Performance

Specification	Value
Technology	60 nm
DC Power	19.92 μ V
Frequency Range	
FTR	
PN@1MHz	-80.8 dBc/Hz
FoM@1MHz	165.4
FoMT@1MHz	

Table 2.2: Performance Table

Where[1],

$$\text{FoM} = |\text{PN}| + 20\log\left(\frac{f_0}{\Delta f}\right) - 10\log_{10}\left(\frac{\text{Pdc (mW)}}{1\text{mW}}\right)$$

$$\text{FoMT} = |\text{PN}| + 20\log\left(\frac{f_0}{\Delta f}\right) - 10\log_{10}\left(\frac{\text{Pdc (mW)}}{1\text{mW}}\right) + 20\log\left(\frac{\text{FTR}}{10}\right)$$

$$\text{FTR} = \left[\frac{(f_{\max} - f_{\min})}{f_c}\right] \times 100\%; \quad f_c = \frac{(f_{\max} + f_{\min})}{2}$$

[1]Tuning not be designed, so blanks could not be filled