Marwadi University
Faculty of Technology
Department of Information and Communication Technology

Subject Code: 01CT1514

Subject Name: VLSI Design

B. Tech. – Year – III (Semester V)

Objectives: The objective of this course is to introduce students with various concepts and methods of digital system design techniques. To acquire knowledge of MOS Transistor, understand CMOS Fabrication process and learn the design of CMOS Logic circuits and subsystems. Learning this course would improve the employment potential of students in VLSI and Semiconductor industry.

Credits Earned: 04 Credits

Course Outcomes: After completion of this course, student will be able to:

1. Acquire basics of VLSI design flow, design methodologies, design quality, design for manufacturability and testability (Apply)
2. Develop fundamentals in fabrication of MOSFETs and MOS transistor (Understand)
3. Analyze MOS inverters with its static and switching characteristics (Analyze)
4. Analyze combinational and sequential MOS logic circuit (Analyze)
5. Acquire basic concepts of low power CMOS logic circuits (Apply)

Pre-requisite of course: Elementary knowledge about Electronics including some experience of circuit designing and logic development. Fundamentals of Computer Programming & Utilization. Basic knowledge of digital electronics and real-life digital systems.

Teaching and Examination Scheme:

Teaching Scheme (Hours)			Credits	Theory Marks			Tutorial / Practical Marks		Total Marks
				E	I		V	T	
Theory	Tutorial	Practical		ESE	IA	CSE	Viva	Term Work	
3	0	2	4	50	30	20	25	25	150

Contents:

Unit	Topics	Contact Hours
1	**Introduction** Overview of VLSI design methodology, VLSI design flow, Design hierarchy, Concept of regularity, Modularity, and Locality, VLSI design style, Design quality, package technology, introduction to FPGA and CPLD, computer aided design technology.	3

2	**Fabrication of MOSFET** Introduction, Fabrication Process flow: Basic steps, Wafer formation, Photolithography, Gate oxide, gate and drain formation and Contacts and Metallization. nMOS Fabrication. C-MOS n-Well Process, Layout Design rules, full custom mask layout design.	5
3	**MOS Transistor Theory** Introduction and I-V Characteristics, Non ideal I-V effects: Velocity saturation, mobility degradation and Channel length modulation. Non ideal I-V effects: Body Effect, Sub threshold conduction, Junction leakage, MOSFET scaling and small geometry effects.	8
4	**MOS Inverters** Introduction, Resistive load inverter, Inverters with n-type MOSFET load, CMOSInverter, Propagation delay, Interconnect delay, switching power dissipation of inverter	7
5	**Combinational and Sequential CMOS Logic Circuits** MOS logic circuit with depletion load, CMOS logic circuits, Complex logic circuit, pass transistor circuits, CMOS with transmission gate, Multiplexer and XOR gate using CMOS transmission gate, Level sensitive latches and edge triggered flip flops.	8
6	**Chip I/P and O/P Circuits** ESD protection, Input circuits, Output circuits, On chip Clock Generation and Distribution, Latch –Up and its Prevention	2
7	**Low-power CMOS logic circuits** Introduction, Overview of Power Consumption, Low power design, Leakage power dissipation, Reduction in switching activity, Gated clock signals	4
8	**Design for manufacturability** Introduction, Process variations, Basic concepts and definitions	2
9	**Design for Testability** Introduction, Fault types and models, Controllability and observability, Various techniques to identify the faults.	3
	Total Hours	42

Suggested Text books / Reference books:

1. Sung Mo Kang,Yusuf Leblebici, “CMOS Digital Integrated Circuits Analysis and Design”, TataMcGraw Hill, 3rd Edition, 2003.
2. Neil H.E.Weste, David Harris, “CMOS VLSI Design”, Pearson,3rd Edition. 2005, Reprint, 2012.
3. Douglas A. Pucknell, Kamran Eshraghian,“Basic VLSI Design”, Prentice Hall of India, 3rdEdition, Reprint 2009.
4. John P. Uyemura, “Introduction to VLSI circuits and systems”, Wiley, 2rd Edition 2002, Reprint2014.

Suggested Theory distribution:

The suggested theory distribution as per Bloom's taxonomy is as per follows. This distribution serves asguidelines for teachers and students to achieve effective teaching-learning process.

Distribution of Theory for course delivery and evaluation					
Remember	Understand	Apply	Analyze	Evaluate	Create
15%	15%	4%	10%	10%	10%

Suggested List of Experiments:

1. Introduction to SPICE tool.
2. Develop the current-voltage characteristics of NMOS transistor.
3. Develop the current-voltage characteristics of PMOS transistor.
4. Implement NAND gate using CMOS transistors and simulate the design.
5. Implement NOR gate using CMOS transistors and simulate the design.
6. CMOS implementation of XOR and XNOR gate. Simulate the design.
7. Draw CMOS inverter and simulate the design with input and output waveforms.
8. Draw the layout of NAND and NOR gate and simulate the design.
9. Draw the layout of AND and OR gate and simulate the design.
10. Implement the 2x1 MUX using Transmission gate and simulate the design.
11. Develop layout of CMOS inverter and simulate it.
12. Measure propagation delay of CMOS inverter.
13. Develop the D-latch using CMOS transmission gate and simulate it.
14. Develop the edge triggered D flip flop and simulate it.

Major Equipment/software: SPICE Circuit simulator

List of Open-Source Software/learning website: NPTEL, LTSPICE Spice circuit simulator

Instructional Method:

1. Course delivery is combined use of white board/black board and power point presentation usingprojector as per requirement.
2. Students will be assessed with continuous evaluation approach with assignments and quizzes atregular interval.
3. For effective communication with students, canvas LMS (Learning Management System) is used.

Supplementary Resources:

1. NPTEL Videos on CMOS VLSI Design
2. https://nptel.ac.in/courses/108/107/108107129

3. https://nptel.ac.in/courses/117/101/117101058/
4. https://nptel.ac.in/courses/117/101/117101004
5. http://ece-research.unm.edu/jimp/vlsi