Subject Code: 01CT0301

Subject Name: Computer Organization and Architecture

B. Tech. Year – II (Semester III)

Objective: To conceptualize the concepts of organizational and architectural issues of a digital computer. Further, analyze performance issues in processor and memory design of a digital computer. Also, understanding various data transfer techniques in digital computer and to analyze processor performance improvement using instruction level parallelism.

Credits Earned: 04 Credits

Course Outcomes: After completion of this course, student will be able to:

1. Apply knowledge of the processor's internal registers and operations by use of a PC based microprocessor simulator (Apply).
2. Understand and describe the basics of various architectural units of the computer system (Understand).
3. Apply the knowledge of combinational and sequential logical circuits to mimic a simple computer architecture (Apply).
4. Analyze various features of microprocessor, memory and I/O devices including concepts of system bus (Analyze).
5. Write assembly language programs and download the machine code that provides solution to real-world control problems (Apply).
6. Analyze the importance of parallelism and stall in computer architecture (Analyze).

Pre-requisite of course: Digital Electronics

Teaching and Examination Scheme:

Teaching Scheme (Hours)			Credits	Theory Marks			Tutorial / Practical		Total Marks
				E	I		V	T	
Theory	Tutorial	Practical		ESE	IA	CSE	Viva	Term Work	
3	0	2	4	50	30	20	25	25	150

Contents:

Unit	Topics	Contact Hours
1	**Introduction to Computer Architecture:** Basic computer data types, instruction codes, instruction cycle, computer registers, computer instructions, timing and control, memory-reference instructions, input-output and interrupt, complete computer description, design of basic computer	06
2	**Introduction to Computer Organization:** Instruction codes, computer registers, computer instructions, timing and control, instruction cycle, memory-reference instructions, input-output andinterrupt, complete computer description.	05
3	**Fundamentals of Micro programmed Control:** Control Memory, Address sequencing, Micro program Example, design ofcontrol Unit	04
4	**Concepts of Central Processing Unit:** Introduction, general register organization, stack organization, instruction format, addressing modes, data transfer and manipulation,program control, reduced instruction set computer (RISC)	07
5	**Computer Arithmetic:** Introduction, addition and subtraction, multiplication algorithms (booth multiplication algorithm), division algorithms, floating point arithmetic operations, decimal arithmetic unit.	07
6	**Introduction to Pipeline:** Flynn's taxonomy, parallel processing, pipelining, arithmetic pipeline,instruction, pipeline, RISC Pipeline	04
7	**Input-Output Organization:** Input-output interface, asynchronous data transfer, modes of transfer, DMA, input - output processor (IOP) priority interrupt, CPUIOP communication, serial communication.	05
8	**Memory Organization:** Memory hierarchy, main memory, auxiliary memory, associativememory, cache memory, virtual memory.	04
	TOTAL HOURS	**42**

Suggested Text books / Reference books:

1. M. Morris Mano, Computer System Architecture, Pearson 3e, 1992.
2. Andrew S. Tanenbaum and Todd Austin, Structured Computer Organization, PHI, 6e, 2016.
3. M. Murdocca & V. Heuring, Computer Architecture & Organization, WILEY, 2007.
4. John Hayes, Computer Architecture and Organization, McGraw Hill, 1998.

Suggested Theory distribution:

The suggested theory distribution as per Bloom's taxonomy is as per follows. This distribution serves as guidelines for teachers and students to achieve effective teaching-learning process.

Distribution of Theory for course delivery and evaluation					
Remember	Understand	Apply	Analyze	Evaluate	Create
20%	20%	30%	15%	10%	05%

Suggested List of Experiments:

1. Introduction to 8085 Microprocessor Trainer board with explanation of necessary hardware connection with microprocessor.
2. Data Transfer (Copy) Operations
    a. Write the data 41h into register C and copy it to Accumulator
    b. Load Register H with 34h and Register L with ABh.
    c. Copy 32h in all the Registers.
    d. Load accumulator with the content of memory whose address is D000h using three different techniques.
    e. Exchange the content of memory location D000h and D001h using direct addressing and indirect addressing.
3. Arithmetic Operations
    a. Load Register B and C with 55h and 66h. Add Register B, C and store the result in Register D.
    b. Add two 16-bit numbers with and without using DAD. (HL+BC and store the answer in HL)
    c. Add the content of memory location D000h, D001h and store the result at memory locations D040h and D041H.
    d. Transfer the array (3 byte) of data starting from D000h to the locations starting from D050h by memory pointer with and without LDA/STA.
    e. Subtract two 16-bit numbers. (HL-BC and store answer in HL)

4.
    a. Assume register B holds 93h and the accumulator holds 15h. Illustrate the result of instruction ORA B, XRA B and CMA.
    b. Load the data byte 8EH in register D and F7H in register E. Mask the higher order bits (D7-D4) from both the data bytes.
5. Write an assembly language program to generate time delay using following three different approaches. No need to generate specific delay. You can load the value of your choice.
    a. Using a simple Register
    b. Using Register Pair
    c. Using loop within a loop
6. Write an assembly language program to count from 0 to 9(modulo 10 counter) with some delay between each count. Also display the count at output port 00H. At the count of 9 the counter should reset to 0 and repeat the sequence continuously.
7. Write an assembly language program to clear all the flag bits in flag register. Use the concept of PUSH and POP instruction to demonstrate this task. Load the accumulator with 00H. Logically OR the accumulator with itself to set zero flag and display flag bits on port 01H.
8. Write an assembly language program to convert a BCD number into Binary. Assume any two-digit number of your choice as an input BCD number.
9. Write an assembly language program to convert a binary number into un-packed BCD number.

    (Assume any binary number available in memory).
10. Write an assembly language program to convert a packed BCD number into seven segment code and display. Use common cathode type seven segment display. Assume the packed BCD number is available in memory.
11. Write an assembly language program to multiply two 8-bit numbers stored in Register A & Register B.
12. Write an assembly language program to divide two 8-bit numbers stored in Register A & Register B.
13. Write an assembly language program to find out largest number from given array stored at 5 consecutive memory locations starting from C030H and store the result to memory location C040h.
14. Write an assembly language program to find out smallest number from given array stored at 5 consecutive memory locations starting from C030H and store the result to memory location C040h.

Instructional Method:

1. The course delivery method will depend upon the requirement of content and need of students. The teacher in addition to conventional teaching method by black board, may also use any of tools such as demonstration, role play, Quiz, brainstorming, MOOCs etc.
2. The internal evaluation will be done on the basis of continuous evaluation of students in the laboratory and class-room.

3. Students will use supplementary resources such as online videos, NPTEL videos, e-courses, Virtual Laboratory

Supplementary Resources:

1. https://www.javatpoint.com/computer-organization-and-architecture-tutorial
2. https://www.geeksforgeeks.org/computer-organization-and-architecture-tutorials/
3. https://nptel.ac.in/courses/106/103/106103068/
4. https://tutorialspoint.dev/computer-science/computer-organization-and-architecture
5. https://www.studytonight.com/computer-architecture/