Unit - 5

Pentium Processor

Pentium is one of the powerful family member of Intels X86 microprocessor.

It is an advanced Superscalar 32-bit microprocessor, introduced in the year 1993 that contains around 3.1 million transistors.

It has a 64-bit data bus and 32-bit address bus that offers 4Gb of physical memory space.

The advanced of pentium processor is pentium pro

A Special category of microprocessor that involves a parallel approach for instruction execution

More than one instruction gets executed in one clock cycle is called as Superscalar processor

The Superscalar processor uses the approach of simultaneously executing two instructions in one clocks cycle.

Architecture of Pentium :-

Bus unit of the architecture send the control signal and fetches code & data from external memory & I/o devices.

Paging unit

Code cache in order to load the instructions into the execution unit, fetching the instruction in a sequential manner

Branch target buffer & Prefetch buffer operates together ↓ hold the respective address

TLB (translation look aside buffer) converts linear address into the physical address

The pentium family of processors originated from the 80486 microprocessor. The term "Pentium processor" refers to a family of microprocessor that share a common architecture and instruction set. It runs at a clock frequency of either 60 (or) 66 MHz and has 3.1 million transistors. Some of the features of pentium architecture are:

Complex instruction set computer (CISC) architecture with reduced instruction set computer (RISC) performance

64-Bit Bus

Upward code compatibility

Pentium processor uses superscalar architecture and hence can issue multiple instructions per cycle

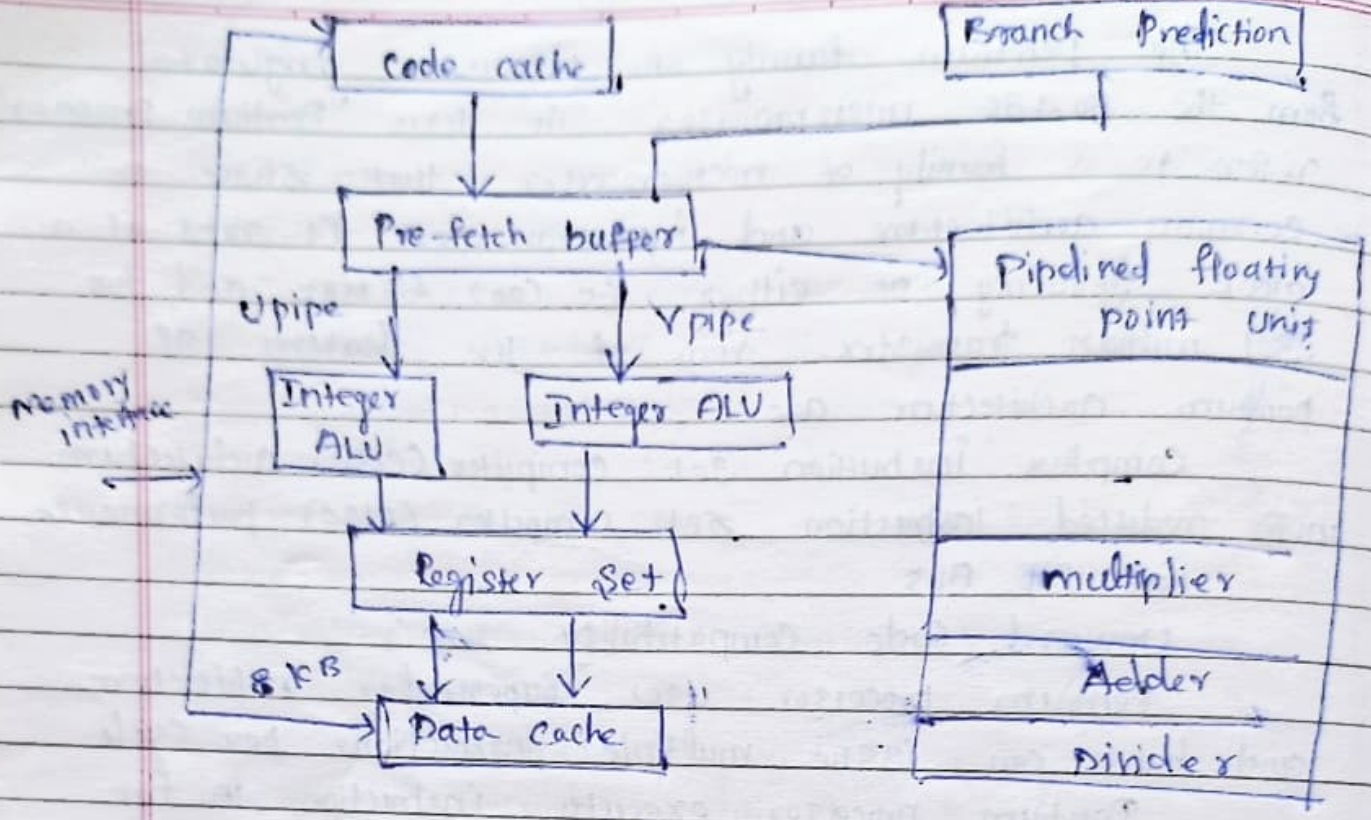
Pentium procesor executes instruction in five stages. This staging, (or) pipelling allows the processor to overlap multiple instructions so that it take less time to execute two instructions in a row.

The pentium processor fetches the branch target instruction before it executes the branch instruction.

The pentium processor has two separate 8-KB caches on chip, one for instructions and one for data. It allows the pentium processor to fetch data & instructions from the cache simultaneously.

When data is modified, only the data in the cache is changed. Memory data is changed only when the pentium processor replaces the modified data in the cache with a different set of data.

The pentium processor has been optimized to run critical instructions in fewer clock cycles than the 80386 processor.



Architecture Of Pentium.

The pentium processor has two primary operating modes

1) Protected mode
2) Real mode

*i) Memory System of Pentium:-

The pentium processor has a memory space of 4GB (2^{32} bytes)

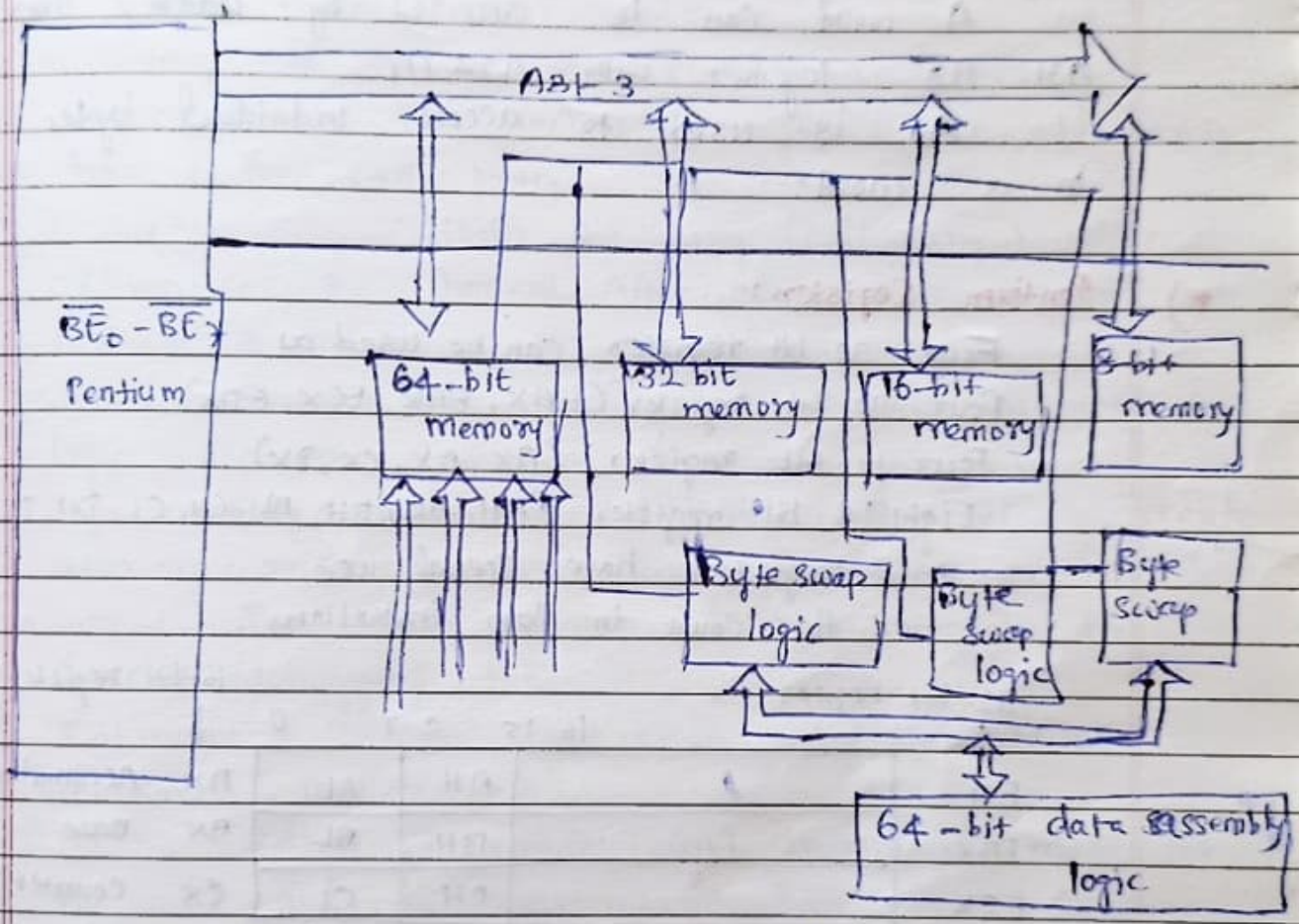
Has separate I/O space with 64KB of addressable locations

The memory space is organized as a sequence of 64-bit quantities

Each 64-bit locations has eight individually addressable bytes at consecutive memory address.

The I/O space is organized as sequence of 32 bit quantities.

Each 32 - bit quantity has four individually addressable byte at consecutive memory address.



64 bit memories are organized as array of quad words. Quadwords begin at address evenly divisible by 8.

Address line A31-A3 are used to access quadwords & $\overline{BE7}$ - $\overline{BE0}$ are used to access individual bytes coinbin o quadcoord.

32 bit memories are organized as array of dwords (block of 4 bytes)

Dwords begins at addresses evenly divisible by 4.

A Dwords can be accessed by address line A31 - A32.

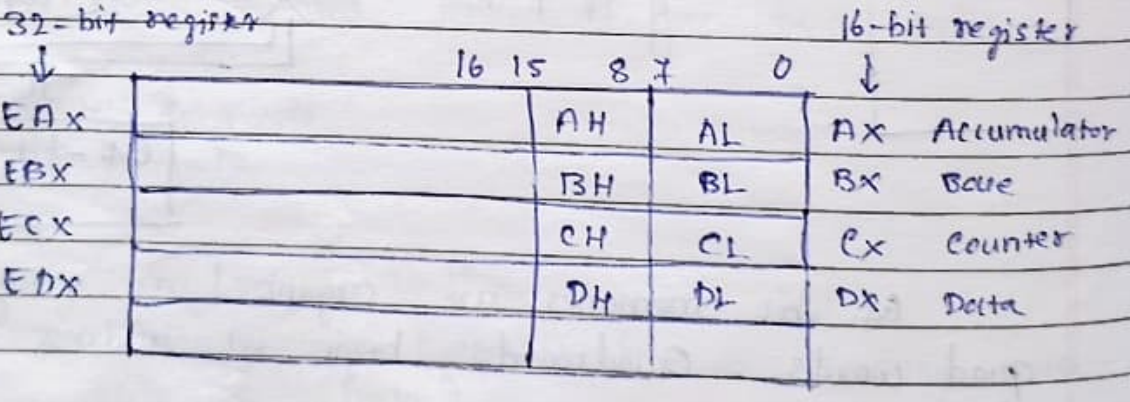
16 bit memories are organized as array of words (words is block of 2 bytes) words begin at addresses evenly divisible by 2.

A word can be accessed by address lines $A_{31} - A_3$ together with A_2 & A_1.

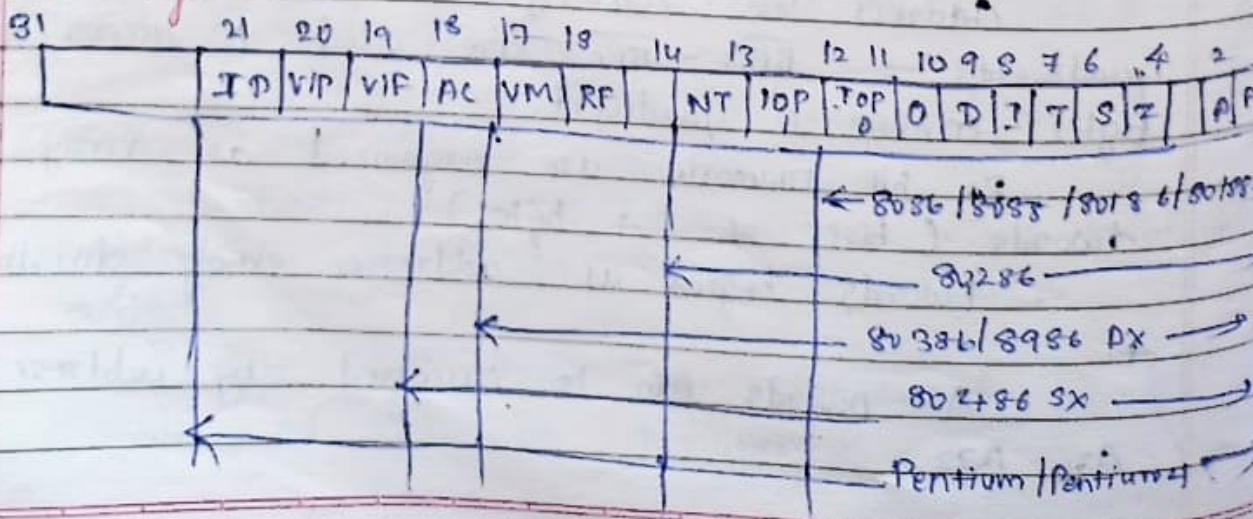
A_0 is used to access individual bytes in a word.

*) Pentium Registers :-

Four 32-bit registers can be used as
Four 32-bit register (EAX, EBX, ECX, EDX)
Four 16-bit register, (AX, BX, CX, DX)
Eight 8-bit register (AH, AL, BH, BL, CH, CL, DH, DL)
Some registers have special use
ECX for count in loop instructions.



E flags :-



Flag bits with a brief description of function.

→ C(carry) Holds the carry after addition (or) borrow after Subtraction
also indicates error conditions

→ Parity is the count of ones in a number. expressed as even (or) odd. Logic 0 for odd parity; logic 1 for even parity

→ Auxillary carry: Holds the carry (half carry) after addition (or) the borrow after Subtraction between bit positions 3 and 4 of the result

Zero :- Shows that the result of an arithmetic (or) logic operation is zero

Sign :- Flag holds the arithmetic sign of the result after an arithmetic (or) logic instruction executes

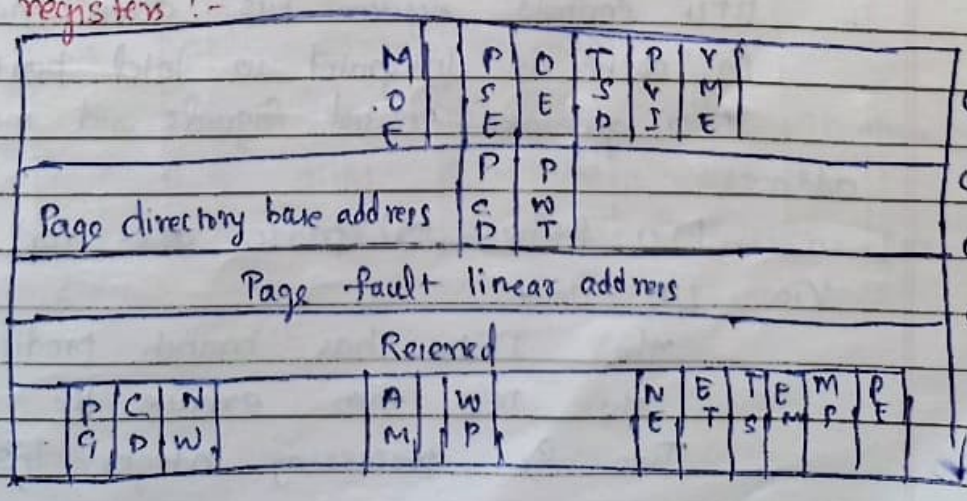
Trap :- The trap enables trapping through an on-chip debugging time

Interrupt :- Controls operation of the INTR (interrupt request pin)

D :- Selects increment (or) decrement mode for the DI and SI registers

Overflow :- occurs when signed numbers are added (or) Subtracted

Control registers :-



CD Cache disable controls the internal cache. If CD=1, the cache will not fill the new data. If CD=0 misses will cause the cache to fill with new data.

If NW=1, the data cache is inhibited from cache write though.

*) Pentium Memory Management :-

*) Pentium Pro architecture :-

5ith gen x86 microprocessor introduced in November 1, 1995.

Successor of intel pentium microprocessor capable of dual & qual processor configuration

36 bit address bus supports up to 64GB memory, 256 (or) 512KB L2 cache, 16KB L1 cache

Pipeline is divided into 3 sections

fetch and decode unit, dispatch and execution unit & retire unit

Intel pentium pro microprocessor takes CISC instructions and converts them into RISC micro operation.

The system bus connects to L2 cache

- BIU controls system bus access via L2 cache

L2 cache is integrated in intel pentium pro

BIU generates control signals and memory address.

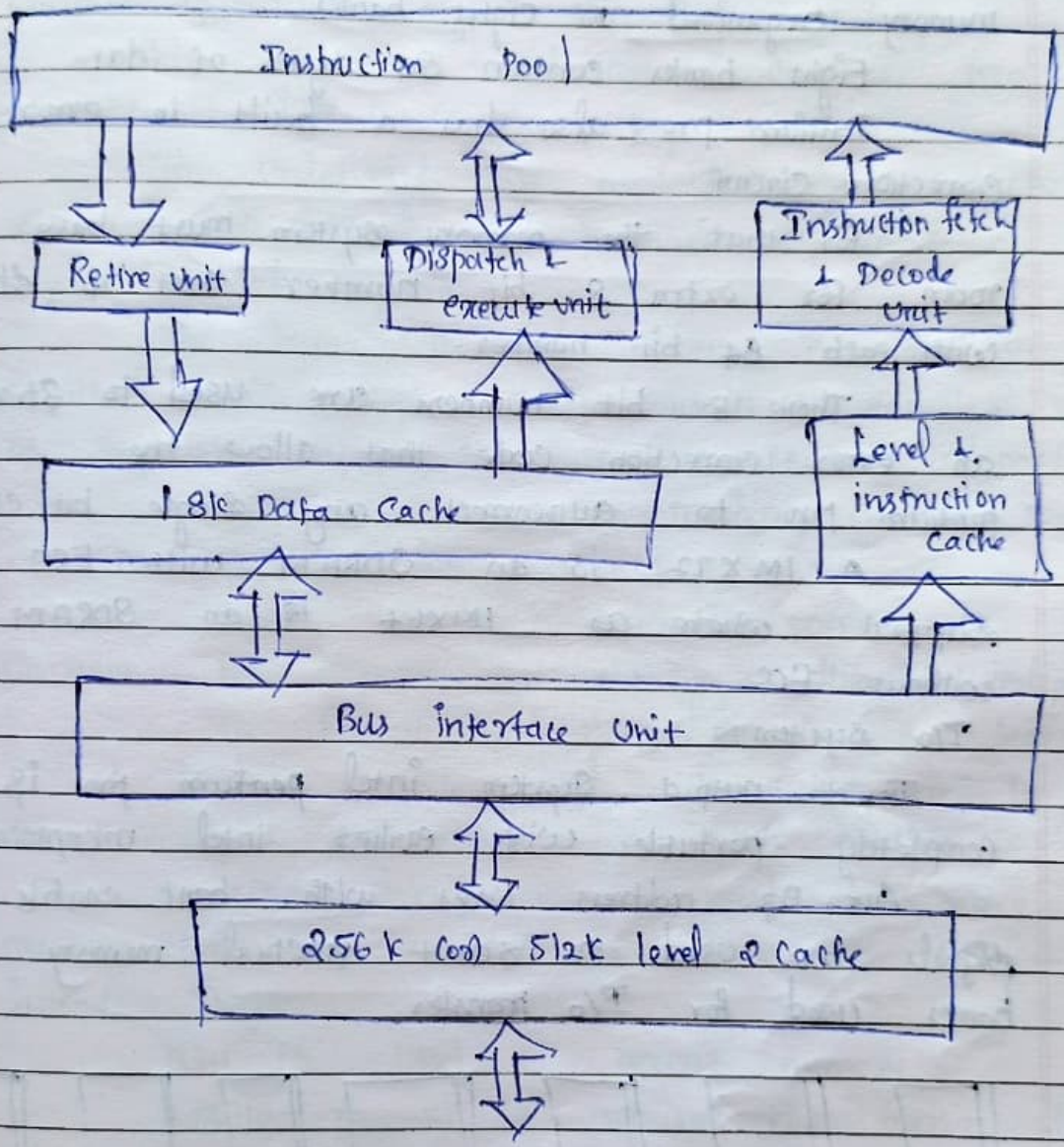
BIU fetches (or) passes data (or) instruction via L1 cache.

the IFU has branch prediction logic

The DEU then execute the instructions

Two for processing integer instruction

and one for processing floating point instruction simultaneously



- Lastly RU checks the instruction pool & removes decoded instructions that have been executed
- RU can remove three decoded instructions per clock pulse

*) The Memory System:- (Pentium Pro)

Pentium pro uses 64 bit data bus to address memory organized in eight banks.

Eight banks contain 8G bytes of data.

Pentium pro also has a built in error correction circuit.

For that the memory system must have room for extra 8 bit number that is stored with each 64 bit number.

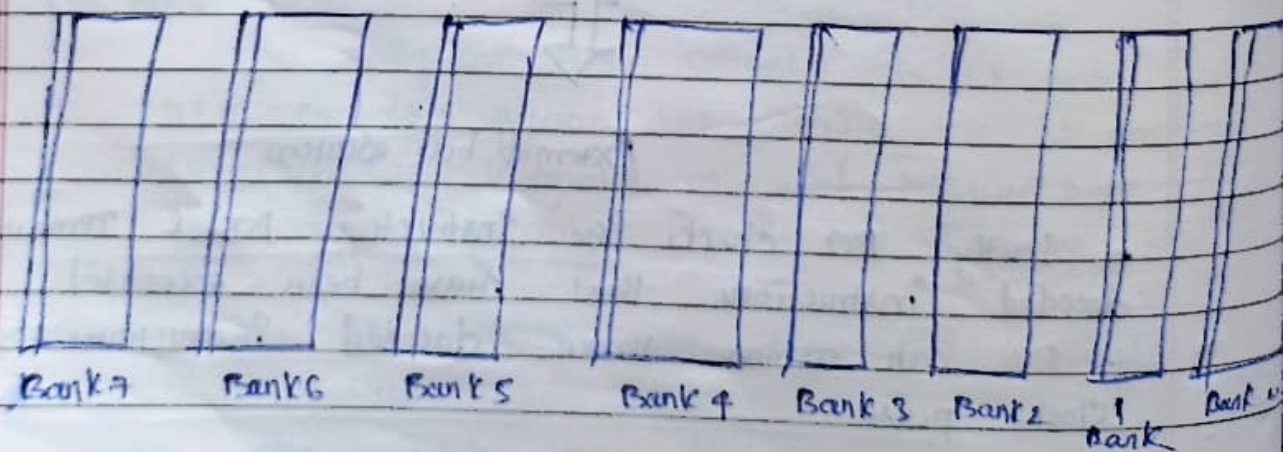
These 8 bit numbers are used to store an error correction code that allow the pentium pro to autocorrect any single bit error.

A 1MX72 is an SDRAM with ECC support where as 1MX64 is an SDRAM without ECC.

I/O System :-

Input output System intel pentium pro is completely portable with earlier intel microprocessor

A15 - A3 address lines with bank enable signals are used to select practical memory banks used for I/O transfer.



Eight bit memory banks in penticum pro

Hyper Threading Technology:-

The most recent innoration and new to the pentium is called hyper threading technology.

This significant advancement combines two microprocessor into a single package.

To understand this new technology, which shows a traditional dual processor system & a hyper-threaded system.

The hyper-threaded processor contains two execution units that each contain a complete set of registers capable of running software independently.

There two separate machine contexts share a common bus interface unit.

During machine operation on each processor is capable of running a thread independently

The bus interface unit contains the level 2 and level 3 caches and the interface to the memory & I/O structure of the machine.

When microprocessor needs to access memory (or) I/O it must store the bus interface unit

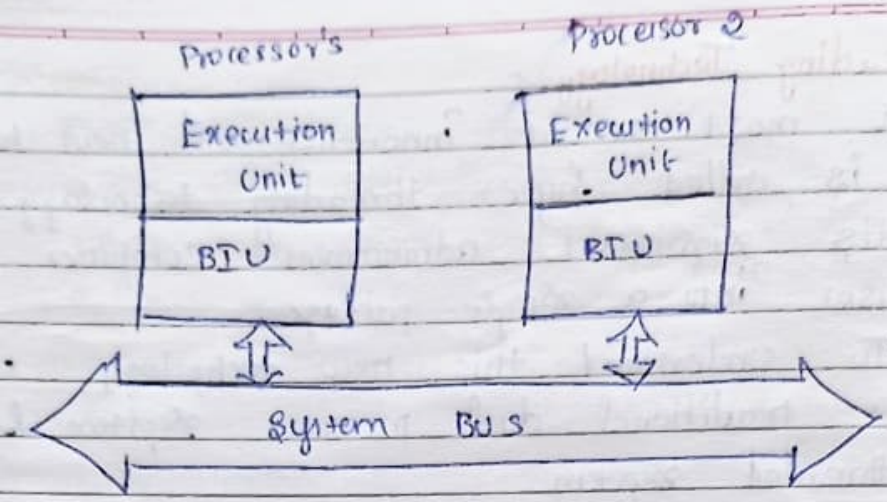
BIU is used to access memory

While memory is accessed in bursts that fill caches, it is became idle.

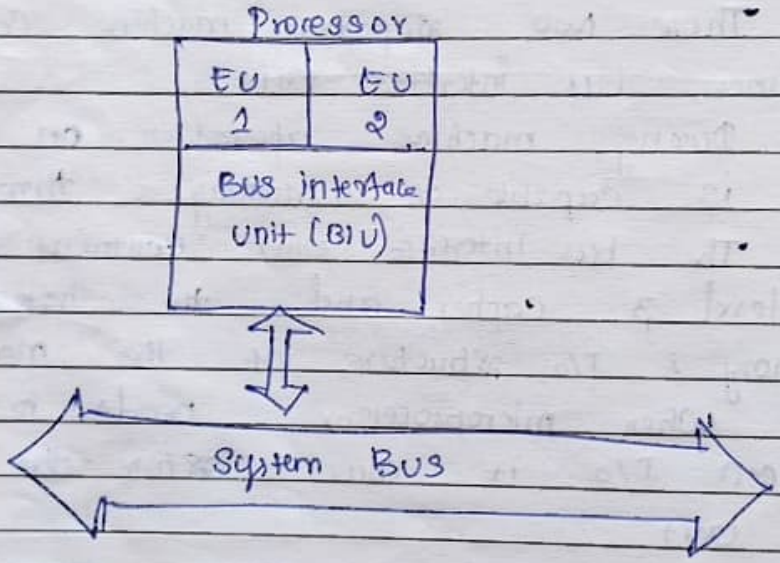
Because of a second processor can use this idle time to access memory while other processor is busy executing instructions

Threads run on a different processor in a system that has either dual processor (or) hyper threaded processor increasing performance.

In future architecture may include even more processors to handle additional threads.



a) Dual Processor System



b) Hyper threaded System

*) CPUID:

CPUID instruction accesses information that indicates the type of microprocessor as well as feature supported by the microprocessor

Table list the latest feature available to the CPUID instruction

To access this feature. EAX is loaded with the input number listed in the table. Then CPUID instruction is executed.

The CPUID instruction usually returns information in the EAX, EBX, ECX, EDX registers in real or protected mode.

Addition features have been added to CPUID instruction when compared to previous version

EXP input value	Output register
0	EAX = maximum i/p value EBX = "ineG" ECX = "lene" EDX = "letn"
1	EAX = Version information EBX = Feature info. ECX = Extended feature info n EDX = Feature information
2	EAX, EBX, ECX, EDX
3	ECX & EDX serial number in the pentium only
4	EAX, EBX, ECX, EDX
5	EAX, EBX, ECX, EDX

80000000 H	EAX	Extended information
80000001 H	EAX	Reserved
80000002 H	EAX, EBX, ECX, EDX	Processor brand string
80000004 H		
80000006 H	ECX	Cache information

*) Memory interface:-

Memory interface pentium 4 typically uses the intel 945, 965, 975 chip set

These chip sets provide a dual pipe memory bus to the microprocessor with each pipe interfaced to a 32 bit wide section of memory

The two pipes function together to compromise the 64 bit wide data path to the microprocessor Because of the dual pipe arrangements.

The memory must be populated with pairs of DDR 2 memory devices operating at 600 MHz, 800 MHz (or) 1033 MHz.

According to intel the ADR2 arrangement provided a 300% increase in speed over a memory populated with pc-100 memory.

Multiple core technology :-

New Versions of pentium 4 and core 2 contains either data con quad Cores

Each core is separate version of the microprocessor that independently executes a separate task

Three Versions are currently available

The pentium D - which contains two cores with separate cache.

a core 2 Dual version that contains a shared cache.

Two Core 4 quad core version contain four cores.

Intel seems to have share cache for multiple core microprocessor.

A recent article from intel stated that in future the pentium (or) whatever it will be called contain upto 80 cores.

The core 2 Duo contain either 2M (or) 4M byte cache & operates frequencies to 3GHz.

As single - core processors hit their physical limits of complexity and speed, multi-core computing is becoming more popular. In modern times, the majority of systems are multi-core.

Many-core (or) massively multi-core systems refer to systems with a huge number of CPU such as tens (or) hundreds.

In the early 2000s, Intel and AMD released the first multicore processor. In moder times, CPUs come with two (dual-core), four (quad-core), six ("hexa-core") and eight ("octa-core") cores ("octo-core").

*) Pentium Memory Management :-

A hardware component liable in handling different accesses to memory requested by CPU is known as memory management unit (MMU), which is also termed as paged memory management unit (PMMU). The main functions of MMU can be categorized as follows

Translation of virtual addresses to physical addresses which is also known as Virtual Memory Management (VMM).

The Memory system for pentium microprocessor is 4G bytes in size just as in 80386 DX and 80486 microprocessor.

Pentium uses a 64-bit data bus to address memory organized in eight banks that each contain 512M bytes of data.

Most microprocesser including pentium also supports virtual memory concept with the help of memory management unit. Virtual memory is used to manage the resource of physical memory.

It supports the execution of processes partially resident in memory, only the most recently used portions of a processes address space actually occupy physical memory the rest of the address space is stored on disk until needed.

The Intel pentium microprocessor supports both segmentation and segmentation with paging.

Another important feature supported by pentium processor is the memory protection

Virtual Memory Management in Pentium:-

The memory management unit in pentium is upward compatible with the 80386 and 80486 microprocessors. The linear address space for pentium microprocessor is 4G bytes that means from 0 to (232-1)

MMU translates the virtual address to physical address in less than a single clock cycle for a "HIT" and also it minimizes the cache fetch time for a "MISS".

CPU generates logical address which are given to segmentation unit which produces linear addresses which are then given to paging unit and thus paging unit generates physical addresses in main memory.

Logical address to physical address Translation in pentium:-

Pentium can run in both modes (i.e) real or protected. Real mode does not allow multi tasking as there is no protection for one process to interfere with another. whereas in protected mode each processes runs in a separate code segment.

Segments have different privilege levels preventing the lower privilege process to run a higher privilege (eg: operating system).

Pentium running in protected mode supports both segmentation and segmentation with paging.

Segmentation:-

This process helps in dividing programs into logical blocks and then placing them in

different memory area.

This makes it possible to regulate access to critical sections of the application and helps identify bugs during the development process.

Segment registers are now called segment selectors because they do not map directly to a physical address but point to an entry of the descriptor table.

Selector to Descriptor :-

Find the segment entry of the table, this is the segment descriptor corresponding to the segment.

There are two types of Descriptor table. Global descriptor table and Local Descriptor table.

Global descriptor:-

It consists of segment definitions that apply to all programs like the code belonging to OS segments created by OS before CPU switched to protected mode.

Local descriptor:-

These tables are unique to an application.

Optimizing Address Translation in Pentium Processor:

The main goal of memory management for address translation is to have all translations in less than a single clock cycle for a "HIT" and minimize cache fetch time for a "Miss".

On page fault the page must be fetched from disk and it takes millions of clock cycles.