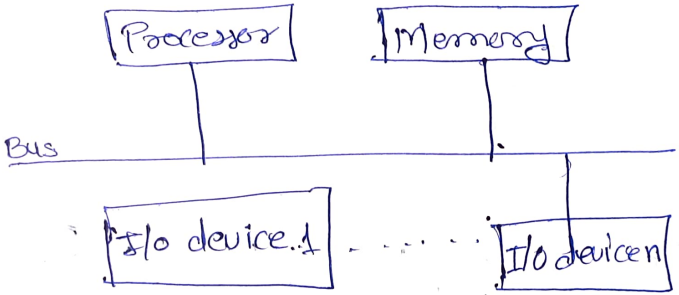
Unit No :— 2
Input and Output Organization

Accessing I/O devices

- In Computing, I/O refers to the communication between an information processing system and Outside the world.
- Input are the signals or data received by the system
- Ouput are the signals or data sent from it.
- I/O devices are used by person or othe system to communicate with computer.

I/O Bus and Interface Modules

- I/O Bus
  - Data Lines
  - Address Lines
  - Control lines
- Interface Modules



- A bus is shared communication link which uses one set of wires to connect multiple subsystems.
- Most modern computer use single bus arrangement for connecting I/O devices to CPU & Memory
- The bus enables all the devices connected to it. to exchang infn.

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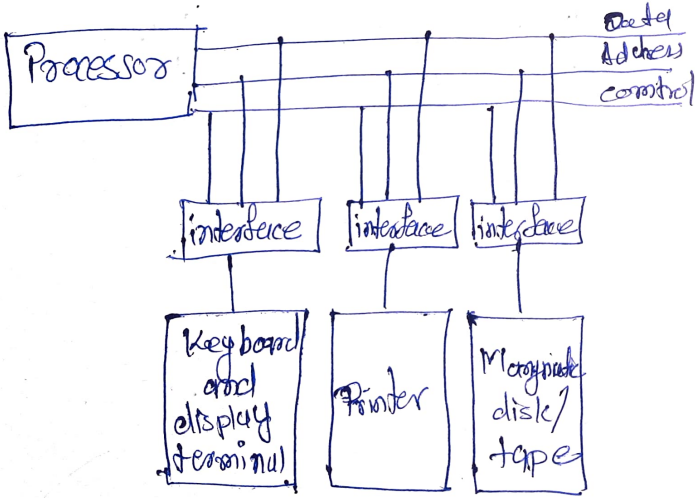
- Bus consists of 3 set of lines
  - Address,
  - Data
  - Control

1) Processor places a particular address (unique for an I/O Devices) on address lines
2) Device which recognizes this address responds to the commands issued on the control lines.
3) Processor requests for either Read/write the data will be placed on Data lines.



* I/O Command
  * Control Command
  * Status Command
  * Input Command
  * Output Command

* I/O Bus versus Memory Bus

⇒ Computer buses can be used to communicate with memory and I/O

1) Use two separate buses, one for memory and other for I/O
   * I/O processor

2) Use one common bus for both memory and I/O but have separate control lines for each:
   Isolated I/O or I/O Mapped I/O
   * IN/OUT : I/O Instruction
   * MOV or LD : Memory read/write Instruction

3) Use one common bus for memory and I/O with common control lines: Memory Mapped I/O
   * MOV or LD: I/O and Memory read/write Instruction

Input/Output Mechanism

* Memory-mapped I/O
* Programmed I/O
* Interrupts
* Direct Memory Access

* Memory-Mapped I/O :—

- I/O devices and the memory share the same address space, the arrangement is called Memory mapped I/O
- In memory-mapped I/O portions of address space are assigned to I/O devices and reads and write to those addresses are interpreted as commands to the I/O device.

* Programmed I/O :—

- In this case, use dedicated I/O instructions in the processor.
- These I/O instructions can specify both the device numbers and the command word

- The processor communicates the device address via a set of wires normally included as part of the I/O bus.
- The actual command can be transmitted over the data lines in the bus.

* Interrupt :—

- When a Process is executed by the CPU and when a user Request for another Process, then this will create disturbance for the Running Process.
- This is also called as interrupt
- Interrupts can be generated by User.
- Type of Interrupts
  * Internal Interrupt
  * Software Interrupt
  * External Interrupt

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Direct Memory Access (DMA)

- To transfer large blocks of data at high speed, between External devices & Main Memory, DMA approach is often used.
- DMA controller allows data Transfer directly between I/O device and Memory with minimal intervention of processor.
- DMA Controller acts as a processor but it is controlled by CPU.
- To initiate transfer of a block of words the processor sends the following data to controller
  - The starting address of the memory block
  - The word count
  - Control to specify the mode of transfer such as read or write
  - A control to start the DMA transfer

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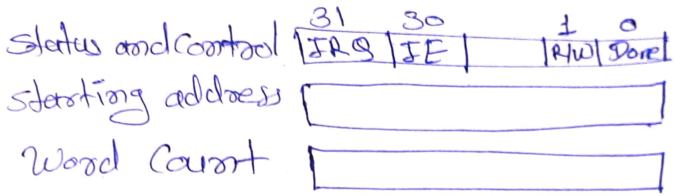
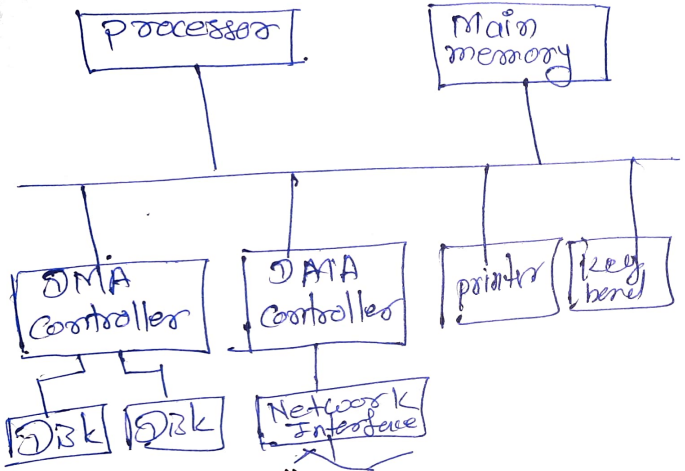
- DMA controller performs the requested I/O operation and sends a interrupt to the processor upon completion



- In DMA Interface
- First register store the starting address
- Second register store word count
- Third register contains status and control flags.

Bits and Flags	1	0
R/W	READ	Write
Done	Data transfer finished	
IRQ	Interrupt request	
IE	Raise interrupt (enable) after Data Transfer	

DMA Controller in a Computer System



- BR (Bus Request)
  → To request CPU for bues
- BG (Bus Grant)
  - CPU activates BG O/p to inform DMA that bues are available.

When DMA takes controls of bus system the transfer with memory can be made in the following ways

a) Burst transfer mode
b) Cycle stealing mode

* The two basic schemes for communication on the bus are -
  1) Synchronous
  2) Asynchronous

1) Synchronous bus -
- If a bus is synchronous (eg. processor-memory), it includes a clock in the control lines and a fixed protocol for communicating that is relative to the clock.
- This type of protocol can be implemented easily in a small finite state machine.
- Because the protocol is predetermined and involves little logic the bus can run very fast and the interface logic will be small.

Synchronous buses have two major disadvantages
→ Every device on the bus must run at the same clock rate
→ and, because of clock skew problems synchronous buses can not be long if they are fast

2) Asynchronous bus :—

- It is not clocked.
- It is can accommodate a wide variety of devices. and the bus can be lengthened without worrying about clock skew or synchronization problems.
- To coordinate the transmission of data between sender and receiver an asynchronous bus uses a handshaking protocol

* Interface Circuits :—

- * Address Decoder
- * Control Circuits
- * Data registers
- * Status registers

- This required to co-ordinate I/O transfers constitute the devices interface circuits.