Shivaji University , Kolhapur

Question Bank For Mar 2022 (Summer) Examination

Subject Code: 83856

Subject Name: B.Tech. CBCS of Part IV Semester 7 – Advanced Computer Architecture

Question Bank 1

Question No.	Unit No.	Question	Marks
1	1	Choose the correct option representing the relationship among processor cycle t_p , memory cycle time t_m , device average access time t_d . A. $t_d < t_m < t_p$ B. $t_m < t_d < t_p$ C. $t_m > t_d > t_p$ D. $t_d > t_m > t_p$	1
2	1	The interleaving of CPU and I/O operations among several programs is called _____. A. Batch processing B. Time sharing C. Multitasking D. Multiprogramming	1
3	1	In SIMD computer, which of the following scheme is used to partitions the set of PEs into enabled and disable sets? A. Routing scheme B. Broadcasting C. Network topology D. Masking scheme	1
4	2	In pipeline, the computer clock period is defined by A. Maximum of time delays of all stages plus time delay of latch B. Minimum of time delays of all stages plus time delay of latch C. Average of time delays of all stages plus time delay of latch D. None of the above	1
5	2	Ideally, a linear pipeline with k stages can process n tasks in _____ clock periods A. k-(n+1) B. k*(n-1) C. k+(n+1) D. k+(n-1)	1
6	2	In the S access memory organization, which address bits are used to retrieve the information from particular module	1

		A. Higher (n-m) bits B. Lower (n-m) bits C. Higher m bits D. Lower m bits	
7	3	A memory hierarchy takes advantage of A. Principle of Locality B. Principle of Multithreading C. Principle of Multiaccess D. None of the above	1
8	3	A cache that has just one block per set (so a block is always placed in the same location) is called _____. A. direct-mapped cache B. fully associative cache C. multilevel cache D. None of the above	1
9	4	In associative memory, which registered is used to enable or disable the bit slices to be involved in the parallel comparison operations across all the words in the associative memory? A. Masking register B. Temporary register C. Indicator register D. Comparand register	1
10	4	Which register is used to handle the IF statements in Vector loops? A. Vector length register B. Scalar register C. Vector mask register D. None of the above	1
11	5	GPUs have the following type of parallelism that can be captured by the programming environment: A. Multithreading B. MIMD C. SIMD D. instruction-level E. All the above	1
12	5	In GPU computational structure, a Grid consists of A. ThreadBlocks B. Threads C. Registers D. None of the above	1
13	6	Multiprocessors are computers consisting of _____ processors. A. Tightly coupled B. Loosely coupled C. Medium coupled D. None of the above	1

14	6	Symmetric (shared memory) multiprocessors are sometimes called _____. A. Cache only memory access B. Uniform memory access C. Nonuniform memory access D. All the above	1
15	1	List and explain the parallel processing mechanisms in uniprocessor computers.	7
16	1	Explain how to evaluate the cost of an Integrated Circuit.	7
17	2	Explain basic concept of pipelined processors with space-time diagrams.	7
18	2	Explain Handler's classification of pipeline processor according to levels of processing.	7
19	3	What is principle of locality? Explain the typical memory hierarchy.	7
20	3	Explain the set associative scheme of placing the block in a cache.	7
21	4	What is Vector Operand? Explain the classification of vector instructions into four primitive types with example.	7
22	4	State the three types of pipelined vector processing methods and explain the horizontal vector processing method with example.	7
23	5	Explain the data routing and masking mechanisms for processing elements in SIMD computers.	7
24	5	Explain NVIDIA GPU Computational Structure.	7
25	6	Explain the basic structure of a centralized shared-memory multiprocessor based on a multicore chip.	7
26	6	What is cache coherence protocol? Explain the two classes of cache coherence protocols.	7

Question Bank 2

Question No.	Unit No.	Question	Marks
1	1	Which of the following is the technique used to improve energy efficiency in modern microprocessors? A. Do nothing well B. Dynamic Voltage-Frequency Scaling (DVFS) C. Overclocking D. All the above	1
2	1	Which of the following equation is correct? A. MTBF = MTTF - MTTR B. MTBF = MTTF + MTTR C. MTTF = MTBF + MTTR D. MTTF = MTBF – MTTR	1

3	1	Which of the following equation is correct? A. Module availability = MTTF/ (MTTF + MTTR) B. Module availability = MTBF/ (MTTF + MTTR) C. Module availability = MTBF/ (MTTF - MTTR) D. d) Module availability = MTTF/ (MTTF - MTTR)	1
4	2	S access memory configuration is suitable for A. Sequential address words B. Non-sequential address words C. Both (a) and (b) D. None of the above	1
5	2	The reciprocal of the clock period is called A. Throughput B. Efficiency C. Frequency D. None of the above	1
6	2	Ideally, nonpipelined processor with k stages can process n tasks in _____ clock periods A. k*(n-1) B. k*(n+1) C. n*(k-1) D. n*k	1
7	3	Which type of cache miss occur even if you had an infinite sized cache? A. Compulsory B. Capacity C. Conflict D. None of the above	1
8	3	To reduce the Hit time and Power, the first level caches should be _____. A. Small B. Large	1
9	4	In associative memory, which registered is used to hold the current match patterns in the associative memory? A. Masking register B. Temporary register C. Indicator register D. Comparand register	1
10	4	In the Bit parallel organization, the comparison operation is performed A. All words at a time B. One word at a time C. One bit slice at a time D. All bit slices which are not masked off at a time	1
11	5	In GPU computational structure, _____ is assigned to the multithreaded SIMD Processor. A. Grid B. Thread Blocks C. Threads	1

		D. All of the above	
12	5	In GPU memory structure, local memory is shared by A. All threads in multithreaded SIMD Processor. B. All threads in a Thread Block C. All Grids D. None of the above	1
13	6	Distributed shared memory multiprocessors are sometimes called _____. A. Cache only memory access B. Uniform memory access C. Nonuniform memory access D. All the above	1
14	6	_____ defines the behavior of reads and writes with respect to accesses to other memory locations. A. Coherence B. Consistency C. Serialization D. Realization	1
15	1	Explain the Flynn's classification of computer architectures with neat diagrams.	7
16	1	Define the two states of service with respect to an SLA. Explain the two main measures of dependability.	7
17	2	Explain the basic structure of linear pipeline processor	7
18	2	Explain Ramamoorthy and Li's classification of pipeline processor according to pipeline configurations and control strategies.	7
19	3	What is Miss rate? Explain three categories of cache misses in three Cs Model.	7
20	3	List and explain six basic cache optimizations in short.	7
21	4	Explain the three special vector instructions with example: i) Compare ii) Compress iii) Merge	7
22	4	State the three types of pipelined vector processing methods and explain the vertical vector processing method with example.	7
23	5	Explain the architectural configuration of SIMD array processors.	7
24	5	Explain the programming in GPU with CUDA.	7
25	6	Explain the basic architecture of a distributed-memory multiprocessor.	7
26	6	What are the challenges of parallel processing?	7

Question Bank 3

Question No.	Unit No.	Question	Marks
1	1	The energy required per transistor is proportional to the product of the _____ driven by the transistor and the square of the _____. A. Capacitive load, Voltage B. Voltage, Current C. Capacitive load, Current D. Voltage, Resistance	1
2	1	Increase in volume A. decrease the cost B. decreases the learning curve C. both (A) and (B) D. None of the above	1
3	1	Commodities are products that are sold by multiple vendors in large volumes and are essentially identical. A. multiple vendors, different B. single vendor, different C. single vendors, identical D. multiple vendors, identical	1
4	2	In ideal case, the maximum efficiency that can be achieved with linear pipeline is A. 1 B. f C. k D. None of the above	1
5	2	In the S access memory organization, total time required to access k consecutive words in sequence starting in module i with a memory access time Ta and a latch delay of τ if i+k<=M A. τ + kTa B. τ + (k-1)Ta C. Ta + (k-1)τ D. Ta + kτ	1
6	2	A pipeline stage is A. Sequential circuit B. Combinational circuit C. Both sequential circuit and combinational circuit D. None of the above	1
7	3	Which type of cache miss occur even if you had an infinite sized cache? A. Compulsory B. Capacity C. Conflict D. None of the above	1
8	3	To reduce the Hit time and Power, the first level caches should be _____.	1

		A. Small B. Large	
9	4	In vector processor, the set of vector instructions that could potentially execute together is called _____ . A. chime B. convoy C. stride D. chaining	1
10	4	Which technique is used to tackle the problem where the vector is longer than the maximum length? A. chaining B. stride C. data mining D. strip mining	1
11	5	In SIMD computer, which of the following scheme is used to specify the various patterns to be set up in the interconnection network for inter-PE communications? A. Routing scheme B. Broadcasting C. Network topology D. Masking scheme	1
12	5	The primary mechanism for supporting sparse matrices is _____using index vectors. A. Masking operation B. gather-scatter operations C. stride operations D. chaining operations	1
13	6	In _____ cache coherence protocol, the sharing status of a particular block of physical memory is kept in one location. A. Directory based B. Snooping C. Consistency D. None of the above	1
14	6	Which cache coherence protocol consumes more bandwidth? A. Write invalidate protocol B. Write update protocol C. Write broadcast protocol D. Both (A) and (B)	1
15	1	Explain the functional structure of SIMD array processor.	7
16	1	Why understanding of cost and its factors is essential for designers? Explain the major factors that influence the cost of a computer.	7
17	2	Explain any four performance evaluation factors for pipeline processors.	7

18	2	Draw and explain S-access memory organization.	7
19	3	What is way prediction? How it is used to reduce the cache hit time?	7
20	3	Explain the use of loop interchange to reduce the miss rate with example.	7
21	4	Explain the different approaches to enhance to vector processing capability.	7
22	4	What are Associative memories? Why they are called as content addressable?	7
23	5	Explain the set of parameters defining the SIMD computer.	7
24	5	Write note on conditional branching in GPU.	7
25	6	What is Multiprocessor Cache Coherence?	7
26	6	With neat diagram, explain a write invalidate cache coherence protocol for a private write-back cache.	7

Question Bank 4

Question No.	Unit No.	Question	Marks
1	1	Which of the following is used to decide whether system is up or down? A. Service accomplishment B. Service level agreements C. Service interruption, D. All of the above	1
2	1	_____ is a measure of the service accomplishment with respect to the alternation between the two states of accomplishment and interruption. A. Module availability B. Module reliability C. Module efficiency D. None of the above	1
3	1	The percentage of manufactured devices that survives the testing procedure is called as A. Quality product B. Tested product C. Yield D. Volume	1
4	2	In the S access memory organization which address bits are used to address to all M memory modules simultaneously A. Higher (n-m) bits B. Lower (n-m) bits C. Higher m bits D. Lower m bits	1
5	2	Ideally, nonpipelined processor with k stages can process n tasks in _____ clock periods	1

		A. k*(n-1) B. k*(n+1) C. n*(k-1) D. n*k	
6	2	In ideal case, the maximum throughput that can be achieved with linear pipeline is A. 1/τ B. f C. both (a) and (b) D. k	1
7	3	In _____ , extra bits are kept in the cache to predict the way, or block within the set of the next cache access. A. Set prediction B. Cache prediction C. Way prediction D. None of the above	1
8	3	Which factor is deciding how many outstanding misses to support? A. The temporal and spatial locality in the miss stream B. The bandwidth of the responding memory or cache C. Supporting many misses at a higher level D. The latency of the memory system E. All of the above	1
9	4	In vector processor, the set of vector instructions that could potentially execute together is called _____ . A. chime B. convoy C. stride D. chaining	1
10	4	Which technique is used to tackle the problem where the vector is longer than the maximum length? A. chaining B. stride C. data mining D. strip mining	1
11	5	Thread level parallelism is utilized by the following software model A. Parallel processing B. Request level parallelism C. Multiprogramming D. All the above	1
12	5	To distinguish between functions for the GPU (device) and functions for thesystem processor (host), CUDA uses _____ for the former and _____ for the latter. A. _device_ , _host_ B. _gpu_ , _cpu_ C. _graphics_ , _system_ D. None of the above	1

13	6	Use of replication of data in multiple caches leads to reduction in A. Access latency B. Required memory bandwidth C. Contention for shared data D. All the above	1
14	6	A memory system is coherent if it A. Preserve the program order B. Preserve coherent view of memory C. Ensures write serialization D. All the above	1
15	1	Explain functional design of an MIMD Multiprocessor System.	7
16	1	Explain the dynamic and static power consumption in CMOS chips.	7
17	2	What is the advantage of Interleaved Memory Organizations? Define memory bandwidth and explain the factors affecting on memory bandwidth?	7
18	2	Illustrate three classes of data-dependent hazards according to various data update patterns.	7
19	3	Explain the use of nonblocking caches to increase the cache bandwidth.	7
20	3	Explain the use of blocking to reduce the miss rate with example.	7
21	4	Explain the architecture of a typical vector processor with multiple functional pipes with neat diagram.	7
22	4	Explain bit serial and bit parallel architectures.	7
23	5	Explain the components of Processing Element (PE) in SIMD computer.	7
24	5	List and explain the fundamental decisions that determines the architecture of an interconnection network for a SIMD machine.	7
25	6	Explain the two snooping coherence protocols.	7
26	6	Explain directory based cache coherence protocol.	7

Question Bank 5

Question No.	Unit No.	Question	Marks
1	1	In the system architecture of the CDC-6600, _____ is used to keep track of the availability of the functional units and registers being demanded. A. Program Counter B. Tracker C. Scoreboard D. Pipeline	1

2	1	_____ is a measure of the continuous service accomplishment (or, equivalently, of the time to failure) from a reference initial instant. A. Module availability B. Module reliability C. Module efficiency D. None of the above	1
3	1	Which of the following statement is correct? A. execution time is the reciprocal of performance B. execution time is directly proportional to the performance C. execution time is independent of performance D. None of the above	1
4	2	The efficiency of linear pipeline is measured by the percentage of A. busy time-space span over total time-space time B. idle time-space span over total time-space time C. busy time-space span over idle time-space time D. None of the above	1
5	2	In ideal case, the maximum throughput that can be achieved with linear pipeline is A. $1/\tau$ B. f C. both (a) and (b) D. k	1
6	2	In the S access memory organization which address bits are used to address to all M memory modules simultaneously A. Higher (n-m) bits B. Lower (n-m) bits C. Higher m bits D. Lower m bits	1
7	3	Request the missed word first from memory and send it to the processor as soon as it arrives and let the processor continue execution while filling the rest of the words in the block is called _____. A. Early restart B. Critical word first C. Critical block first D. None of the above	1
8	3	In associative memory, which registered is used to hold the key operand being searched or being compared with? A. Masking register B. Temporary register C. Indicator register D. Comparand register	1
9	4	The primary mechanism for supporting sparse matrices is _____using index vectors.	1

		A. Masking operation B. gather-scatter operations C. stride operations D. chaining operations	
10	4	When an array is allocated memory, it is laid out in either row-major (as in C) or column-major (as in Fortran) order and is called as _____. A. linearization B. quantization C. discretization D. normalization	1
11	5	In GPU computational structure, _____ is assigned to the multithreaded SIMD Processor. A. Grid B. Thread Blocks C. Threads D. All of the above	1
12	5	CUDA produces the _____ for the GPU. A. C and C++ B. C and C++ dialects C. Java D. C#	1
13	6	_____ ensures that all writes to the same location are seen in the same order. A. Write realization B. Read realization C. Write serialization D. Read sterilization	1
14	6	In _____ cache coherence protocol, every cache that has a copy of the data from a block of physical memory could track the sharing status of the block. A. Directory based B. Snooping C. Consistency D. None of the above	1
15	1	Explain the Flynn's classification of computer architectures with neat diagrams.	7
16	1	Find the die yield for dies that are 1.5 cm on a side and 1.0 cm on a side, assuming a defect density of 0.4 per cm2 and α is 4.	7
17	2	Draw and explain C-access memory organization.	7
18	2	Explain in short how basic scheduling and loop unrolling is used to increase the ILP.	7
19	3	Explain the use of write merging to reduce the cache miss penalty with neat figure.	7
20	3	Explain the use of compiler-controlled prefetching to reduce the miss penalty or miss rate.	7

21	4	Explain the basic structure of a vector architecture, VMIPS.	7
22	4	Illustrate the use of associative memory for the storage and retrieval of student file containing Name, Sex, Department, Age & Class, and query given below: Query: Search for those students whose ages are in the range (21, 31).	7
23	5	Compare Configuration-I and Configuration-II of SIMD computer.	7
24	5	With neat diagram, explain the calculation of the summation S(k)= $\sum_{i=1}^{k} A_i$, k= 0, 1, … ,7 in a SIMD machine.	7
25	6	What is cache coherence protocol? Explain the two classes of cache coherence protocols.	7
26	6	With neat diagram, explain a write invalidate cache coherence protocol for a private write-back cache.	7