SB-03

Total No. of Pages : 3

Seat No.	

Final Year B.Tech. (Part - I) (Computer Science and Engineering)
(Semester - VII) (CBCS) Examination, January-2023
ADVANCED COMPUTER ARCHITECTURE
Sub. Code : 83856

Day and Date : Friday, 6 - 01 - 2023 **Total Marks : 70**

Time : 10.30 a.m. to 1.00 p.m.

Instructions : **1) All questions are compulsory.**
2) Figures to the right indicate full marks.
3) Assume Suitable data wherever necessary.

Q1) Rewrite the sentence with correct answer. **[14]**

a) Which of the following is the technique used to improve energy efficiency in modern microprocessors?

i) Do nothing well

ii) Dynamic Voltage-Frequency Scaling (DVFS)

iii) Overclocking

iv) All of the above

b) Which of the following equation is correct?

i) MTBF = MTTF – MTTR ii) MTBF = MTTF + MTTR

iii) MTTF = MTBF + MTTR iv) MTTF = MTBF – MTTR

c) Which of the following equation is correct?

i) Module availability = MTTF/ (MTTF + MTTR)

ii) Module availability = MTBF/ (MTTF + MTTR)

iii) Module availability = MTBF/ (MTTF – MTTR)

iv) Module availability = MTTF/ (MTTF – MTTR)

d) S access memory configuration is suitable for

i) Sequential address words ii) Non - sequential address words

iii) Both (i) and (ii) iv) None of the above

e) The reciprocal of the clock period is called

i) Throughput ii) Efficiency

iii) Frequency iv) None of the above

P.T.O.

f) Ideally, nonpipelined processor with k stages can process n tasks in _____ clock periods

i) k*(n-1) ii) k*(n+1)
iii) n*(k-1) iv) n*k

g) Which type of cache miss occur even if you had an infinite sized cache?

i) Compulsory ii) Capacity
iii) Conflict iv) None of the above

h) To reduce the Hit time and Power, the first level caches should be ____.

i) Small ii) Large
iii) - iv) -

i) In associative memory, which registered is used to hold the current match patterns in the associative memory?

i) Masking register ii) Temporary register
iii) Indicator register iv) Comparand register

j) In the Bit parallel organization, the comparison operation is performed

i) All words at a time
ii) One word at a time
iii) One bit slice at a time
iv) All bit slices which are not masked off at a time

k) In GPU computational structure, _____ is assigned to the multithreaded SIMD Processor.

i) Grid ii) Thread Blocks
iii) Threads iv) All of the above

l) In GPU memory structure, local memory is shared by

i) All threads in multithreaded SIMD Processor
ii) All threads in a Thread Block
iii) All Grids
iv) None of the above

m) Distributed shared memory multiprocessors are sometimes called _____.

i) Cache only memory access
ii) Uniform memory access
iii) Nonuniform memory access
iv) All of the above

n) _____ defines the behavior of reads and writes with respect to accesses to other memory locations.

i) Coherence ii) Consistency
iii) Serialization iv) Realization

Q2) Solve any 2 of the following questions. (7 Marks Each)

a) Explain the Flynn's classification of computer architectures with neat diagrams. **[7]**

b) Explain the basic structure of linear pipeline processor. **[7]**

c) What is Miss rate? Explain three categories of cache misses in three Cs Model. **[7]**

Q3) Solve any Two of the following questions. (7 Marks Each)

a) Define the two states of service with respect to an SLA. Explain the two main measures of dependability. **[7]**

b) Explain Ramamoorthy and Li's classification of pipeline processor according to pipeline configurations and control strategies. **[7]**

c) List and explain six basic cache optimizations in short. **[7]**

Q4) Solve any two of the following questions. (7 Marks Each)

a) Explain the three special vector instructions with example **[7]**

i) Compare

ii) Compress

iii) Merge

b) Explain the architectural configuration of SIMD array processors. **[7]**

c) Explain the basic architecture of a distributed-memory multiprocessor. **[7]**

Q5) Solve any two of the following questions. (7 Marks Each)

a) State the three types of pipelined vector processing methods and explain the vertical vector processing method with example. **[7]**

b) Explain the programming in GPU with CUDA. **[7]**

c) What are the challenges of parallel processing? **[7]**

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SE - 13

Total No. of Pages : 4

Seat No.	

Final Year B. Tech. (Computer Science and Engineering)
(Semester - VII) (CBCS) Examination, March - 2023
ADVANCED COMPUTER ARCHITECTURE
Sub. Code : 83856

Day and Date : Thursday, 15 - 06 - 2023 **Total Marks : 70**

Time : 2.30 p.m. to 5.00 p.m.

Instructions :
1) **All questions are compulsory.**
2) **Figures to the right iindicate full marks.**
3) **All questions carry equal marks.**

Q1) a) Choose the correct option representing the relationship among processor cycle t_p, memory cycletime t_m, device average access time t_d. **[1]**

i) $t_d < t_m < t_p$ ii) $t_m < t_d < t_p$

iii) $t_m > t_d > t_p$ iv) $t_d > t_m > t_p$

b) The interleaving of CPU and I/O operations among several programs is called _____. **[1]**

i) Batch processing

ii) Time sharing

iii) Multitasking

iv) Multiprogramming

c) In SIMD computer, which of the following scheme is used to partitions the set of PEs into enabled and disable sets? **[1]**

i) Routing scheme ii) Broadcasting

iii) Network topology iv) Masking scheme

d) In pipeline, the computer clock period is defined by **[1]**

i) Maximum of time delays of all stages plus time delay of latch

ii) Minimum of time delays of all stages plus time delay of latch

iii) Average of time delays of all stages plus time delay of latch

iv) None of the above

P.T.O.

456

e) Ideally, a linear pipeline with k stages can process n tasks in _____clock periods **[1]**

i) k-(n+1) ii) k*(n-1)

iii) k+(n+1) iv) k+(n-1)

f) In the S access memory organization, which address bits are used to retrieve the information from particular module **[1]**

i) Higher (n-m) bits ii) Lower (n-m) bits

iii) Higher m bits iv) Lower m bits

g) A memory hierarchy takes advantage of **[1]**

i) Principle of Locality

ii) Principle of Multithreading

iii) Principle of Multiaccess

iv) None of the above

h) A cache that has just one block per set (so a block is always placed in the same location) is called _____. **[1]**

i) direct-mapped cache ii) fully associative cache

iii) multilevel cache iv) None of the above

i) In associative memory, which registered is used to enable or disable the bit slices to be involved in the parallel comparision operations across all the words in the associative memory? **[1]**

i) Masking register ii) Temporary register

iii) Indicator register iv) Comparand register

j) Which registeris used to handle the IF statements in Vector loops? **[1]**

i) Vector length register ii) Scalar register

iii) Vector mask register iv) None of the above

k) GPUs have the following type of parallelism that can be captured by the programming environment: **[1]**

i) Multithreading

ii) MIMD

iii) SIMD

iv) Instruction-level

v) All the above

456

l) In GPU computational structure, a Grid consists of **[1]**

i) ThreadBlocks ii) Threads

iii) Registers iv) None of the above

m) Multiprocessors are computers consisting of _____processors. **[1]**

i) Tightly coupled ii) Loosely coupled

iii) Medium coupled iv) None of the above

n) Symmetric (shared memory) multiprocessors are sometimes called _____. **[1]**

i) Cache only memory access ii) Uniform memory access

iii) Non uniform memory access iv) All the above

456

Q2) Solve any two of the following question (7 Marks Each)

a) List and explain the parallel processing mechanisms in uniprocessor computers. **[7]**

b) Explain basic concept of pipelined processors with space-time diagrams. **[7]**

c) What is principle of locality? Explain the typical memory hierarchy. **[7]**

Q3) Solve any two of the following questions (7 Marks Each)

a) Explain how to evaluate the cost of an Integrated Circuit. **[7]**

b) Explain Handler's classification of pipeline processor according to levels of processing. **[7]**

c) Explain the set associative scheme of placing the block in a cache. **[7]**

Q4) Solve any two of the following question (7 Marks Each)

a) What is Vector Operand? Explain the classification of vector instructions into four primitive types with example. **[7]**

b) Explain the data routing and masking mechanisms for processing elements in SIMD computers. **[7]**

c) Explain the basic structure of a centralized shared-memory multiprocessor based on a multicore chip. **[7]**

Q5) Solve any two of the following question (7 Marks Each)

a) State the three types of pipelined vector processing methods and explain the horizontal vector processing method with example. **[7]**

b) Explain NVIDIA GPU Computational Structure. **[7]**

c) What is cache coherence protocol? Explain the two classes of cache coherence protocols. **[7]**

456

QP Code: 9028QP

Seat No.	

Total No. of Pages: 3

Winter Examination Oct/Nov 2023

Subject Name: Bachelor of Engineering_67541_83856_83990 _ Advanced Computer Architecture_29.11.2023_10.30 AM To 01.00 PM

Subject Code: 83856

Day and Date: - Wednesday, 29-11-2023 **Total Marks: 70**

Time: - 10:30 am to 01:00 pm

Instructions.:

1) All questions are compulsory
2) Figures to the right indicate full marks
3) Assume suitable data wherever necessary and mention it boldly

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Q.1. **Q.1 Solve MCQs. (1 Marks Each)** **[14]**

1. Which of the following equation is correct?
1. Module availability = MTTF/ (MTTF + MTTR)
2. Module availability = MTBF/ (MTTF + MTTR)
3. Module availability = MTBF/ (MTTF - MTTR)
4. Module availability = MTTF/ (MTTF - MTTR)

2. In the S access memory organization, total time required to access k consecutive words in sequence starting in module i with a memory access time Ta and a latch delay of τ if i+k<=M
1. τ + kTa
2. τ + (k-1)Ta
3. Ta + (k-1)τ
4. Ta + kτ

3. Increase in volume
1. decrease the cost
2. decreases the learning curve
3. both (A) and (B)
4. None of the above

4. In SIMD computer, which of the following scheme is used to partitions the set of PEs into enabled and disable sets?
1. Routing scheme
2. Broadcasting
3. Network topology
4. Masking scheme

5. In ideal case, the maximum throughput that can be achieved with linear pipeline is
1. 1/τ
2. f
3. both (a) and (b)
4. k

9464

6. Ideally, a linear pipeline with k stages can process n tasks in_____ [14]
clock periods
1. k-(n+1)
2. k*(n-1)
3. k+(n+1)
4. k+(n-1)
7. In _____ , extra bits are kept in the cache to predict the way, or block within the set of the next cache access.
1. Set prediction
2. Cache prediction
3. Way prediction
4. None of the above
8. Which type of cache miss occur even if you had an infinite sized cache?
1. Compulsory
2. Capacity
3. Conflict
4. None of the above
9. Which technique is used to tackle the problem where the vector is longer than the maximum length?
1. chaining
2. stride
3. data mining
4. strip mining
10. The primary mechanism for supporting sparse matrices is_____using index vectors.
1. Masking operation
2. gather-scatter operations
3. stride operations
4. chaining operation
11. In GPU computational structure, _____ is assigned to the multithreaded SIMD Processor.
1. Grid
2. Thread Blocks
3. Threads
4. All of the above
12. Thread level parallelism is utilized by the following software model
1. Parallel processing
2. Request level parallelism
3. Multiprogramming
4. All the above

9484

13. A memory system is coherent if it
1. Preserve the program order
2. Preserve coherent view of memory
3. Ensures write serialization
4. All the above
14. In _____ cache coherence protocol, every cache that has a copy of the data from a block of physical memory could track the sharing status of the block.
1. Directory based
2. Snooping
3. Consistency
4. None of the above

Q.2. **Q2) Solve any two of the following question (7 Marks Each)** **[14]**
1. Explain the functional structure of SIMD array processor.
2. Define the two states of service with respect to an SLA. Explainthe two main measures of dependability.
3. Explain Handler's classification of pipeline processor according to levels of processing.

Q.3. **Q3) Solve any two of the following question (7 Marks Each)** **[14]**
1. Draw and explain S-access memory organization.
2. List and explain six basic cache optimizations in short.
3. Explain the use of nonblocking caches to increase the cache bandwidth.

Q.4. **Q4) Solve any two of the following question (7 Marks Each)** **[14]**
1. Explain the architecture of a typical vector processor with multiple functional pipes with neat diagram.
2. What is Vector Operand? Explain the classification of vector instructions into four primitive types with example.
3. Explain the components of Processing Element (PE) in SIMD computer.

Q.5. **Q5) Solve any two of the following question (7 Marks Each)** **[14]**
1. Explain NVIDIA GPU Computational Structure.
2. Explain the basic structure of a centralized shared-memory multiprocessor based on a multicore chip.
3. Explain directory based cache coherence protocol.

9484