```
`timescale 1ns / 1ps

module fpu_unpack (
    input  wire [63:0] in,         // 64-bit IEEE 754 input
    output wire        sign,       // Sign bit
    output wire [10:0] exponent,   // Exponent field
    output wire [52:0] mantissa,   // Mantissa with implicit leading 1
    output wire        is_zero,    // Input is zero
    output wire        is_inf,     // Input is infinity
    output wire        is_nan,     // Input is NaN
    output wire        is_denorm   // Denormalized number
);

    // Extract fields
    assign sign     = in[63];
    assign exponent = in[62:52];
    wire [51:0] frac = in[51:0];

    // IEEE 754 exponent constants
    localparam [10:0] EXP_ZERO = 11'b00000000000;
    localparam [10:0] EXP_INF  = 11'b11111111111;

    // Classify input
    assign is_zero   = (exponent == EXP_ZERO) && (frac == 52'b0);
    assign is_inf    = (exponent == EXP_INF)  && (frac == 52'b0);
    assign is_nan    = (exponent == EXP_INF)  && (frac != 52'b0);
    assign is_denorm = (exponent == EXP_ZERO) && (frac != 52'b0);

    // Add implicit leading 1 for normalized numbers
    assign mantissa = (exponent == EXP_ZERO) ? {1'b0, frac} : {1'b1, frac};

endmodule
```