```
`timescale 1ns / 1ps

module fpu_pack (
    input  wire        sign,           // Final sign bit
    input  wire [10:0] exponent,       // Final exponent (after normalization)
    input  wire [52:0] mantissa,       // Final mantissa (with implicit 1)
    input  wire        is_zero,        // Input was zero
    input  wire        is_inf,         // Input was infinity
    input  wire        is_nan,         // Input was NaN
    output reg  [63:0] out             // 64-bit IEEE 754 packed output
);

    // Constants for special values
    localparam [10:0] EXP_INF  = 11'b11111111111;
    localparam [51:0] QNAN_PAYLOAD = 52'h0008000000000; // quiet NaN payload

    always @(*) begin
        if (is_nan) begin
            // NaN: Exponent = all 1s, mantissa ≠ 0 (quiet NaN format)
            out = {sign, EXP_INF, QNAN_PAYLOAD};
        end
        else if (is_inf) begin
            // Infinity: Exponent = all 1s, mantissa = 0
            out = {sign, EXP_INF, 52'b0};
        end
        else if (is_zero) begin
            // Zero: All bits zero except sign
            out = {sign, 11'b0, 52'b0};
        end
        else begin
            // Normalized number: pack result, drop implicit 1
            out = {sign, exponent, mantissa[51:0]};
        end
    end

endmodule
```