```
module alu_8bit (
    input  wire [2:0] opcode,
    input  wire [7:0] acc,
    input  wire [4:0] imm,       // 5-bit immediate
    output reg  [7:0] result
);
    always @(*) begin
        case (opcode)
            3'b000: result = acc + imm;       // ADDI
            3'b001: result = acc - imm;       // SUBI
            3'b010: result = acc & imm;       // ANDI
            3'b011: result = acc | imm;       // ORI
            3'b100: result = acc ^ imm;       // XORI
            3'b101: result = ~acc;            // NOT (imm ignored)
            3'b110: result = acc + 1;         // INC
            3'b111: result = acc - 1;         // DEC
            default: result = 8'h00;
        endcase
    end
endmodule
```