

Electronics Workshop II, Project-1

Audio Amplifier

Aryan Agrawal, A Sai Rithvik
2023102050, 2023102060

Table 21

Abstract—The aim of the project is to build an audio amplifier with the following specifications:

- Supply Voltage = -5 to 5 V
- Gain = $G_1 \times G_2 \geq 500$ (Combined Pre-amp and Gain stage)
- Input small signal voltage = 10-20 mV peak-to-peak
- Frequency = Audible Range (20 Hz to 20 kHz)
- Power ≥ 1.5 W
- Filter should not attenuate the input signal
- Power Amplifier should not provide voltage gain
- Load = 10 Ω

This document provides a comprehensive analysis and implementation of an Audio Amplifier. The project focuses on designing, simulating, and testing an amplifier circuit to achieve improved audio signal amplification. Key factors like gain, efficiency, and distortion are carefully evaluated.

I. INTRODUCTION

Audio amplifiers play a crucial role in various applications such as sound systems, musical equipment, and broadcasting. This project focuses on designing an efficient and cost-effective amplifier.

1) *Component Values Chosen:* We use IC-7805 for positive voltage regulation (12V to 5V) and IC-7905 for negative voltage regulation (-12V to -5V). We used capacitor values 10 μF and 1 μF in our design.

II. PRE-AMPLIFIER STAGE

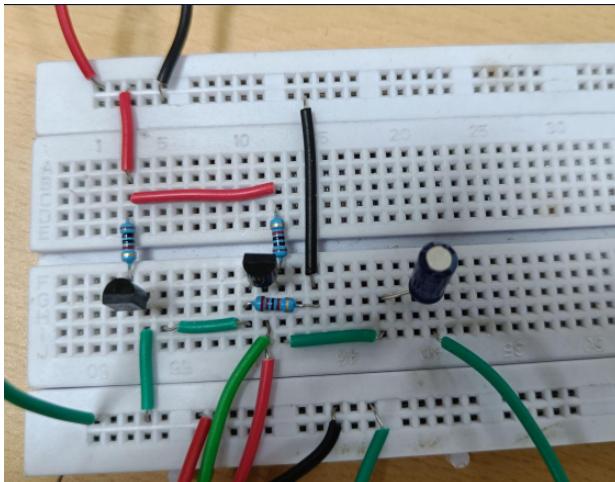


Fig. 1: Pre Amp Hardware Circuit

A. Purpose

The pre-amplifier stage is required for initial amplification. Its main purpose is to improve the signal-to-noise ratio (SNR), so we want an amplifier with a high Common Mode Rejection Ratio (CMRR). The noise removal occurs due to a subtraction of voltages at the input nodes. Ideally, the input resistance should not be low, as this will cause the amplifier to draw a high current, which the microphone cannot supply, leading to ineffective operation of the amplifier. For this reason, the common-emitter differential amplifier can be used, as it has a high input and low output impedance, with good noise performance.

B. DC Analysis

First, we will do a DC analysis of the configuration. We first determine the current flowing through the emitter of both BJTs. The base biasing voltage is 0 for both BJTs, and we assume a drop of 0.7V from the base to the emitter across each BJT. So we have a voltage difference of 4.3V at the emitter resistor. Designing for the emitter current to be 5.8 mA, we get the following.

$$R_E = \frac{4.3V}{5.8mA} = \boxed{740 \Omega} \quad (1)$$

Let $R_{c1} = R_{c2}$. Then by symmetry, the collector currents will be half of the emitter current:

$$I_C = \frac{I_E}{2} = \frac{5.8mA}{2} = \boxed{2.9mA} \quad (2)$$

Now that we have I_C , we find the transconductance g_m :

$$g_m = \frac{I_C}{V_T}, \quad V_T = 26mV \quad (3)$$

Substituting values:

$$g_m = \frac{2.9mA}{26mV} = \boxed{0.112 S} \quad (4)$$

The input impedance of the circuit is roughly $r_\pi \approx \beta/g_m$. Assuming $\beta \approx 295$ for the BC547B (value matched from LTSpice simulation), $r_\pi \approx 2634\Omega$. The output impedance is given by the resistor R_{c2} and we will see in the small signal analysis that it is low by design.

C. AC analysis

From AC analysis we get:

By KVL we know:

$$V_{out} = -g_{m2}V_{\pi2}R_{c2} \quad (5)$$

$$V_{\pi1} = V_{in1} - V_E \quad (6)$$

$$V_{\pi2} = V_{in2} - V_E \quad (7)$$

We can start by writing a KCL at the emitter node:

$$\left(\frac{V_{\pi1}}{r_{\pi1}}\right) + g_{m1}(V_{\pi1}) + g_{m2}(V_{\pi2}) + \left(\frac{V_{\pi2}}{r_{\pi2}}\right) - \frac{V_E}{R_E} = 0 \quad (8)$$

$$V_E = \frac{V_{in1}x_1 + V_{in2}x_2}{x_1 + x_2 + \frac{1}{R_E}} \quad (9)$$

where

$$g_{m1} + \frac{1}{r_{\pi1}} = x_1 \quad (10)$$

$$g_{m2} + \frac{1}{r_{\pi2}} = x_2 \quad (11)$$

For the final gain expression, we need to solve for $V_{\pi2}$. Using equation (7) we obtain:

$$V_{\pi2} = \frac{(V_{in2} - V_{in1})x_1 + \frac{V_{in2}}{R_E}}{x_1 + x_2 + \frac{1}{R_E}} \quad (12)$$

where x . Since R_E is sufficiently large, we can neglect the terms with it in the denominator. At this stage, we assume “matching” of the BJTs, that is, β_1 and β_2 are equal. Recall that $g_{m1} = g_{m2}$ follows from symmetry, so matching implies $r_{\pi1} = r_{\pi2}$, which in turn implies $x_1 = x_2$. Using this, we can simplify to get:

$$V_{\pi2} = \frac{(V_{in2} - V_{in1})}{2} \quad (13)$$

So the input output relation is given by:

$$V_{out} = \frac{-g_{m2}(V_{in2} - V_{in1})R_{c2}}{2} \quad (14)$$

This subtraction of voltages demonstrates how the differential amplifier removes common mode noise! In our circuit, we have set

$$V_{in2} = -V_{in1} \quad (15)$$

This makes analysis much simpler and introduces a “virtual ground” at the emitter node ($V_E = 0$). The final gain equation with respect to V_{in1} is:

$$\frac{V_{out}}{V_{in1}} = g_m R_C \quad (16)$$

We designed our Pre-amp for a gain of 24.7, which gives the following value of $R_c = R_{c1} = R_{c2}$:

$$R_C = \frac{24.7}{0.112} = 220 \Omega \quad (17)$$

As desired, the output impedance for the pre-amp is low.

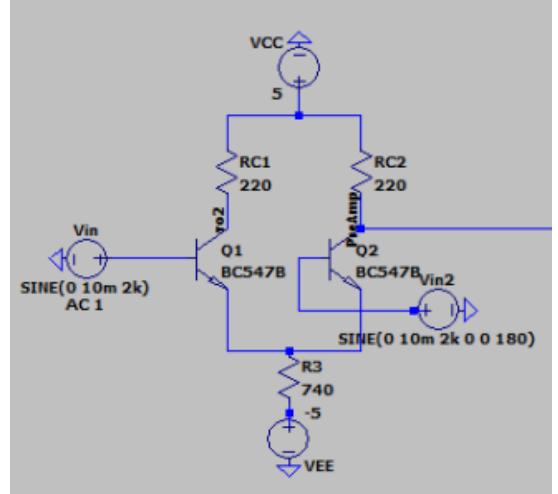


Fig. 2: Pre-Amplifier Circuit with values

D. Result Plots and Verification

To validate our design, we performed SPICE simulations and hardware testing. The results are presented below.

1) *SPICE Simulations:* The LTSpice simulation output for the pre-amplifier circuit is shown in Figure 4.

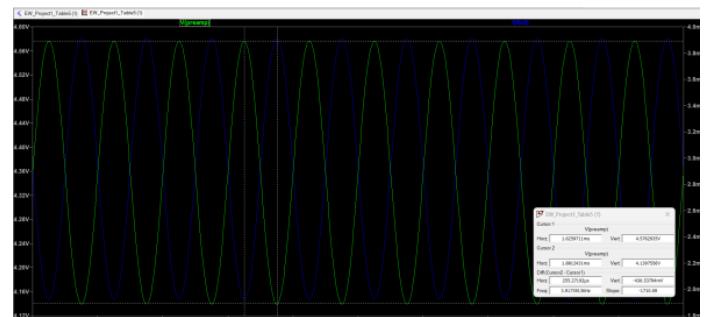


Fig. 3: Pre-Amplifier Circuit Simulation Output



Fig. 4: Common Mode Gain Measurement

From the simulation results:

- **Collector current:** $I_C \approx 2.9183$ mA (blue trace).
- **Transconductance:** $g_m = \frac{I_C}{V_T} \approx 0.112$ S.
- **Output amplitude** (green trace): ≈ 437 mV.
- **Amplitude gain:** $A_v = \frac{437 \text{ mV}}{20 \text{ mV}} \approx 21.85$.

The common mode output was obtained when an 20mV peak-to-peak input was given.

$$\text{Common Mode Gain} = \frac{2.936}{20} = 0.147 \quad (18)$$

Thus, we can calculate the CMRR from the known equation:

$$\text{CMRR} = 20\log\left(\frac{A_d}{A_c}\right) = 20\log\left(\frac{21.85}{0.147}\right) = 43.44 \quad (19)$$

2) *Hardware Output:* The hardware output, captured using a Digital Storage Oscilloscope (DSO), is shown in Figure 6.

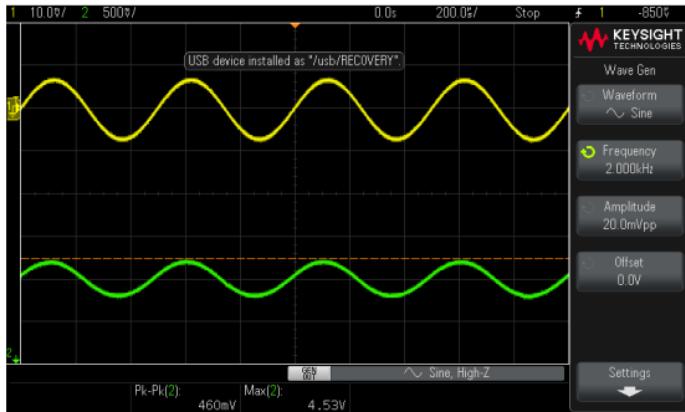


Fig. 5: Pre-Amplifier Circuit Hardware Output

We get **Experimental gain:** $A_v = \frac{460 \text{ mV}}{20 \text{ mV}} \approx 23$.

3) *Comparison:* Table I presents a comparison of theoretical, simulation, and hardware values.

TABLE I: Comparison of Theoretical, Simulation, and Hardware Values

Parameter	Theoretical Value	Simulation Value	Hardware Value
Gain (A_v)	24.7	21.85	23
I_C	2.9 mA	2.9183 mA	2.72 mA

The results show that the theoretical, simulation, and hardware values are in close agreement, confirming the validity of our design.

III. GAIN STAGE

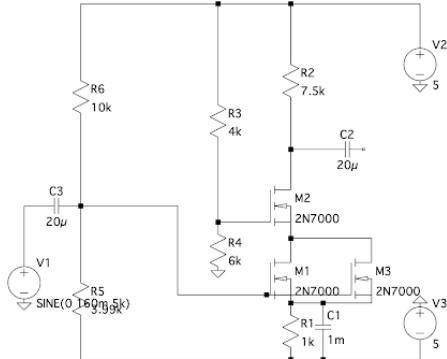


Fig. 6: Circuit Diagram of our gain amplifier

A. Working

For this stage, we made a Cascode Amplifier using 2N7000 mosfet. Another mosfet is added in parallel to the gain mosfet to improve its gain further. We decided this the right way to go because:

- Cascode amplifiers provide a higher gain than traditional amplifiers (especially after having an additional mosfet in parallel).
- It also has improved Bandwidth, making it ideal high frequency applications.
- Trade offs include lower voltage swing and more complexity, which we found to be worth the benefits.

Before we can elaborate on the calculations through which we can verify the functioning of the circuit, here is an overview on the function of individual components.

- **Biassing Point Resistors (R6, R5):** I fixed the operating point of mosfets (2N7000) at -2.5V. This value is selected with in view the V_{TH} of the 2N7000 2.5V. $V_{GS} > V_{TH}$ for mosfet to be on.
- **Drain and Emitter Resistance (R2, R1):** These resistances are integral to our gain. Changing these values directly affects our output. We tried to figure out these values by doing small signal analysis on the mosfet.
- **Cascode mosfet Resistances (R3, R4):** These resistances are needed to bias the gate voltage of our cascode mosfet. The cascode mosfet does not affect our gain, rather it is just enough to make sure that the mosfet is on.

B. Calculations

- 1) *Biassing the amplifier:* Our amplifier only works when our mosfets are on i.e. ($V_{GS} \geq V_{TH}$).

Therefore, using KCL

$$\frac{5 - V}{R_6} = \frac{5 + V}{R_5} \quad (20)$$

fixing $V = -2.5$,

$$\frac{R_6}{R_5} = 3; \quad (21)$$

I took $R_6 = 10\text{k}\Omega$, $R_5 = 3.3\text{k}\Omega$

2) *Small signal analysis:* Lets consider a simplified circuit and its analysis:

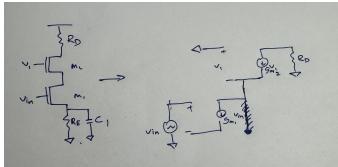


Fig. 7: simplified cascode circuit small signal analysis

I have not included the second mosfet that I have included in parallel with M1. But this analysis will suffice.

Note that M2 (cascode mosfet) does not participate in the gain of the amplifier at all (See that input voltage to the mosfet is constant).

So we can calculate gain as usual:

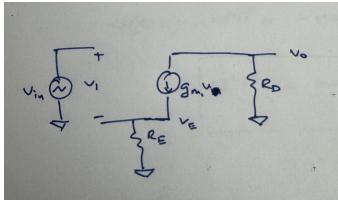


Fig. 8: small signal analysis

from the figure:

$$v_{in} = v_1 + g_m v_1 R_E \quad (22)$$

$$v_1 = \frac{v_{in}}{1 + g_m R_E} \quad (23)$$

since, $v_o = -g_m v_1 R_D$

$$v_o = -\frac{g_m v_{in} R_D}{1 + g_m R_E} \quad (24)$$

$$A_v = -\frac{g_m R_D}{1 + g_m R_E} \quad (25)$$

Because we used two mosfets in parallel

$$gm = gm_1 + gm_2 = 2gm_1 \text{ (considering two mosfets are same)} \quad (26)$$

$$A_v = -\frac{2gm R_D}{1 + 2gm R_E} \quad (27)$$

3) *calculating transconductance:* We know,

$$gm = \frac{\delta(i_d)}{\delta v_{gs}} \quad (28)$$

From the simulation we found $gm = 0.43mS$

4) *Finding values:* From eq(27) and taking $A_v = 50$ and also finalising $R_E = 1k$ we get the value of R_D to be:
 $R_D \approx 7.5K$

For Source capacitor, we took a capacitor with large enough capacitance (1mF) so as to not block any ac voltage.

C. Result Plots and Verification

To validate our design, we performed SPICE simulations and hardware testing. The results are presented below.

a) *SPICE Simulation:* The LTSpice simulation output for the Gain Stage circuit is shown in Figure 9

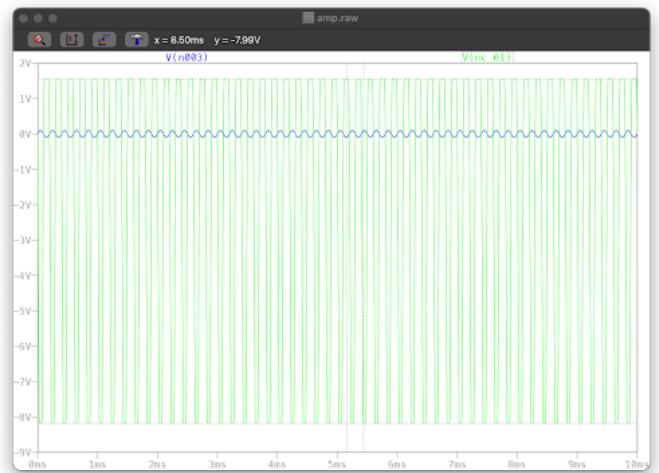


Fig. 9: Gain stage Circuit Simulation Output

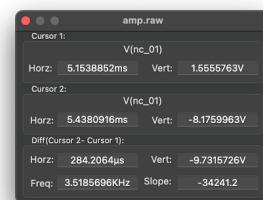


Fig. 10: Cursor results

As we see can the desired gain has been achieved.

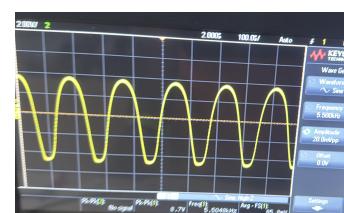


Fig. 11: Hardware output

IV. ACTIVE BAND-PASS FILTER

We built a second-order active bandpass filter by cascading salien-key active low-pass filter and salien-key active high-pass filter.

We referred to salien-key architecture as documented by TI.

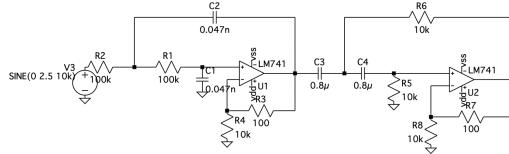


Fig. 12: Filter Circuit

A. Working of the Active Band-Pass Filter

The filter task is to remove unwanted frequency components from our amplifiers. We achieve this by using a bandpass filter that allows only select frequency components (20Hz - 20KHz) to pass through without attenuation.

As discussed earlier the filter is implemented by cascading a low-pass filter and high-pass filter.

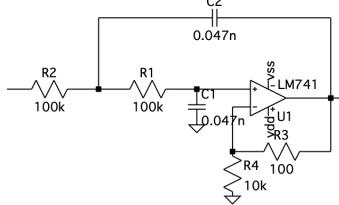


Fig. 13: low-pass filter circuit

I) Low-pass filter:

- Here R1, R2 and C1, C2 determine the cutoff frequency of the filter. If R1 = R2 = R, C1 = C2 = C. (explained in calculations)

$$f_c = \frac{1}{2\pi RC} \quad (29)$$

- R3, R4 are responsible for the gain from the filter. (explained in calculations)

$$K = 1 + \frac{R_3}{R_4} \quad (30)$$

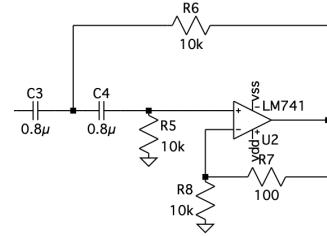


Fig. 14: high-pass filter circuit

2) high-pass filter:

- Here R5, R6 and C3, C4 determine the cutoff frequency of the filter. If R5 = R6 = R, C3 = C4 = C. (explained in calculations)

$$f_c = \frac{1}{2\pi RC} \quad (31)$$

- R7, R8 are responsible for the gain from the filter. (explained in calculations)

$$K = 1 + \frac{R_7}{R_8} \quad (32)$$

B. Theoretical Analysis

We will first focus on realization of the low pass filter since the high pass filter is more or the same.

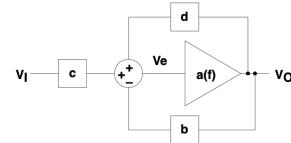


Fig. 15: General Block diagram of Sallen-Key filter

By observing the above figure, we can find out the transfer function from gain block analysis:

$$\frac{V_o}{V_i} = \left(\frac{c}{b}\right) \frac{1}{1 + \frac{1}{a(f) \cdot b}} - \frac{d}{b} \quad (33)$$

If we assume $a(f) \cdot b \gg 1$ (as in the case of OpAmps).

$$\frac{V_o}{V_i} = \left(\frac{c}{b}\right) \frac{1}{1 - \frac{d}{b}} \quad (34)$$

Now considering a low-pass Sallen-key filter:

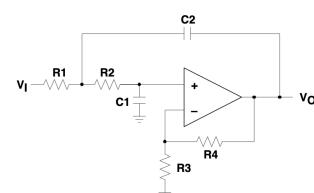


Fig. 16: standard low pass sallen-key filter

By substituting appropriate impedances for b, c and d in equation (63) we get:

$$\frac{V_o}{V_i} = \frac{K}{s^2(R_1R_2C_1C_2) + s(R_1C_1 + R_2C_1 + R_1C_2(1 - k)) + 1} \quad (35)$$

Where $K = 1 + \frac{R_4}{R_3}$ is the gain, From the above equation we can find out the f_c , Q and other such factors by comparing it to the standard second-order low pass transfer function:

$$H_{LP} = \frac{K}{-(\frac{f}{f_c})^2 + \frac{jf}{Qf_c} + 1} \quad (36)$$

Therefore,

$$f_c = \frac{1}{2\pi\sqrt{R_1R_2C_1C_2}} \quad (37)$$

For convenience if we assume $R_1 = R_2$ and $C_1 = C_2$ then,

$$f_c = \frac{1}{2\pi RC} \quad (38)$$

Similar Process applies for High pass filters as well.

1) *Component Selection Based on Cutoff Frequencies*: The cutoff frequency of the high-pass section is determined by R_1 and C_1 , while the cutoff frequency of the low-pass section is determined by R_2 and C_2 . Given the design requirements:

- The high-pass filter should have a cutoff frequency of $f_L = 20$ Hz.
- The low-pass filter should have a cutoff frequency of $f_H = 20$ kHz.

We chose the resistance values to both be equal to $750\text{k}\Omega$ which has the advantage of providing a high input impedance, and convenient capacitance values at the cutoff frequencies. The equality of resistances, as mentioned before ensures unity gain in the midband and attenuation of other frequencies.

a) *Calculation of C_1 for the High-Pass Filter*:: The cutoff frequency for a high-pass filter is given by:

$$f_L = \frac{1}{2\pi R_1 C_1} \quad (38)$$

Rearranging for C_1 :

$$C_1 = \frac{1}{2\pi R_1 f_L} \quad (39)$$

Substituting $R_1 = 10\text{k}\Omega$ and $f_L = 20$ Hz:

$$C_1 = \frac{1}{2\pi(10 \times 10^3)(20)} \quad (40)$$

$$C_1 \approx 0.8\mu\text{F} \quad (41)$$

b) *Calculation of C_2 for the Low-Pass Filter*:: The cutoff frequency for a low-pass filter is given by:

$$f_H = \frac{1}{2\pi R_2 C_2} \quad (42)$$

Rearranging for C_2 :

$$C_2 = \frac{1}{2\pi R_2 f_H} \quad (43)$$

Substituting $R_2 = 100\text{k}\Omega$ and $f_H = 20\text{kHz}$:

$$C_2 = \frac{1}{2\pi(100 \times 10^3)(20 \times 10^3)} \quad (44)$$

$$C_2 \approx 80\text{ pF} \quad (45)$$

But, there is a catch: By selecting f_c to be exactly 20 KHz, we risk attenuation for frequency components that we may require. For this, We decided on a higher f_c value to be sure.

C. Result Plots

Simulations done in LTSpice; We evaluate our filter by frequency response.

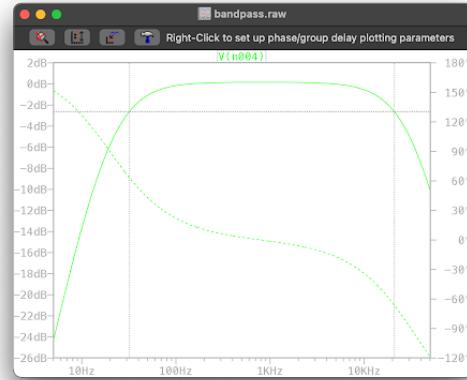


Fig. 17: LTSpice simulation output after the filter stage

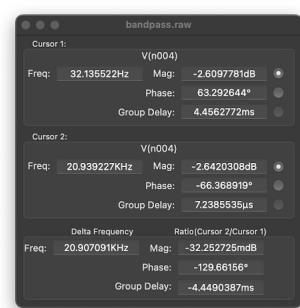


Fig. 18: frequency cutoffs

We see a typical bandpass response from our filter. Another thing to note is that the filter is not contributing anything to

gain (see 0dB).

The cutoff frequencies satisfy the constraints given. Also notice the sharp decline and rise in the graph, this is a feature of the second order filter. This will help us in filtering noise better.

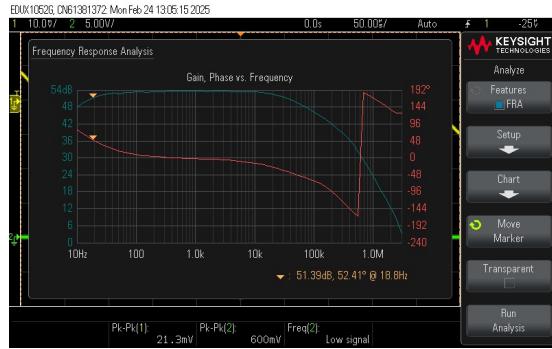


Fig. 19: Hardware implementation: Filter output

Note: This is the output of the filter in the total circuit. We can observe the characteristic bandpass filter response. We can also verify that the cut-off frequencies are appropriate.

V. POWER AMPLIFIER

A. Working:

For a power amplifier, we mainly consider three topologies:

1) Class A Amplifier

Operates with a continuously conducting transistor, providing high linearity and low distortion. However, it has low efficiency (typically around 25-30%) and is mainly used in high-fidelity audio applications.

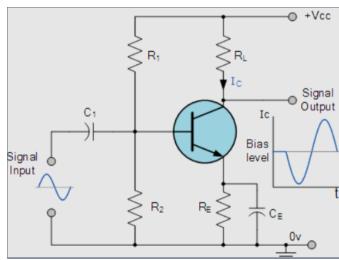


Fig. 20: Class A Power Amplifier

2) Class B Amplifier

Uses two complementary transistors for push-pull operation, making it more efficient (50-70%). However, it introduces crossover distortion, which can degrade audio quality.

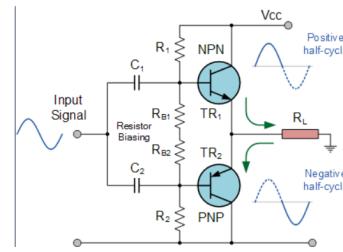


Fig. 21: Class B Power Amplifier

3) Class AB Amplifier

A hybrid between Class A and Class B, designed to reduce crossover distortion while maintaining relatively high efficiency (50-60%). It is widely used in high-power audio applications.

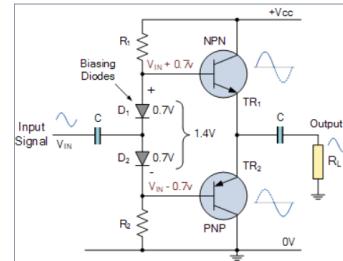


Fig. 22: Class AB Power Amplifier

In our design, we will use a **Class AB amplifier** since it provides a good balance between efficiency and distortion, eliminating the crossover distortion present in Class B amplifiers while being more power-efficient than Class A.

The class AB power amplifier receives the amplified and filtered output from the preceding stages, and amplifies the current thus amplifying the overall power being supplied to the 8Ω speaker at the output.

B. LTSpice Simulations:

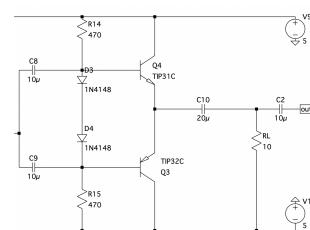


Fig. 23: Power Amplifier Circuit in LTSpice

1) Current Amplification Analysis: Power amplification means that the current is being amplified. We can test whether the current is being amplified by measuring the input and output currents. If the output current is greater than the input current while the output voltage remains the same as the input voltage, then our power amplifier is functioning correctly.

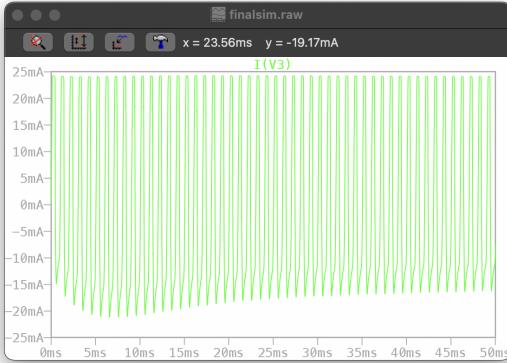


Fig. 24: Input Current to Power Amplifier

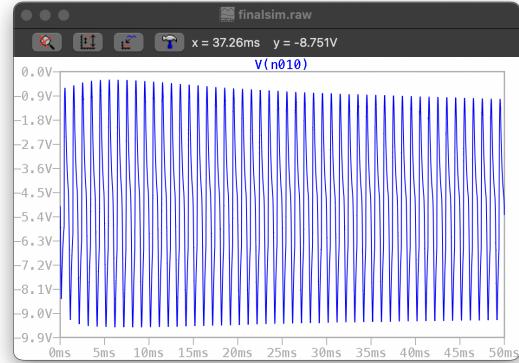


Fig. 27: Output voltage from Power Amplifier

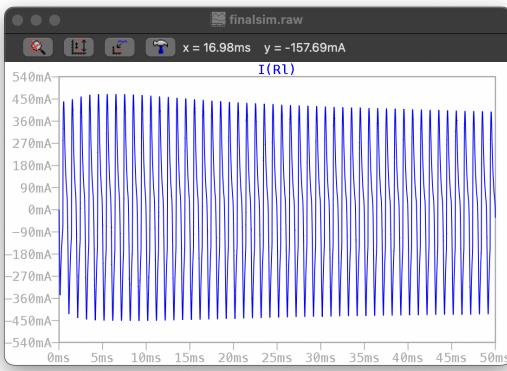


Fig. 25: Load current after power amplification

From Fig. 24, we can see that the peak-to-peak value of the input current is $7.37A$, and from Fig. 25, the peak-to-peak value of the output current is $1A$. Hence, we can conclude that the current is being amplified, and the power amplifier is successfully increasing the power.

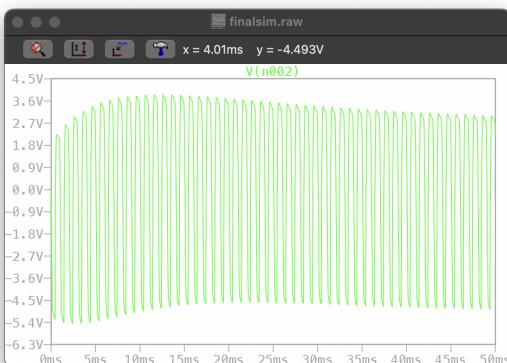


Fig. 26: Input voltage to Power Amplifier

2) *Voltage Consistency Analysis:* From Fig. 26, we observe that the input voltage matches the output voltage shown in Fig. 27. Since we have already confirmed that the current is being amplified, this ensures that the **power amplifier is operating correctly and effectively increasing the power without altering the voltage**.

C. Hardware Simulations:

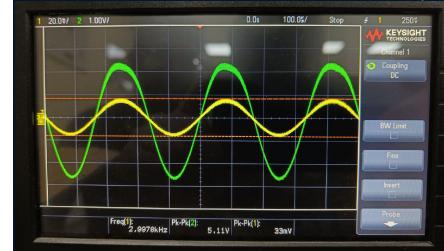


Fig. 28: Power Amplifier Output in relation to input

From the two figures above, we can confirm that our hardware implementation of the power amplifier is functioning correctly.

VI. PROBLEMS FACED

In Ce gain amplifier we faced difficulties in finding biasing point of bc547b because it differs slightly in simulation and hardware. We also faced difficulties in accurately setting 3-dB cutoff for band-pass filter. Power of op-amp was max $1.09W$ as compared to our requirement of $1.5W$.

VII. IMPROVEMENTS

- We made significant improvements to our filter by making second order filter using sallen-key architecture
- Our gain amplifier is also heavily modified and works quite well.

VIII. CONCLUSION

This project successfully demonstrates the design and implementation of an audio amplifier with improved gain and efficiency.