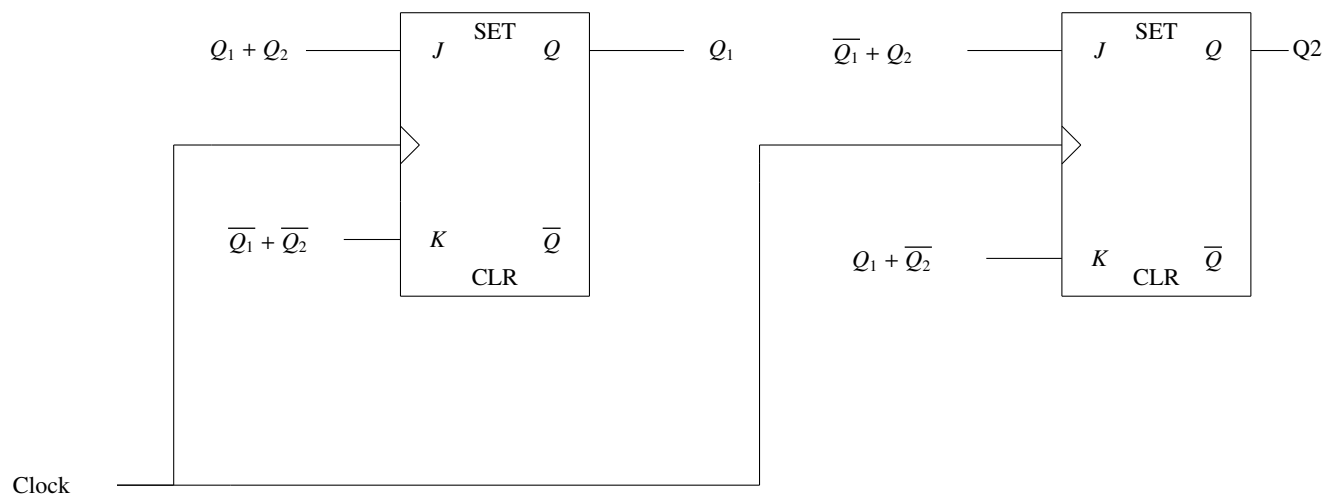


# Gate IN2018, 44

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1. A 2-bit synchronous counter using two J-K flip flops is shown. The expression for the inputs to the J-K flip flops are also shown in the figure. The output sequence of the counter starting from  $Q_1Q_2 = 00$  is GATE-IN2018,44



- A.  $00 \rightarrow 11 \rightarrow 10 \rightarrow 01 \rightarrow 00 \dots$
- B.  $00 \rightarrow 01 \rightarrow 10 \rightarrow 11 \rightarrow 00 \dots$
- C.  $00 \rightarrow 01 \rightarrow 11 \rightarrow 10 \rightarrow 00 \dots$
- D.  $00 \rightarrow 10 \rightarrow 11 \rightarrow 01 \rightarrow 00 \dots$