ARYAN LALL

aryanlall53@gmail.com • Linkedin • Github

Dual Degree (B.Tech + M.Tech), Electrical Engineering
Indian Institute of Technology Bombay, Mumbai, India

SCHOLASTIC ACHIEVEMENTS

- Pursuing minor degree in **Computer Science and Engineering** [*Present*]
- Recipient of the prestigious Undergraduate Research Award (**URA01**) from IIT Bombay ['*20*]
- Bestowed with **Institute Technical Special Mention** award for outstanding contribution to the Technical community of IIT Bombay for the session 19'-20' ['*20*]
- Secured **99.08%** percentile in JEE-advanced among 2.2 Lakh candidates ['*17*]
- Selected amongst **45** candidates, all over India for **Indian Statistical Institute** (B.Math) ['*17*]
- Secured General Rank **38** in West Bengal-JEE among 1.27 Lakh candidates ['*17*]

INTERNSHIPS

Qualcomm - Hardware Intern [*May '20 - Jul '20*]
Development of Static Timing Model for Vector Processor and Reusable Python components for UVM Testbench

- Developed the Static Timing Analysis model for a class of register-to-register Vector Processors to compute the execution time of a given set of low-level instruction codes, following in-order execution
- Currently writing a **paper** on the static timing model developed, covering all the dependencies and constraints existing among various instructions and proposed solution to the problems along with the results
- Developed an Iterative Constraint Randomization solver for generating various valid combinations of vector processor instructions and cut down the overall computation time by a factor of **500**
- Developed a **GUI** interface to ease up the process of Regression testing in vector processor testbench
- Developed the Python package to allocate memory spaces for different registers in a given vector processor instruction, either Linearly or Randomly with an option of overlapping

KEY PROJECTS

FPGA Implementation of Sparse Recovery Algorithms [Documentation] [*Aug '20 - Present*]
Guide: Prof. Siddharth Tallur | Electrical engineering department

- Working on the implementation of Orthogonal Matching Pursuit algorithm on a resource limited FPGA
- Optimized the design and data-flow path to drastically reduce memory and resource consumption

CrakX - Transforming your Preparation [View] [*Jul '20 - Present*]
App to help navigate through the latest campus resources to boost placement and internship preparation

- Developed a flutter based app that helps navigate through various campus resources including sample resumes, success stories, tips, interview questions, etc. guiding for a better preparation
- Conceptualized the entire backend architecture of the application along with the development of top-notch frontend/UI and hence established a smooth flow of data between user application and database
- Acquired **2.5k+** users in one month, followed by appreciation from IIT Bombay and users across the country

FPGA Based Emoji Detector [Documentation][Video] [*Oct '19 - Dec '19*]
GoPynq Competition - Organized by Xilinx during Techfest (Asia's largest Science and Technology festival)

- Secured **1st** position in the competition with a team of 4 members, competing against **30** other colleges across India from behalf of IIT Bombay, with the final round involving submission of a working prototype
- Interfaced various components including web-cam with FPGA, essential for detection and processing while implementing algorithms such as PCA for Image segmentation and Emoji detection for executing on the SoC.

IIT Bombay Student Satellite Project

Star-Tracker based Attitude Determination System [Abstract] [*Aug '19 - Present*]
A CubeSat-compatible modular Star Tracker based Attitude Determination System to be tested on PS4-OP by ISRO

- Conceptualized the Electrical framework for STADS module, required for performing various on-board tasks including power-distribution, data transmission and benchmarked various space-grade components
- Developed **faster** algorithms to increase the update-rate and interfaced memory devices(SRAM) with FPGA
- Established the flow of flight code and the scheduling of various tasks performed by the onboard system
- Currently developing an **FPGA**-based framework for storing and processing Star images onboard

Advitiy - Second Generation Satellite of IIT Bombay [*Feb '18 - Jun '19*]
Advitiy is the 2nd student satellite of IITB, technically advanced and efficient version of the 1st, Pratham

- Devised and implemented an algorithm based on I-V curves of solar cells in **MATLAB** to figure out the suitable series-parallel configuration of solar panels for delivering the maximum power in an orbit
- Implemented perturb and observe method for maximum power point tracking (**MPPT**) to estimate the maximum available power from solar panels using MATLAB simulink models
- Established different communication protocols including **USART** and **I^2C** between **AVR** microcontrollers and sensors for data acquisition, **PID** implementation, estimation of attitude and health monitoring data

PS4-OP Payload Team [Paper] [*Jul '19 - Present*]

This mission aims to design a space-based experiment to be flown on PSLV Stage 4 Orbital Platform

- Actively participated in searching suitable experimental payloads which can be launched on-board stage 4 of the Polar Satellite Launch Vehicle (PSLV) by ISRO
- Researched on various instruments and algorithms to determine upper atmospheric density and satellite drag

Ultra-fast Current-Voltage (I-V) curve scanner [Documentation] [*May '19 - Jul '19*]

Guide: Prof.Narendra Shiradkar | Electrical Engineering Department

- Developed and successfully tested **I-V tracer circuit** for power semiconductor devices using **pulsed I-V** measurement technique and designed PCB for the circuit on **EagleCAD** software
- Optimized the code and improved the standard circuit to achieve a minimum pulse width of **56µs** with current measuring capability till 20A and reduced analog reading time of Arduino by **75%**
- Module to be deployed for accelerated testing of solar panels, monitoring the health of by-pass diodes, in manufacturing lines and as testing measurement equipment for various purposes

Smart Paper Cutter [*Nov '18 - Dec '18*]

2nd *runner-up in 7th inter IIT Tech meet 2018 among 23 IITs*

- Designed a **cost-effective** and **environment-friendly** cutter, which segregates unused portion of used paper
- Implemented **image-processing** techniques including Fast Fourier transform for ruled pages, to recognize the unused portion of paper with the help of contours and draw margins where it is supposed to be cut
- Machine capable of saving **Rs.54,000** annually, by reusing old papers with a peak power consumption of **12W**

COURSE PROJECTS

Control using Brainwaves [Documentation] [*Jan '20 - Mar '20*]

Guide: Prof. Debraj Chakrabarty | Electrical engineering department

- Developed a single-channel low-cost circuit of electroencephalographic (EEG) signal acquisition
- Designed a low-power noiseless filter bank to extract the frequencies of interest (8Hz-40Hz) and analyzed various techniques for feature extraction and classification of acquired signals

Pipelined Processor Design [Documentation] [*Apr '19*]

Guide: Prof.Virendra Singh | Electrical engineering department

- Developed a **6**-stage pipelined processor using **VHDL**, which was capable of executing 15 instruction sets provided with an 8-register and **16**-bit computing system
- Optimized the architecture performance by including Hazard mitigation blocks and Branch predictors

Handwritten expression solver [*Nov '18*]

Guide: Prof.Sunita Sarawagi | Computer science and engineering department

- Developed a solver that recognizes handwritten math expression from image and subsequently evaluate it
- Executed segmentation of digits and symbols from given expression using image-processing techniques
- Developed a 3 layered **Convolutional Neural Network** for recognizing the segmented digits and symbols

POSITIONS OF RESPONSIBILITY

Subsystem Head, Electrical Subsystem [*Feb '19 - Present*]

IIT Bombay Student Satellite Project

- Supervised **15** membered inter-disciplinary team of two subdivisions, **Power** and **On-Board Computer** to design the power distribution circuit, interface with peripherals and implementation of control algorithm
- Established **quality assurance** practices in Electrical subsystem to ensure reliable design process
- Executed three-step recruitment process to shortlist **18** students for the subsystem from **70+** applicants evaluating their technical ability, practical approach and team work

TECHNICAL SKILLS AND INTERESTS

Languages and libraries	C/C++, Python, VHDL, LaTeX, HTML5, CSS, SciPy, OpenCV, NumPy, PyTorch
Tools	Vivado, Quartus, MATLAB, Eagle, Android Studio, NGspice, AutoCAD
Interests	Processor design and testing, Digital VLSI, Analog circuits, Sensors and Simulations

EXTRA-CURRICULAR

- **National Cadet Corps(NCC)** [*Jul '17 - Apr '18*]
  - Attended **Annual Training Camp** and **Republic Day parade** held in 2nd Maharashtra Engineering Regiment NCC (Annual Training Camp is 10 days winter camp organized by every NCC unit across the nation at the end of every year, in which rigorous training is given to the cadets)
  - Fired 7 rounds of **0.22mm** Rifle and performed a cultural drama in annual training camp [*Dec '17*]
- Enthusiastic long-distance runner(5Km in Crossy GC, held at IIT Bombay), swimmer, cricketer and cyclist
- Volunteered in social initiative **SOULS**, under Techfest to encourage school children to use solar energy; students made 5k solar lamps and lighted them simultaneously setting a **Guinness world record** [*Oct '18*]