ARYAN LALL

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Dual Degree (B.Tech + M.Tech), Electrical Engineering
Indian Institute of Technology Bombay, Mumbai, India

SCHOLASTIC ACHIEVEMENTS

- Pursuing minor degree in **Computer Science and Engineering** [*Present*]
- Recipient of the prestigious Undergraduate Research Award (**URA01**) from IIT Bombay ['*20*]
- Bestowed with **Institute Technical Special Mention** award for outstanding contribution to the Technical community of IIT Bombay for the session 19'-20' ['*20*]
- Secured **99.08%** percentile in JEE-advanced among 2.2 Lakh candidates ['*17*]
- Selected amongst **45** candidates, all over India for **Indian Statistical Institute** (B.Math) ['*17*]
- Secured General Rank **38** in West Bengal-JEE among 1.27 Lakh candidates ['*17*]

INTERNSHIPS

Qualcomm | Machine Learning and Software Intern [*May '21 - Jul '21*]
Beam selection for 5G networks and Evaluation of Timeloop/Accelergy framework for energy estimation

- Build a robust model for performing the K-top beam selection task to identify the strongest **5G** channel
- Preprocessed various sensor data including the Lidar point clouds, Camera images and GPS readings to train and test various neural network models and obtained **91%** accuracy in top-10 beam selection task
- Evaluated and tested the Accelergy/Timeloop framework for power estimation of DNN hardware accelerators
- Analysed the Open Virtual Platform (**OVP**) for developing and simulating the embedded software

Qualcomm | Hardware Intern [*May '20 - Jul '20*]
Development of Static Timing Model for vector processor and reusable python components for UVM Testbench

- Developed the Static Timing Analysis model for a class of register-to-register Vector Processors to compute the execution time of a given set of low-level instruction codes, following in-order execution
- Submitted a research **paper** on the static timing model developed in the **IEEE HPCA** 2022 conference
- Developed an Iterative Constraint Randomization solver for generating various valid combinations of vector processor instructions and cut down the overall computation time by a factor of **500**
- Developed a **GUI** interface to ease up the process of Regression testing in vector processor testbench

KEY PROJECTS

TinyML - Machine Learning for Edge-Devices | Master's Thesis [Documentation] [*Jul '21 - Present*]
Guide: Prof. Siddharth Tallur | Electrical Engineering department

- Investigated toolchain for deploying machine learning frameworks on **cheaper** and **energy-efficient** devices
- Optimized and Implemented **TFLite** models on embedded devices and resource-constrained FPGAs
- Designed the FPGA hardware block for overcoming the limited high-speed memory and available data bandwidth while comparing its performance with other embedded devices using a benchmark application
- Evaluating applications in various domains including **Genomics** for leveraging the developed toolchain

Title Generation using NLP [*Jan '21 - Apr '21*]
Guide: Prof. Pushpak Bhattacharyya | Computer Science and Engineering department

- Fine-tuned a pre-trained **T5 Transformer** to generate an appropriate title for the input document and article
- Utilized **scientific papers** and **news articles** as dataset and employed **PyTorch** framework for model training
- Implemented and compared a **Bi-LSTM** seq2seq encoder-decoder architecture with attention using Keras

Product Review Sentiment Analysis [*Jan '21 - Apr '21*]
Guide: Prof. Pushpak Bhattacharyya | Computer Science and Engineering department

- Preprocessed the customer review dataset and applied **Synonym Replacement** method for **data augmentation**
- Implemented RNN, LSTM, Bi-LSTM, GRU, and Bi-GRU networks for sentiment analysis using Keras framework
- Compared accuracy and F1-score for the pre-trained word embeddings of **Word2Vec**, **GloVe** and **fastText**

CrakX App | One Stop Solution to all placement needs [View] [*Jul '20 - Present*]
App to help navigate through the latest campus resources to boost placement and internship preparation

- Developed a **Flutter** based app that helps navigate through **1000+** campus placement and internship resources
- Conceptualized the entire backend architecture of the application along with the development of top-notch frontend/UI and hence established a smooth flow of data between user application and database
- Acquired **5k+** users since launch, followed by appreciation from IIT Bombay and users across the country

FPGA Implementation of Sparse Recovery Algorithms [Documentation] [*Aug '20 - Dec '20*]
Guide: Prof. Siddharth Tallur | Electrical Engineering department

- Implemented the Orthogonal Matching Pursuit algorithm on a resource constrained FPGA
- Optimized the design and data-flow path to drastically reduce memory and FPGA resource consumption
- Performed comprehensive comparison with existing works and submitted the paper in **IEEE TVLSI** Journal

FPGA Based Emoji Detector [Documentation][Video] [*Oct '19 - Dec '19*]

GoPynq Competition - Organized by Xilinx during Techfest (Asia's largest Science and Technology festival)

- Secured **1st** position in competition with a 4-member team, competing against **30** other colleges across India
- Interfaced various components including web-cam with FPGA, essential for detection and processing
- Implemented algorithms such as PCA for Image segmentation and Emoji detection for executing on the SoC

IIT Bombay Student Satellite Project

Star-Tracker based Attitude Determination System [Abstract] [*Aug '19 - Present*]

A CubeSat-compatible modular Star Tracker based Attitude Determination System to be tested on PS4-OP by ISRO

- Conceptualized the Electrical framework for STADS module, required for performing various on-board tasks including power-distribution, data transmission and benchmarked various space-grade components
- Developed **faster** algorithms to increase the update-rate and interfaced memory devices(SRAM) with FPGA
- Currently developing an **FPGA**-based framework for storing and processing Star images onboard

Advitiy - Second Generation Satellite of IIT Bombay [*Feb '18 - Jun '19*]

Advitiy is the 2nd student satellite of IITB, technically advanced and efficient version of the 1st, Pratham

- Devised and implemented an algorithm based on I-V curves of solar cells in **MATLAB** to figure out the suitable series-parallel configuration of solar panels for delivering the maximum power in an orbit
- Established different communication protocols including **USART** and **I^{2}C** between **AVR** microcontrollers and sensors for data acquisition, **PID** implementation, estimation of attitude and health monitoring data

PS4-OP Payload Team [Paper] [*Jul '19 - Present*]

This mission aims to design a space-based experiment to be flown on PSLV Stage 4 Orbital Platform

- Actively participated in searching suitable experimental payloads which can be launched on-board stage 4 of the Polar Satellite Launch Vehicle (**PSLV**) by **ISRO**
- Researched on various instruments and algorithms to determine upper atmospheric density and satellite drag

COURSE PROJECTS

Handwritten expression solver [*Nov '18*]

Guide: Prof. Sunita Sarawagi | Computer science and engineering department

- Developed a solver that recognizes handwritten math expression from image and subsequently evaluates it
- Executed segmentation of digits and symbols from given expression using image-processing techniques
- Developed a 3 layered **Convolutional Neural Network** for recognizing the segmented digits and symbols

Control using Brainwaves [Documentation] [*Jan '20 - Mar '20*]

Guide: Prof. Debraj Chakrabarty | Electrical engineering department

- Developed a single-channel low-cost circuit of electroencephalographic (EEG) signal acquisition
- Designed a low-power noiseless filter bank to extract the frequencies of interest (8Hz - 40Hz) and analyzed various machine learning techniques for feature extraction and classification of acquired signals

Pipelined Processor Design [Documentation] [*Apr '19*]

Guide: Prof. Virendra Singh | Electrical engineering department

- Designed a **8-register**, **16-bit** & **6-staged** pipelined processor using VHDL, capable of executing 15 instructions
- Optimized the architecture performance by including Hazard mitigation blocks and Branch predictors

POSITIONS OF RESPONSIBILITY

Subsystem Head, Electrical Subsystem [*Feb '19 - Jun '20*]

IIT Bombay Student Satellite Project

- Supervised **15** membered inter-disciplinary team of two subdivisions, **Power** and **On-Board Computer** to design the power distribution circuit, interface with peripherals and implementation of control algorithm
- Established **quality assurance** practices in Electrical subsystem to ensure reliable design process
- Executed three-step recruitment process to shortlist **18** students for the subsystem from **70+** applicants

TECHNICAL SKILLS AND INTERESTS

Languages	C/C++, Python, VHDL, Verilog, LaTeX, HTML5, CSS, JavaScript, Assembly, Dart
Tools	Vivado, Quartus, MATLAB, Eagle, Android Studio, NGspice, AutoCAD, ADS, Origin9
Interests	Machine learning, Processor design and testing, Digital VLSI, Analog circuits

EXTRA-CURRICULAR

- **National Cadet Corps(NCC)** [*Jul '17 - Apr '18*]
  - Attended **Annual Training Camp** and **Republic Day parade** held in 2nd Maharashtra Engineering Regiment NCC (Annual Training Camp is 10 days winter camp organized by every NCC unit across the nation at the end of every year, in which rigorous training is given to the cadets)
  - Fired 7 rounds of **0.22mm** Rifle and performed a cultural drama in annual training camp [*Dec '17*]
- Enthusiastic long-distance runner(5Km in Crossy GC, held at IIT Bombay), swimmer, cricketer and cyclist
- Volunteered in social initiative **SOULS**, under Techfest to encourage school children to use solar energy; students made 5k solar lamps and lighted them simultaneously setting a **Guinness world record** [*Oct '18*]