ECSE 548 - Project Status Report: 8-bit Booth Multiplier

Marco Kassis, Aryan Mojtahedi, Dimitrios Stamoulis and Louis-Charles Trudeau
Department of Electrical and Computer Engineering, McGill University, Montreal, Canada

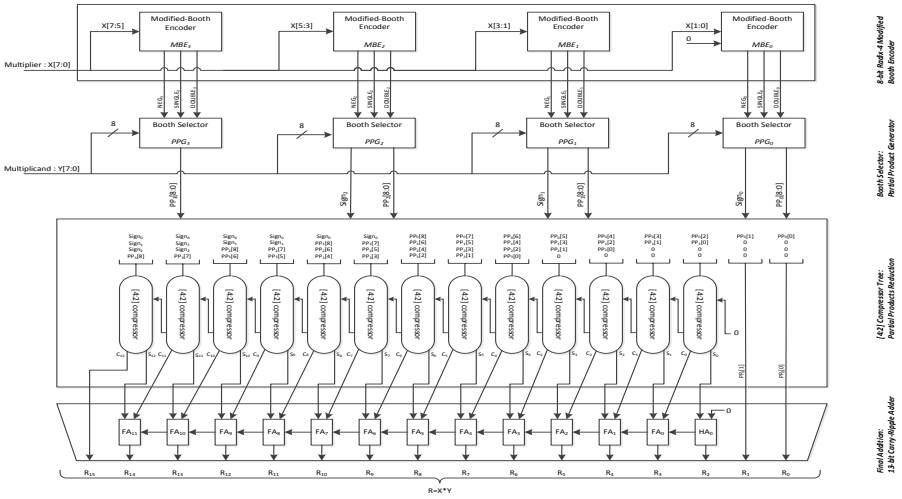

Fig. 1. Top-Level Design

I. Introduction

The current document is the submitted Project Status Report written in LaTeX IEEE format. The steps of our design plan were completed under **version control**. The proper GitHub Repo has been created [1].

II. Completed Deliverables[2]

Design part:

- **Exploration of the Modified Booth algorithm:** The theoretical background was studied based on related online material and our textbook[3].
- **Application in the 8-bit multiplier case:** Having the functionality of our design well defined, we proceed with the Top-Level design of our 8-bit Booth Multiplier. The outcome of such an exploration is presented in Figure 1.

Implementation part:

- **Circuit schematics:** We first implemented any required basic logic gates (e.g optimized XNOR gate) and added them to the `muddlib07.jelib` Electic library. The building blocks of our design (e.g Booth Encoder, Partial Product Generator etc) were created and added to the `wordlib8.jelib` Electic library. The top-level schematic was added to the `mips8.jelib` Electic library.
- **Verified correctness of modules:** All the designed schematics they do pass the DRC check using Electric.
- **Complete testbenching procedure** The proper Verilog decks were generated using Electic. All the individual submodules and the main building blocks were tested using the appropriate Modelsim testbenches.

III. Encountered Issues

No issues were issues encountered in carrying out the aforementioned deliverables. The implementation were straight-forward and the verification of their correctness was completed with the proper DRC checks and Modelsim testbenches.

IV. Changes in the implementation plan

No need for any changes in the implementation procedure. On the contrary, we are one week ahead based on our initial implementation plan and we have already started studying the layout (area minimization, transistor sizing etc)

References

[1] GitHub - Project Repository, https://github.com/dstamoulis/anonymous-dinosaurs.

[2] GitRepo - Project Status Report, https://github.com/dstamoulis/anonymous-dinosaurs/tree/master/ProjectStatusReport.

[3] Weste and Harris, *CMOS VLSI Design*, 4^{th} edition, Addison-Wesley, 2011.