ECSE 548 - Project Proposal: 8-bit Booth Multiplier

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I. Introduction

The current document is the submitted Project Proposal for the ECSE 548: Introduction to VLSI Systems course. Our project team (`myCourses-Group 4`) consists of Mr Marco Kassis, Mr Aryan Mojtahedi, Mr Dimitrios Stamoulis and Mr Louis-Charles Trudeau. A brief description of the intended project follows.

II. Intended result of the project

A. System to be designed

The selected system to be designed is the 8-bit Booth Multiplier [1][2]. Standard static logic CMOS will be used. The principles of the *Booth encoding* and its hardware implementations are extensively presented in the ECSE 548 textbook[3].

B. Manner of Evaluation

The main design and implementation criterion is the design cost. More specifically, the total number of transistors and the die area (μm^2) will be used as the main metrics for our system to be directly evaluated.

Other performance metrics could be evaluated as well. Metrics such as the critical path, the maximum propagation time based on logic gates and the max frequency could be explored.

C. Optimization Approach

The expected optimization approach focuses on the logic minimization of the inspected system.

D. Potential Extensions

- Integrating the module in the MIPS processor built in ECSE 548 Labs.
- Implementing the Booth multiplier using dynamic logic CMOS or Pass-Transistor logic (PTL).

III. Design Plan

Our first action point is to fully understand the modified booth algorithm. By choosing the right radix-r encoding, we can produce N/r partial products that depend on r bits of the multiplier. This strategy not only reduces the amount of partial products but also leads to a faster and smaller partial product summation. Radix-4 seems to be an optimal solution to build a 8x8 bit multipliers in terms of layout and propagation delay.

Having the encoding that will be ported to an implementation level, our next step is to explore the main parts of our architecture. For each one of them, their logic circuit should be drawn. The fundamental cells to be implemented are the Booth encoder, the Booth selector, the Partial products addition and the Final addition (CPA). The system's architecture is presented in Figure 1:

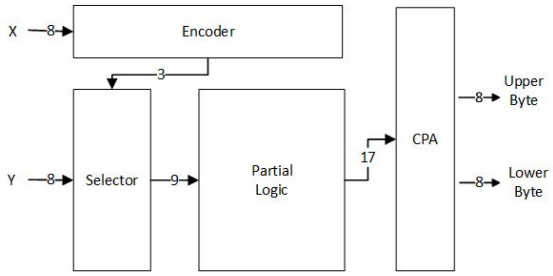

Fig. 1. System Architecture

Finally, the last part of our design plan is the actual implementation of the aforementioned modules. For the schematic and layout cells to be designed, the `Electric` open-source software [4] will be used.

IV. Deliverable for the mid-project status report

Design part :

- Exploration of the Modified Booth algorithm
- Application in the 8-bit multiplier case (Truth table, Logic Circuit etc)

Implementation part :

- Fully designed circuit schematic (`.ic`, `.sch` cells)
- Verified correctness of modules (DRC, NCC, ERC)
- Complete testbenching procedure (ModelSim Simulations)

References

[1] A. Booth, "A signed binary multiplication technique", *Quarterly J. Mechanics and Applied* Mathematics, vol. IV, pt. 2, Jun. 1951, pp. 236-240.

[2] O. MacSorley, "High-Speed arithmetic in binary computers", *Proc. IRE*, vol. 49, pt. 1, Jan. 1961, pp. 67-91.

[3] Weste and Harris, *CMOS VLSI Design*, 4^{th} edition, Addison-Wesley, 2011.

[4] Electric open-source EDA system, http://www.staticfreesoft.com/.